软件启动

1. 进入 Xmanager->选择 njupt01->username:选择 eda1-eda45 其中一个->password：1->password for root：njupt
2. 右键 open in terminal
3. 输入：cd DFTC1_2013.03/lab7_topdown
4. 输入：source /home/eda/bashrc

Scan 流程

Scan 流程如下：以 top down 流程为例

Scan 部分

注意下划线，空格和斜杠，需严格按照示例输入

1、启动 dc 工具

```
[wangyb@server01 lab7_topdown]$ dc_shell | tee topdown0401.log

                        Design Compiler Graphical
                              DC Ultra (TM)
                               DFTMAX (TM)
                           Power Compiler (TM)
                              DesignWare (R)
                              DC Expert (TM)
                            Design Vision (TM)
                            HDL Compiler (TM)
                            VHDL Compiler (TM)
                               DFT Compiler
                            Design Compiler(R)

                Version K-2015.06-SP5-2 for linux64 - Apr 11, 2016

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            or distribution of this software is strictly prohibited.
Initializing...
```

注释：tee 是将所有的命令显示出来，放到 topdown0401.log 文件中，其中.log 为后缀，前面为文件名，可随意取。

2、读取设计文件

```
dc_shell> read_ddc mapped/ORCA.ddc
Loading db file '/home/pktt/wangyb/njupt/DFTC1_2013.03/ref/db/sc_max.db'
Loading db file '/home/pktt/wangyb/njupt/DFTC1_2013.03/ref/db/io_max.db'
Loading db file '/home/pktt/wangyb/njupt/DFTC1_2013.03/ref/db/rams_max.db'
Loading db file '/home/pktt/wangyb/njupt/DFTC1_2013.03/ref/db/special.db'
Loading db file '/usr/eda/synopsys/syn_K201506SP5_2/libraries/syn/dw_foundation.sldb'
Loading db file '/usr/eda/synopsys/syn_K201506SP5_2/libraries/syn/gtech.db'
Loading db file '/usr/eda/synopsys/syn_K201506SP5_2/libraries/syn/standard.sldb'
  Loading link library 'cb13fs120_tsmc_max'
  Loading link library 'cb13io320_tsmc_max'
  Loading link library 'cb13_tsmc_memory_max'
  Loading link library 'cb13special'
  Loading link library 'gtech'
Reading ddc file '/home/pktt/wangyb/njupt/DFTC1_2013.03/lab7_topdown/mapped/ORCA.ddc'.
Information: Checking out the license 'DesignWare'. (SEC-104)
Loaded 16 designs.
Current design is 'ORCA'.
ORCA CLOCK_GEN ORCA_TOP RESET_BLOCK PCI_CORE PARSER CONTEXT_MEM RISC_CORE BLENDER SDRAM_IF PCI_RFIFO
```

注释：出现 dc_shell 标志成功启动工具，读取 ddc 文件，ddc 文件是 neltist 文件+constraint 文件，前期保存而来，所以会自动显示 current design，如果单独读入 netlist 文件需要设计 current design 和 link 命令。

```
dc_shell> set current_design ORCA
ORCA
dc_shell> link

  Linking design 'ORCA'
  Using the following designs and libraries:
  --------------------------------------------------------------------------
  * (16 designs)              /home/pktt/liuxt/lxt/ces_dftc1_2013.03/DFTC1_2013.
03/lab7_topdown/mapped/ORCA.ddc, etc
  cb13fs120_tsmc_max (library) /home/pktt/liuxt/lxt/ces_dftc1_2013.03/DFTC1_2013
.03/ref/db/sc_max.db
  cb13io320_tsmc_max (library) /home/pktt/liuxt/lxt/ces_dftc1_2013.03/DFTC1_2013
.03/ref/db/io_max.db
  cb13_tsmc_memory_max (library) /home/pktt/liuxt/lxt/ces_dftc1_2013.03/DFTC1_20
13.03/ref/db/rams_max.db
  cb13special (library)       /home/pktt/liuxt/lxt/ces_dftc1_2013.03/DFTC1_2013.
03/ref/db/special.db
  dw_foundation.sldb (library) /usr/eda/synopsys/syn_O-2018.06-SP5-1/libraries/s
yn/dw_foundation.sldb

1
```

注释：link 意义在于是否设计文件所需要的 cell 和库相对应，相对应则为 1，不对应则为 0。

3、setup timing

```
dc_shell> set test_default_dalay 0
0
dc_shell> set test_default_bidir_delay 0
0
dc_shell> set test_default_strobe 40
40
```

注释：这步骤的设定，可以在 command mode 中指定，也可以写在 synopsys_dc.setup 档中.主要是在设定将来 ATE 使用时, Timing 的规范.

4、设置 dft 信号

```
dc_shell> set_dft_signal -view existing_dft -type ScanClock -timing {45 55} -port {pclk sdr_clk sys_clk}
Accepted dft signal specification for modes: all_dft
1
dc_shell> set_dft_signal -view existing_dft -port prst_n -type Reset -active_state 0
Accepted dft signal specification for modes: all_dft
1
dc_shell> set_dft_signal -view existing_dft -port scan_en -type ScanEnable -active_state 1
Accepted dft signal specification for modes: all_dft
1
dc_shell> set_dft_signal -view existing_dft -type Constant -active_state 1 -port test_mode
Accepted dft signal specification for modes: all_dft
1
```

注释：set_dft_signal 是用来指定输入输出端口为 DFT 信号。

- view 有两种类型，一种是 existing_dft，一种是 spec。所谓 existing_dft，就是告诉工具，这个 port 已经被用作某种类型的 DFT 信号了，此时扫描链已经插入了。所谓 spec，就是告诉工具，下面指定的 port 将被用做某种类型的 DFT 信号。
- type 是用于指定 DFT 信号的类型，包括 Reset,Constant,TestMode,TestData,ScanDataIn,ScanDataOut,ScanMasterClock,ScanSlaveClock 等。

- port 是用于指定规则适用的端口。
- active_state 用于指定 Reset，ScanEnable，TestMode，Constant 是高电平有效，还是低电平有效。

这里 timing 设置将 port 端口 pclk、sdr_clk.sys_clk 设置为 ScanClock 模式，因为 timing 在设置 dft 已经存在，所以设置为 existing 模式，并且在 45 时刻上升，55 时刻下降。

5、创建测试协议

```
dc_shell> create_test_protocol
In mode: all_dft...
Information: Starting test protocol creation. (TEST-219)
  ...reading user specified clock signals...
Information: Identified system/test clock port sys_clk (45.0,55.0). (TEST-265)
Information: Identified system/test clock port pclk (45.0,55.0). (TEST-265)
Information: Identified system/test clock port sdr_clk (45.0,55.0). (TEST-265)
  ...reading user specified asynchronous signals...
Information: Identified active low asynchronous control port prst_n. (TEST-266)
1
```

注释：功能：根据当前设计指定的规则，比如 set_dft_signal，set_scan_path，set_scan_configuration 来创建测试协议。

6、drc 规则检查

```
dc_shell> dft_drc
In mode: all_dft...
  Pre-DFT DRC enabled
Warning: Design 'ORCA' contains 3 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)
Warning: A non-unate path in clock network for clock 'SDRAM_CLK'
 from pin 'I_ORCA_TOP/I_SDRAM_IF/sd_mux_dq_out_0/Z' is detected. (TIM-052)
Warning: Gated clock latch is not created for cell 'I_CLOCK_GEN/U5'on pin 'I0' in design 'ORCA'. (TIM-141)
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_RISC_CORE/U3'on pin 'B1' in design 'ORCA'. (TIM-141)
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_PCI_READ_FIFO/PCI_RFIFO_RAM'on pin 'CE1' in design 'ORCA'. (TIM-141)
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_PCI_WRITE_FIFO/PCI_WFIFO_RAM'on pin 'CE2' in design 'ORCA'. (TIM-141)
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_SDRAM_READ_FIFO/SD_RFIFO_RAM'on pin 'CE1' in design 'ORCA'. (TIM-141)
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_SDRAM_WRITE_FIFO/SD_WFIFO_RAM'on pin 'CE2' in design 'ORCA'. (TIM-141)
Warning: Gated clock latch is not created for cell 'I_CLOCK_GEN/U2'on pin 'A2' in design 'ORCA'. (TIM-141)
Warning: A non-unate path in clock network for clock 'SDRAM_CLK'
```

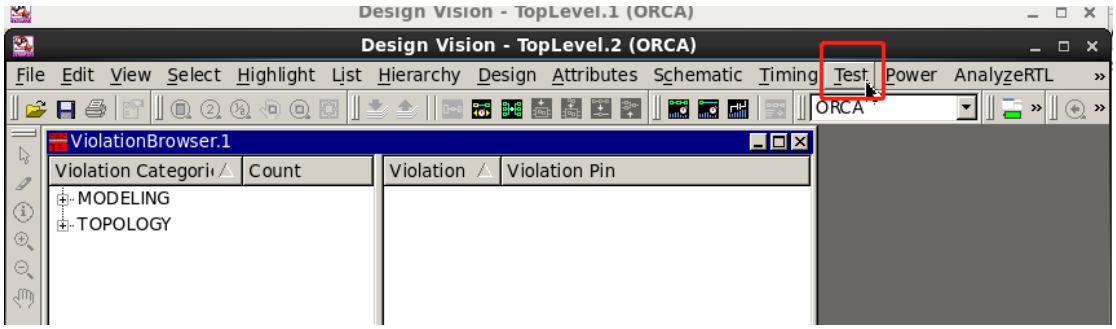
注释：这个是插入扫描链之前的规则检查，即对先前指定的规则检查。

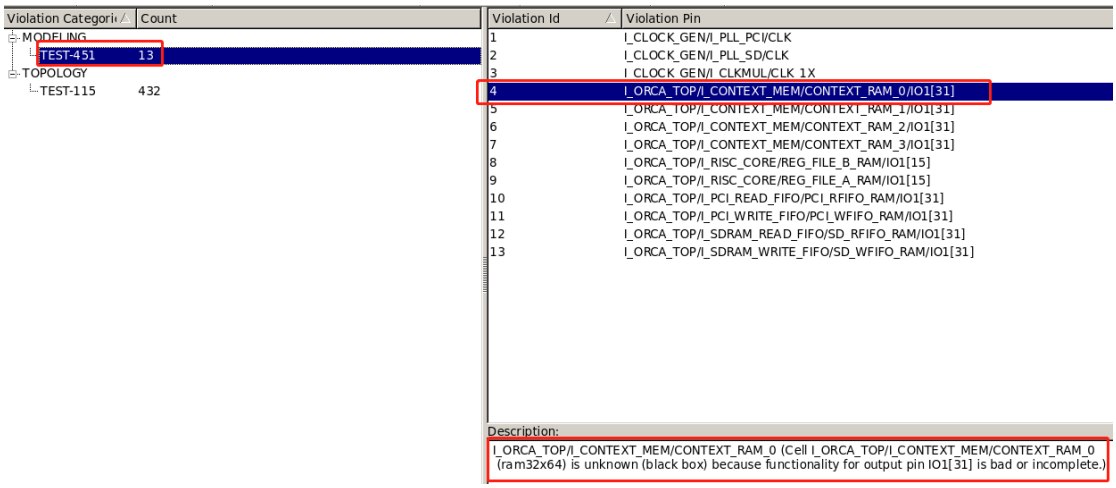
可以利用 gui 界面进行查看设计规则

6.1、启动 gui 界面

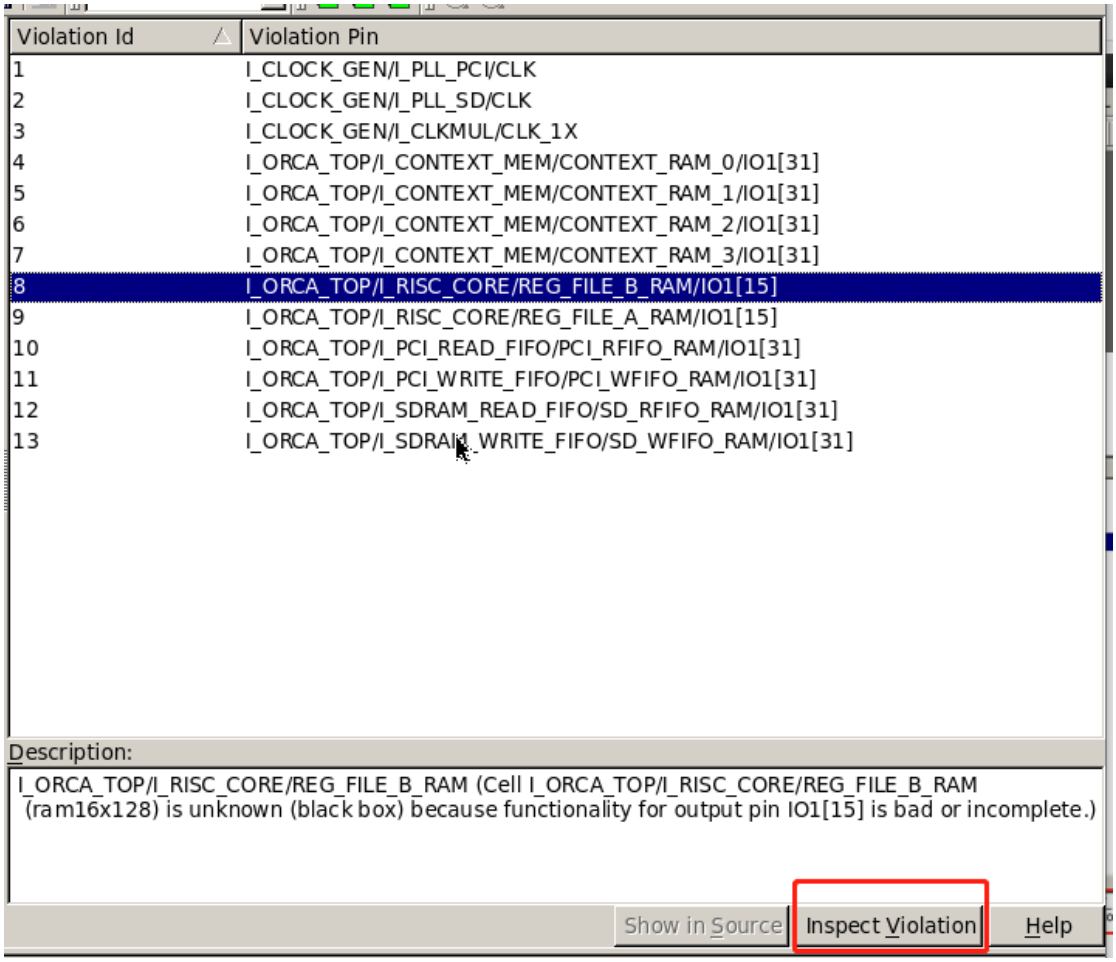
```
dc_shell> start_gui
dc_shell> current design is 'ORCA'.
4.1
Current design is 'ORCA'.
dc_shell>
```

6.2、Test/Run DFT DRC





注释：可以查看每个规则检查，基础学习主要修复时钟，复位是否可控。



注释：可以利用电路界面进行查看 violation

drc 结果

```
-------------------------------------------------------------
  DRC Report

  Total violations: 445

-------------------------------------------------------------

13 MODELING VIOLATIONS
    13 Cell has unknown model violations (TEST-451)

432 TOPOLOGY VIOLATIONS
   432 Improperly driven three-state net violations (TEST-115)

Warning: Violations occurred during test design rule checking. (TEST-124)

-------------------------------------------------------------
  Sequential Cell Report

  32 out of 2958 sequential cells have violations

-------------------------------------------------------------

SEQUENTIAL CELLS WITH VIOLATIONS
      *  32 cells have test design rule violations
SEQUENTIAL CELLS WITHOUT VIOLATIONS
      *2926 cells are valid scan cells

Information: Test design rule checking completed. (TEST-123)
Current design is 'ORCA'.
Current design is 'ORCA'.
1
```

7、查看 scan 状态

```
dc_shell> report_scan_state

****************************************
Report : test
          -state
Design : ORCA
Version: K-2015.06-SP5-2
Date   : Thu Apr  1 15:20:34 2021
****************************************

Scan state                   : scan cells replaced with loops

1
```

```
dc_shell> report_dft_signal

****************************************
Report : DFT signals
Design : ORCA
Version: K-2015.06-SP5-2
Date   : Thu Apr  1 15:24:23 2021
****************************************

========================================
TEST MODE: all_dft
VIEW     : Specification
========================================
No DFT signals defined in this mode.

****************************************
Report : DFT signals
Design : ORCA
Version: K-2015.06-SP5-2
Date   : Thu Apr  1 15:24:23 2021
****************************************

========================================
TEST MODE: all_dft
VIEW     : Existing DFT
========================================
Port               SignalType          Active    Hookup    Timing    Usage
----------         ----------          ------    ------    ------    -----
test_mode          Constant            1         -
scan_en            ScanEnable          1         -
sys_clk            ScanMasterClock     1         -         P 100.0 R 45.0 F 55.0
sys_clk            MasterClock         1         -         P 100.0 R 45.0 F 55.0
sdr_clk            ScanMasterClock     1         -         P 100.0 R 45.0 F 55.0
sdr_clk            MasterClock         1         -         P 100.0 R 45.0 F 55.0
pclk               ScanMasterClock     1         -         P 100.0 R 45.0 F 55.0
pclk               MasterClock         1         -         P 100.0 R 45.0 F 55.0
prst_n             Reset               0         -         P 100.0 R 55.0 F 45.0
```

8、设置扫描链配置

```
dc_shell> set_scan_configuration -chain_count 6 -add_lockup true -clock_mixing mix_clocks
Accepted scan configuration for modes: all_dft
1
```

注释：利用 set_scan_configuration 来对全局的 scan chain 进行配置。比如扫描链的类型，长度，个数等等信息。需要特别注意的是多时钟的构建，DFT 在默认的时候是为每个时钟域创建一个 scan chain，使用 set_scan_configuration -clock_mixing mixing_clocks 就允许多个时钟域的信号位于同一个扫描链上。当有不同的时钟串在一起，将会加入 lock-up 单元，解决多个时钟串 chain 问题。

9、对每条扫描链输入输出端口设置

```
for {set i 0} {$i < 6} {incr i} {
    set hookup_cell pad_iopad_$i
    set_dft_signal -view spec -port pad[$i] -type ScanDataIn -hookup_pin $hookup_cell/CIN
    set hookup_cell sdram_A_iopad_$i
    set_dft_signal -view spec -port sd_A[$i] -type ScanDataOut -hookup_pin $hookup_cell/I
    set_scan_path chain$i -view spec -scan_data_in pad[$i] -scan_data_out sd_A[$i]
}
```

```
dc_shell> source ./scripts/settings_insert_dft.tcl
Accepted scan configuration for modes: all_dft
Accepted dft signal specification for modes: all_dft
Accepted dft signal specification for modes: all_dft
Warning: Scan chain 'chain0' overwrites an earlier specification. (TESTDB-255)
Accepted scan path specification for mode: Internal_scan
Accepted dft signal specification for modes: all_dft
Accepted dft signal specification for modes: all_dft
Warning: Scan chain 'chain1' overwrites an earlier specification. (TESTDB-255)
Accepted scan path specification for mode: Internal_scan
Accepted dft signal specification for modes: all_dft
Accepted dft signal specification for modes: all_dft
Warning: Scan chain 'chain2' overwrites an earlier specification. (TESTDB-255)
Accepted scan path specification for mode: Internal_scan
Accepted dft signal specification for modes: all_dft
Accepted dft signal specification for modes: all_dft
Warning: Scan chain 'chain3' overwrites an earlier specification. (TESTDB-255)
Accepted scan path specification for mode: Internal_scan
Accepted dft signal specification for modes: all_dft
Accepted dft signal specification for modes: all_dft
Warning: Scan chain 'chain4' overwrites an earlier specification. (TESTDB-255)
Accepted scan path specification for mode: Internal_scan
Accepted dft signal specification for modes: all_dft
Accepted dft signal specification for modes: all_dft
Warning: Scan chain 'chain5' overwrites an earlier specification. (TESTDB-255)
Accepted scan path specification for mode: Internal_scan
```

注释：其中每个 scan input 和 scan output 都使用了 hookup pin 连接。

10、preview_dft

```
dc_shell> preview_dft -show scan_summary
Warning: The cache_read directory ../dc_dw_cache is not readable.  (SYNOPT-10)
Warning: The cache_write directory ../dc_dw_cache is not writable. So no cache elements car
Warning: Design 'ORCA' contains 3 high-fanout nets. A fanout number of 1000 will be used fc
Warning: A non-unate path in clock network for clock 'SDRAM_CLK'
 from pin 'I_ORCA_TOP/I_SDRAM_IF/sd_mux_dq_out_0/Z' is detected. (TIM-052)
Warning: Gated clock latch is not created for cell 'I_CLOCK_GEN/U5'on pin 'I0' in design '(
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_RISC_CORE/U3'on pin 'B1' i
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_PCI_READ_FIFO/PCI_RFIFO_RA
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_PCI_WRITE_FIFO/PCI_WFIFO_F
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_SDRAM_READ_FIFO/SD_RFIFO_F
Warning: Gated clock latch is not created for cell 'I_ORCA_TOP/I_SDRAM_WRITE_FIFO/SD_WFIFO_
Warning: Gated clock latch is not created for cell 'I_CLOCK_GEN/U2'on pin 'A2' in design '(
Warning: A non-unate path in clock network for clock 'SDRAM_CLK'
 from pin 'I_ORCA_TOP/I_SDRAM_IF/sd_mux_dq_out_0/Z' is detected. (TIM-052)

Information: Starting test design rule checking. (TEST-222)
Warning: Violations occurred during test design rule checking. (TEST-124)
Information: Test design rule checking completed. (TEST-123)
  Architecting Scan Chains
```

注释：在做 inser_dft 之前查测试点的信息，扫描链的信息。根据这些信息来确定所加的 dft 规格是否完备。

```
Number of chains: 6
Scan methodology: full_scan
Scan style: multiplexed_flip_flop
Clock domain: mix_clocks
Scan enable: scan_en (no hookup pin)

Chain      Scan Ports (si --> so)        # of Cells   Inst/Chain              Clock (port, time, edge)
-----      ----------------------        ----------   ----------              ------------------------
S chain0   pad[0] -->  sd_A[0]                488   I_ORCA_TOP/I_SDRAM_IF/DQ_out_1_reg_0_
                       (sdr_clk, 55.0, falling)
S chain1   pad[1] -->  sd_A[1]                488   I_ORCA_TOP/I_SDRAM_IF/mega_shift_1_reg_29__8_
                       (sdr_clk, 55.0, falling)
                                                    I_ORCA_TOP/I_BLENDER/latched_clk_en_reg
                                                                           (sys_clk, 55.0, falling)
                                                    I_ORCA_TOP/I_PARSER/r_pcmd_out_reg_0_
                                                                           (pclk, 45.0, rising)
S chain2   pad[2] -->  sd_A[2]                488   I_ORCA_TOP/I_PCI_CORE/mega_shift_reg_26__7_
                       (pclk, 45.0, rising)
S chain3   pad[3] -->  sd_A[3]                488   I_ORCA_TOP/I_PCI_CORE/mega_shift_reg_56__15_
                       (pclk, 45.0, rising)
                                                    I_ORCA_TOP/I_RESET_BLOCK/sdram_rst_ff_reg
                                                                           (sdr_clk, 45.0, rising)
S chain4   pad[4] -->  sd_A[4]                487   I_ORCA_TOP/I_SDRAM_IF/mega_shift_0_reg_20__12_
                       (sdr_clk, 45.0, rising)
                                                    I_ORCA_TOP/I_BLENDER/rem_blue_reg
                                                                           (sys_clk, 45.0, rising)
S chain5   pad[5] -->  sd_A[5]                487   I_ORCA_TOP/I_BLENDER/s4_op1_reg_5_
                       (sys_clk, 45.0, rising)
1
```

注释：6 条 chain 达到平衡，clock mixing 满足条件。

11、insert_dft

```
dc shell> insert dft
```

insert_dft（注意下划线）

12、检查上 chain 后的 DRC 以及查看测试覆盖率

```
dc_shell> dft_drc -coverage_estimate
In mode: internal_scan...
Warning: The cache_read directory ../dc_dw_cache is not readable.  (SYNOPT-10)
Warning: The cache_write directory ../dc_dw_cache is not writable. So no cache
  Design has scan chains in this mode
  Design is scan routed
  Post-DFT DRC enabled

Information: Starting test design rule checking. (TEST-222)
  Loading test protocol
  ...basic checks...
  ...basic sequential cell checks...
  ...checking vector rules...
  ...checking clock rules...
  ...checking scan chain rules...
  ...checking scan compression rules...
  ...checking X-state rules...
  ...checking tristate rules...
  ...extracting scan details...
  ...saving simulation value info...


            Pattern Summary Report
 ---------------------------------------------
 #internal patterns                         0
 ---------------------------------------------


     Uncollapsed Stuck Fault Summary Report
 ---------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT      70491
 Possibly detected                PT         67
 Undetectable                     UD       1231
 ATPG untestable                  AU       3302
 Not detected                     ND        105
 ---------------------------------------------
 total faults                              75196
 test coverage                            95.35%
 ---------------------------------------------
  Information: The test coverage above may be inferior
               than the real test coverage with customized
               protocol and test simulation library.
Current design is 'ORCA'.
1
Current design is 'ORCA'.
```

13、保存网表文件、ddc 文件、spf 文件

```
dc_shell> change_names -rule verilog -hierarchy
Warning: In the design ORCA_TOP_test_1, net 'pll_sdram_fb' is connecting multiple ports. (UCN-1)
Warning: In the design ORCA_TOP_test_1, net 'pll_pci_fb' is connecting multiple ports. (UCN-1)
1
dc_shell> write -f verilog -h -o ./ORCA_scan.v
Writing verilog file '/home/pktt/liuxt/lxt/ces_dftc1_2013.03/DFTC1_2013.03/lab7_topdown/ORCA_scan.v'.
Warning: Verilog 'assign' or 'tran' statements are written out. (VO-4)
1
dc_shell> write -format ddc -hierarchy -output ./ORCA_scan.ddc
Writing ddc file './ORCA_scan.ddc'
1
dc_shell> set test_stil_netlist_format verilog
verilog
```

```
dc_shell> write_test_protocol -o ./ORCA.spf
Writing test protocol file '/home/pktt/liuxt/lxt/ces_dftc1_2013.03/DFTC1_2013.03/lab7_topdown/ORCA.spf' for mode 'Internal_scan'...
1
dc_shell> change_names -rule verilog -hierarchy
Warning: In the design ORCA_TOP_test_1, net 'sdram_clk' is connecting multiple ports. (UCN-1)
Warning: In the design ORCA_TOP_test_1, net 'pclk' is connecting multiple ports. (UCN-1)
1
dc_shell> write -f verilog -h -o ./ORCA_scan.v
Writing verilog file '/home/pktt/liuxt/lxt/ces_dftc1_2013.03/DFTC1_2013.03/lab7_topdown/ORCA_scan.v'.
Warning: Verilog 'assign' or 'tran' statements are written out. (VO-4)
1
```

注释：这些文件最好一起保存，保存 netlist 和 spf 文件用于 Tetramax。