A Novel Floating Lossy Inductance Realization Topology With NICs Using Current Conveyors

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***Abstract*—A negative-impedance converter (NIC) is a useful component in the circuit synthesis theory especially for active *RC* filter design. In this brief, usefulness of the NIC is shown in a floating inductance realization topology that is an alternative application area for the component. A new floating parallel *RL* realization topology employing two NICs and three passive components is presented.**

***Index Terms*—Active filters, current conveyors, inductance simulators.**

I. Introduction

ALTHOUGH there are several examples of floating inductance simulators in the literature, most of the presented topologies have complicated structures and a systematic design topology is not given. For example, there are four current conveyors in references [1]–[6]. Reference [7] uses three current conveyors. Although, Senani [8], [9] proposes floating lossy and lossless inductors with two current conveyors and five or three passive components, they did not present a systematic design topology, an approach similar to many papers in the literature.

Negative-impedance converters (NIC) are useful elements since the beginning of circuit synthesis theory. Firstly, in 1954, Linvill proposed NICs for circuit synthesis in active filter design [10]. However, in our work, usefulness of NIC is presented in a floating inductance realization topology that is an alternative application area for the component.

The proposed topology provides a new lossy floating inductance with two NICs and a minimum number of passive components.

II. Negative Impedance Converter

"There are two kinds of NIC, such as the voltage-inversion type (V-NIC) and current-inversion type (I-NIC). In V-NICs, we see that the current is transmitted through the ports unchanged while the voltage at one-port is inverted with respect to that at the other port." [11] In this brief, we discuss I-NICs, which means that the voltage at each port is the same but the current at one port is inverted with respect to that at the other port [11].

In the implementation of the NIC, the second-generation current conveyor (CCII) can be used. The circuit symbol of CCII is shown in Fig. 1(a). Considering the nonidealities arising from the physical implementation, its terminal relationship can be given as [12]

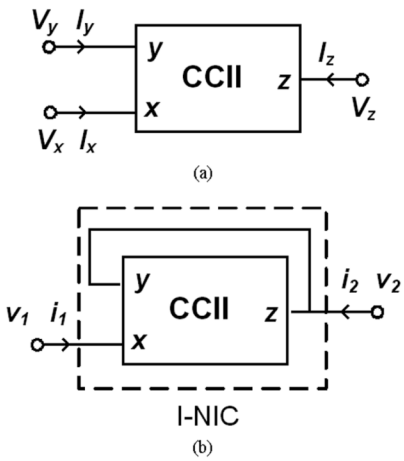

Fig. 1. (a) Circuit symbol of the CCII. (b) Current inversion type NIC obtained from CCII-.

$$V_X = \beta V_Y \quad I_Y = 0 \quad I_Z = \pm\alpha I_X \tag{1}$$

where α and β are, respectively, current and voltage gains which can be expressed as $\alpha = 1 - \varepsilon_i$, $\beta = 1 - \varepsilon_v$, with $|\varepsilon_i| \ll 1$, $|\varepsilon_v| \ll 1$. Here, ε_i denotes the current tracking error and ε_v denotes the voltage-tracking error.

Scheme of I-NIC obtained from CCII is shown in Fig. 1(b) and its terminal relationship by taking the nonidealities into consideration can be given as

$$v_1 = \beta v_2, \quad i_2 = \alpha i_1. \tag{2}$$

III. Proposed Floating Parallel *RL* Circuit

Many floating inductors have been proposed but the possibility of lossy realizations was not emphasized. For many applications, as the one given in this brief, parallel *RL* structures are adequate. Firstly, a parallel *RL* structure behaves as an actual inductor up to the frequency value where the parallel resistor R becomes the dominant component at $f = R/2\pi L$. This situation is depicted in Fig. 8. Secondly, a series resistance with a low value or a parallel resistance with a high value represents the power loss in an actual inductor where the resistors are frequency dependent [13]. Therefore, the proposed parallel *RL* structure can simulate an actual physical inductor in a certain frequency range.

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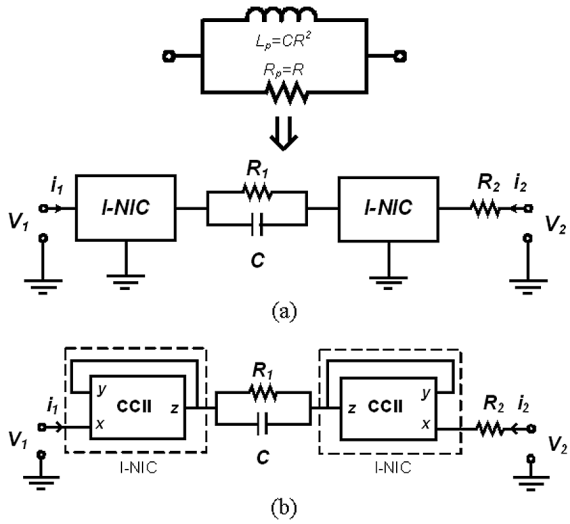

Fig. 2. Floating lossy inductance generation procedure: for $R_1 = R_2$ a parallel *RL* circuit is obtained. (a) Block diagram. (b) Circuit diagram.

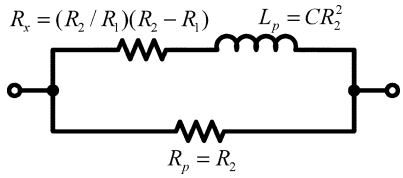

Fig. 3. Equivalent floating impedance circuit for $R_1 \neq R_2$.

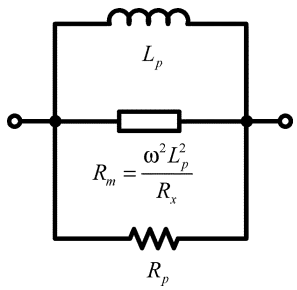

Fig. 4. Approximately equivalent floating impedance circuit valid for the frequencies $f \gg R_x/(2\pi L_p)$ to illustrate effect of resistor mismatches.

The proposed actively simulated floating parallel *RL* topology is shown in Fig. 2(a). The corresponding circuit is given in Fig. 2(b). The two-port short circuit admittance representation of the circuit is given as

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{sCR_1}{R_2 - R_1 + sCR_1R_2} + \frac{1}{R_2 - R_1 + sCR_1R_2} \right) \times \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad (3)$$

The floating immittance represented with (3) has the equivalent circuit as given in Fig. 3. For $R_1 = R_2 = R$, R_x will be zero and a parallel *RL* circuit is obtained that is characterized with the equation

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{1}{R} + \frac{1}{sCR^2} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad (4)$$

Due to (4) the floating parallel *RL* circuit has the equivalent resistor value $R_p = R$ and the equivalent inductance value $L_p = CR^2$. Passive sensitivities of the proposed circuit for this L value are $|S_R^{L_p}| = 2$ and $|S_C^{L_p}| = 1$. This sensitivity calculation may give satisfactory results for many cases, since the synchronous change of the matched integrated circuit resistors due to their tolerances are on the order of 10% a relatively large variation compared to the mismatch ranges that are on the order of only 0.1% [14]. Now let us examine the effects of the resistor mismatches on the realized equivalent inductance and resistance values. We start with (3) or its representation in Fig. 3. One can write the two-port short-circuit admittance representation of the circuit in Fig. 3 as

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{1}{R_x + sL_p} + \frac{1}{R_p} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad (5)$$

When the numerator and denominator of the appropriate terms are divided by sL_p, we obtain

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{1/(sL_p)}{R_x/(sL_p) + 1} + \frac{1}{R_p} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad (6)$$

In order to take the effects of series mismatch component R_x into consideration, the approximation $1/(1+x) \approx 1-x$, which is valid for $|x| \ll 1$, is used since $R_x/(\omega L_p) \ll 1$ for sufficiently small mismatch levels. Thus, (6) converts to

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{1}{sL_p} \left(1 - \frac{R_x}{sL_p} \right) + \frac{1}{R_p} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad (7)$$

Rearranging (7) gives

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{1}{sL_p} - \frac{R_x}{s^2 L_p^2} + \frac{1}{R_p} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad (8)$$

In (8), $1/(sL_p)$ and $1/R_p$ are desired terms. However, an additional term $-R_x/(s^2L_p^2)$ representing a frequency dependent resistive element in parallel to R_p also exists. The value of this parallel mismatch resistor is $R_m = \omega^2 L_p^2/R_x$. In this case the equivalent circuit representation can be given as in Fig. 4. It is valid for the frequencies $f \gg R_x/(2\pi L_p)$, an easily satisfied condition for moderate frequency ranges with a small mismatch series resistor R_x. From Fig. 4, we observe that an overall parallel *RL* is obtained with values L_{eq} and R_{eq} where $L_{\text{eq}} = L_p$ and $R_{\text{eq}} = R_m // R_p$. Note that R_{eq} can be written as

$$R_{\text{eq}} = R_p - \frac{R_p^2 R_x}{R_p R_x + \omega^2 L_p^2}. \quad (9)$$

From (9), one can observe that the mismatch of resistors introduces an additional term to R_p. To keep this contribution small the condition is $|R_m| \gg |R_p|$. By defining a mismatch parameter $k = R_1/R_2$ the equivalent resistor R_{eq} can be written as follows:

$$R_{\text{eq}} = R_2 + \frac{(k-1)R_2}{1 - k + k\omega^2 C^2 R_2^2}. \quad (10)$$

The sensitivity of R_{eq} to the mismatch parameter k can be calculated as

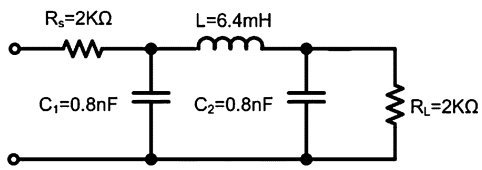

Fig. 5. Application example: third-order Butterworth low-pass ladder filter.

$$\left|S_k^{R_{\rm eq}}\right| = \left|\frac{1}{1+k\left(\omega^2C^2R_2^2-1\right)}\right|. \tag{11}$$

For $\omega^2C^2R_2^2 \gg 1$, the sensitivity to the mismatch parameter k will be less than one in magnitude. As a numerical example for $\omega = 10^5$ rad/s, $C = 500$ pF, $R_1 = 20\,020\ \Omega$, and $R_2 = 20\,000\ \Omega$ corresponding to 0.1% mismatch, the magnitude of the sensitivity is one; for $C = 200$ pF it is 6.3. Note that the sensitivity deteriorates with a reduced C value if R_2 is kept constant. The above condition is equivalent to $\omega^2CL_{\rm eq} \gg 1$ thus low resistor mismatch sensitivities can easier be obtained with larger inductance values. On the other hand, since $L_{\rm eq} = L_p$ under the conditions stated above, the realized inductance value is insensitive to mismatches. However one should always take into account the effect of passive element tolerances that may be on the order of 10%.

Finally, the quality factor of our proposed parallel *RL* circuit can be given in terms of resistor and capacitor values for $R = R_1 = R_2$ in Fig. 2 as

$$Q = \frac{1}{2\pi fCR}. \tag{12}$$

When active component nonidealities as given in (2)are considered, the two-port short circuit admittance representation of the circuit is given in (13), shown at the bottom of the page.

IV. Simulations

The functionality of the lossy inductor is tested on a third-order Butterworth *LC* passive ladder prototype shown in Fig. 5. It is a low-pass filter that was simulated with PSpice using both a floating ideal inductor and using our proposed parallel *RL* structure. The cufoff frequency of the filter is 100 kHz. The proposed inductor circuit in Fig. 2(b) is realized with the following passive element values: $R = R_1 = R_2 = 20$ kΩ, $C = 16$ pF and is used in the example circuit in Fig. 5. The commercially available CFOA AD844/AD of Analog Devices are employed as active components with supply voltages of $V_{\rm DD} = 12$ V and $V_{\rm SS} = -12$ V. I-NICs are implemented by connecting Y and Z ports of an AD844 integrated circuit as shown in Fig. 2(b). The frequency response of the example circuit together with ideal response is depicted in Fig. 6. In the figure, the value of

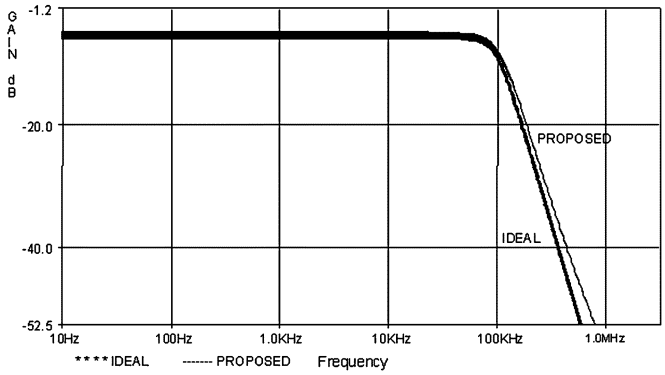

Fig. 6. PSpice simulation illustrating the frequency response.

R_1 is swept with a variance of ±1% and a total of 50 simulations were performed to observe the change in the frequency response. Fig. 6 shows that there is only a slight variation in the frequency response of the realized filter due to resistor mismatches. This is an expected result since the dominant component of the parallel *RL* circuit is inductance that is insensitive to the resistor mismatches in the frequency range of interest.

For an analog filter, the dynamic range is very important, because it gives information about signal handling capability of the circuit. To illustrate voltage swing capability, a transient analysis is performed by applying a sinusoidal signal to the realized filter. The time-domain output signal waveforms are shown in Fig. 7. The frequency of the input signal is $f_0 = 90$ kHz. The total harmonic distortion of the filter designed with the proposed circuit gives a low total harmonic distortion (THD) value such as 0.01% for peak-to-peak 1.3-V output signal amplitude.

Fig. 8 shows that the magnitudes of the impedances of an ideal inductor and a lossy inductor that is a parallel *RL* circuit can be made very close for a set of selected values over many decades. The critical frequency of the lossy inductor where R_p becomes the dominant component in the parallel *RL* circuit at $R_p = 2\pi fL$ is $f = R/2\pi L = 20\ {\rm k}\Omega/(2\pi 6.4\ {\rm mH}) = 497.6$ kHz. The effect of a parallel resistor on the frequency response will not be very important for the example low-pass filter that has a cufoff frequency of 100 kHz. Thus, the proposed parallel *RL* circuit can be successfully used for replacing a lossless inductor up to this frequency.

V. Conclusion

In this brief, a simple floating inductance with a parallel resistor employing two NICs is proposed. The circuit can be designed with two active and a minimum number of passive components, such as two resistors and a single capacitor. Also, the proposed floating parallel *RL* structure can provide an easy way of implementing parallel *RLC* resonators with a minimum

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} \frac{\alpha_2\beta_2}{R\alpha_1\beta_1(1+sCR-\beta_2\alpha_2)} + \frac{sC\alpha_2\beta_2}{\alpha_1\beta_1(1+sCR-\beta_2\alpha_2)} & -\frac{\alpha_2}{R\alpha_1(1+sCR-\beta_2\alpha_2)} - \frac{sC\alpha_2}{\alpha_1(1+sCR-\beta_2\alpha_2)} \\ -\frac{\beta_2}{R\beta_1(1+sCR-\beta_2\alpha_2)} - \frac{sC\beta_2}{\beta_1(1+sCR-\beta_2\alpha_2)} & \frac{1}{R(1+sCR-\beta_2\alpha_2)} + \frac{sC}{1+sCR-\beta_2\alpha_2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{13}$$

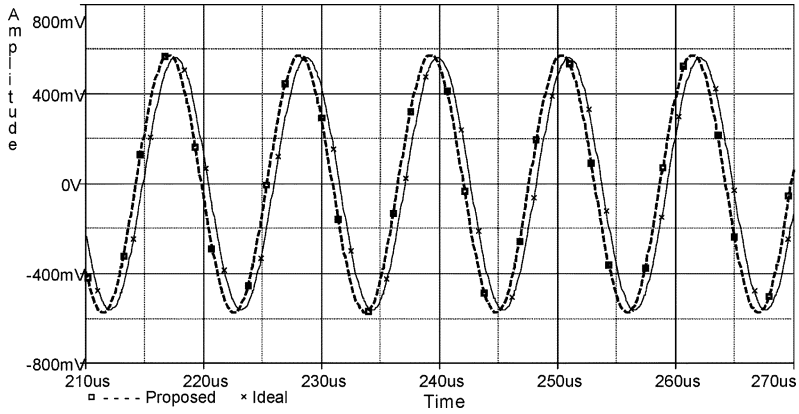

Fig. 7. Time-domain output waveforms of the low-pass filter with an ideal inductor and the proposed inductor simulator circuits to illustrate the dynamic ranges at 90 kHz and for a signal with 1.3-V peak-to-peak value.

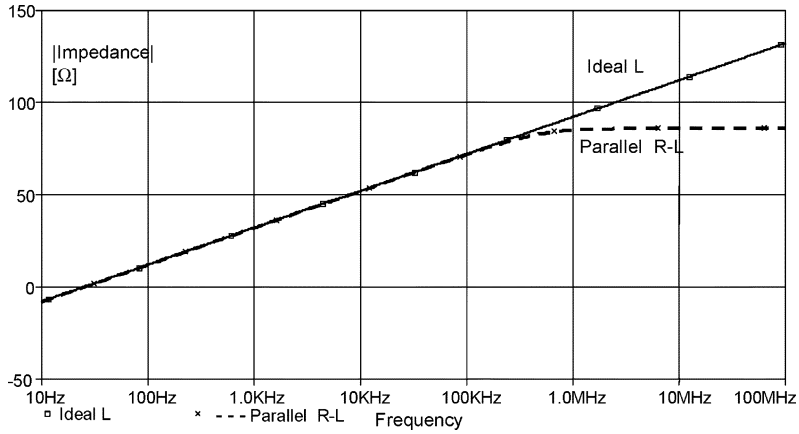

Fig. 8. Magnitude of the impedance of an ideal inductance, $L = 6.4$ mH and parallel *RL* impedance with $L = 6.4$ mH and $R = 20$ kΩ. Up to the frequency where the resistance becomes dominant ($R = 2\pi fL$), both impedances can be assumed to be equal over many decades.

number of passive components. The brief shows that floating parallel *RL* circuits can be used instead of actual inductor for some applications such as low-pass filters. Moreover, in our work, usefulness of NIC is presented in a floating inductance realization topology that is an alternative application area for the component. Simulation results are included to verify theoretical results presented.

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