Toward Multiple-Bit-Per-Cell Memory Operation With Stable Resistance Levels in Phase Change Nanodevices

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***Abstract*— Resistance drift of the amorphous states of multilevel phase change memory (PCM) cells is currently a great challenge for the commercial implementation of a reliable multiple-bit-per-cell memory technology. This paper reports observation of a stable intermediate state for a multilevel PCM cell that is achieved through nonuniform heating with a square current injection top electrode. Drift coefficient of the intermediate state is an order of magnitude lower than reset and has weaker temperature dependence. Using finite-element simulations and an analytical model for the subthreshold current–voltage characteristics, based on thermally activated hopping of charge carriers across Coulombic donor-like traps, we conclude that the defect density is two orders of magnitude larger in the intermediate state. We attribute the low drift coefficient of the intermediate state to a large number of stable interfacial defects which dominate the electron transport. Current findings give way to a more stable ultrahigh-density PCM device.**

***Index Terms*— Multiple-bit-per-cell memory, phase change memory (PCM), resistance drift.**

I. Introduction

PHASE change random access memory is currently regarded as a strong candidate for emerging nonvolatile solid-state memory technology with its promising properties such as high signal to noise ratio, nano-second operation time, low power consumption, and scalability and compatibility with other technologies [1], [2]. Phase change memory (PCM) also has the potential for multilevel storage due to at least 3–5 orders of magnitude difference in the resistance levels of amorphous and crystalline states. Various methods for achieving intermediate resistance levels have been proposed such as using multilayer stacks of phase change materials [3], [4], graded doping of phase change layer(s) [5], [6], or engineering the contact geometry [7], [8]. It has been shown that in PCM cells with a top contact geometry with sharp corners, current crowding effects allow controlling of the crystalline fraction of the chalcogenide material in the device [8]. Hence, a mixed phase in the active region where amorphous and crystalline phases coexist leads to an intermediate resistance state (IRS).

Long-term reliability of a PCM depends on the stability of the logic levels. A potential obstacle in this matter is the resistance drift of the amorphous phase, which has been well investigated in the literature and explained by the structural relaxation (SR) mechanism [9], [10]. Rearrangement of the atomic structure results in annihilation of traps and causes an increase in resistance over time, which is characterized by a temperature-dependent parameter called the drift coefficient ν. ν is around 0.1 for reset, i.e., high-resistance state (HRS) and is less than 0.01 for set, low-resistance state (LRS) [9], [11]. Furthermore, the long-term drift of the resistance levels can lead to overlapping of adjacent states and loss of data [12]. In this paper, we show that the resistance drift in IRS achieved by utilizing a square-top contact is considerably low, which qualifies this state as a stable logic level in multiple-bit-per-cell operation.

II. Resistance Drift Measurements

Electrical measurements have been performed on PCM devices with a $Ge_2Sb_2Te_5$ (GST) phase change layer (50-nm thick) that is in contact with 50-nm $W_{0.8}Ti_{0.2}$ (WTi) top and bottom electrodes. The top contact is shaped by e-beam lithography and ion milling to have circular or square geometry with a submicrometer size. Electrical connection is achieved via Ta (5 nm)/Au (150 nm) electrodes in contact with PCM cells isolated by Al_2O_3. Fig. 1 shows a schematic of the device along with the measurement setup which allows application of RF and dc signals simultaneously via a bias-tee and supports detection of the change in electrical characteristics right after a nanosecond voltage pulse. A variable load resistance of 100 Ω–10 kΩ has been used for protective

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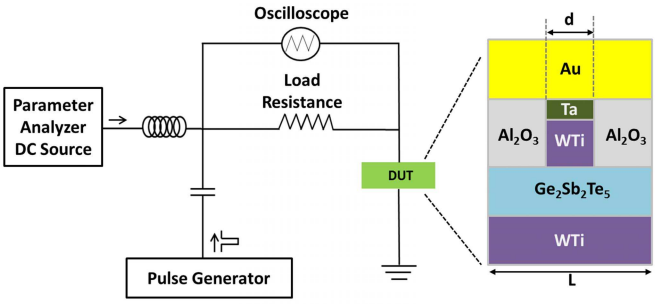

Fig. 1. Schematic of the measurement setup for monitoring the electrical characteristics of a PCM device with illustrated layer structure.

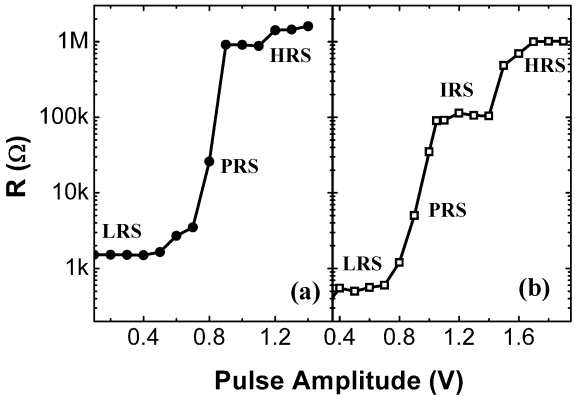

Fig. 2. Resistance of the PCM device is plotted as a function of programming pulse amplitude for a pulse with 100-ns width and 2-ns trailing edge for (a) 75-nm circular-top contact device and (b) 130-nm square-top contact PCM cell. The corresponding resistance levels are labeled on the plots.

purposes and to monitor the drift. A custom sample stage with a heater is utilized for temperature-dependent measurements.

The device illustration in Fig. 1 displays the smaller dimension heater layer below the top electrode patterned in a circular or square geometry. The diameter/side-length d of the top heater contact varies between 60 and 600 nm and the width L of the GST layer is adjusted so that it is at least three times the heater length. Tailoring the contact geometry to have corners favors a heterogeneous current distribution inside the active region as shown in [8], which results in a stable IRS having a wide range of programming amplitudes different from a partial set/reset (PRS).

Fig. 2 shows the programmable resistance levels of a square contact device (130-nm length), in comparison with a circular-top contact device (75-nm diameter), as a function of pulse amplitude for a fixed pulse width of 100 ns with 2 ns leading and trailing edges. In Fig. 2(a), the circular device displays typical switching dynamics, jumping from 1.8 kΩ for set state (LRS) to 1-MΩ reset state (HRS) for a pulse amplitude of 0.9 V. Typically, in PCM devices resistance levels with partial switching are also achieved by proper choice of programming voltages PRS. For example a 0.8 V pulse amplitude leads to a PRS (30 kΩ) in the circular device as illustrated in Fig. 2. On the other hand, for the square-top contact device [Fig. 2(b)] between an LRS of 550 Ω and an HRS of 1 MΩ, there is a stable resistance level IRS at

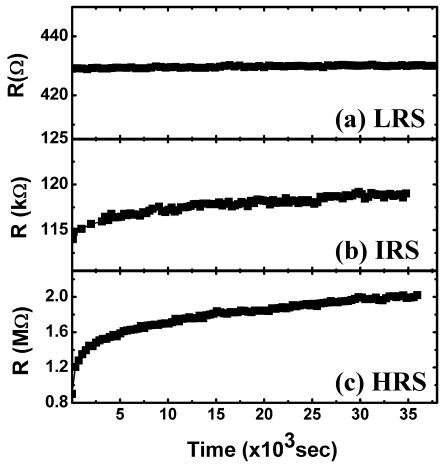

Fig. 3. Time evolution of resistance for (a) set state, (b) intermediate state, and (c) reset state for a 130-nm square-top contact device recorded after the device is programmed with the appropriate pulse.

115 kΩ for a range of pulse amplitudes (1.05–1.4 V). PRS is also present in the square contact device, such as 5.5 kΩ in Fig. 2(b). Typically, there is 0.2–0.5 V of a programming range where the resistance is 50–100 times higher than LRS and 1/50th–1/10th of HRS for square devices.

Typical threshold reset current densities of our devices, for programming pulses of 50–100-ns widths, are in the range 8–20 MA/cm^2. A systematic study is presented in [7]. These values are comparable to those reported in the literature for similar-sized devices which are tens of MA/cm^2 [13], [14].

The long-term stability of the resistance levels are evaluated by monitoring the resistance drift at a particular state. Fig. 3 shows the time evolution of resistance for LRS, IRS, and HRS for up to 10 h after a programming pulse is applied to the device, switching it from a set or a reset state. The resistance change is almost nonexistent in set state; whereas it is very dramatic for reset state revealing a 1-MΩ shift in 10 h. For IRS, resistance increases from 115 kΩ to almost 120 kΩ in the same period of time indicating a smaller variation. The data can be fit to the following drift equation:

$$R = R_0 \left(\frac{t}{t_0}\right)^{\nu} \tag{1}$$

where R_0 is the initial resistance of the device at $t = t_0$ and ν is the drift coefficient. The relative change in resistance is compared for different states in Fig. 4, by plotting the resistance normalized with respect to its initial value at $t_0 = 100$ s. The coefficient ν is calculated by fitting the data to the above equation and is indicated by the slope of the data in the logarithmic plot of Fig. 4. The steep change for HRS leads to a high coefficient of $\nu = 0.1070 \pm 0.0012$, whereas the steady resistance of LRS yields $\nu = 0.00090 \pm 0.00006$. ν for HRS typically takes on values between 0.07 and 0.109. These are in line with the values reported in [9], [10], [15], and [16].

IRS displays an almost steady behavior with a low drift coefficient. $\nu = 0.0101 \pm 0.0003$ for this sample, an order of magnitude smaller than ν for HRS. While partial reset

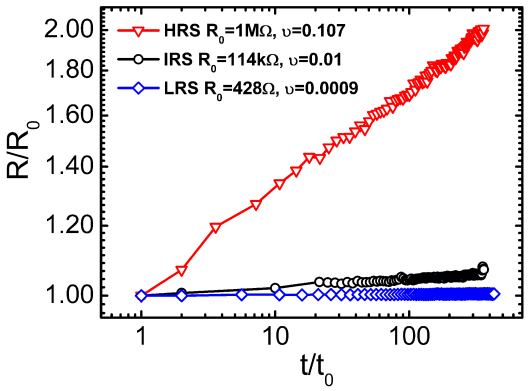

Fig. 4. Relative change in resistance is plotted for the device in Fig. 3 comparing the change for reset, intermediate and set states. $t_0 = 100$ s, R_0 values for HRS, IRS and LRS are 1 MΩ, 114 kΩ and 428 Ω, respectively.

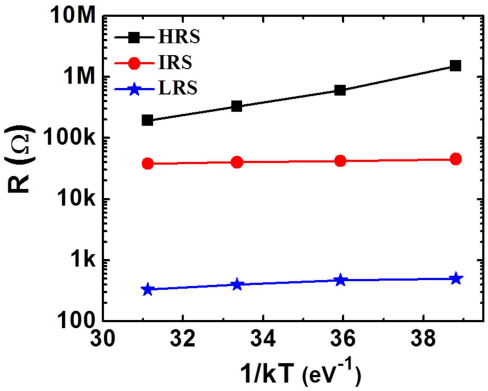

Fig. 5. Temperature dependence of the initial resistance levels of HRS (squares), IRS (circles), and LRS (stars).

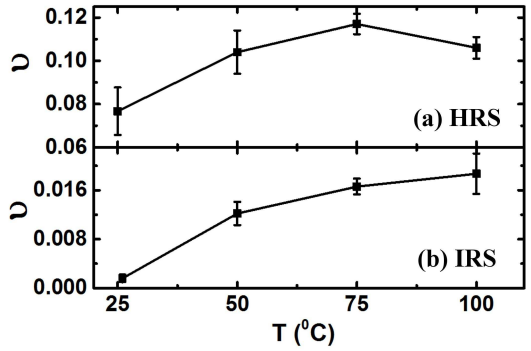

Fig. 6. Variation of the drift coefficient with temperature for (a) reset and (b) intermediate states. Drift coefficients are extracted at each temperature from the resistance drift after programming.

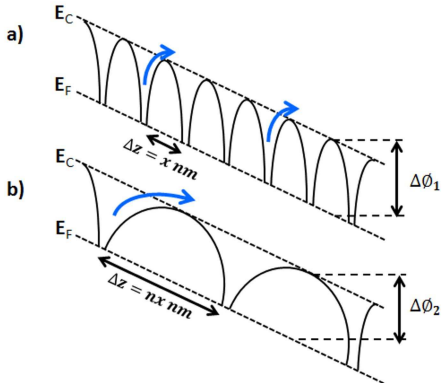

Fig. 7. Schematic of the hopping conduction mechanism through traps in a PCM device.

states display a variety of drift coefficient values depending on the exact resistance (smaller with decreasing resistance) in the range 0.02–0.09 [15], [17], [18], we have consistently observed much lower drift coefficients for the stable IRS (as low as 0.0016 as in the case of the sample in Fig. 6). This indicates that IRS having a wider programming range is far more stable than a PRS.

Lower drift coefficients in IRS can be explained by an increased number of defect states reducing the overall activation energy for traps E_A, as discussed in Section III. An analysis of the temperature dependence of the device resistances can help evaluate E_A. In Fig. 5, all the three resistance levels are plotted against $1/k_BT$, where k_B is the Boltzmann constant and T is the temperature, which varies between 25 °C and 100 °C. The data follow Arrhenius formalism:

$$R = R_0 \exp\left(\frac{E_A}{k_B T}\right). \tag{2}$$

The data are fit to the above equation to estimate E_A. A considerable amount of change with temperature is observed for HRS and the fit yields a barrier activation energy of 0.23 eV, consistent with [19] and [9]. There is minimal change for LRS and IRS. IRS reveals a very small activation energy of 0.02 eV. Studies that evaluate the behavior of E_A with annealing conditions and amorphous layer thickness show that it is smaller in devices with a higher number of closely packed defect states and with very thin amorphous layers [9], [15], [20].

Resistance drift is monitored for the same sample, at different temperatures as displayed in Fig. 6. Due to accelerated annihilation of bulk defect states, the resistance drift in HRS appears to increase with temperature, from 0.07 at room temperature to 0.12 at 75 °C, after which it begins to decrease due to spontaneous crystallization. The interesting behavior is that the drift coefficient of IRS plateaus at this temperature having increased from 0.0016 to 0.02.

III. Physical Interpretation

In order to understand the conduction mechanism in IRS, the data are compared with the existing models in the literature. Conduction through a PCM cell is dominated by thermally activated hopping of charge carriers across coulombic donor-like traps [21], [22]. The drift mechanism in the amorphous phase is explained by thermal annihilation of defects. Fig. 7(a) shows a schematic drawing of the energy profile for the amorphous phase. Defect energy levels are introduced between the Fermi level E_F and the conduction band E_C. For a relatively large number of defects, intertrap distances are short and the barrier height depends linearly on

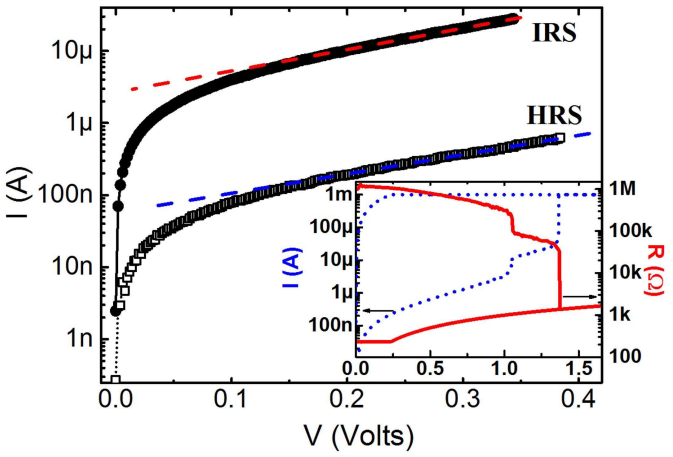

Fig. 8. I–V characteristics in the subthreshold regime for reset (squares) and intermediate (circles) states of a 90-nm square contact PCM cell. The linear fits to $\ln I(V)$, indicated by the dashed lines, reveal the STS. Inset: the full switching dynamics, I on the left scale with a dotted line and R on the right scale with a solid line, starting from an HRS to an IRS then to LRS with a limit current of 1 mA.

the applied voltage bias V (Poole voltage dependence) [21]

$$\Delta\phi_1 \approx E_C - E_F - \frac{qV\Delta z}{k_B T} \tag{3}$$

where q is the electron charge, V is the voltage across the device, and Δz is the average distance between the traps.

As the trap concentration is reduced, the intertrap distance gets bigger as illustrated in Fig. 7(b), resulting in an increase in the device resistance. Poole–Frenkel model predicts that as the traps become independent, the energy barrier becomes [21]

$$\Delta\phi_2 \approx E_C - E_F - q\sqrt{\frac{qV}{\pi\varepsilon u_a}} \tag{4}$$

where ε is the dielectric constant of the amorphous chalcogenide and u_a is the thickness of the amorphous region. In the hopping conduction mechanism, the current through the device I can be expressed as a function of the trap concentration in the gap above the Fermi level, $N_{T,\text{tot}}$

$$I = 2qAN_{T,\text{tot}}\frac{\Delta z}{\tau_0}\exp\left(-\frac{E_C - E_F}{k_B T}\right)\sinh\left(\frac{qV}{k_B T}\frac{\Delta z}{2u_a}\right) \tag{5}$$

where A is the area of the top contact and τ_0 is the characteristic attempt to escape time [19]. For large voltages, in the subthreshold regime, $\Delta\phi$ and hence $\ln\ (I(V))$ vary linearly with V. The slope of the $\ln\ (I(V))$ curve, the so-called subthreshold slope (STS), can be formulized as

$$\text{STS} = \frac{\partial \ln(I)}{\partial V} = \frac{q}{k_B T}\frac{\Delta z}{2u_a}. \tag{6}$$

The current–voltage (I–V) characteristics are investigated in Fig. 8. The inset shows the full switching dynamics starting from an HRS toward a crystalline state. The interesting behavior is that the device switches to the stable IRS before being set. In the subthreshold voltage regime, $\ln(I)$ is observed to scale linearly with V for both IRS and HRS, shown by the dashed lines of Fig. 8 indicating the existence of a high number of closely packed defect states. The amorphous thickness is estimated using the threshold voltage V_{th} and electric field F_{th} as $u_a = V_{\text{th}}/F_{\text{th}}$ [23]. This, together with the STS extracted from the fits to the I–V curve, is utilized to calculate the intertrap distance Δz. Table I lists these parameters obtained from the I–V curves for the sample of Fig. 8 and along with a different square contact sample.

TABLE I
PARAMETERS EXTRACTED FROM I–V CURVES

Sample	State	STS	R (kΩ)	u_a (nm)	Δz (nm)	v	N (#/cm^3)
A	IRS	5.29	22	13.2	3.5	0.002	2.9x10^{21}
	HRS	4.67	3500	23.8	5.5	0.062	1.3x10^{19}
B	IRS	6.95	27	13	4.7	0.02	1.3x10^{21}
	HRS	6.24	1330	20	6.8	0.11	2.1x10^{19}

At low voltages, electrons can hop between traps in forward and reverse directions reducing (5) to a linear I–V regime [19]

$$I \approx \frac{q^2 AN_{T,\text{tot}}\Delta z^2}{k_B T\tau_0 u_a}\exp\left(-\frac{E_C - E_F}{k_B T}\right)V. \tag{7}$$

The slope of $I(V)$, of Fig. 8, in this regime yields the device resistance as 27 kΩ for IRS and 1.33 MΩ for HRS, also listed in Table I. The total number of traps $N_{T,\text{tot}}$ can be calculated using these resistance values in (7)

$$N_{T,\text{tot}} \approx \frac{I}{V}\frac{k_B T\tau_0 u_a}{q^2 A\Delta z^2}\exp\left(\frac{E_C - E_F}{k_B T}\right). \tag{8}$$

An estimate for the energy difference between E_F and E_C can be acquired from temperature-dependent measurements in the low-bias regime. In [19], it is shown that at low bias E_A is independent of the voltage and $E_A = E_C - E_F - k_B T$. The activation energy estimated in Section II for HRS 0.23 eV is used to calculate the energy difference as $E_C - E_F = 0.26$ eV. Even though the activation energy term E_A changes in time, this energy difference remains constant and is used to evaluate the time dependence of $N_{T,\text{tot}}$ for HRS and IRS.

It is evident from Table I that programming the device for an IRS induces a thinner amorphous layer. The intertrap distance is smaller than that for HRS indicating a larger number of defects, indeed a two orders of magnitude difference is recorded for most samples. Fig. 9 shows the variation of the number of defects as a function of wait time after programming, which is acquired using the I–V data at each time using time-independent $E_C - E_F = 0.26$ eV. While HRS defect population decreases by a factor of 4, for a wait time of 100 min, the IRS defect population appears to be almost constant in time, suggesting a tiny decrease only in the second decimal digit.

For further clarification, we refer to a previous study of a comprehensive 3-D finite-element model with adaptive meshing as discussed in detail in [8]. In summary, this model is a multiphysics approach that takes into account temperature- and phase-dependent electrical and thermal characteristics of the materials. In addition, homogeneous and heterogeneous nucleation and growth kinetics are considered to obtain a complete picture of the switching.

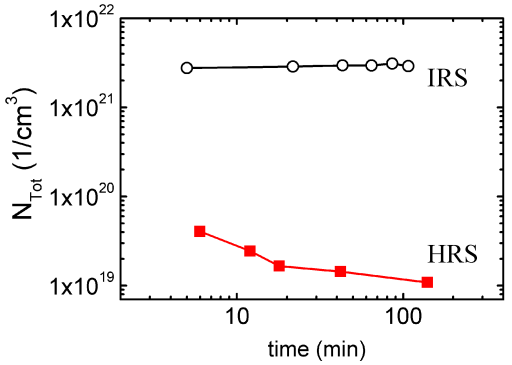

Fig. 9. Effective number of defects is calculated for various wait times after programming in IRS and HRS.

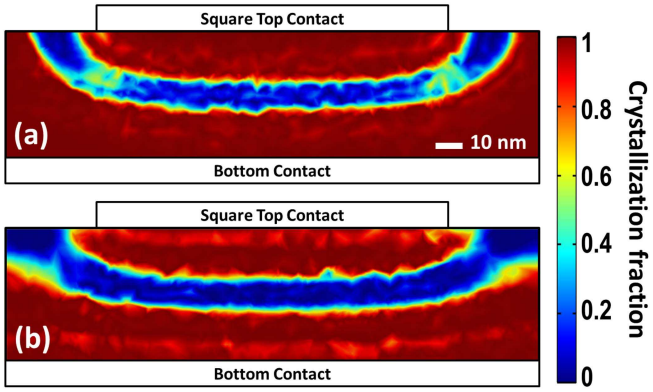

Fig. 10. Simulation of the vertical cross section of a 130-nm square-top contact device taken through the center right after a programming pulse of 100-ns width and 42-ns trailing edge with amplitudes a) 0.95 V, b) 1.1 V setting it to a IRS (a) or HRS (b). Crystallization fraction f inside the phase change layer is shown in color code which corresponds to $f = 1$ (red) for crystalline and $f = 0$ (blue) for amorphous phases. The colors between the two represent regions with a mixture of crystalline and amorphous phases.

Fig. 10 demonstrates the result of the simulation for a 130-nm square-top contact PCM device, after a programming voltage pulse is applied to the set state. Phase transition occurs in a dome-shaped active region inside the GST layer [2], [24], [25] which is fully amorphous for an HRS of 178 kΩ achieved with a 1.1 V 100-ns pulse [Fig. 10(b)]. IRS in Fig. 10(a) is obtained by a 0.95 V pulse and the corresponding resistance is 18.3 kΩ. The amorphous region in IRS is thinner and has areas with mixed phase indicated by yellow to green areas. These regions are a result of the current crowding effect, which causes hot spots within the active region [8] and form current shunting paths. Therefore, IRS has a lower resistance and a much lower E_A. The increased number of defects in IRS is explained by the smaller amorphous thickness to amorphous–crystalline interfacial area ratio. Therefore, the conduction in IRS is dominated by interface states instead of bulk defects. This accounts for the surprisingly low drift coefficient for IRS. While annihilation of bulk defects causes a drastic resistance increase in HRS, they impose only a small change in IRS.

IV. Conclusion

The resistance drift behavior observed in the reset state of all samples is found to be consistent with the conventional SR mechanism. The conduction characteristics obtained from subthreshold I–V measurements reveal thermally assisted hopping of carriers off defect states introduced in the band gap of the amorphous GST with an initial activation energy of 0.23 eV. The intertrap distance is estimated to be 5.5–7 nm with an effective trap concentration on the order of 10^{19} 1/cm^3. The drift coefficient of HRS (0.07–0.1) is strongly temperature dependent due to accelerated annihilation of bulk defects.

We compare HRS with a stable IRS with a wide range of programming amplitudes in samples with square contact geometry. Simulations show that IRS has regions of mixed phase inside the active region of the GST. This zone is thought to provide a large interfacial area between the amorphous and crystalline regions and therefore a smaller amorphous thickness to amorphous-crystalline interfacial area ratio. Our data suggest that the conduction is through defect states just like HRS but with a smaller intertrap distance and a much larger effective defect density, 10^{21} 1/cm^3. This can be explained by considering the significant contribution of interfacial defects to the total defect density in the case of a thin mixed phase active layer in IRS.

Furthermore, unlike the bulk defects that annihilate in time increasing the intertrap distance, the interfacial defects are found to be stable, yielding at least an order of magnitude decrease in the drift coefficient of IRS. The residual low drift can still be attributed to the bulk SR mechanism, which explains the small increase in the drift coefficient with temperature as well.

We conclude that an intermediate mixed phase state with a large programming window that is induced in a nonuniform current injection device displays a much superior long-term stability compared with the fully amorphous reset state. The current in IRS is dominated by conduction of carriers through interfacial defect states which do not anneal away in time. Such a stable set of IRS levels can potentially be utilized in future multiple-bit-per-cell memory technologies that meet the long-term reliability and data stability requirements.

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