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**ELE227 FUNDAMENTALS OF DIGITAL SYSTEM LABORATORY**

**PRELIMINARY WORK-1**

**Student**

**Name: Egemen Can**

**Surname: Ayduğan**

**ID: 21728036**

**1)**

**a.**

**b.**

**c.**

**d.**

**e.**

**2)**

**a.**

**b.**

**c.**

**d.**

**e.**

**3.A)**

**VHDL Implementation:**

entity pre3vhdl is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : in STD\_LOGIC;

F : out STD\_LOGIC);

end pre3vhdl;

architecture Behavioral of pre3vhdl is

begin

F <= ((not A)and(not B)and C)or

((not A)and B and (not C))or

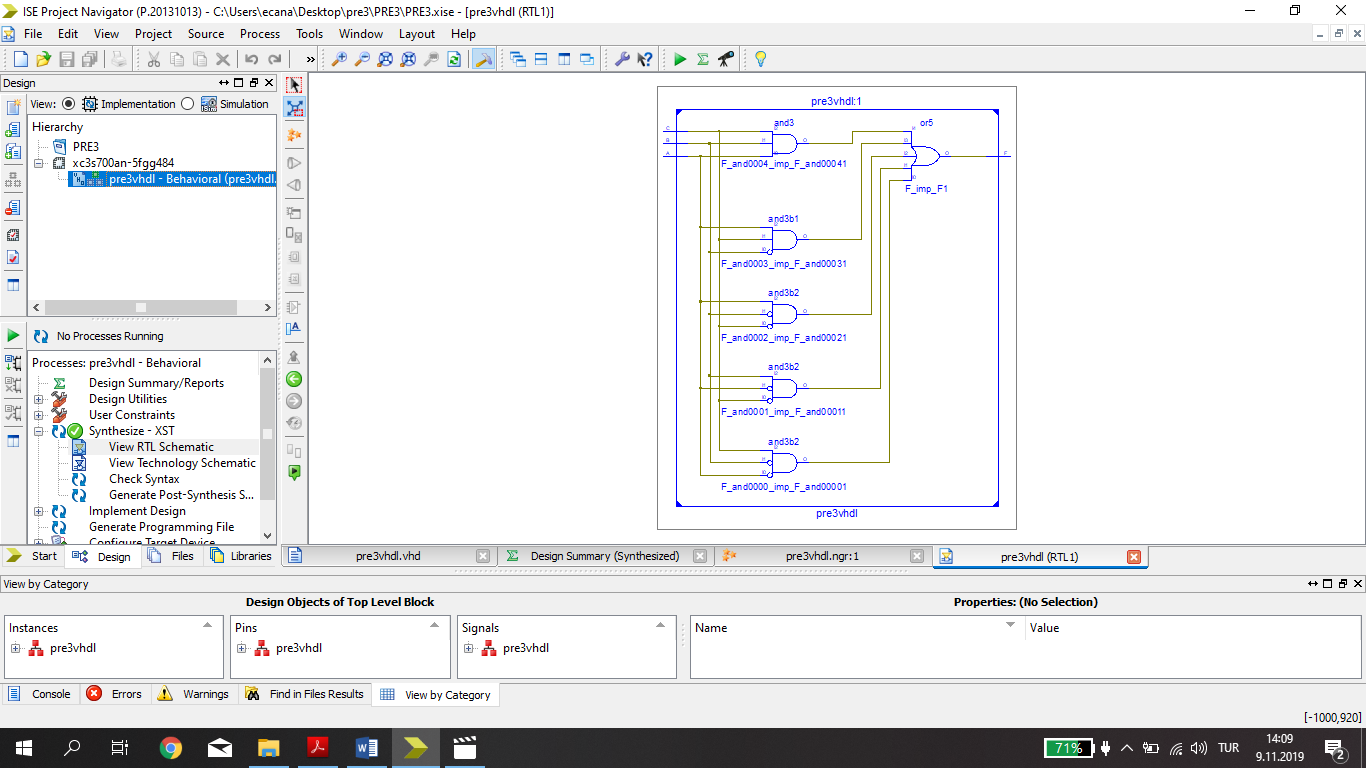
(A and(not B)and (not C))or

(A and(not B)and C)or

(A and B and C);

end Behavioral;

**RLT Schematic:**



**3.B)**

**TEST BENCH INPUT:**

stim\_proc: process

begin

-- hold reset state for 100 ns.

A <='0';

B <='0';

C <='0';

wait for 100 ns ;

A <='0';

B <='0';

C <='1';

wait for 100 ns ;

A <='0';

B <='1';

C <='0';

wait for 100 ns ;

A <='1';

B <='0';

C <='0';

wait for 100 ns ;

A <='1';

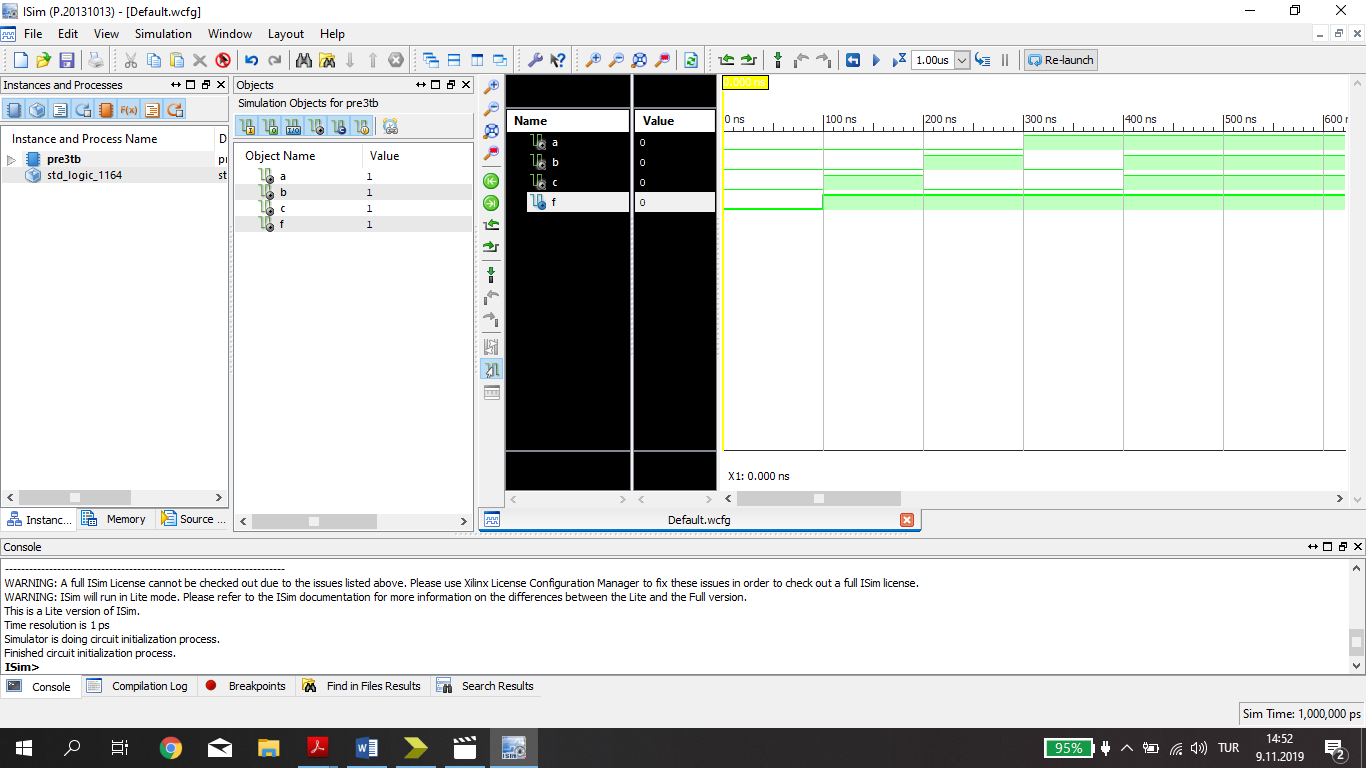
B <='1';

C <='1';

wait;

end process;

**TEST BENCH RESULTS:**



**4.A)**

**T1=**

**T2=**

**T3=**

**T4=**

**F1=**

**F2=**

**4.B)**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **T1** | **T2** | **T3** | **T4** | **F1** | **F2** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **0** | **1** | **0** | **1** | **1** | **1** | **1** |
| **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **0** | **1** | **0** | **1** | **0** | **1** |
| **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **1** |
| **1** | **0** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1** | **1** | **1** | **0** | **0** | **0** | **1** | **1** | **1** | **1** |
| **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** |

**4.C)**

**4.D)**

**VHDL Implementation:**

entity PRE4 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : in STD\_LOGIC;

D : in STD\_LOGIC;

F1 : out STD\_LOGIC;

F2 : out STD\_LOGIC);

end PRE4;

architecture Behavioral of PRE4 is

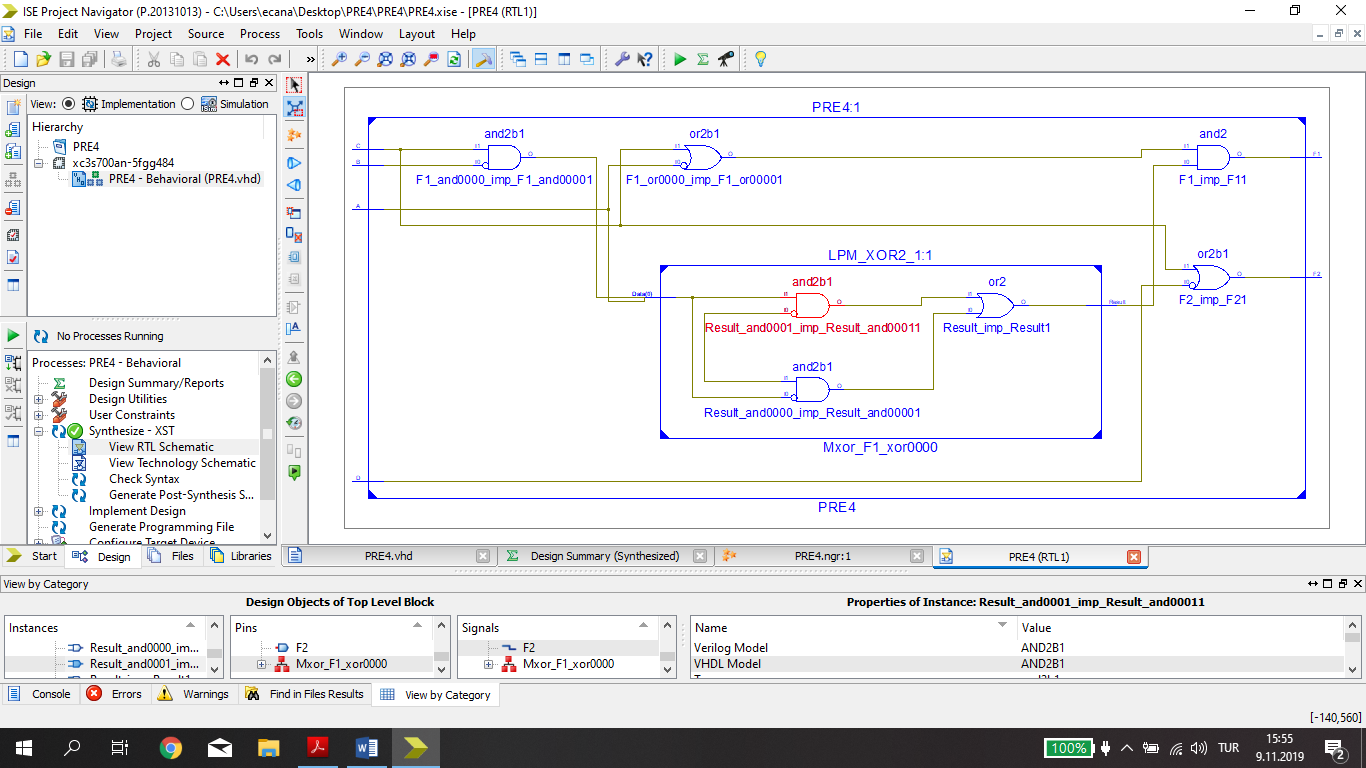
begin

F1 <= ( A xor ((not B)and C)) and ((not A) or C);

F2 <= (C and D) or (not D);

end Behavioral;

**RLT Schematic:**



**4.E)**

**TEST BENCH INPUT:**

stim\_proc: process

begin

-- hold reset state for 100 ns.

A <= '0';

B <= '0';

C <= '0';

D <= '0';

wait for 100 ns;

A <= '0';

B <= '0';

C <= '0';

D <= '1';

wait for 100 ns;

A <= '0';

B <= '0';

C <= '1';

D <= '0';

wait for 100 ns;

A <= '0';

B <= '1';

C <= '0';

D <= '0';

wait for 100 ns;

A <= '1';

B <= '0';

C <= '0';

D <= '0';

wait for 100 ns;

A <= '1';

B <= '1';

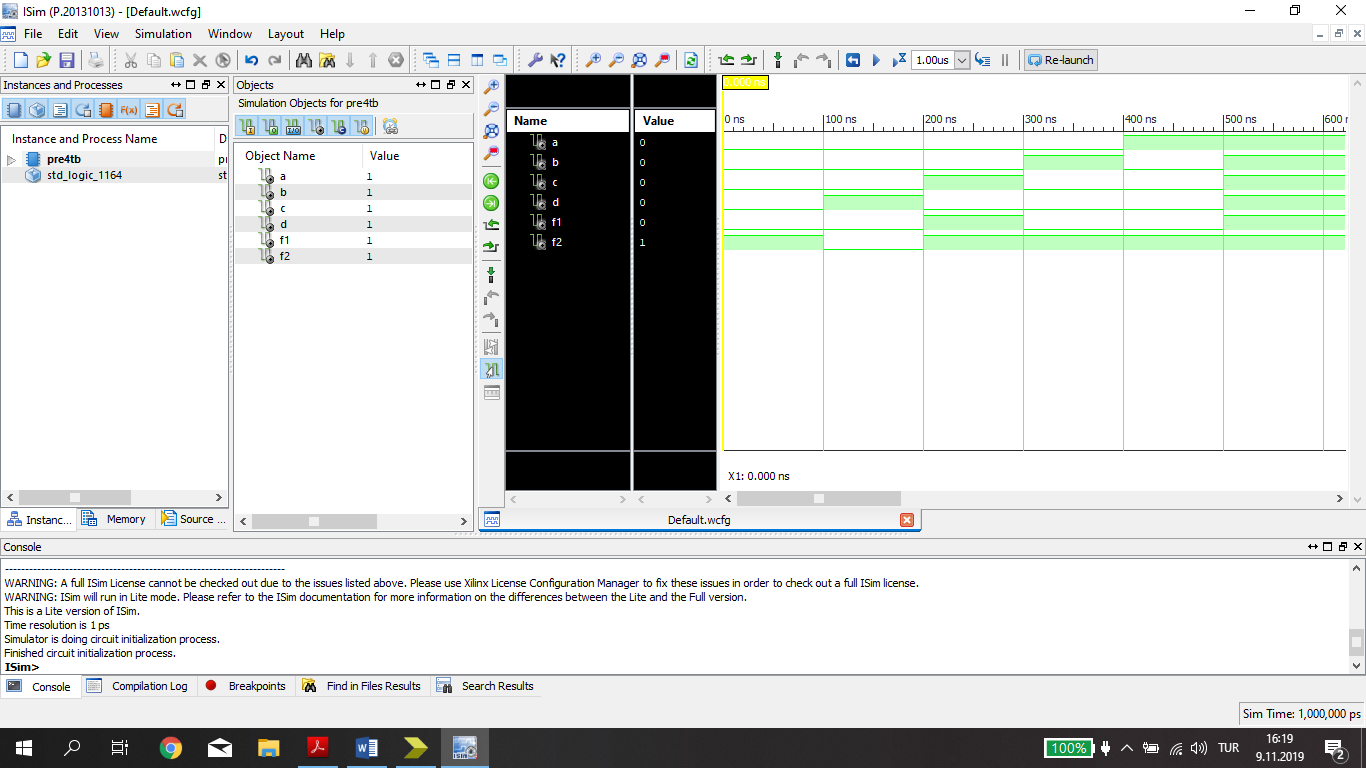
C <= '1';

D <= '1';

wait;

end process;

**TEST BENCH RESULTS:**



**5.A)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **x** | **y** | **z** | **A** | **B** | **C** |
| **0** | **0** | **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **0** | **0** | **1** | **1** |
| **0** | **1** | **1** | **1** | **0** | **0** |
| **1** | **0** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **1** | **0** | **0** |
| **1** | **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** | **0** |

**A =**

**B=**

**C=**

**5.B)**

**5.C)**

**VHDL Implementation:**

entity PRE5VHDL is

Port ( x : in STD\_LOGIC;

y : in STD\_LOGIC;

z : in STD\_LOGIC;

A : out STD\_LOGIC;

B : out STD\_LOGIC;

C : out STD\_LOGIC);

end PRE5VHDL;

architecture Behavioral of PRE5VHDL is

begin

A <= ((not x)and y and z)or(x and(not y)and z)or

(x and y and (not z))or (x and y and z);

B <= ((not x)and (not y) and z)or((not x) and y and (not z))or

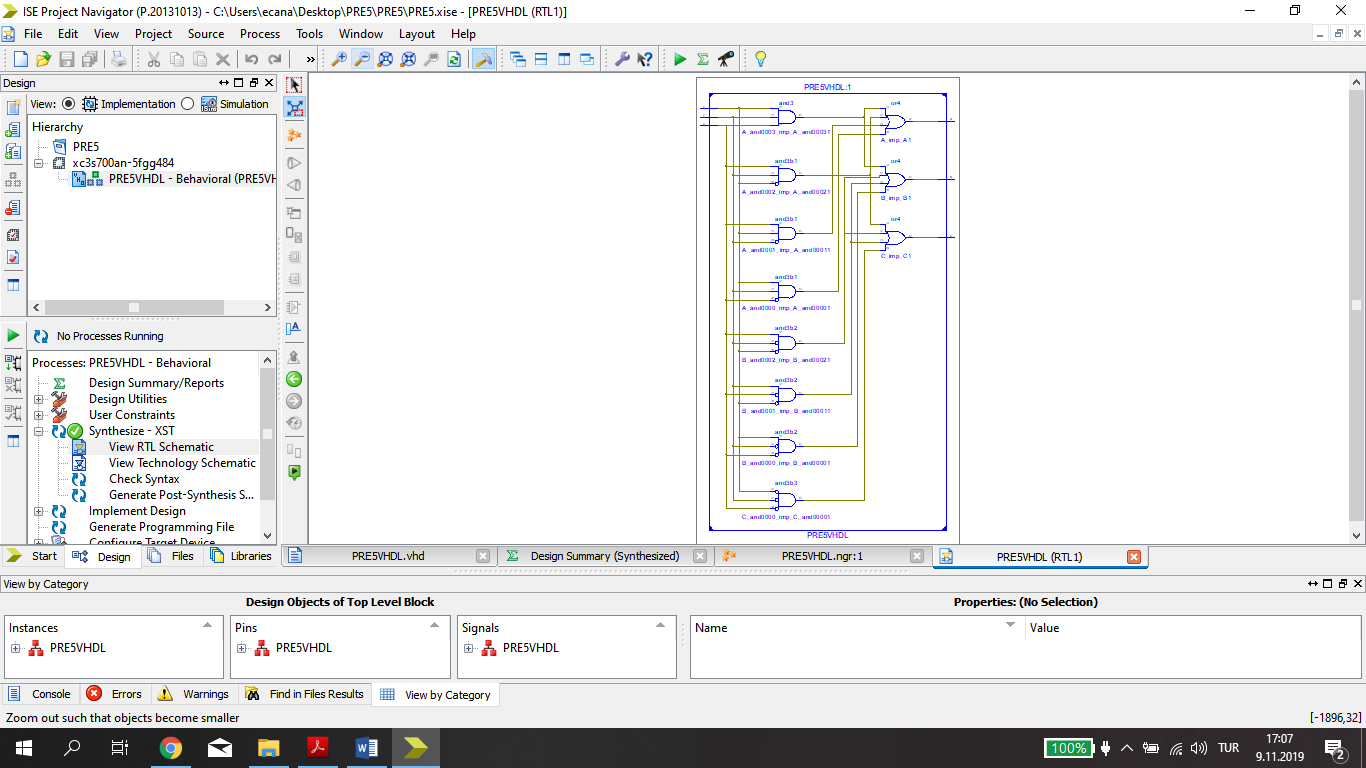
(x and (not y) and (not z))or (x and y and z);

C <= ((not x)and (not y) and (not z))or((not x) and y and (not z))or

(x and (not y) and (not z))or (x and y and (not z));

end Behavioral;

**RLT Schematic:**



**5.D)**

**TEST BENCH INPUT:**

stim\_proc: process

begin

-- hold reset state for 100 ns.

x <='0';

y <='0';

z <='0';

wait for 100 ns;

x <='0';

y <='0';

z <='1';

wait for 100 ns;

x <='0';

y <='1';

z <='0';

wait for 100 ns;

x <='0';

y <='1';

z <='1';

wait for 100 ns;

x <='1';

y <='0';

z <='0';

wait for 100 ns;

x <='1';

y <='0';

z <='1';

wait for 100 ns;

x <='1';

y <='1';

z <='0';

wait for 100 ns;

x <='1';

y <='1';

z <='1';

-- insert stimulus here

wait;

end process;

**TEST BENCH RESULTS:**

