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**ELE227 FUNDAMENTALS OF DIGITAL SYSTEM LABORATORY**

**PRELIMINARY WORK-2**

**Student**

**Name: Egemen Can**

**Surname: Ayduğan**

**ID: 21728036**

**1.)**

**VHDL Implementation:**

entity HALFADDER is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

S : out STD\_LOGIC;

C : out STD\_LOGIC);

end HALFADDER;

architecture Behavioral of HALFADDER is

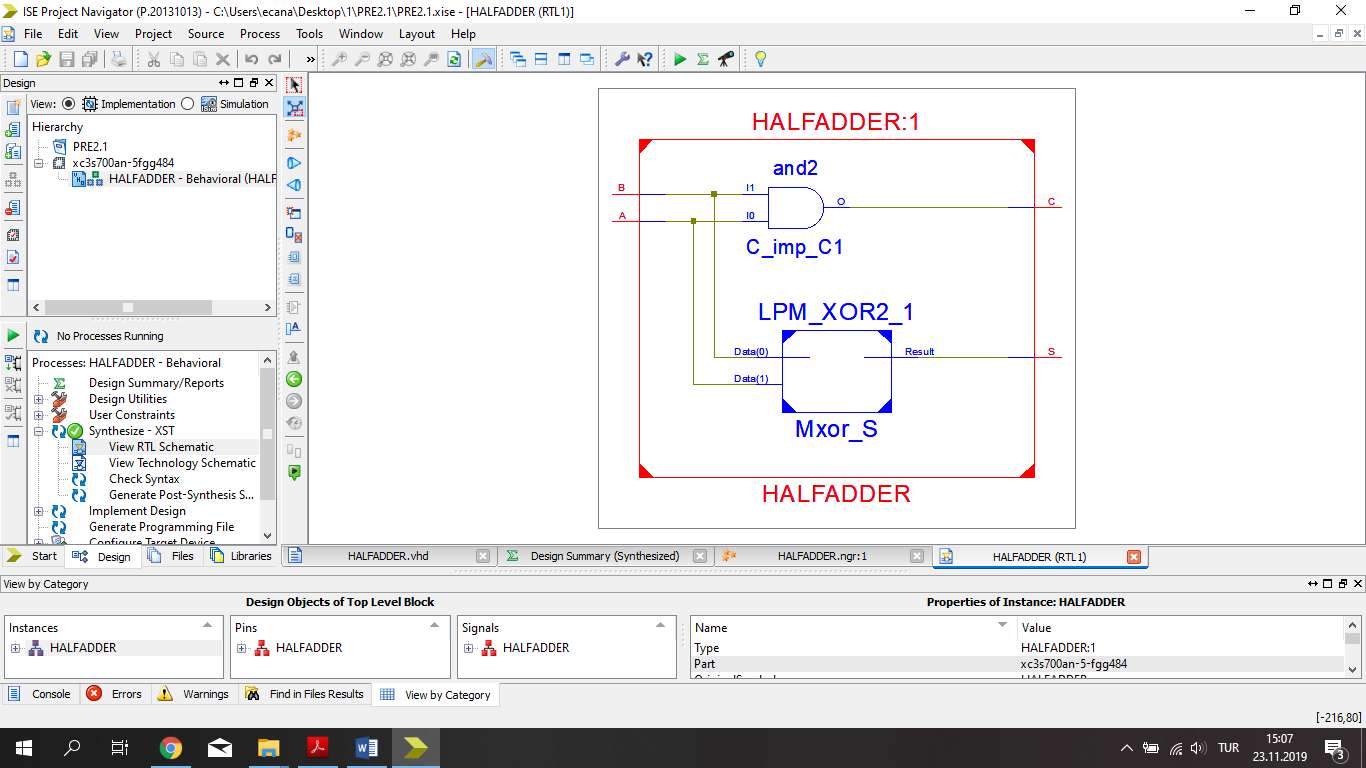
begin

S <= A xor B;

C <= A and B;

end Behavioral;

**RLT Schematic:**



**TEST BENCH INPUT:**

stim\_proc: process

begin

-- hold reset state for 100 ns.

A <= '0';

B <= '0';

wait for 100 ns;

A <= '0';

B <= '1';

wait for 100 ns;

A <= '1';

B <= '0';

wait for 100 ns;

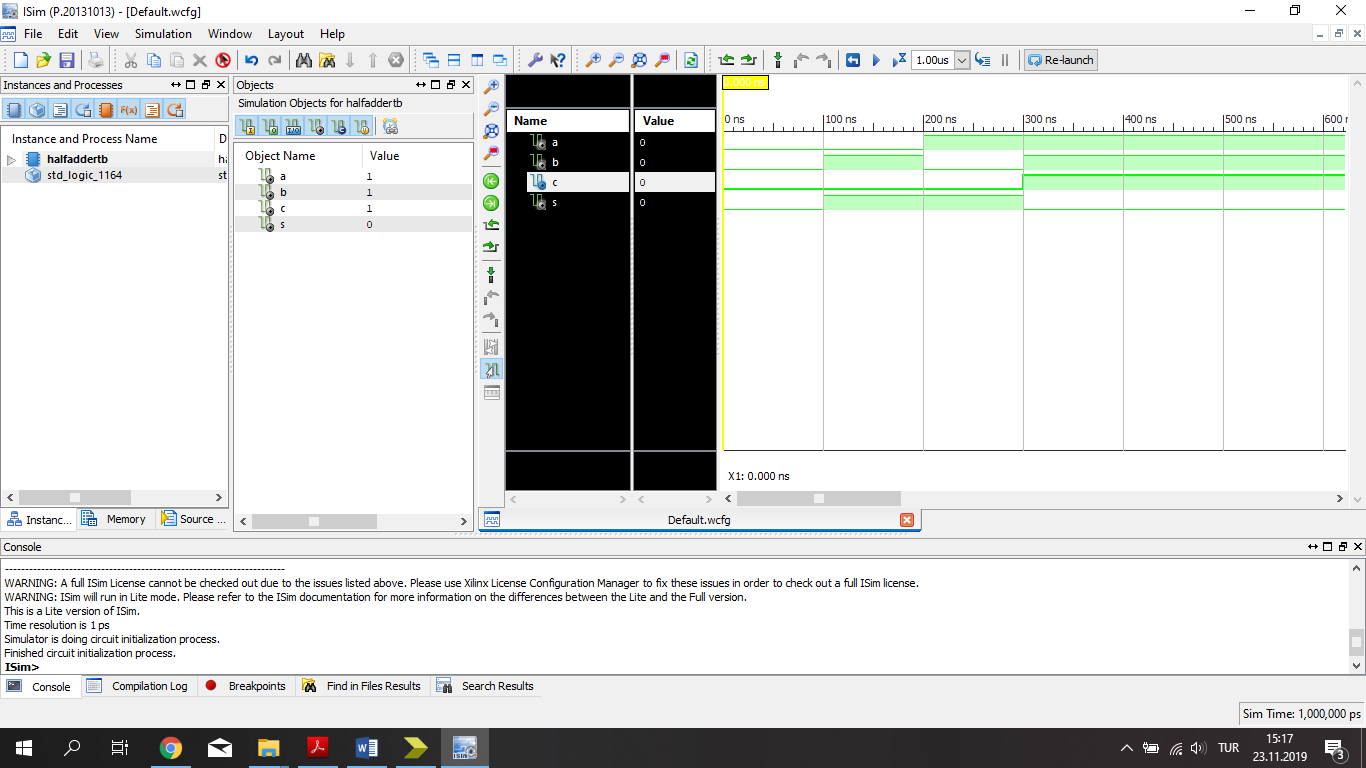
A <= '1';

B <= '1';

wait;

end process;

**TEST BENCH RESULTS:**



**2.)**

**Circuit Diagram:**

|  |
| --- |
|  |

**VHDL Implementation**

entity FA is

Port ( x : in STD\_LOGIC;

y : in STD\_LOGIC;

z : in STD\_LOGIC;

T : out STD\_LOGIC;

F : out STD\_LOGIC);

end FA;

architecture Behavioral of FA is

component HA

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

S : out STD\_LOGIC;

C : out STD\_LOGIC);

end component;

signal T1:STD\_LOGIC;

signal T2:STD\_LOGIC;

signal T3:STD\_LOGIC;

begin

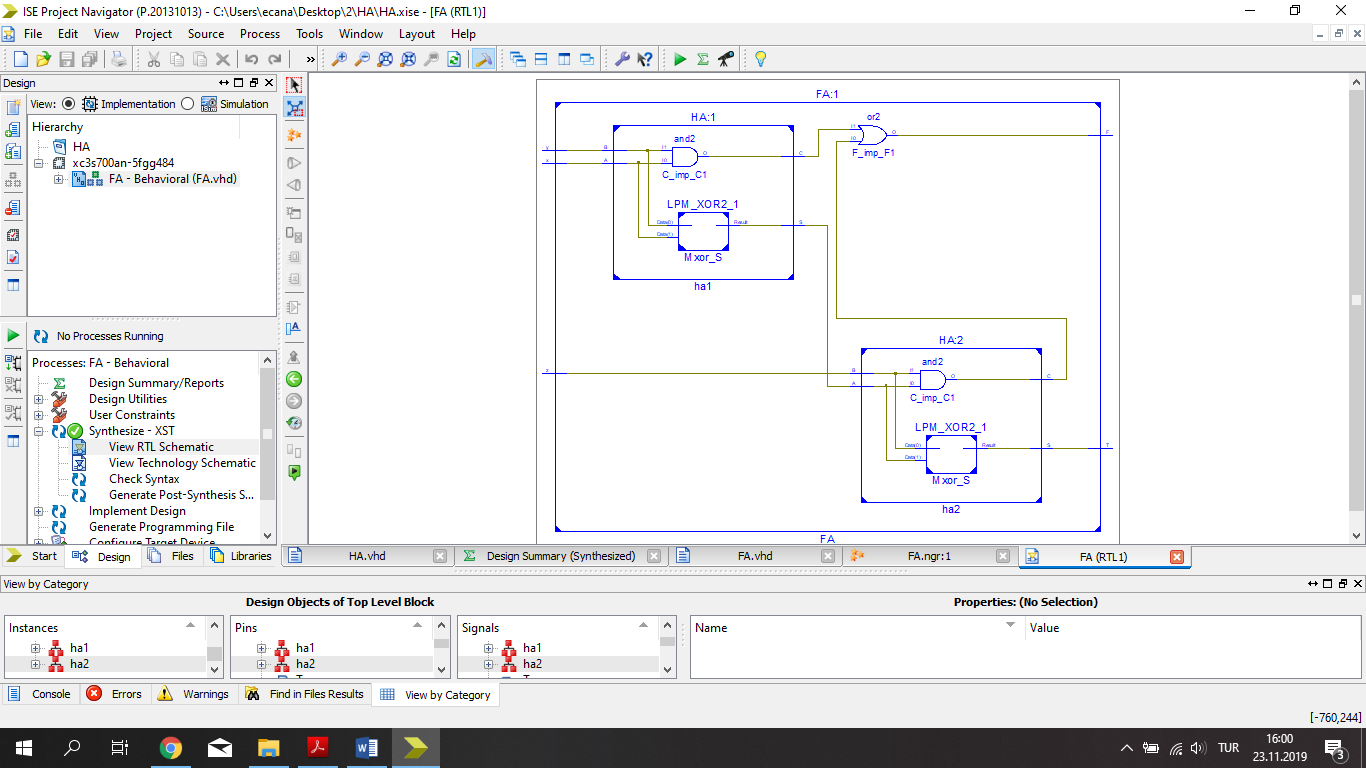
ha1 : HA port map(x,y,T1,T2);

ha2 : HA port map(T1,z,T,T3);

F <= T3 or T2;

end Behavioral;

**RLT Schematic:**



**TEST BENCH INPUT:**

stim\_proc: process

begin

-- hold reset state for 100 ns.

x <= '0';

y <= '0';

z <= '0';

wait for 100 ns;

x <= '0';

y <= '0';

z <= '1';

wait for 100 ns;

x <= '0';

y <= '1';

z <= '0';

wait for 100 ns;

x <= '0';

y <= '1';

z <= '1';

wait for 100 ns;

x <= '1';

y <= '0';

z <= '0';

wait for 100 ns;

x <= '1';

y <= '0';

z <= '1';

wait for 100 ns;

x <= '1';

y <= '1';

z <= '0';

wait for 100 ns;

x <= '1';

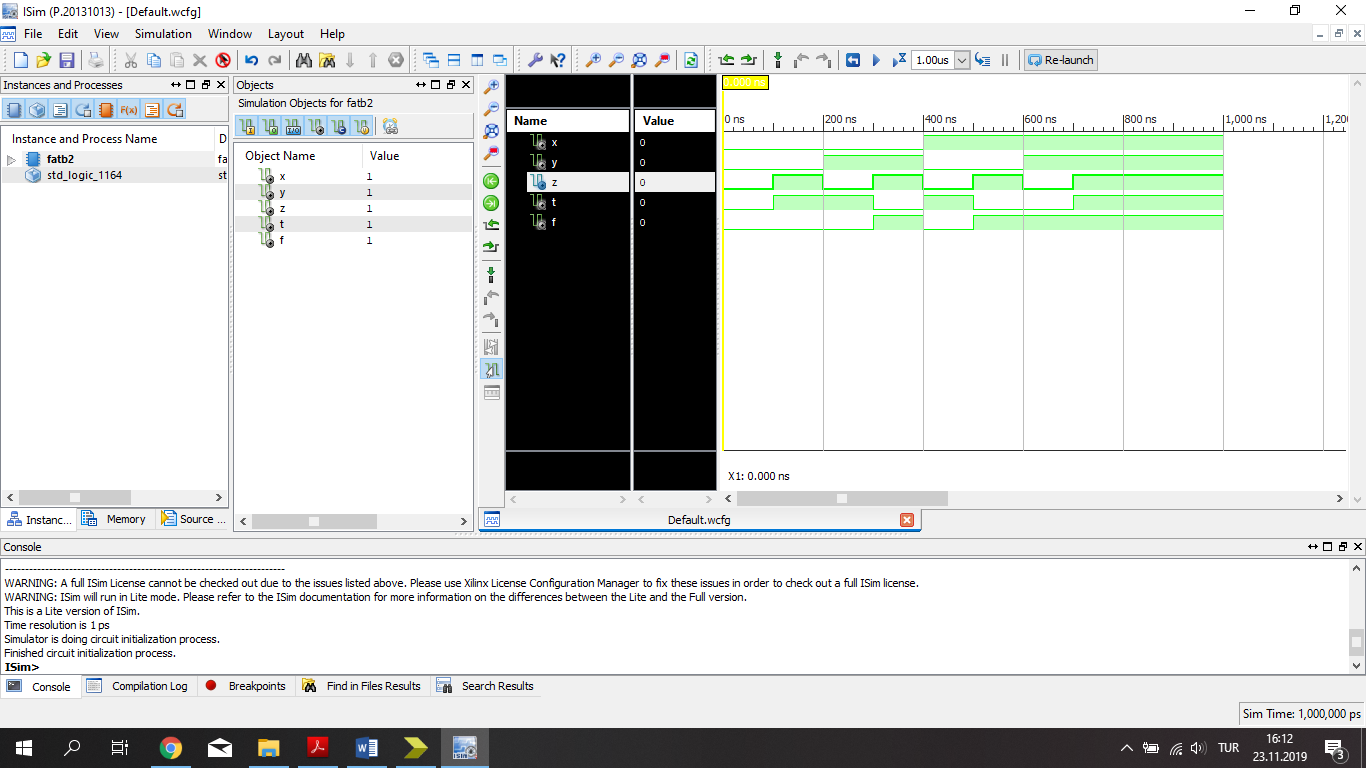
y <= '1';

z <= '1';

wait;

end process;

**TEST BENCH RESULTS:**



**3.)**

**VHDL Implementation**

entity ThreebitAddSub is

Port ( A : in STD\_LOGIC\_VECTOR (2 downto 0);

B : in STD\_LOGIC\_VECTOR (2 downto 0);

M : in STD\_LOGIC;

S : out STD\_LOGIC\_VECTOR (2 downto 0);

C : out STD\_LOGIC);

end ThreebitAddSub;

architecture Behavioral of ThreebitAddSub is

component FA

Port ( x : in STD\_LOGIC;

y : in STD\_LOGIC;

z : in STD\_LOGIC;

T : out STD\_LOGIC;

F : out STD\_LOGIC);

end component;

signal C1,C2,G1,G2,G3 : STD\_LOGIC ;

begin

G1 <= B(0) xor M;

G2 <= B(1) xor M;

G3 <= B(2) xor M;

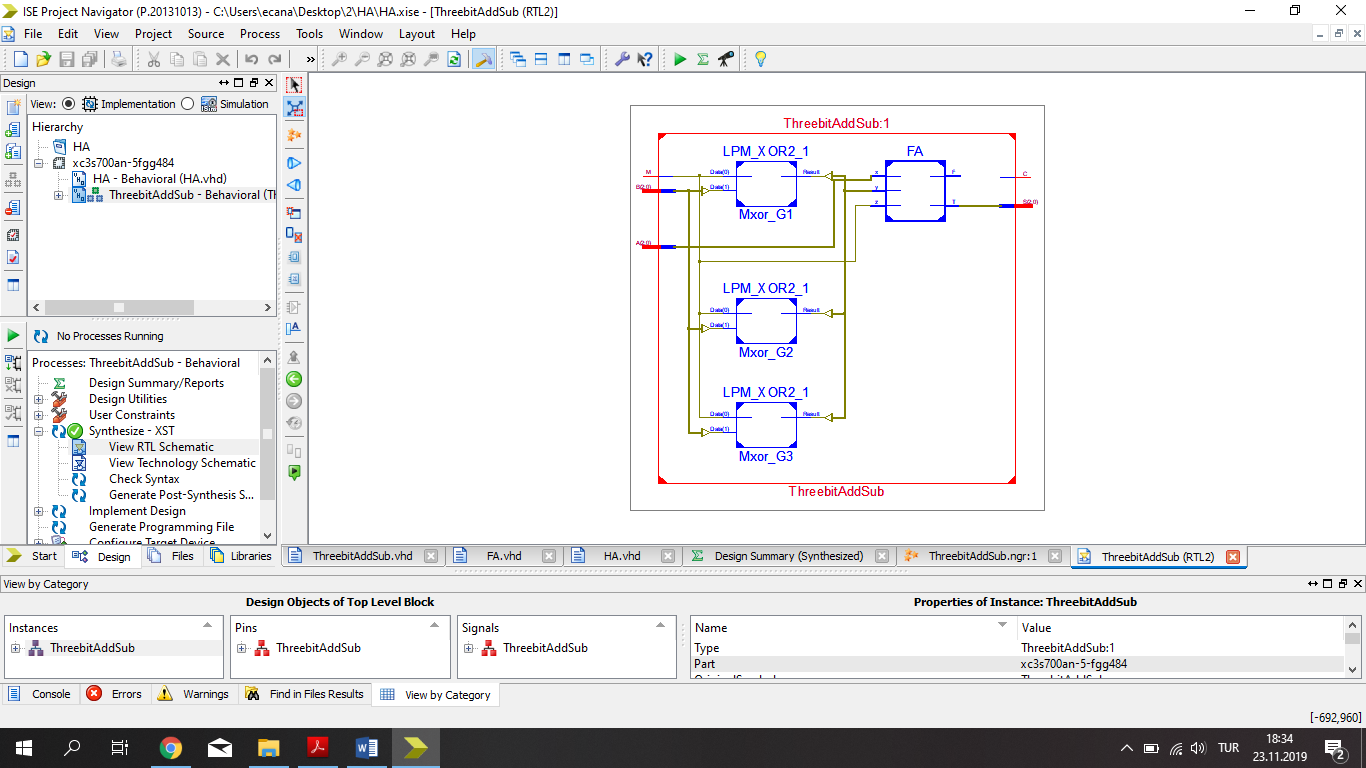
FA1: FA port map(A(0),G1,M,S(0),C1);

FA2: FA port map(A(1),G2,C1,S(1),C2);

FA3: FA port map(A(2),G3,C2,S(2),C);

end Behavioral;

**RLT Schematic:**



**TEST BENCH INPUT:**

stim\_proc: process

begin

A <= "011";

B <= "010";

M <= '0';

wait for 100 ns;

A <= "110";

B <= "001";

M <= '0';

wait for 100 ns;

A <= "101";

B <= "010";

M <= '1';

wait for 100 ns;

A <= "111";

B <= "101";

M <= '1';

wait for 100 ns;

A <= "111";

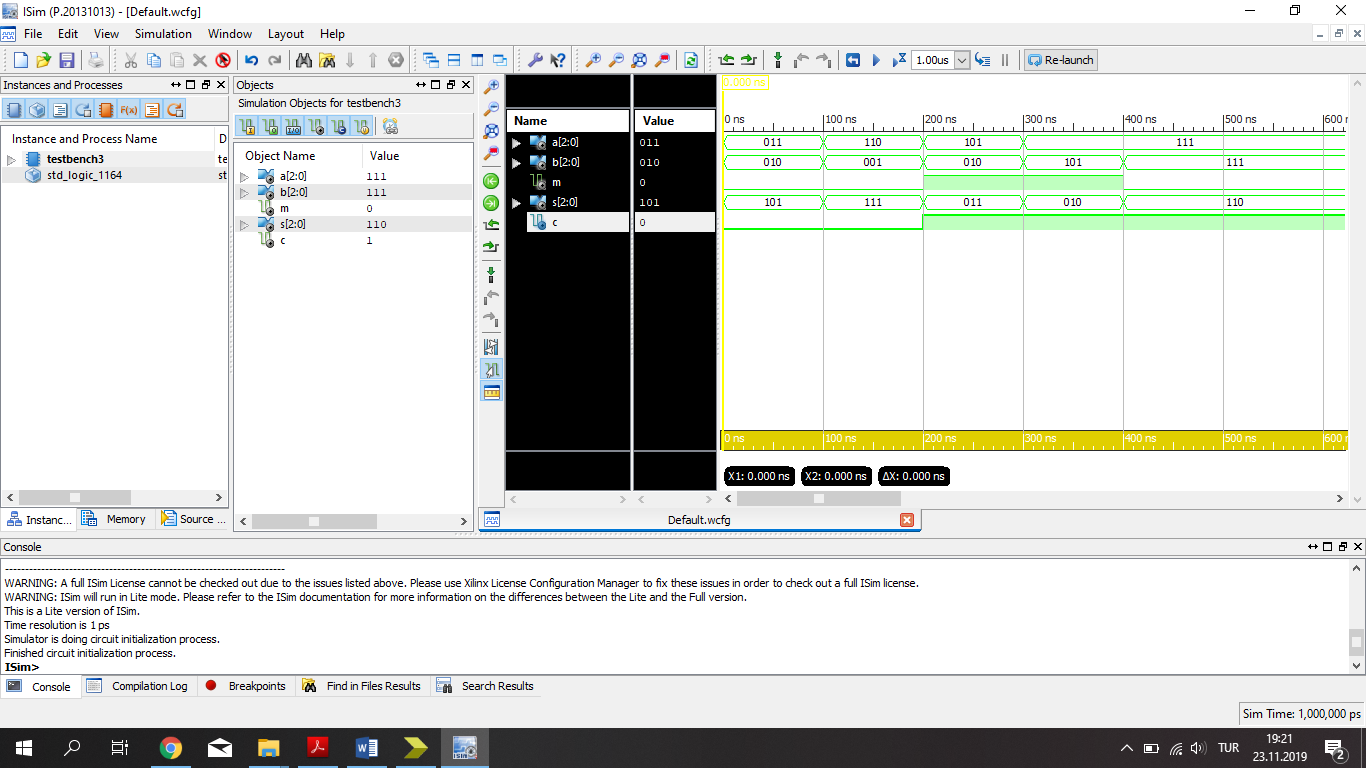
B <= "111";

M <= '0';

wait;

end process;

**TEST BENCH RESULTS:**



**4.)**

**VHDL Implementation**

entity MULTI is

Port ( A : in STD\_LOGIC\_VECTOR (2 downto 0);

B : in STD\_LOGIC\_VECTOR (1 downto 0);

S : out STD\_LOGIC\_VECTOR (4 downto 0));

end MULTI;

architecture Behavioral of MULTI is

component FA

Port ( x : in STD\_LOGIC;

y : in STD\_LOGIC;

z : in STD\_LOGIC;

T : out STD\_LOGIC;

F : out STD\_LOGIC);

end component;

signal C: STD\_LOGIC\_VECTOR (6 downto 0) ;

begin

S(0) <= A(0)and B(0);

M1: FA port map('0',C(0),C(1),S(1),C(2));

M2: FA port map(C(2),C(3),C(4),S(2),C(6));

M3: FA port map('0',C(6),C(5),S(3),S(4));

C(0) <= (A(0)and B(1));

C(1) <= (A(1)and B(0));

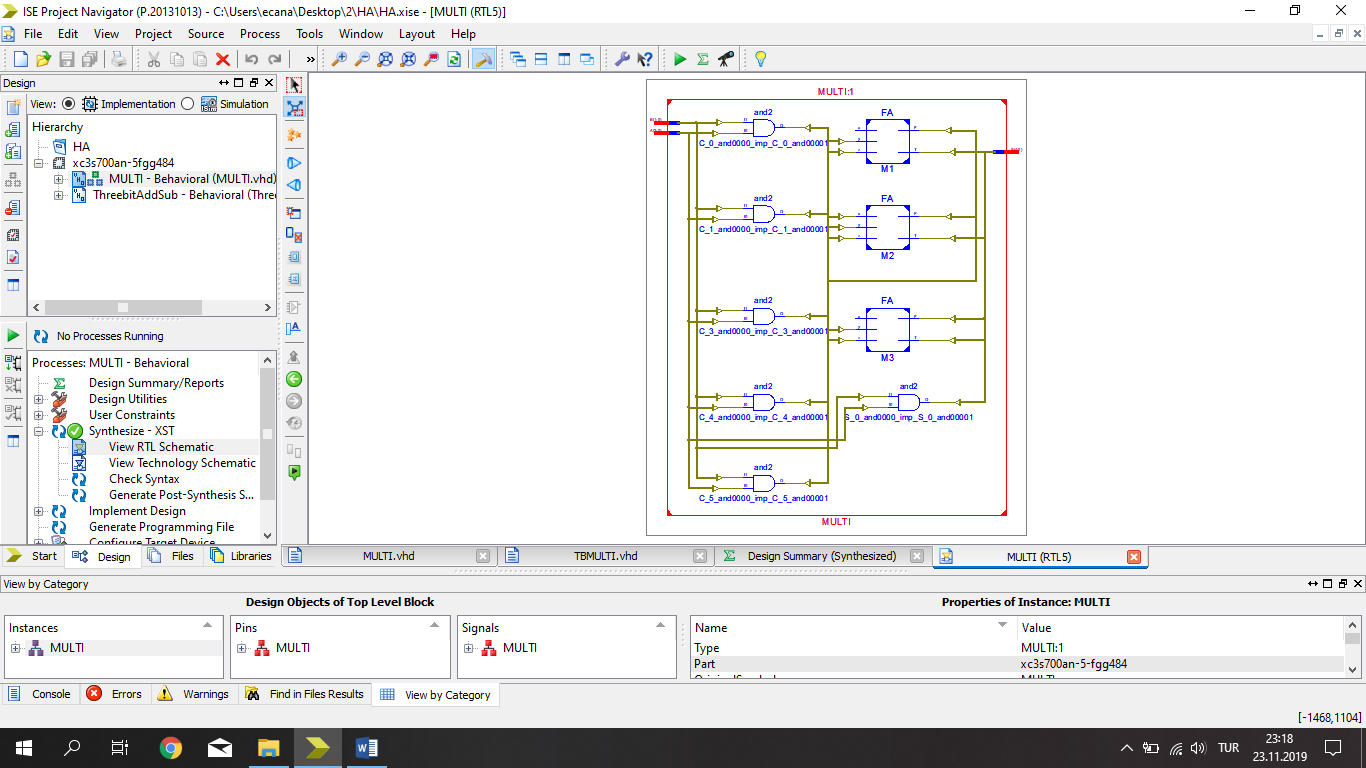
C(3) <= (A(1)and B(1));

C(4) <= (A(2)and B(0));

C(5) <= (A(2)and B(1));

end Behavioral;

**RLT Schematic:**



**TEST BENCH INPUT:**

stim\_proc: process

begin

A <="000";

B <="00";

wait for 100 ns;

A <="001";

B <="01";

wait for 100 ns;

A <="010";

B <="10";

wait for 100 ns;

A <="101";

B <="11";

wait for 100 ns;

A <="111";

B <="01";

wait for 100 ns;

A <="110";

B <="11";

wait for 100 ns;

A <="111";

B <="11";

wait for 100 ns;

wait;

end process;

**TEST BENCH RESULTS:**

