Lab 7 : Design of Multicycle MIPS ISA

Learning outcomes:

- Modeling MIPS Multi-cycle datapath in Verilog
- Implementation of FSM based controller

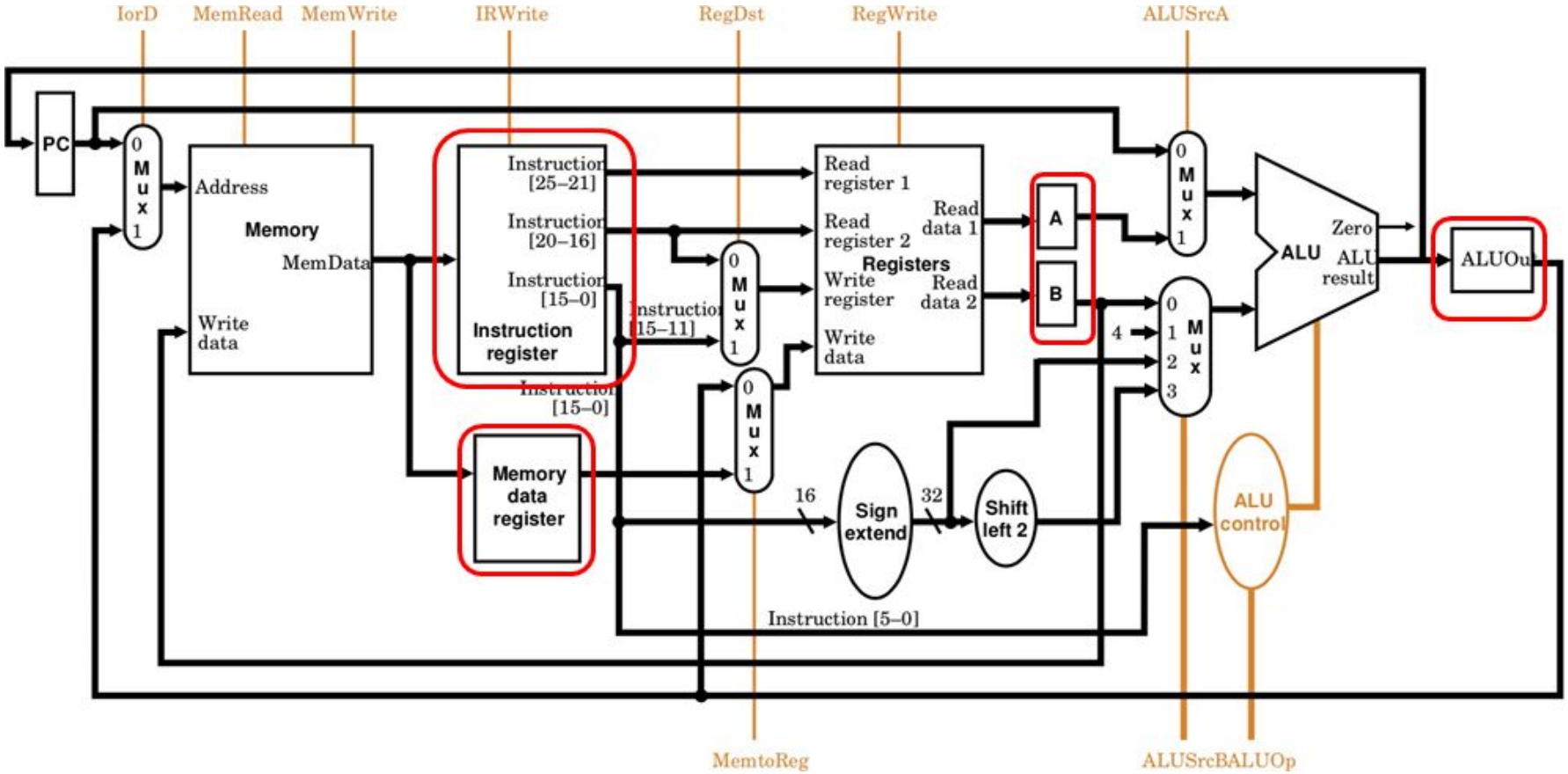
Various phases in multicycle design

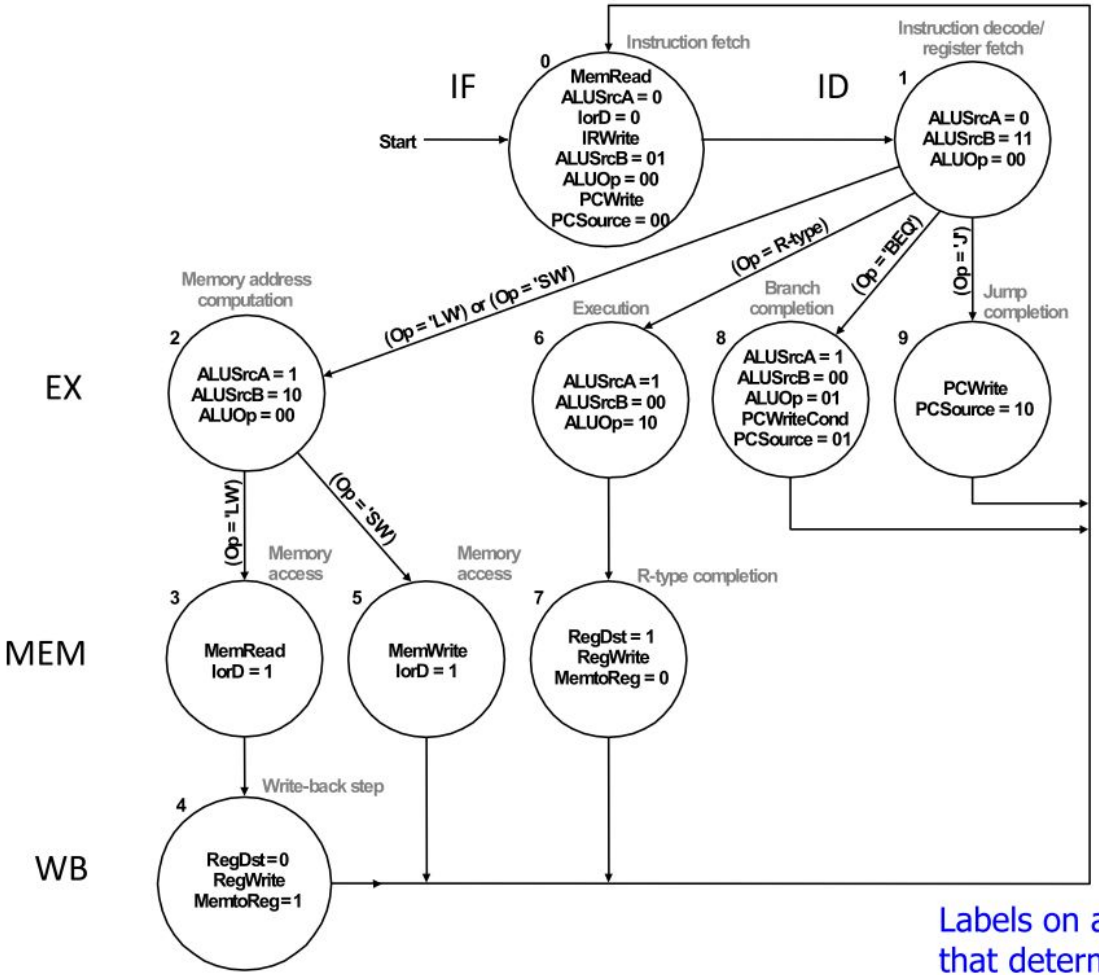
Break instructions into the following potential execution steps – not all instructions require all the steps – each step takes one clock cycle

1. Instruction fetch and PC increment (IF)
2. Instruction decode and register fetch (ID)
3. Execution, memory address computation, or branch completion (EX)
4. Memory access or R-type instruction completion (MEM)
5. Memory write completion (WB)

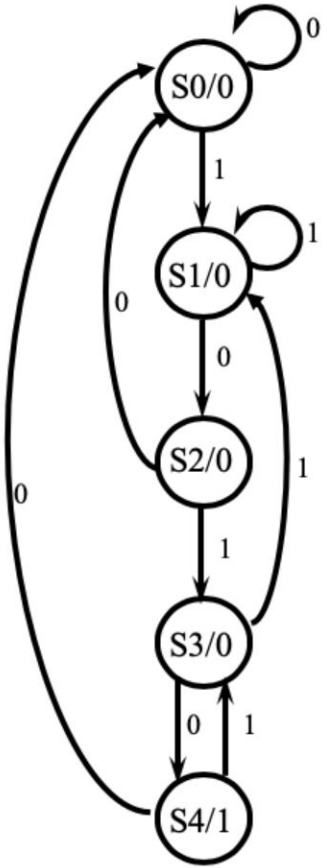
Each MIPS instruction takes from 3 – 5 cycles (steps)

Multi-cycle Datapath Design



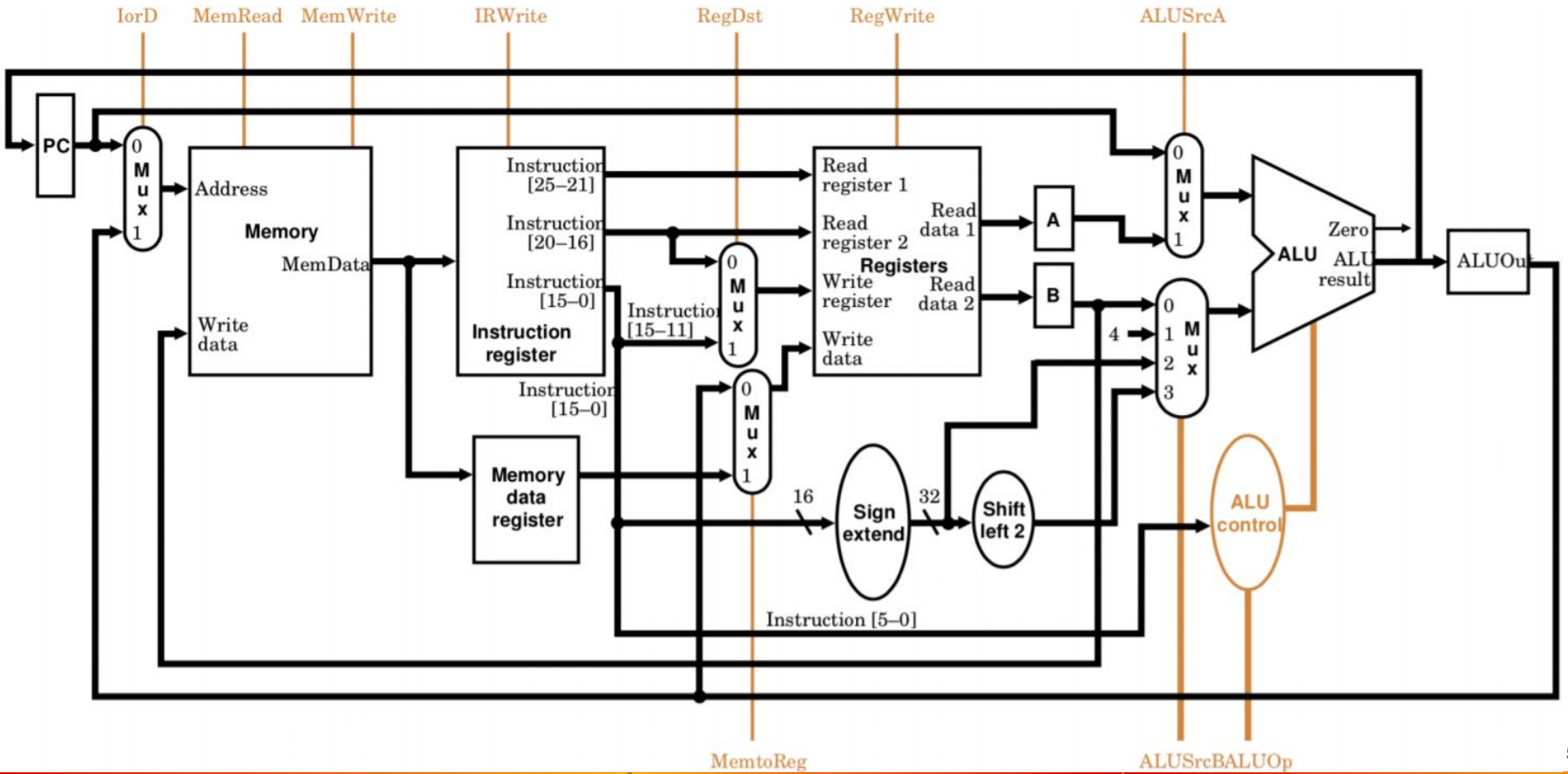


Labels on arcs are conditions that determine next state

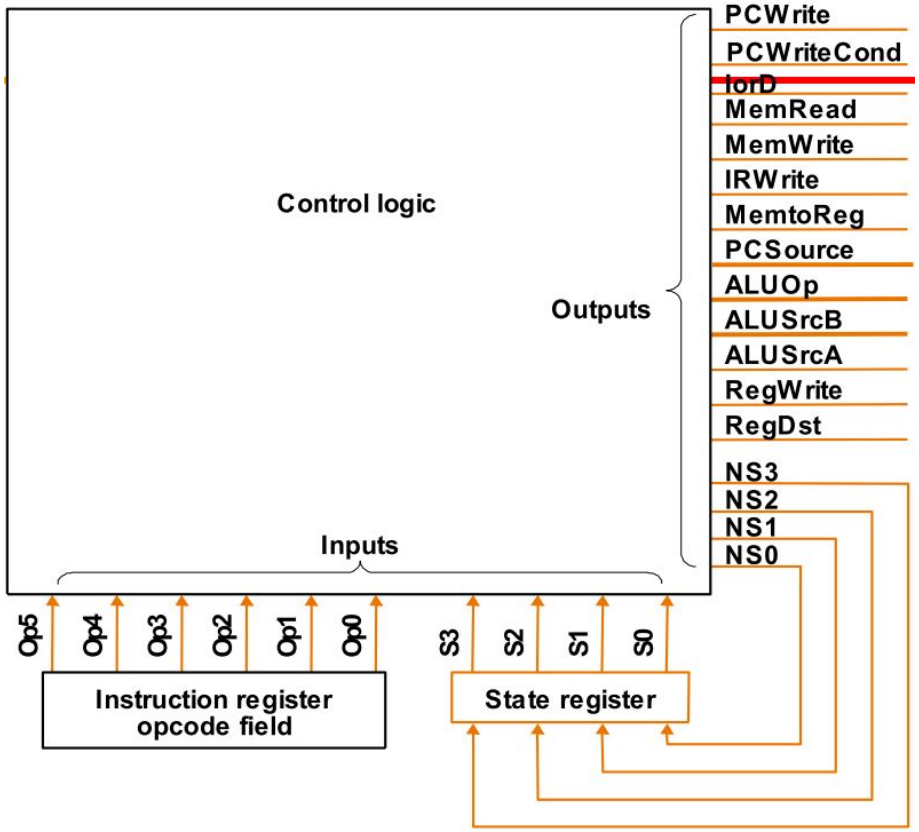


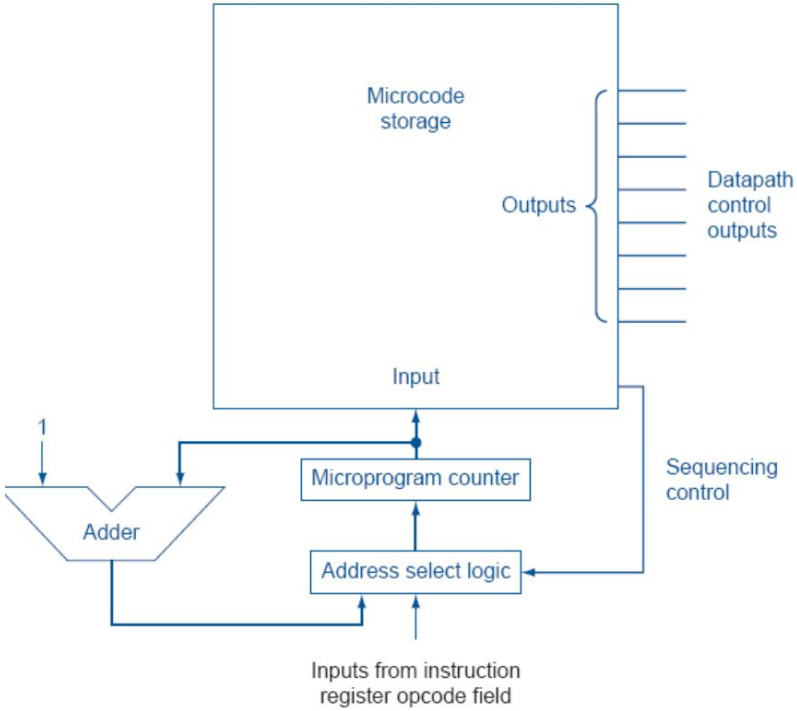
Moore Overlapping-1010

Control Signals In Multi-cycle datapath

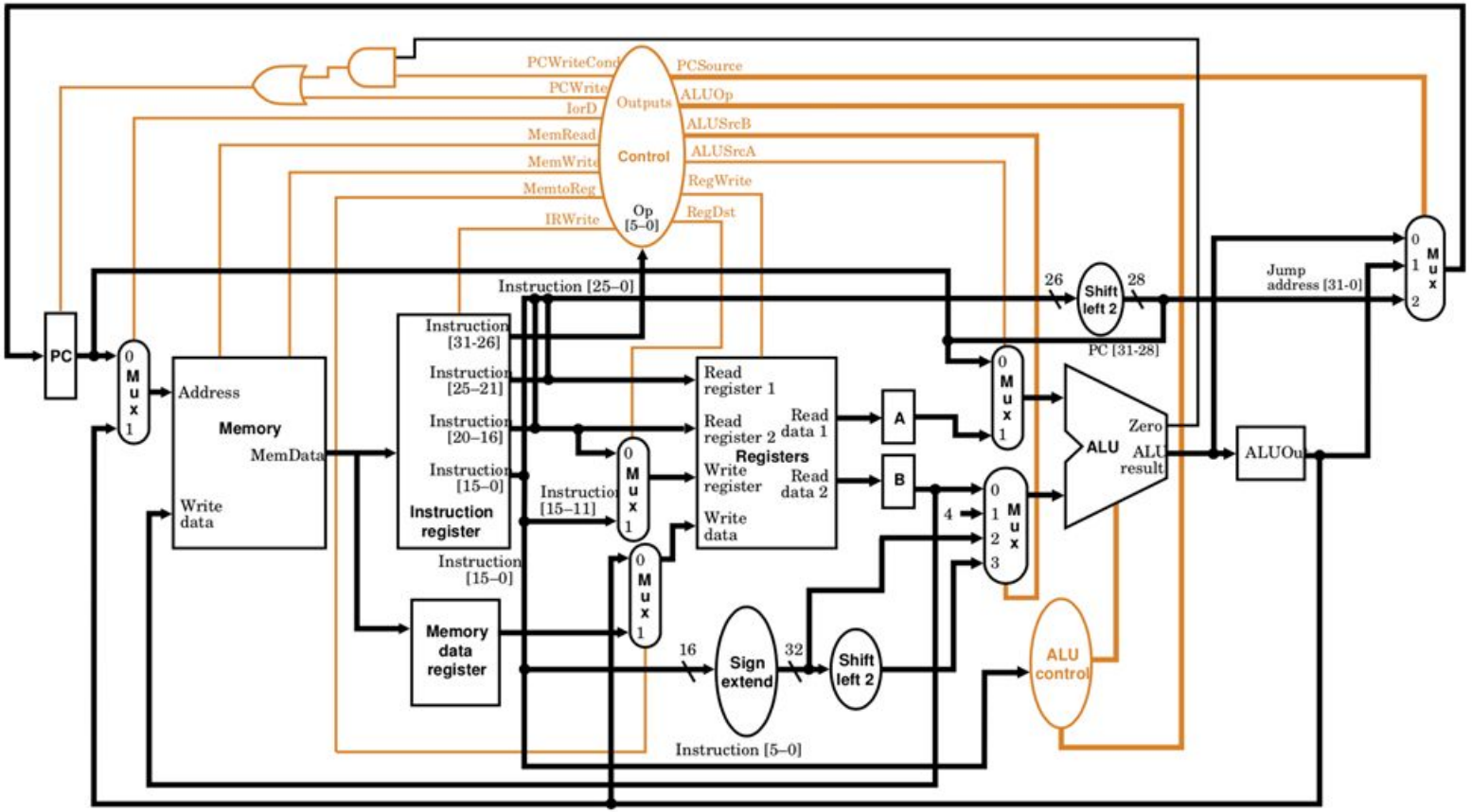


Control logic implementation





The big-picture



Verilog code and references

1. Refer this for the MIPS multicycle control module.
2. Refer this video for general state-machine verilog practices.
   a. Refer to this sequence detector [1010- Moore based] code
3. Refer this for the memory module.
4. Complete MIPS Multi-cycle