A 64-GBaud 64-QAM Optical Coherent Transmitter with Monolithically Integrated Driver and I/Q Modulator in 45-nm SOI CMOS

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***Abstract*—This paper presents an optical coherent transmitter consisting of an analog output stage and two Mach-Zehnder Modulators (MZM). For monolithic integration of electrical and optical parts, a Cherry-Hooper-based 3-bit high speed R-2R ladder DAC and a push-pull output driver is realized to achieve high speed pulse amplitude modulation (PAM) signal generation, amplification and electrical-optical connection. The designed MOSFET variable resistors in DAC also provide pre-distortion to compensate nonlinearity of later stages. Simulations results show the combination of DAC, and the output driver achieves over 59GHz 3-dB bandwidth with differential inputs, permitting 64GBaud PAM-8 signal processing. Implemented in a 45nm silicon photonic (Si-Ph) CMOS SOI process, the optical transmitter reaches 384Gb/s channel speed with 64-QAM modulation, at the electrical power cost of about 600mW.**

Keywords*—Pulse Amplitude Modulation (PAM), optical coherent transmitter, quadrature amplitude modulation (QAM), digital-to-analog converter (DAC), monolithic integration.

I. INTRODUCTION

The increasing demand for high-speed data transmission in data centers emphasizes the importance of new tuning and detection methods beyond traditional direct approaches. Recently, coherent optical modulation, which enables both amplitude and phase modulation, shows great potential for much higher channel speed for next-generation datalink design. Quadrature amplitude modulation (QAM) provides double data rate in a single channel at same baud rate compared to non-return-to-zero(NRZ) or pulse amplitude modulation(PAM). As an example in Fig.1, at the same 64GBaud baud rate, 4-QAM (QPSK) provides 128Gb/s bit rate as 16-QAM provides double bit rate at 256Gb/s and 64-QAM provides triple bit rate at 384Gb/s [1], [2].

As shown in Fig. 1, the input signal is modulated by the corresponding driver, modulated by electrical-optical (EO) modulator like Mach-Zehnder (MZM), transmitted by optical fiber and finally arrives at optical coherent receiver. In coherent receiver, optical signal is converted to two differential electrical signals by optical 90° hybrid and photodetectors (PD). Transimpedance amplifiers (TIA) and later processing circuits could then recover the original signal [3], [4].

For traditional optical transmitters, previous designs commonly combine several NRZ signals into one PAM signal on EO modulators [5]. But in coherent transmitter with high-order modulation like 64-QAM, it costs much more chip area to achieve such optical signal combination and may encounter more layout issues like inter-channel interference and variant time delay of different input signals. In this paper (Fig. 1a), we move the generation of PAM signal to electrical domain, which enables finer signal tuning and simplifies the layout work.

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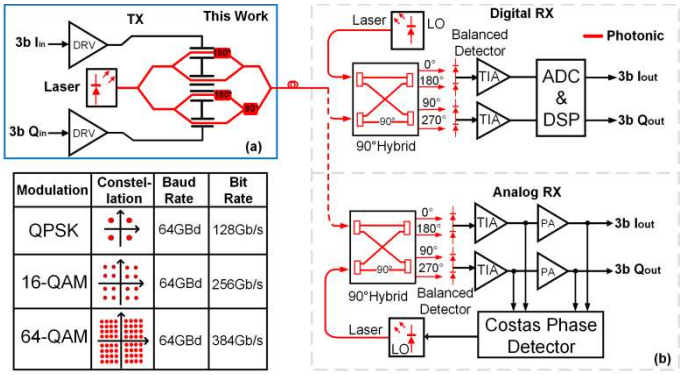
II. DESIGN OF OPTICAL COHERENT TRANSMITTER

The optical part of the coherent transmitter is mainly composed of two MZMs, a 90° phase shifter (PS), two multimode interference couplers (MMI) and several optical waveguides. Two orthogonal PAM optical signals are combined into one QAM signal at MMI and then transmitted through optical waveguides.



Modulation	Constellation	Baud Rate	Bit Rate
QPSK		64GBd	128Gb/s
16-QAM		64GBd	256Gb/s
64-QAM		64GBd	384Gb/s

Fig. 1. Coherent transceiver, (a) transmitter, (b) different types of receivers

Considering the high requirements of extinction ratio (ER) in optical signal transmission, modulator driver should be capable of high output swing. So, a push-pull output driver is adopted in our design for low-power high-swing applications. Besides, for PAM signal generation, a 3-bit DAC with Cherry-Hooper feedback is proposed, which provides a better isolation between NRZ input and PAM output. Capacitor coupling is used to connect two subcircuits, enabling different DC biasing. The entire EO structure is shown in Fig. 2.

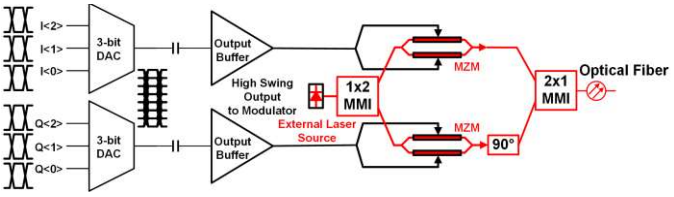


Fig. 2. Optical coherent transmitter

III. DESIGN OF PAM GENERATOR & OUTPUT DRIVER

A. 3-bit Cherry-Hooper-based DAC as PAM Generator

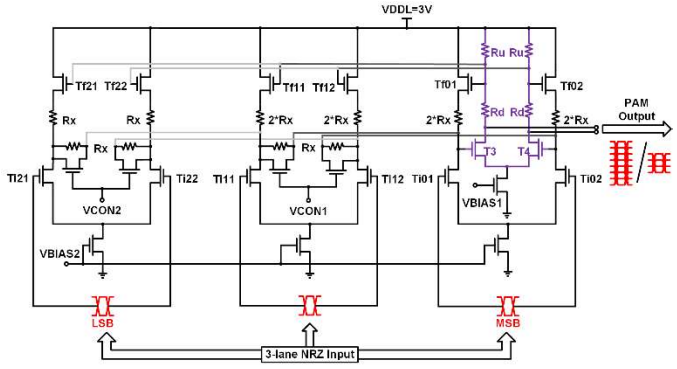


Fig. 3. Proposed 3-bit Cherry-Hooper-based DAC

The proposed 3-bit DAC is shown in Fig. 3. R-2R ladder DAC structure is used in the Cherry-Hooper feedback loop (R_X

and 2*R_X in the figure), with tunable transistor resistor controlled by V_{CON1} and V_{CON2} for pre-distortion. Six common-drain transistors T_f serve as source follower to drive a current of several milliamperes for the feedback. Due to the low-impedance node at the gate of T_f transistors created by feedback, the output resistance of the proposed DAC structure is mainly determined by R_d and is wideband. It could hardly be affected by input variations and V_{CON} tuning as well, which makes the impedance matching with the output driver much easier.

B. Push-pull Output Driver

Fig. 4 demonstrates the structure of the proposed output driver. C_{C1-4} are coupling capacitors to support different DC biasing between stages. Cascode structure is introduced to provide higher swing and lower Miller capacitance. Complementary push-pull structure is able to provide similar output swing and reduce the power consumption of the output driver by half compared to traditional resistor-load common-current logic (CML) output driver. R_o is used to match the modulator impedance. Inductive peaking technique is used at input and output node of the output driver. The bandwidth of the output driver and the entire transmitter could be effectively extended with suitable peaking inductance.

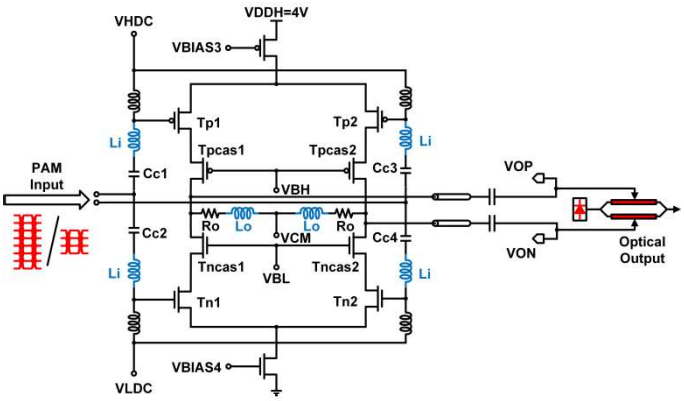


Fig. 4. Proposed output driver

IV. Simulation of the Transmitter

Fig. 5 shows the layout of the proposed optical coherent transmitter implemented in 45nm Si-Ph CMOS SOI process. The unmodulated external laser is input via a grating coupler. The total chip at the cost of 6.8mm^2 area.

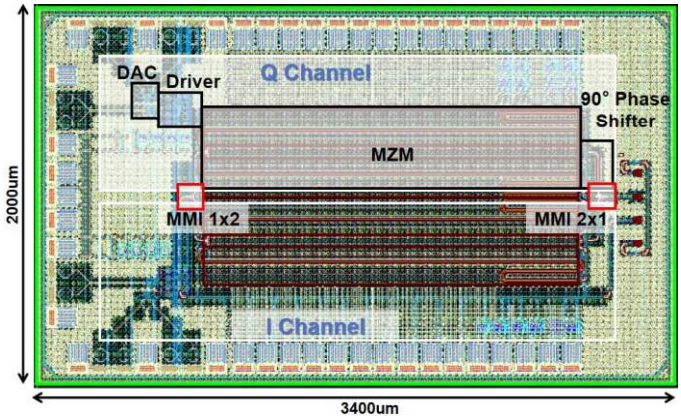


Fig. 5. Layout of the proposed coherent optical transmitter

Fig. 6 shows the simulated electrical AC response of the entire transmitter with different one-hot input code. With the contribution of the inductive peaking from L_o and L_i, a 6.8dB low-frequency gain and over 62GHz 3-dB bandwidth is achieved at the most significant bit (MSB). Combining the two coherent I and Q channels, the QAM error vector magnitude (EVM) of 64GBaud modulated 64-QAM and 16-QAM signals could achieve 10.9% (-19.3dB) and 8.7% (-21.2dB) respectively. Level separation mismatch ratio (RLM) is greater than 0.99 for single-channel PAM-4 output thanks to proper pre-distortion settings. (simulated eye and constellation diagram shown in Fig. 7) Besides, simulation results show the total electrical power of about 600mW for the transmitter.

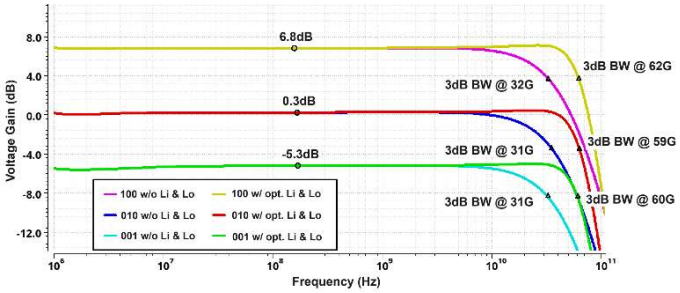


Fig. 6. Electrical response with different input codes

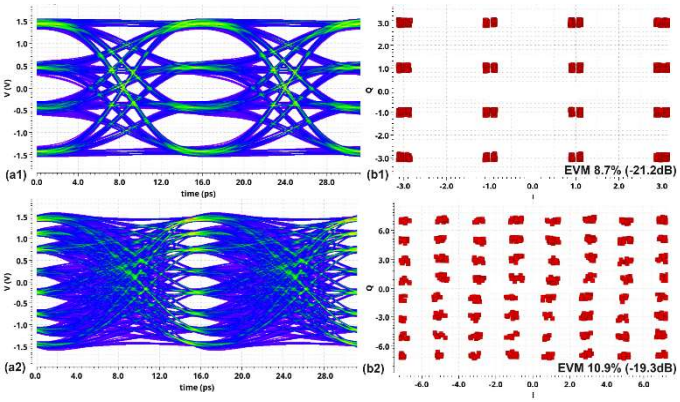


Fig. 7. Simulated output profile under optimum settings at 64GBaud, (a) single-channel electrical output eye-diagram, (b) constellation diagram

TABLE I. Performance Comparison with Published Transmitter

	Process	*BW (GHz)*	*Elec. Swing (Vppd)*	*Modulation*	*Speed (Gbps)*	*Power Efficiency (pJ/bit)*
[a]This work	45nm SOI	59	3	64-QAM	384	1.56
[5]	90nm CMOS	>25	2.16	PAM-4	50	2.70
[a][6]	0.13μm SiGe	40	3	PAM-4	100	7.2
[7]	55nm SiGe	42.2	2.2	NRZ	60	2.08
[8]	28nm CMOS	40	2.4	PAM-4	56	2.05

[a.] Simulation results

V. Conclusion

TABLE I. demonstrates the performance summary and comparison to some previous works. The proposed coherent transmitter shows the capability of running on highest single-channel data rate with competitive power efficiency.

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