Broadband Driver Circuits Design for mm-Wave Applications

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***Abstract*—This UROP report proposed a new perspective to design an ultra-broadband Doherty power amplifier with distributed structure, showing the progress and learning outcome and thinking for this UROP project. The proposed distributed Doherty power amplifier (DDPA) is promising to realize high power added efficiency (PAE) as well as drain efficiency (DE) at both maximum power 6-dB power back-off (PBO) on a broad frequency range. Due to the limited time frame of the project, this report includes only theoretical analysis and pre-layout simulation results. Implemented in Intel 16 FinFET process, over 30% PAE and >10dBm output power is achieved at both maximum power and 6dB PBO throughout the whole bandwidth (30GHz to 100GHz).**

***Index Terms*—Broadband, distributed amplifier (DA), Doherty power amplifier (DPA), millimeter-wave, power back-off (PBO), traveling-wave amplifier.**

I. Introduction

MODERN high-speed wireless communication protocol occupies most of sub-6GHz frequency band, increasingly emphasizing the significance of mm-wave and sub-THz systems. To satisfy various frequency choices of different mm-wave and sub-THz band requirements, broadband power amplification becomes essential in communication system design. At the meantime, using spectrum-efficient modulation technique like 64/256/4K-quadratic amplitude modulation (QAM) to achieve higher data rates is also important [1]. However, these techniques generate modulated signal with high peak-to-average power ratio (PAPR), which decreases the efficiency of power amplification. Consequently, broadband power amplifiers (PA) with high efficiency in deep power back-off (PBO) show great prospect in future multi-band communications.

There were lots of classical methods to achieve high efficiency broadband PAs before integrated circuits (IC) were invented. For efficiency enhancement, a dynamic load modulation technique is proposed in 1936 [2], which can change the impedance seen by main power amplifier in power back-off region to achieve load-line matching among wide output power range. For broadband amplification, traveling-wave amplifier (a.k.a. distributed amplifier) [3] works perfectly to realize power amplification from DC to over 120GHz [4]. However, either Doherty PA or traveling-wave PA have their own drawbacks: Doherty PA suffers from limited bandwidth since its power combiner structure is usually narrowband, while traveling-wave PA is hard to achieve high power efficiency.

Some previous work has already attempted to combine the merits of Doherty PA and traveling-wave PA on PCB-level design [5][6]. This project will go much further to investigate this combination and put up with a new and comprehensive perspective to scrutinize the proposed Doherty traveling-wave PA.

This report is organized as follows. A short overview on Doherty PA bandwidth limitation and traveling-wave PA efficiency limitation is given followed by some possible solutions giving birth to DDPA in Section II. Then design procedure and details will be discussed in Section III, followed by pre-layout simulation results in Section IV. Section V briefly concludes this report.

II. Distributed Doherty PA Architecture

A. Conventional Current-Combined Doherty PAs

A conventional symmetrical current-combined Doherty PA with 50Ω fixed resistive load is shown in Fig. 1. Let's assume that the optimum load-line matching impedance at maximum power of the main PA (carrier PA) is 50Ω, and the impedance transformer typically converts 50Ω load resistance to 25Ω. In the low input power region (half output power point), only the main PA is on, and it sees a 100Ω load impedance before the impedance inverter.

Meanwhile, in the high input power region (maximum output power point), the auxiliary PA (peaking PA) injects the same amplitude of current as the main PA with the same phase into the load, doubling the impedance seen by impedance inverter (to 100Ω). Then the main PA gets a load impedance of 50Ω before impedance inverter.

Besides, for the main PA, the load-line matching impedance at maximum output power is half of that at half output power because of the doubled current and same supply voltage. Therefore, after Doherty impedance modulation, at both half power and maximum power, the main PA achieves load-line matching, resulting in high power efficiency from 6dB power back-off to full power.

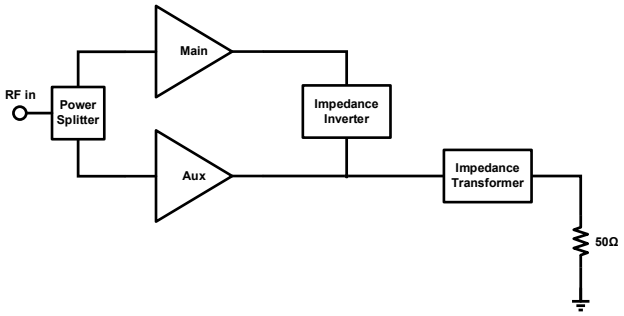

Fig. 1. Conventional DPA topology

However, due to the intrinsic difficulty of the broadband in-phase impedance transformer realization, this structure can hardly apply to broadband applications.

B. Traveling-wave Amplifier

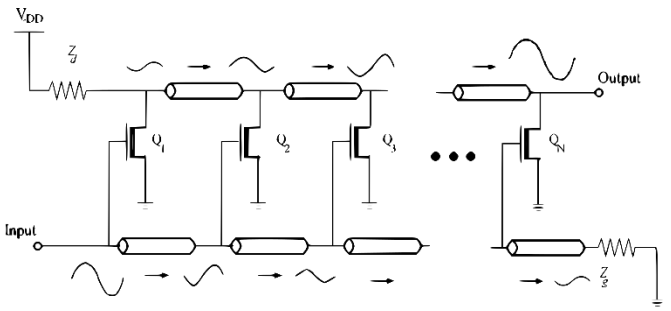

Fig. 2. Traveling-wave Amplifier

Distributed amplifier architecture, also known as traveling-wave amplifier, is shown in Fig. 2. The core idea of distribution is to divide the original large gain stage (typically a HEMT transistor) into different small ones. Between these small gain stages, transmission lines are used for connection. If the characteristic impedance of each transmission line segment is matched, then low reflection and low insertion loss will happen. One prominent advantage of traveling-wave amplifier is that this structure can take transistors into matching consideration, i.e., absorb the input and output parasitic capacitance into transmission lines, making it easier to match input and output impedance, thus achieving higher bandwidth. To save layout area, these transmission lines can also be replaced by lumped artificial version composite of inductors and capacitors.

The biggest drawback of traveling wave amplifier is the power consumption. As is shown in Fig. 2, there are two resistors, Z_d and Z_g, to achieve better impedance matching. These resistors, especially Z_d on the output transmission line, consume nearly half of the DC supply power of the entire circuits, which significantly deteriorated the power efficiency.

C. Proposed DDPA Architecture

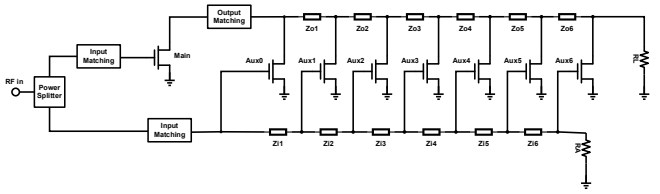

Fig. 3. Proposed DDPA Architecture

The proposed DDPA architecture, shown in Fig. 3, is similar to traditional Doherty PA but distributes auxiliary PA into seven different stages along two distributed transmission lines, the input Zi1…Zi6 and the output Zo1…Zo6. The RF input signal is divided into two branches after Wilkinson power divider. One of them passes through the input transmission line, feeds the gate of seven gain stages, and is finally terminated by a matching resistor R_A. The signal of the other branch is amplified by the main PA and then travels along the output transmission line. The main PA is biased as class A/AB/B PA and the seven auxiliary PAs are biased as class-C PA and will start working at a particular transition point. Two parallel transmission lines guarantee that the phase is easy to get matched at each power combining node because a branch of signal amplified by each PA will meet similar transmission line delay along the transmission path and take similar time terminated at R_L.

The principle of this DDPA is to use distributed transmission line to play the role of the impedance transformer and inverter, thus significantly broadening the bandwidth of this power combining structure.

At low-power region, only the main PA is working, so the whole DDPA is just an ordinary class A/AB/B PA with a long impedance transformer Zo0…Zo5. Starting from transition point, seven class-C auxiliary PAs work and modulate the output transmission line, until reach the maximum output power. As will be shown later, these two situations will result in the same load impedance seen by main PA. That is to say, a little different from conventional Doherty PA, if we fix the output current of the main PA after transition point, then the added current to the real load resistance from auxiliary PAs will not affect the load-line matching of the main PA, realizing high efficiency throughout the whole high-power region.

III. Proposed PA Design

As is stated before, the core of PA network design is to get main PA matched at both low-power region (see Fig. 4) and high-power region (see Fig. 5). In both Fig. 4 and Fig. 5, input transmission lines are neglected because we assume that phase matching is not a problem with well-designed input transmission lines and losses in input lines are negligible. There are two perspectives to design the DDPA.

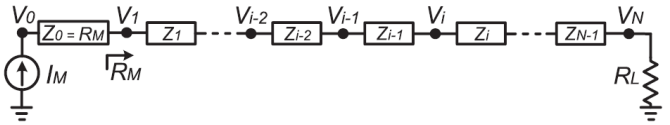

Fig. 4. Equivalent Circuits in Low-power Region

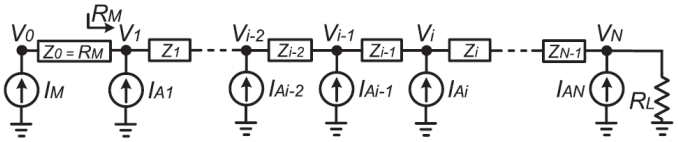

Fig. 5. Equivalent Circuits in High-power Region

A. Transmission Line with Higher Characteristic Impedance

Under this perspective, if we desire some level of PBO-dB, we need to set $Z_0 = R_M = R_L \cdot 10^{\frac{PBO}{10}}$ (i.e., R_L and R_M is the load-line matching impedance of PBO-dB power back-off and maximum output power respectively) and $Z_1 \dots Z_{N-1}$ should be an impedance transformer that match R_L with R_M throughout a wide bandwidth. Klopfenstein taper is a great choice for broadband impedance matching. But considering that distributed transformer is easier to realize in distributed architecture, its discrete version, i.e., Chebyshev impedance transformer, is adopted. Given center frequency, desired fractional bandwidth (FBW) and ripple tolerance, we can quickly derive our version of Chebyshev transformer and thus $Z_1 \dots Z_{N-1}$. Other multi-section stepped impedance transformers like Butterworth are also welcomed and have no significant discrepancy in later analysis. Typically, an increase in the number of sections yields a better performance in terms of bandwidth.

After impedance transformer is set, we can notice that the main PA finally sees the real load resistor R_L after the modulation of impedance transformer. As a result, at PBO-dB power back-off point, the main PA achieves load-line matching.

When input power gets higher and eventually reaches the maximum power. All auxiliary PA will open to the max. At this point, what we desire is to let the main PA see an impedance of a larger load impedance R_M to achieve load-line matching. To meet such requirements, the whole transmission line should become uniform R_M transmission. Let $I_{A0} = I_M$, the uniform condition can be converted to (1), in which the term inside the bracket shows the load modulation by current injection. In this case, we assume that the phase of two combined current is perfectly matched because it is not hard to achieve since the parallel property of input and output transmission lines.

$$Z_{i-1} = Z_i\left(1 + \frac{I_{Ai}}{I_{A0} + \cdots + I_{A(i-1)}}\right) \tag{1}$$

$$I_{Ai} = (I_{A0} + \cdots + I_{A(i-1)} + I_{Ai})Z_i\left(\frac{1}{Z_i} - \frac{1}{Z_{i-1}}\right) \tag{2}$$

From (1), we can get (2). And we can decompose (2) into two factors, the admittance difference between two adjacent stages $\frac{1}{Z_i} - \frac{1}{Z_{i-1}}$, and the fundamental peak-to-peak saturation voltage at load resistor $V_{DD} - V_{KNEE} = (I_{A0} + \cdots + I_{AN})Z_N$.

For the power apart from two critical points (PBO-dB power back-off and maximum power), the current is designed to be as (3) and (4), ensuring the main PA biased at class B and the auxiliary PAs biased at class C.

$$I_{Ai}(V_{in}) = \begin{cases} 0, \ 0 < V_{in} < \dfrac{V_{inm}}{\alpha} \\ I_{Ai}\dfrac{\alpha V_{in} - V_{inm}}{(\alpha - 1)V_{inm}}, \ V_{inm}/\alpha < V_{in} < V_{inm} \end{cases} \tag{3}$$

$$I_M(V_{in}) = \begin{cases} I_M\dfrac{\alpha V_{in}}{V_{inm}}, \ 0 < V_{in} < \dfrac{V_{inm}}{\alpha} \\ I_M, \ V_{inm}/\alpha < V_{in} < V_{inm} \end{cases} \tag{4}$$

In (3) and (4), V_{inm} stands for the input voltage corresponding to the maximum power. With analysis above, we can easily calculate the efficiency and output power under a particular setting. With design parameters shown in table I, we can get the results from Fig. 6 to Fig. 12, illustrating the performance of the architecture.

Table. I. Design Parameters under Perspective A

N=6	PBO=8dB	R_L=1Ω	FBW=120%	f_C=70G
Z_0=6.3Ω, Z_1=4.9Ω, Z_2=3.6Ω Z_3=2.5Ω, Z_4=1.7Ω, Z_5=1.3Ω				
I_M=224mA, I_{A1}=64mA, I_{A2}=100mA, I_{A3}=174mA I_{A4}=253mA, I_{A5}=285mA, I_{A6}=314mA				

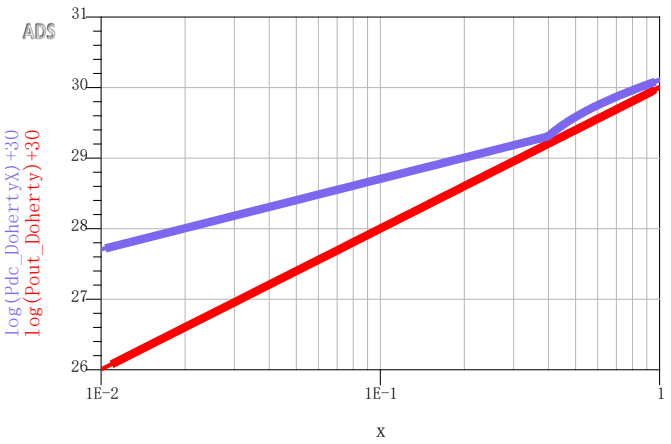

Fig. 6. Power Output & DC Power Supply (dBm) vs Normalized Input Voltage @f_c=70GHz

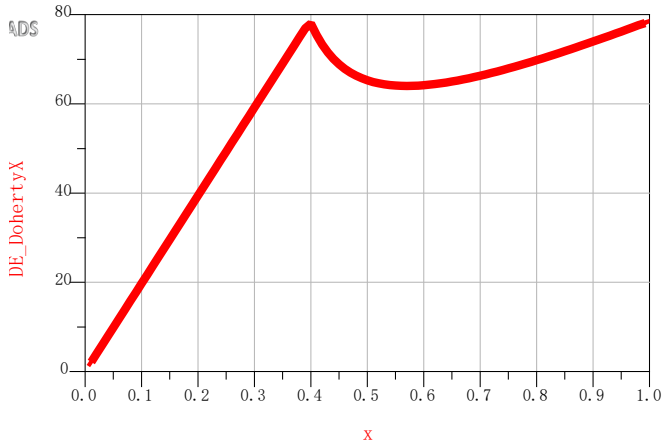

Fig. 7. Drain Efficiency vs Normalized Input Voltage @f_c=70GHz

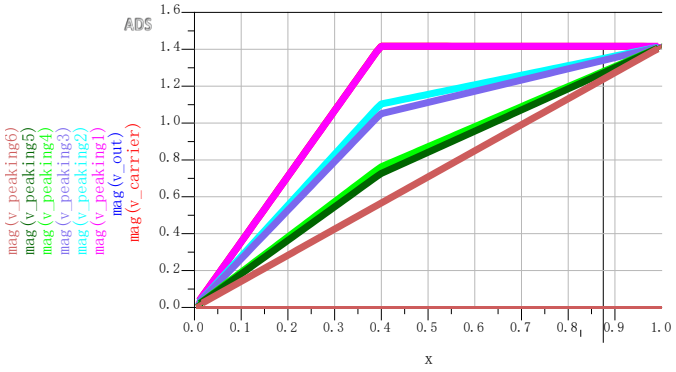

Fig. 8. Voltage Profile vs Normalized Input Voltage @f_c=70GHz

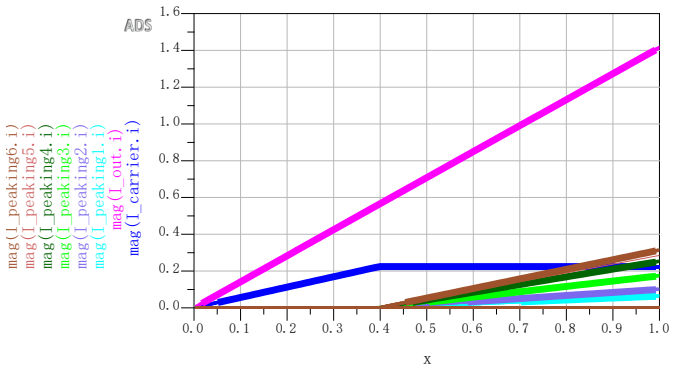

Fig. 9. Current Profile vs Normalized Input Voltage @f_c=70GHz

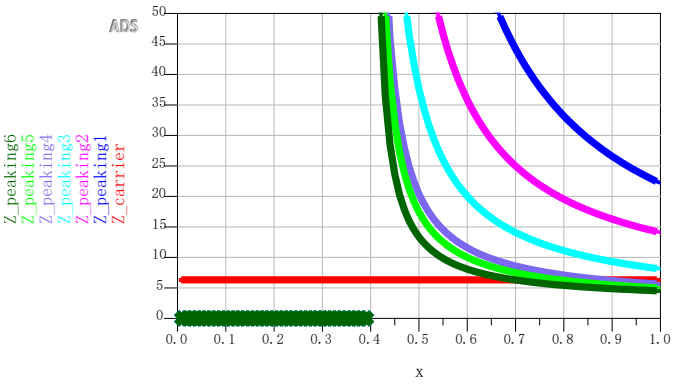

Fig. 10. Load Impedance Profile vs Normalized Input Voltage @f_c=70GHz

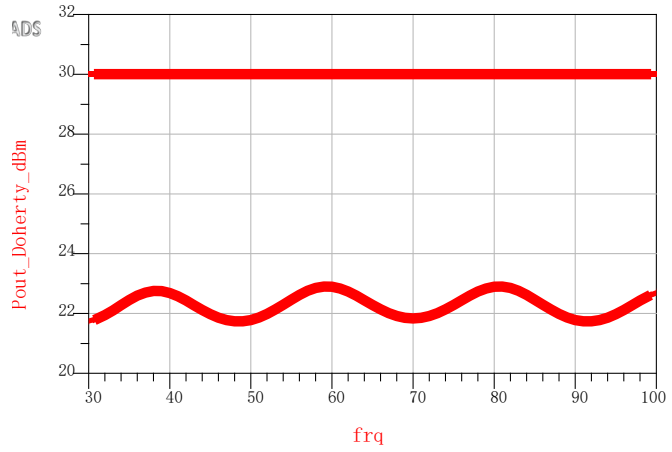

Fig. 11. Output Power (dBm) vs Frequency @ Maximum Power (Above) & 8-dB PBO (Below)

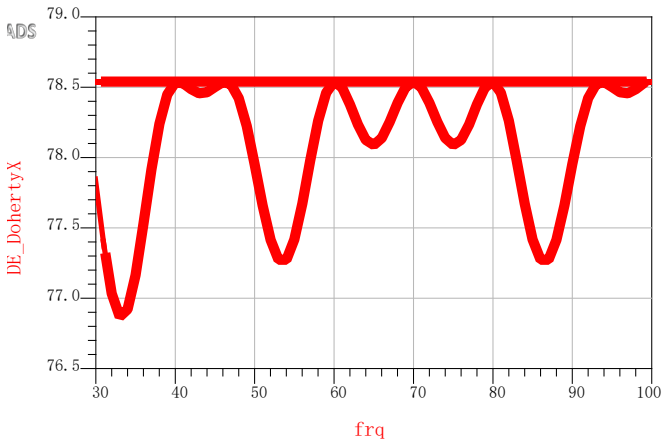

Fig. 12. Drain Efficiency (dBm) vs Frequency @ Maximum Power (Above) & 8-dB PBO (Below)

From Fig. 6 to Fig. 10, this structure shows great Doherty load modulation and high efficiency among a wide power range. From Fig. 11 and Fig. 12, this structure shows desired broadband performance.

B. Transmission Line with Normal Characteristic Impedance

Under this perspective, we first achieve an ordinary class B PA with uniform transmission line matching in Fig. 4, i.e., Z_0=…=Z_{N-1}=R_L. Then at low-power region, this structure just acts as a class B PA, which achieves maximum output power at transition point.

After the transition point, all other auxiliary PA starts to work. Due to load modulation caused by injected current, the main PA cannot see a uniform R_L transmission line this time. However, to meet the requirements of load-line matching, we still need to make the reflection coefficient of node V_1 in Fig. 5 to be as small as possible to let the main PA see the original load impedance. This time we can refer to Chebyshev (or other) impedance transformer as well, because it not only achieves smallest reflection coefficient Γ at V_1, but also enables non-zero Γ at all remained nodes, which permits current injection into each node.

So, we need to start with a chosen impedance transformer, and get Γ_i of each node from the impedance transformer, and then equal each desired Γ_i to real reflection ratio $\frac{\Delta Z}{\Sigma Z}$. After substituting the equation with true load modulation, we could get (5), where I_{Zi} stands for the current profile on the right side of each transmission line segment.

$$\Gamma_i = \frac{\left(1+\frac{I_{Ai}}{I_{Z_{i-1}}}\right)Z_i - Z_{i-1}}{\left(1+\frac{I_{Ai}}{I_{Z_{i-1}}}\right)Z_i + Z_{i-1}} \tag{5}$$

From I_{AN} to I_{A1} and I_M=I_{A0}, we could solve all the I_{Ai} in this order. Besides, apart from two critical points, other current profile is same as in perspective A, i.e., equation (3) and (4).

With design parameters shown in table II, we can get the results from Fig. 13 to Fig. 19, illustrating the performance of the architecture.

Table. II. Design Parameters under Perspective B

N=7	PBO=6dB	R_L=10Ω	FBW=115%	f_C=70G
Z_0=…=Z_6=10Ω				
I_M=200mA, I_{A1}=16mA, I_{A2}=39mA, I_{A3}=67mA I_{A4}=90mA, I_{A5}=88mA, I_{A6}=64mA, I_{A7}=30mA				

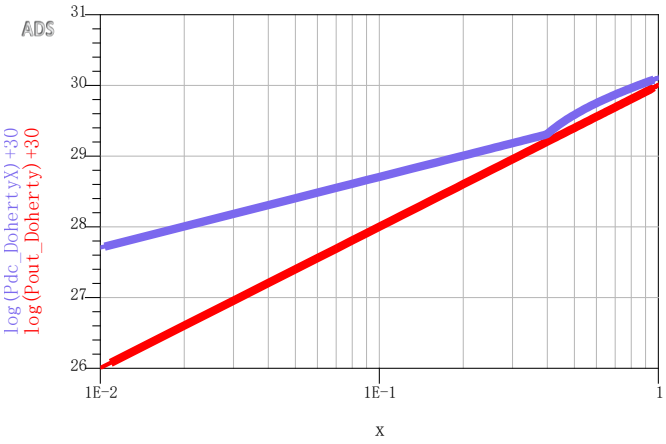

Fig. 13. Power Output & DC Power Supply (dBm) vs Normalized Input Voltage @f_c=70GHz

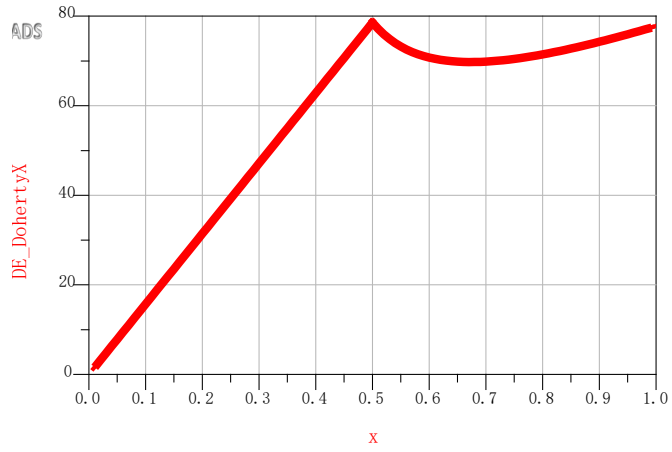

Fig. 14. Drain Efficiency vs Normalized Input Voltage @f_c=70GHz

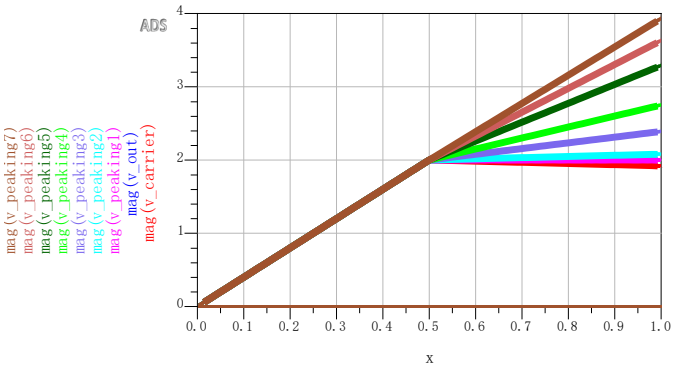

Fig. 15. Voltage Profile vs Normalized Input Voltage @f_c=70GHz

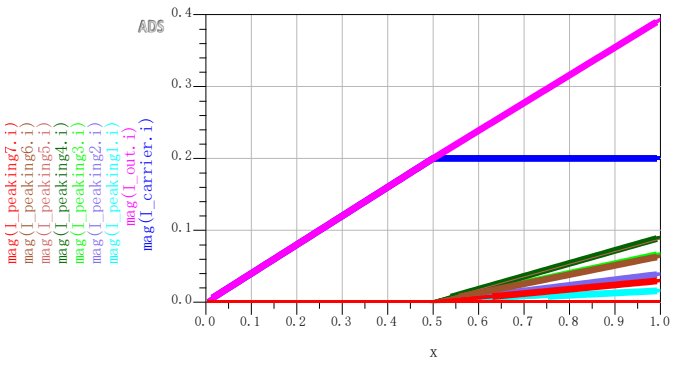

Fig. 16. Current Profile vs Normalized Input Voltage @f_c=70GHz

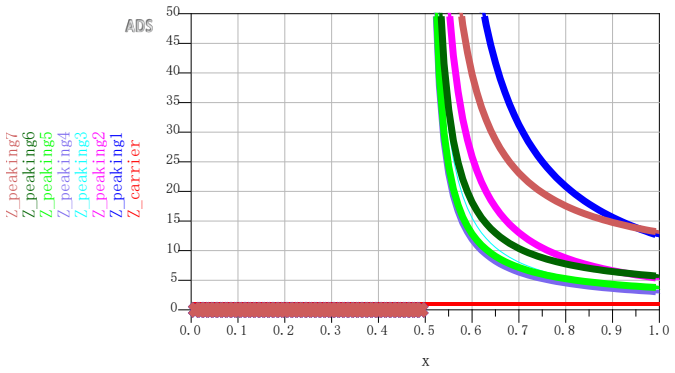

Fig. 17. Load Impedance Profile vs Normalized Input Voltage @f_c=70GHz

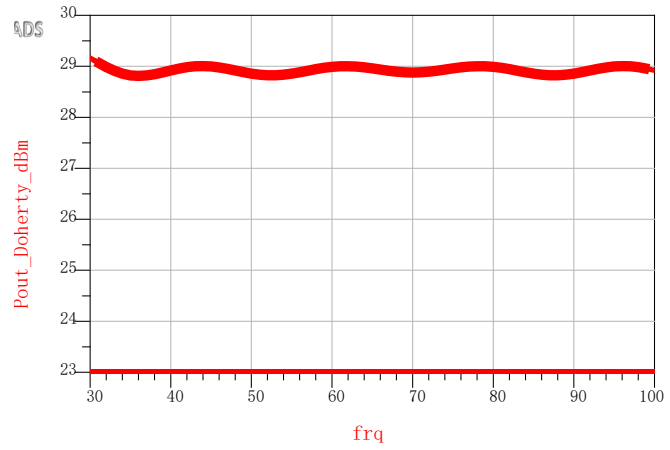

Fig. 18. Output Power (dBm) vs Frequency @ Maximum Power (Above) & 6-dB PBO (Below)

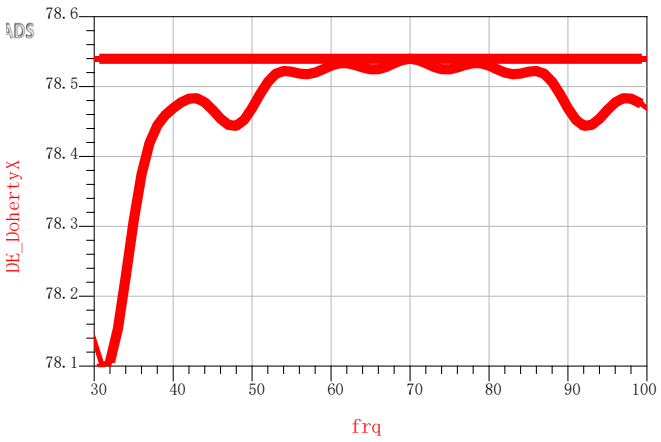

Fig. 19. Drain Efficiency (dBm) vs Frequency @ Maximum Power (Below) & 6-dB PBO (Above)

Ideally, the latter perspective shows comparable performance to the previous one, but both have their own drawbacks. For perspective A, physically non-uniform transmission line is challenging to achieve both in phase matching and in multi-stage cascade; for perspective B, it can be seen from Fig. 15 that to achieve higher efficiency, different gain stages are in need of different power supply, which makes inter-stage coupling a bit difficult.

In this project, we try to sacrifice some power efficiency for simplicity, so perspective B is adopted in the next section.

IV. Pre-Layout Simulation

The real schematic design adopts differential structure, and all the analysis above is just part of the single-ended version or half circuit of the real design. Besides, for the convenience of layout work and parasitic capacitance absorption, transmission line Zi1…Zi6 and Zo1…Zo6 is substitute with lumped artificial transmission lines. All capacitors and inductors use an ideal model for simplicity. The complete schematic is shown in Fig. 20. The input and the output matching networks are both realized with 2-order LC ladder, and 70GHz 50Ω transmission lines is constituted with seven same λ/4 segments realized by lumped approximation (see Fig. 21, in which we can solve L and C from $\sqrt{\frac{L}{C}} = Z$ and $\frac{1}{2\pi\sqrt{LC}} = f_0$). The adjustment in amount of model capacitor C can be used to absorb the parasitic input and output capacitance of the auxiliary PAs.

The power splitter is a 4-stage broadband Wilkinson power divider. The main PA is just a simple high performance RF transistor differential pair with cross connected capacitors. Seven auxiliary PAs share the structure of the main PA, only changing the number of fins for minimum modifications.

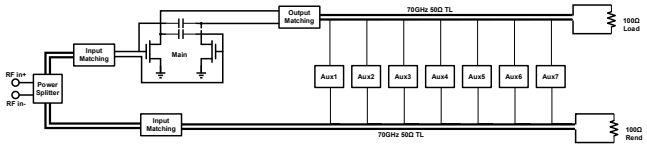

Fig. 20. Designed DDPA Architecture

For the main PA, the input bias is set to V_{gsmi}=0.5V (V_{th}=0.15V, class A/AB) and the output bias is set to V_{gsmo}=0.8V, both added with ideal bias-tee. For the auxiliary PAs, the input bias is set to V_{gsai}=-0.1V (class C) and the output bias is set to V_{gsao}=1V, both added with ideal bias-tee. For better load modulation, the goal peak fundamental current of each stage is shown as follows: I_{Mm}=17mA, I_{A1m}=1.4mA, I_{A2m}=3.3mA, I_{A3m}=5.7mA, I_{A4m}=7.7mA, I_{A5m}=7.5mA, I_{A6m}=5.4mA, I_{A7m}=2.5mA. We change the size of the transistors to accommodate such current profile as close as possible.

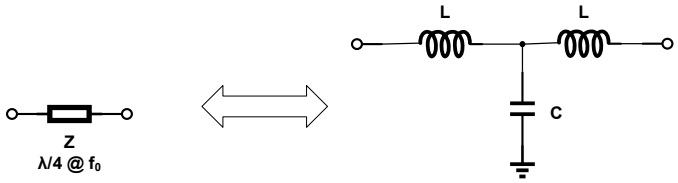

Fig. 21. Lumped Approximation of λ/4 TL

After connecting RF input to differential 100Ω port, we get the main simulation results displayed in Fig. 22 to Fig. 24. It can be shown that the DDPA prototype schematic achieves up to 10dBm output power and over 30% PAE from 30GHz to 100GHz in both power regions.

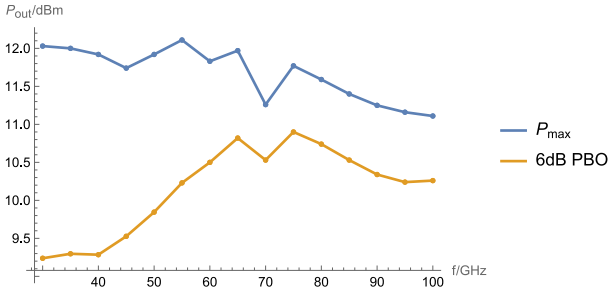

Fig. 22. DDPA Simulation: Output Power vs Frequency

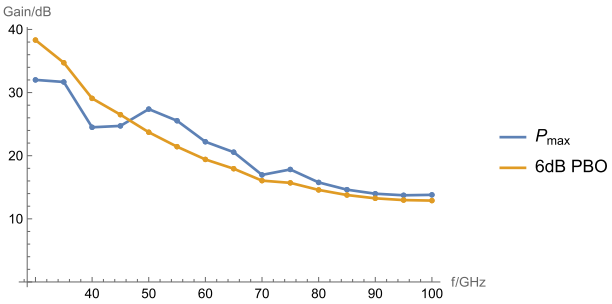

Fig. 23. DDPA Simulation: Power Gain (including the effects of matching) vs Frequency

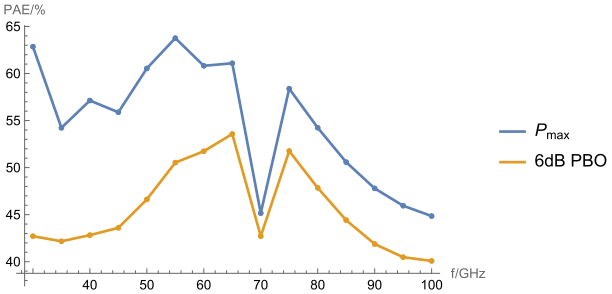

Fig. 24. DDPA Simulation: PAE vs Frequency

V. Conclusion

The report has presented a DDPA structure, an innovative broadband power amplifier architecture with high PAE in deep PBO. It has been shown that combining traveling-wave amplifier and Doherty PA shows great capability in broadband high PAPR signal amplification with only a little more difficulty on layout and fine-tuning works.

In Intel 16 FinFET process, the DDPA prototype schematic achieves over 10dBm output power at both maximum power and 6dB power back-off with PAE over 30% from 30GHz to 100GHz in pre-layout simulations. Due to the time limitation of this UROP project, this project report does not cover layout and EM simulations.

In summary, the proposed power amplifier design technique still shows a promising way to think about high-efficiency broadband PA design, which could be beneficial to general PA design in upcoming mm-wave and sub-THz era.

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References

[1] E. Dahlman et al., "5G wireless access: requirements and realization," in IEEE Communications Magazine, vol. 52, no. 12, pp. 42-47, December 2014.

[2] W. H. Doherty, "A new high-efficiency power amplifier for modulated waves," in The Bell System Technical Journal, vol. 15, no. 3, pp. 469-475, July 1936.

[3] E. L. Ginzton, W. R. Hewlett, J. H. Jasberg and J. D. Noe, "Distributed Amplification," in Proceedings of the IRE, vol. 36, no. 8, pp. 956-969, Aug. 1948.

[4] O. El-Aassar and G. M. Rebeiz, "A 120-GHz Bandwidth CMOS Distributed Power Amplifier with Multi-Drive Intra-Stack Coupling," in IEEE Microwave and Wireless Components Letters, vol. 30, no. 8, pp. 782-785, Aug. 2020.

[5] P. Saad, R. Hou, R. Hellberg and B. Berglund, "A 1.8–3.8-GHz Power Amplifier With 40% Efficiency at 8-dB Power Back-Off," in IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 11, pp. 4870-4882, Nov. 2018.

[6] P. Saad, R. Hou, R. Hellberg and B. Berglund, "Ultra-Wideband Doherty-Like Power Amplifier," 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, USA, 2018.

[7] H. Beshary, I. A. Eshrah, M. A. Y. Abdalla and A. N. Mohieldin, "A Compact Low-Loss On-chip N-Way Wilkinson Power Divider for mm-Wave 5G Applications," 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA, USA, 2020, pp. 444-447.