

## PCB

Board size: 25.4x25.4 mm (1.0x1.0 inches)

- This is the size of the rectangle that contains the board
- Thickness: 1.6 mm (63 mils)
- Material: FR4
- Finish: None
- Layers: 4
- Copper thickness: 35  $\mu$ m

Solder mask: TOP / BOTTOM

- Color: Green

Silk screen: TOP / BOTTOM

- Color: White

Stackup:

Name	Type	Color	Thickness	Material	Epsilon	Loss tangent
F.SilkS	Top Silk Screen					
F.Paste	Top Solder Paste					
F.Mask	Top Solder Mask		10			
F.Cu	copper		35			
dielectric 1	prepreg		100	FR4	4.5	0.020
In1.Cu	copper		35			
dielectric 2	core		1240	FR4	4.5	0.020
In2.Cu	copper		35			
dielectric 3	prepreg		100	FR4	4.5	0.020
B.Cu	copper		35			
B.Mask	Bottom Solder Mask		10			
B.Paste	Bottom Solder Paste					
B.SilkS	Bottom Silk Screen					

## Important sizes

Clearance: 0.2 mm (8 mils)

Track width: 0.25 mm (10 mils)

- By design rules: 0.2 mm (8 mils)

Drill: 0.85 mm (33 mils)

- Vias: N/A mm (N/A mils) [Design: 0.4 mm (16 mils)]
- Pads: 0.85 mm (33 mils)
- The above values are real drill sizes, they add 0.1 mm (4 mils) to plated holes (PTH)

Via: N/A/N/A mm (N/A/N/A mils)

- By design rules: 0.5/0.3 mm (20/12 mils)
- Micro via: yes [0.2/0.1 mm (8/4 mils)]
- Buried/blind via: yes
- Total: 0 (thru: 0 buried/blind: 0 micro: 0)

Outer Annular Ring: 0.18 mm (7 mils)

- By design rules: 0.18 mm (7 mils)

Eurocircuits class: 4A - Using min drill 0.85 mm for an OAR of 0.18 mm

## General stats

Components count: (SMD/THT)

- Top: 2/1 (SMD + THT)
- Bottom: 0/0 (NONE)

Defined tracks:

Used tracks:

- 0.25 mm (10 mils) (3) defined: no

Defined vias:

Used vias:

Holes (excluding vias):

- 0.75 mm (30 mils) (2)

Oval holes:

Drill tools (including vias and computing adjusts and rounding):

- 0.85 mm (33 mils) (2)

## Schematic

Schematic in SVG format

PCB Layers

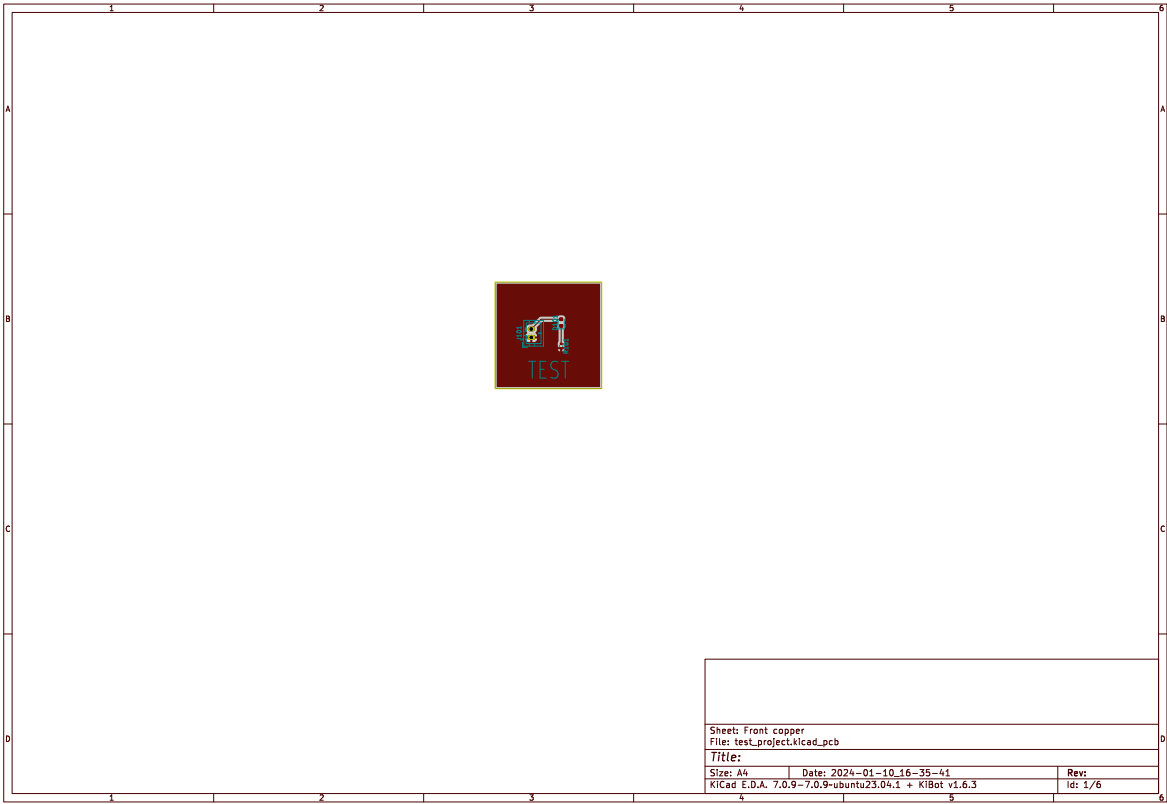


Figure 1: PCB Front copper

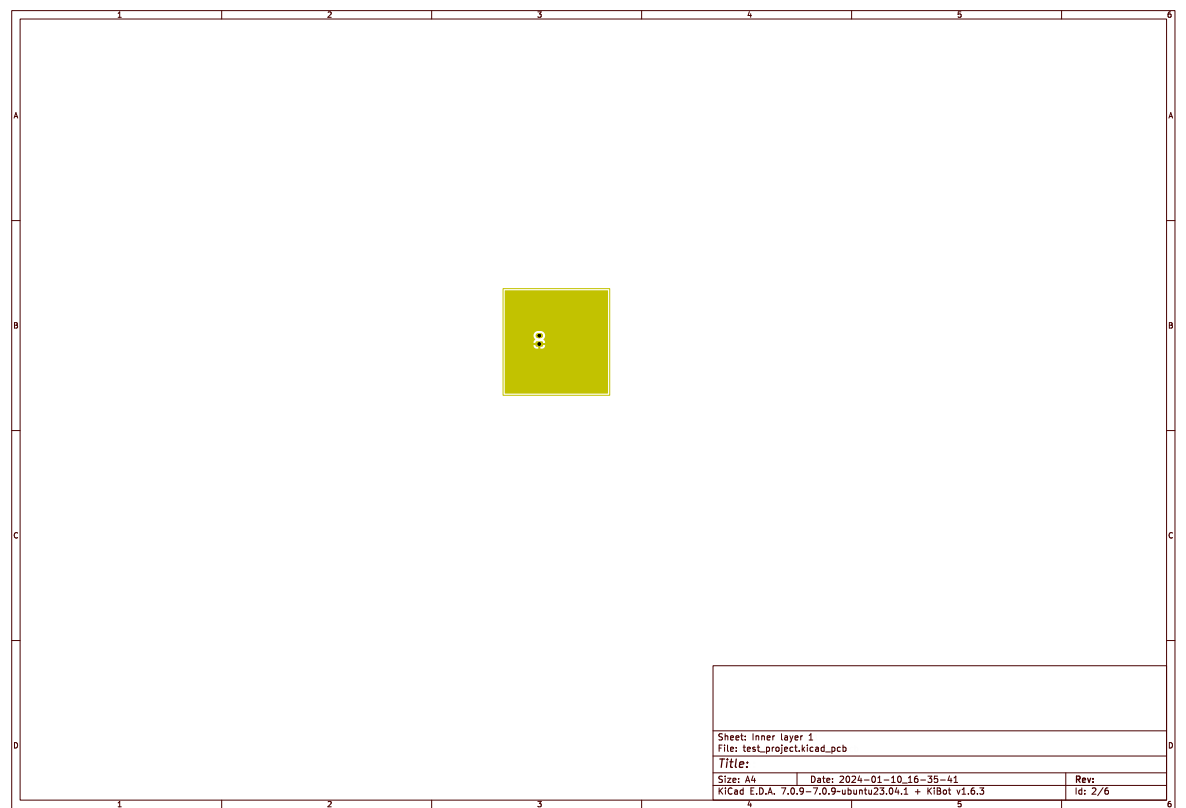


Figure 2: PCB Inner layer 1

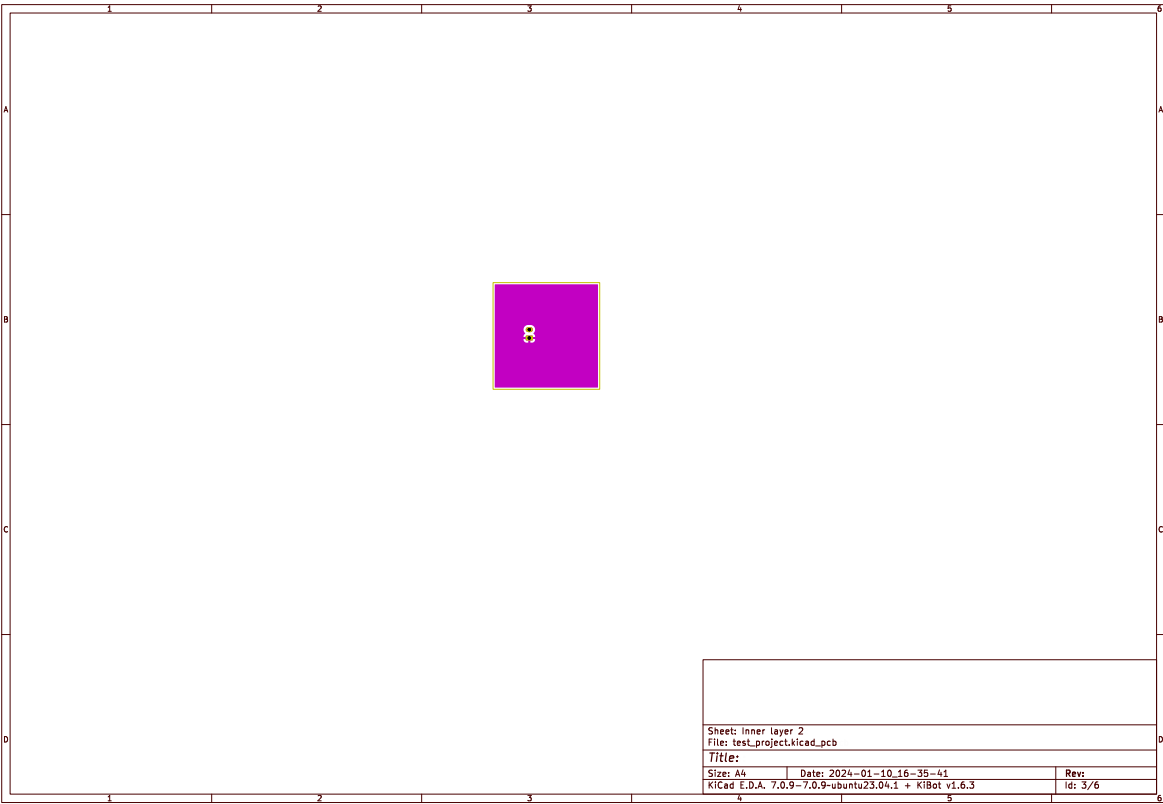


Figure 3: PCB Inner layer 2

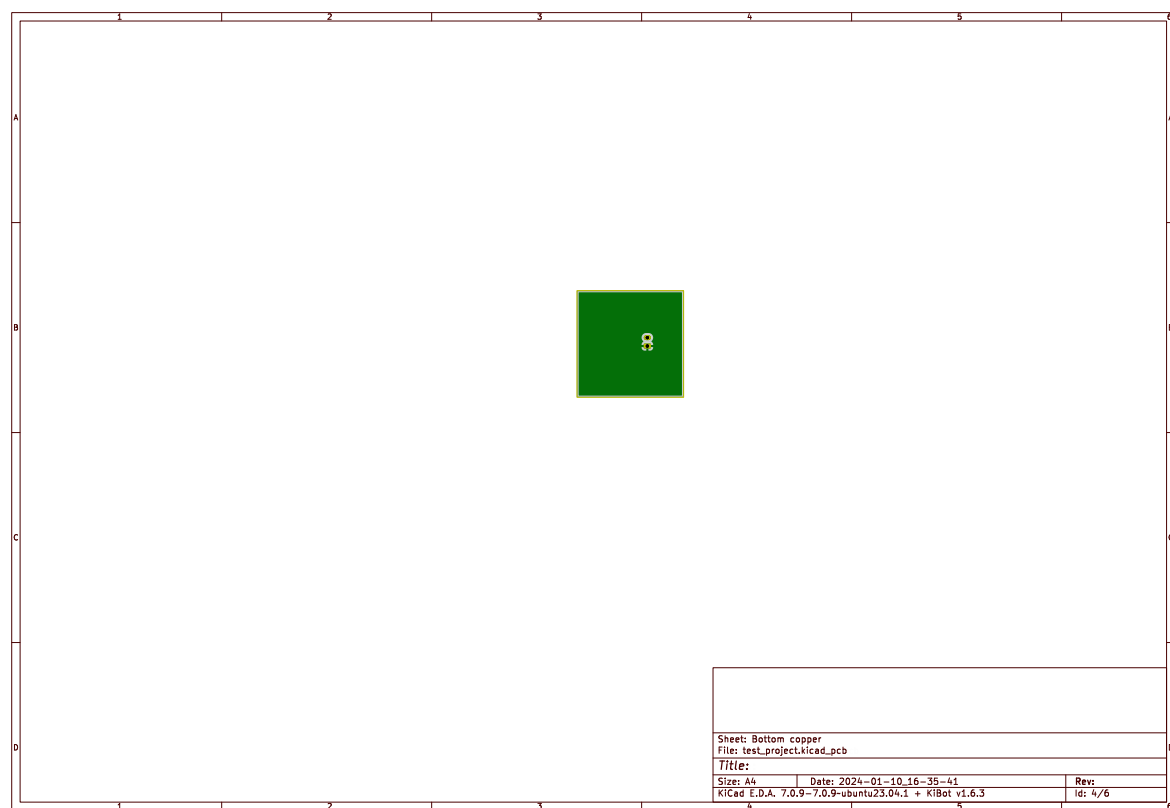


Figure 4: PCB Bottom copper

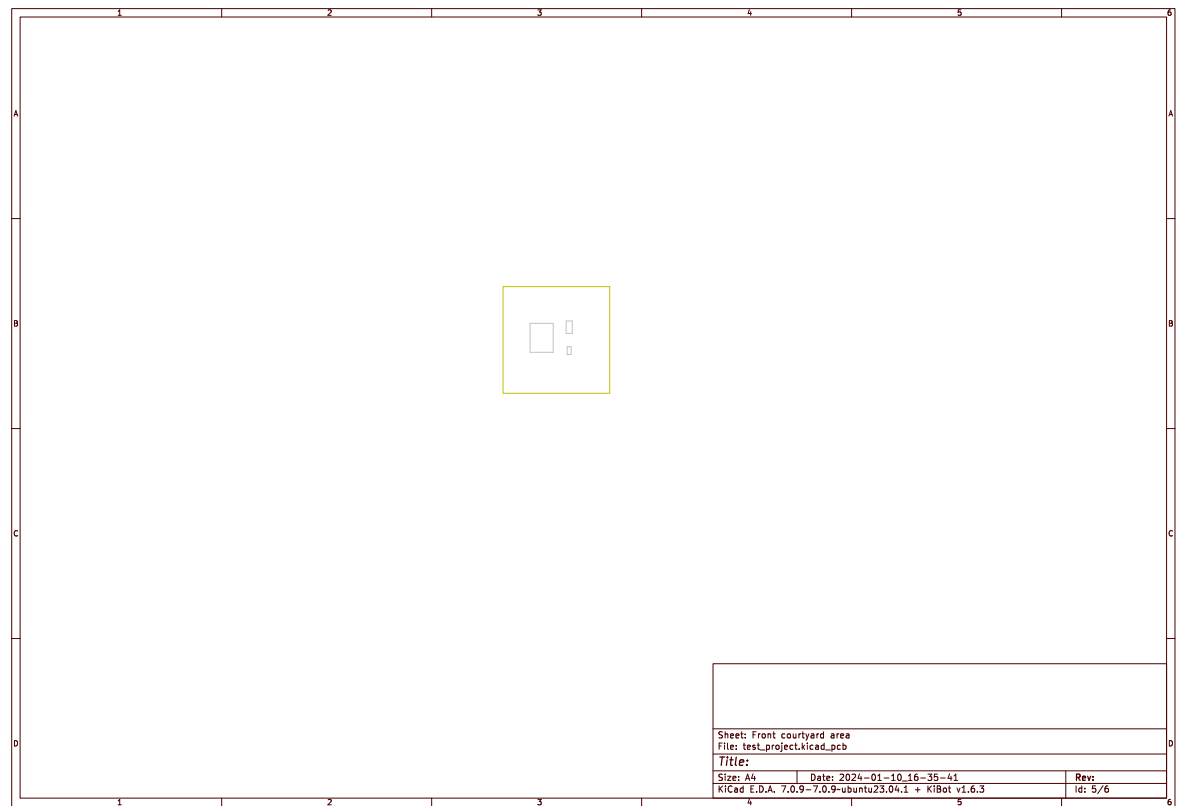


Figure 5: PCB Front courtyard area

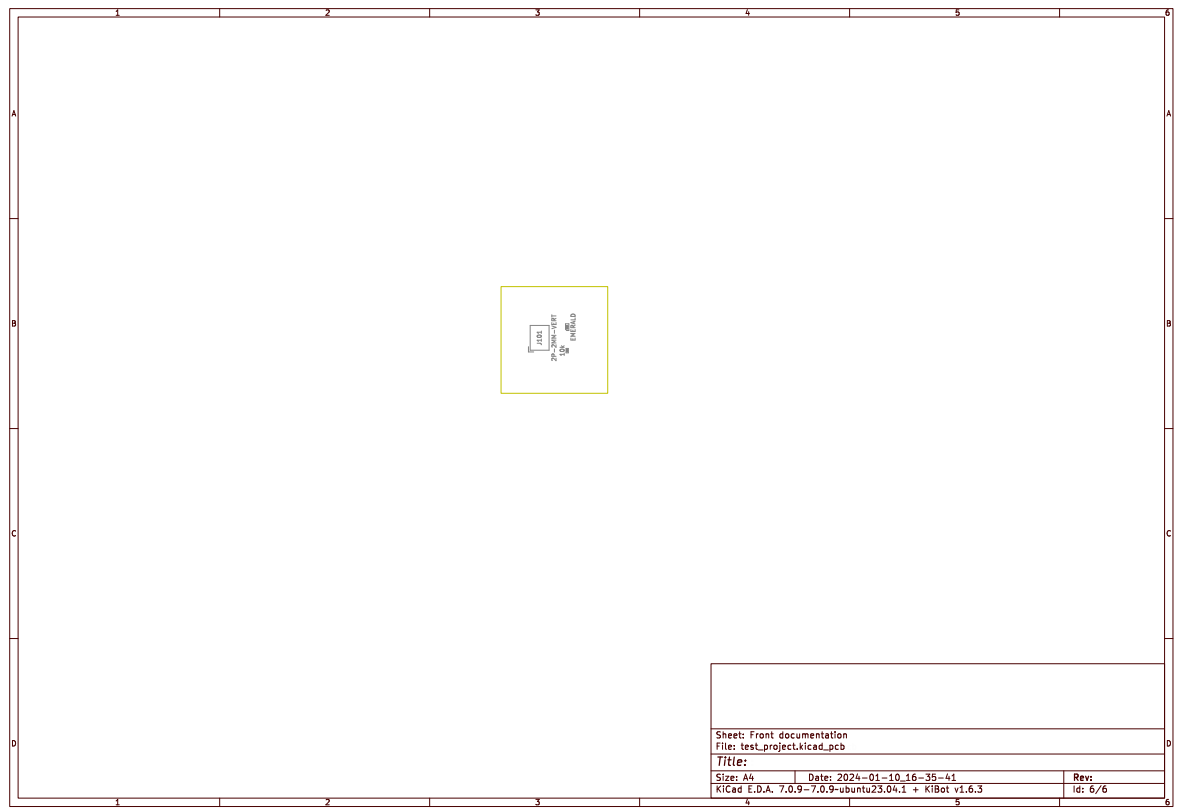


Figure 6: PCB Front documentation