Questions 3 (13 Points): Etch & Litho

Why can we obtain a straight etch profile in HDP as compared to RIE (3 points)

The ability to obtain a **straight (anisotropic) etch profile** in **HDP (High-Density Plasma) etching** versus standard **RIE (Reactive Ion Etching)** is due to several key differences in **plasma density, ion energy, and directionality**. Here's a breakdown:

✅ **Why HDP Provides Straighter Etch Profiles Compared to RIE**

Feature	HDP Etching	RIE Etching
Plasma density	Very high (≥10^{11} ions/cm³)	Moderate (10^{9}–10^{10} ions/cm³)
Ion directionality	Strongly vertical due to bias and collimation	Less directional (more sidewall etching)
Deposition-etch balance	Simultaneous etch + passivation possible	Mostly etching only
Etch profile	Highly anisotropic (straight walls)	More isotropic (tapered or undercut)

1. Higher Ion Density = Better Control
   - HDP uses high-density plasma sources (e.g., inductively coupled plasma or ECR).
   - More reactive species and ions are available, allowing faster and cleaner vertical etching.
2. Better Ion Directionality
   - HDP applies a strong RF bias to the wafer, accelerating ions vertically.
   - This enhances anisotropy by favoring vertical bombardment, minimizing sidewall erosion.
3. Simultaneous Etch and Passivation
   - In HDP, etching gases (like Cl_2 or SF_6) and deposition gases (like O_2 or SiH_4) can be fed simultaneously.
   - This leads to a sidewall passivation layer (e.g., oxide or polymer), which protects the sidewalls during vertical etching.
4. Reduced Microtrenching & Bowing
   - The more uniform and directional ion flow in HDP helps reduce effects like:
     - Microtrenching (excessive etching near trench bottoms)
     - Bowing (curved or sloped sidewalls)

3.2 What material is the anti-reflective coating? Name two examples

Ans: Darc

Photolithography relies on projecting light through a mask to expose patterns on a photoresist. However, reflections from underlying layers (especially metal or silicon) can interfere with the light, leading to:

- Standing wave effects
- Notching or scumming
- Line-edge roughness
- Critical dimension (CD) variations

DARC helps suppress these unwanted reflections, improving pattern fidelity and consistency.

Explain the term "Reflow soldering (3 points)

The PCB is passed through a reflow oven, which gradually heats the board in multiple stages:

- Preheat zone: Slowly raises the temperature to activate the flux and reduce thermal shock.
- Soak zone: Ensures uniform temperature and activates the flux to clean the surfaces.
- Reflow zone: Raises the temperature above the melting point of solder (~217–245°C for SAC alloys) so it flows and forms joints.
- Cooling zone: Solidifies the solder to create strong, reliable electrical and mechanical connections.

Explain the term "underfilling". What is the motivation to do this? (2 points)

Ans: Underfilling is a process in semiconductor packaging where a liquid epoxy or resin is dispensed under a chip (such as a flip-chip or BGA) after it has been attached to a substrate or PCB. The material fills the gap between the chip and the board, surrounding the solder joints.

Explain the term "Burn in". How does it work? What is the motivation to do Burn-in? How do you estimate Burn-in yield and what kind of information do we get from Burn-in yield?

Burn-in is a stress testing process used in semiconductor manufacturing to identify early-life failures (also called infant mortality failures) in integrated circuits (ICs) and electronic components before they are shipped to customers.
Burn-in yield refers to the percentage of devices that pass the burn-in process—that is, the devices that survive the applied stress conditions without failing.

🔷 2. Estimating Burn-in Yield Using Failure Rate
If you want to predict burn-in yield based on device failure rates, use the exponential failure model:

Ques: What is the minimum resolution of a 10 bit angle sensor (total range = 180degree)

Ques: Explain the term 'saturation' of sensors and name at least one example (2 points)

Ques: Explain the difference between repeatability and reproducibility. Why is this important

Ques:
Explain the formation of the so called 'Weiß' Domain

Ques: Explain Hall Effect

Ques: Explain the magnetic hysteresis for ferromagnetic materials eg iron. Explain the related physical mechanisms (11 points)

Magnetic hysteresis refers to the phenomenon where the magnetization of a ferromagnetic material (like iron) **lags behind** the external magnetic field that is applied to it. When a ferromagnetic material is magnetized and then demagnetized, it does not follow the same path—it creates a **hysteresis loop**.

What Happens Step-by-Step:

1. **Initial Magnetization**
   - When a magnetic field HHH is applied to unmagnetized iron, small regions called **magnetic domains** (where atomic magnetic moments are aligned) start to align in the direction of the field.
   - This causes the **magnetization MMM** or **magnetic flux density BBB** to increase.
2. **Saturation**
   - At some point, nearly all domains are aligned. Increasing the magnetic field further won't significantly increase the magnetization. This is called **magnetic saturation**.
3. **Remove the Magnetic Field**
   - When the external field is reduced to zero, the material **retains some magnetization**. This remaining magnetization is called **remanent magnetization** (or **retentivity**).
4. **Apply a Reverse Field**
   - To reduce the magnetization to zero, a **reverse magnetic field** must be applied. The amount of reverse field needed is the **coercive field (coercivity)**.
5. **Reverse Saturation and Loop Formation**
   - If the reverse field continues increasing, the material eventually reaches **saturation in the opposite direction**.
   - Reversing the field again will cause the same process in the opposite direction, creating a **closed loop** called the **hysteresis loop**.

Ques: Explain why Pico second lasers lead to better results regarding side wall quality during laser cut as compared to Nano second laser (4 points)

Ques: In Lase stealth dicing, an IR Laser is used to generate voids and amorphous silicon underneath the surface. Explain why voids etc are not found at the surface

Ans: Concentration of the laser beam is not high on the surface

What is the motivation behind double exposure and explain how it works?
The primary motivation for using double exposure in semiconductor lithography is to print features that are smaller and denser than what a single exposure using the current optical lithography tools and wavelengths can achieve.

What is the motivation for diameter reduction 'neck' in the early phase of the crystal growth process (2 points)

The "neck" (or "Dash neck") in the early phase of crystal growth, particularly in techniques like the Czochralski method used for silicon and other semiconductors, has a crucial and very specific motivation: **to eliminate dislocations and other structural defects from the growing crystal.**

Here's a breakdown of why this is so important and how the neck achieves it:

1. The Problem: Thermal Shock and Initial Defects

When a seed crystal (a small, perfectly formed single crystal) is first brought into contact with the molten material (e.g., molten silicon at over 1400°C), it experiences a **severe thermal shock**. This abrupt temperature difference creates significant thermal stresses within the seed crystal. These stresses are so intense that they inevitably generate **dislocations** and other crystallographic defects in the seed and the initial growth. Dislocations are linear defects in the crystal lattice where atoms are out of their perfect arrangement. If these dislocations were allowed to propagate into the main body of the crystal, they would severely degrade its electrical, optical, and mechanical properties, making it unsuitable for high-tech applications like microchips.

2. The Solution: The "Necking" Process (Dash Method)

To combat these initial defects, the crystal growth process employs a "necking" phase, pioneered by W.C. Dash in 1958:

- **Small Diameter:** After the initial contact and the formation of the first few millimeters of crystal, the pulling rate and temperature are carefully controlled to cause the growing crystal's diameter to rapidly **reduce to a very small size** (typically 2-4 mm for silicon).
- **High Pull Rate:** Simultaneously, the crystal is pulled at a relatively **high speed** (e.g., 4-6 mm/min for silicon).

3. How Necking Eliminates Dislocations:

The combination of small diameter and high pull rate works synergistically to eliminate dislocations:

- **Dislocation Movement:** Dislocations, under stress, tend to move. In a very thin neck, the crystal's cross-sectional area is extremely small, and all crystallographic slip planes (the planes along which dislocations prefer to move) are forced to intersect the outer surface of the growing crystal very quickly.
- **"Growing Out":** As the crystal is pulled rapidly, the dislocations, being mobile under the residual stresses, effectively "move out" of the crystal to its side surfaces and are terminated. There simply isn't enough volume or time for them to propagate and multiply within the confined, fast-growing neck.
- **Stress Management:** The precise balance of temperature gradients and pull speed ensures that there's just enough stress to drive the dislocations out but not so much as to generate new ones.

4. The Result: Dislocation-Free Crystal

After growing a neck of sufficient length (e.g., around 100 mm for silicon), the crystal becomes **dislocation-free**. At this point, the growth parameters are gradually adjusted to increase the diameter of the crystal, forming the "shoulder" or "cone" region, and then the main, large-diameter **single-crystal ingot (boule)** is grown, which will also be free of dislocations.

Analogy: Imagine trying to untangle a long, knotted rope. If you try to pull it fast through a very narrow tube, the knots (dislocations) will either be forced out of the tube's sides or simply cannot pass, leaving a smooth rope behind.

In essence, the necking process is a critical and elegant engineering solution that allows for the production of highly perfect single crystals, which are indispensable for the semiconductor industry and other advanced technologies.

2a. Explain the term ‘yield’. Name three manufacturing process parameters which impact yield (4 points)

The term **'yield'** in manufacturing refers to the **percentage of defect-free or salable products produced from a given amount of raw materials or units started in a production process.** It's a critical Key Performance Indicator (KPI) that measures the efficiency and effectiveness of a manufacturing process.

A higher yield indicates that the process is efficient, minimizes waste, and consistently produces high-quality products. Conversely, a low yield signifies inefficiencies, high rework rates, increased waste, and ultimately, higher manufacturing costs and potentially lower customer satisfaction.

2.2 What is the purpose of the so called ‘bubbler’? Why is there the need to use a bubbler? How does it work 4 points

2.3 Explain the term “electro-migration”. Explain the mechanism of electromigration. Why is it important to avoid it. Us sketches & diagram to explain

2.4 Explain the principle of a mass separator. Why is it important to use it inside ion implanter