GOWIN

PROGRAMMING FOR THE FUTURE

GW2A series of FPGA Products

Package & Pinout User Guide

UG111-1.8E, 12/27/2021

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Revision History

Date	Version	Description
06/18/2018	1.06E	Initial version.
09/12/2018	1.07E	● MBGA196 package information added; ● PBGA256S package information added; ● QFN88 package information added.
01/14/2019	1.08E	● LVDS pairs added in Table 2-1; ● IO BANK description and view of pin distribution updated.
04/11/2019	1.09E	● PG256C package information added; ● MG196 pins description updated; ● EQ144 package information added.
06/04/2019	1.1E	PG484 package outline changed.
07/10/2019	1.2E	The GW2A-55 UG324 package added.
07/29/2019	1.3E	● GW2A-18 PG484 package outline changed; ● GW2A-55 PG484 package outline added.
12/12/2019	1.4E	● GW2A-55 UG324D package information added; ● GW2A-18 PG256E package information added;
03/06/2020	1.5E	● Pin distribution table of GW2A-18 PG256C, UG324, and PG256E updated; ● Pin distribution table of GW2A-55 UG324 and UG324D updated; ● GW2A-18C and GW2A-55C added.
04/16/2020	1.5.1E	I/O Information of GW2A-55 UG324 updated.
09/25/2020	1.6E	The GW2A-55 UG676 package added.
07/16/2021	1.7E	The UG484 and PG256CF packages of GW2A-18 added.
08/25/2021	1.7.1E	PG256 package outline updated.
12/27/2021	1.8E	● The PG256SF package of GW2A-18 added. ● The UG324F package of GW2A-55 added.

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1 About This Guide

1.1 Purpose

This manual mainly contains an introduction to the GW2A series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pin, and package diagrams.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS102, GW2A series of FPGA Products Data Sheet
- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG111, GW2A series FPGA Products Package and Pinout
- UG110, GW2A-18 Pinout
- UG113, GW2A-55 Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
LVDS	Low-Voltage Differential Signaling
GPIO	Gowin Programmable IO
LQ	LQFP
EQ	ELQFP
PG	PBGA
UG	UBGA

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW2A series of FPGA products are the first-generation products of Arora® family. They are available in various forms that offer high I/O compatibility and flexible usage.

2.1 PB-Free Package

The GW2A series of FPGA Products are PB free, in line with the EU ROHS environmental directives. The substances used in the GW2A series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. I/O Information

Table 2-1 Package and Max. I/O Information

Package	Pitch(mm)	Size(mm)	GW2A-18	GW2A-55
QN88	0.4	10 x 10	66（22）	-
LQ144	0.5	22 x 22	119（34）	
EQ144	0.5	22 x 22	119（34）	-
MG196	0.5	8 x 8	114（39）	-
PG256	1.0	17 x 17	207（73）	-
PG256S	1.0	17 x 17	192（72）	-
PG256SF	1.0	17 x 17	192（71）	-
PG256C	1.0	17 x 17	190（64）	-
PG256CF	1.0	17 x 17	190（65）	
PG256E	1.0	17 x 17	162（29）	-
UG324	0.8	15 x 15	239（90）	240（86）
UG324F	0.8	15 x 15	-	240（86）
UG324D	0.8	15 x 15	-	240（72）
UG484	0.8	19 x 19	379（94）	-
UG676	0.8	21 x 21	-	525（97）
PG484	1.0	23 x 23	319（78）	319（76）
PG1156	1.0	35 x 35	-	607（97）

Note!

- The package types in this manual are written with abbreviations. See 1.3 Abbreviations and Terminology;
- ⟷ denotes that the various device pins are compatible when the package types are the same;
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- For GW2A-18 LQ144 package, I/O rate of JTAG pin multiplexing is less than 40 MHz.

2.3 Power Pin

Table 2-2 GW2A Power Pin

VCC	VCCO0	VCCO1	VCCO2
VCCO3	VCCO4	VCCO5	VCCO6
VCCO7	VCCX	VSS	NC
VCCPLLL0	VCCPLLL1	VCCPLLR0	VCCPLLR1
VCCPLLL	VCCPLLR		

2.4 Pin Quantity

2.4.1 Quantity of GW2A-18 Pins

Table 2-3 Quantity of GW2A-18 Pins

Pin Type		GW2A-18												
		QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
I/O Single end/Differential pair /LVDS[1]	BANK0	8/4/2	19/8/4	19/8/4	12/6/4	29/14/10	20/10/8	25/12/8	28/14/12	40/20/10	26/13/5	48/24/12	26/12/8	20/10/8
	BANK1	9/4/4	12/6/6	12/6/6	14/7/6	20/10/10	19/9/9	26/12/11	28/14/11	39/18/10	14/7/3	47/23/12	25/12/11	19/9/9
	BANK2	4/2/1	12/6/3	12/6/3	16/8/5	20/10/7	30/15/11	16/7/5	28/14/10	46/23/11	12/6/2	47/23/11	16/7/5	30/15/11
	BANK3	17/6/3	21/9/5	21/9/5	25/12/7	29/13/10	37/18/10	36/17/9	39/19/11	31/15/8	31/12/4	47/23/11	36/17/9	37/18/9
	BANK4	8/3/3	17/8/6	17/8/6	13/6/4	36/18/12	16/7/7	27/13/11	28/14/12	40/20/10	18/9/3	48/24/12	27/13/11	16/7/7
	BANK5	10/5/5	16/8/5	16/8/5	8/4/3	36/18/11	18/9/8	26/12/9	28/14/12	40/20/10	18/9/4	48/24/12	26/12/9	18/9/8
	BANK6	9/4/4	11/5/3	11/5/3	12/6/5	18/9/8	24/12/8	19/9/7	28/14/11	34/17/8	20/10/4	47/23/12	19/9/7	24/12/8
	BANK7	1/0/0	8/4/2	8/4/2	14/7/5	16/7/5	28/14/11	15/7/5	32/16/11	46/23/11	23/11/4	47/23/12	15/7/5	28/14/11
Max. User I/O[2]		66	119	119	114	207	192	190	239	319	162	379	190	192
Differential Pair		28	54	54	56	99	94	89	119	157	77	187	89	94
TrueLVDS Output		22	34	34	39	73	72	65	90	78	26	94	65	71
VCC		4	0	0	0	6	6	10	11	32	11	12	0	6
VCCX		0	0	0	8	2	8	0	12	8	6	0	0	8
VCCO0		1	1	1	2	2	3	3	3	3	2	4	3	3
VCCO1		1	1	1	2	2	2	3	3	3	2	5	3	2
VCCO2		0	0	0	3	1	3	2	3	3	2	0	2	3
VCCO3		1	2	2	3	2	3	2	3	3	3	5	2	3
VCCO4		1	1	1	2	2	2	3	3	3	2	4	3	2
VCCO5		1	1	1	2	2	2	3	3	3	6	5	3	2
VCCO6		0	0	0	3	1	3	2	3	3	2	0	2	3
VCCO7		1	2	2	3	2	2	0	3	3	2	0	0	2
VCCO6/VCCO7		0	0	0	0	0	0	0	0	0	0	9	0	0
VCCX/VCCO2		0	0	0	0	0	0	0	0	0	0	4	0	0

Pin Type	GW2A-18												
	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
VCCX/VCCO7	0	0	0	0	0	0	2	0	0	0	0	2	0
VCC/VCCPLLL1[3]	0	4	4	0	0	0	0	0	0	0	0	0	0
VCCX/ VCCO2/ VCCO6[3]	2	2	2	0	0	0	0	0	0	0	0	0	0
VCCPLLL0	0	1	1	0	0	0	0	0	0	0	1	0	0
VCCPLLL1	1	0	0	0	0	0	0	0	0	0	1	0	0
VCCPLLR0	0	1	1	0	0	0	0	0	0	0	1	0	0
VCCPLLR1	1	1	1	0	0	0	0	0	0	0	1	0	0
VCCPLLL	0	0	0	0	1	1	1	0	2	0	0	0	1
VCCPLLR	0	0	0	0	1	1	1	0	2	0	0	0	1
VCC/VCCPLLL/VCCPLLR	0	0	0	0	0	0	10	11	0	11	0	10	0
VCC/VCCPLLL0/VCCPLLL1/ VCCPLLR0/VCCPLLR1	0	0	0	15	0	0	0	0	0	0	0	0	0
VSS	7	7	7	39	24	26	33	37	95	52	52	33	26
MODE0	1	1	1	1	1	1	1	1	1	0	1	1	1
MODE1	1	1	1	1	1	1	1	1	1	0	1	1	0
MODE2	0	1	1	0	1	0	1	1	1	0	1	1	1
EXTR	1	1	1	0	1	0	0	0	1	0	0	0	1
JTAGSEL_N	0	0	0	0	0	1	1	1	1	0	1	1	1
NC	0	0	0	0	0	1	2	0	0	4	0	2	1

Note!

- [1]Single end/ Differential/LVDS I/O quantity include CLK pins, and download pins; The EXTR No. is excluded;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3]Pin multiplexing.

2.4.2 Quantity of GW2A-55 Pins

Table 2-4 Quantity of GW2A-55 Pins

Pin Type		GW2A-55					
		UG324	UG324D	PG484	PG1156	UG676	UG324F
I/O Single end/Differential pair/LVDS/LVDS output[1]	BANK0	28/14/10	28/14/10	40/20/10	80/40/14/6	68/34/14/0	28/14/10
	BANK1	28/14/13	28/14/13	39/19/10	79/39/16/4	71/35/16/0	28/14/13
	BANK2	28/14/10	28/14/10	46/23/10	80/40/10/10	66/33/10/3	28/14/10
	BANK3	40/20/9	40/20/9	31/15/8	61/30/9/7	58/29/9/4	40/20/9
	BANK4	28/14/13	28/14/13	40/20/10	80/40/16/4	72/36/16/0	28/14/13
	BANK5	28/14/13	28/14/13	40/20/10	80/40/14/6	68/34/14/0	28/14/13
	BANK6	28/14/9/1	28/5/2	34/17/8	64/32/8/8	56/28/8/4	28/14/9/1
	BANK7	32/16/10	32/5/1	46/23/10	80/40/10/10	66/33/10/3	32/16/10
Max. User I/O[2]		240	240	319	607	525	240
Differential Pair		120	100	157	301	262	120
True LVDS Output		86	71	76	97	97	86
Only True LVDS Output[3]		0	0	0	55	14	0
VCC		11	11	32	32	19	11
VCCX		12	12	8	16	14	12
VCCO0		3	3	3	12	5	3
VCCO1		3	3	3	11	4	3
VCCO2		3	3	3	12	5	3
VCCO3		3	3	3	11	4	3
VCCO4		3	3	3	12	5	3
VCCO5		3	3	3	11	4	3
VCCO6		3	3	3	12	5	3
VCCO7		3	3	3	11	4	3
VCCPLLL		0	0	2	2	2	0
VCCPLLR		0	0	2	2	2	0
VSS		37	37	95	172	77	37
MODE0		0	0	1	1	1	0
MODE1		0	0	1	1	1	0
MODE2		1	1	1	1	1	1
MODE0/MODE1		1	1	0	0	0	1
EXTR		0	0	1	1	0	0
NC		0	0	0	231	0	0
JTAGSEL_N		1	1	1	1	1	1

Note!

- [1]I/O Single end/ Differential pair/LVDS/ LVDS output quantity include CLK pins and download pins, PG484 has no LVDS output; The EXTR No. is excluded;

- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3]Support true LVDS output only, do not support input.

2.5 Pin Definitions

The location of the Pins in the GW2A series of FPGA products varies according to the different packages.

Table 2-5 provides a detailed overview of user I/O, multi-function pins, dedicated pins, and other pins.

Table 2-5 Definition of the Pins in the GW2A series of FPGA Products

Pin Name	I/O	Description
User I/O Pins		
IO[End][Row/Column Number][A/B]	I/O/LVDS	[End] indicates the pin location, including L (left) R(right) B(bottom), and T(top) [Row/Column Number] indicates the pin Row/Column number. If [End] is T (top) or B (bottom), the pin indicates the column number of the corresponding CFU. If [End] is L (left) or R (right), the pin indicates the Row number of the corresponding CFU. [A/B] indicates differential signal pair information.
		LVDS in the I/O column indicates that the pin support LVDS output only.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. These pins can be used as user I/O when the functions are not used.
RECONFIG_N	I, internal weak pull-up	Start new GowinCONFIG mode when low pulse
READY	I/O	When high level, the device can be programmed and configured When low level, the device cannot be programmed and configured
DONE	I/O	High level indicates successful program and configure Low level indicates incomplete or failed to program and configure
FASTRD_N /D3	I/O	In MSPI mode, FASTRD_N is used as Flash access speed port. Low indicates high-speed Flash access mode high indicates regular Flash access mode. Data port D3 in CPU mode
MCLK /D4	I/O	Clock output MCLK in MSPI mode Data port D4 in CPU mode
MCS_N /D5	I/O	Enable signal MCS_N in MSPI mode, active-low Data port D5 in CPU mode
MI /D7	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D7 in CPU mode
MO /D6	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D6 in CPU mode
SSPI_CS_N/D0	I/O	Enable signal SSPI_CS_N in SSPI mod, active-low,

Pin Name	I/O	Description
		Internal Weak Pull Up Data port D0 in CPU mode
SO /D1	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D1 in CPU mode
SI /D2	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D2 in CPU mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode, which needs to be connected with 4.7 K drop-down resistance on PCB
TDI	I, internal weak pull-up	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Select signal in JTAG mode, active-low
SCLK	I	Clock input in SSPI, SERIAL, and CPU mode
DIN	I, internal weak pull-up	Input data in SERIAL mode
DOUT	O	Output data in SERIAL mode
CLKHOLD_N	I, internal weak pull-up	High level, SCLK will be connected internally in SSPI mode or CPU mode Low level, SCLK will be disconnected from SSPI mode or CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode
GCLKT_[x]	I	Pins for global clock input, T(True), [x]: global clock No.
GCLKC_[x]	I	Differential comparation input pin of GCLKT_[x], C(Comp), [x]: global clock No.[1].
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback input pin, T(True)
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pin, T(True)
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pin, C(Comp)
Dedicated Pins		
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
EXTR	NA	External 10K 1% resister grounding
The Other Pins		
NC	NA	Reserved.
VSS	NA	Ground pins
VCC	NA	Power supply pins for internal core logic.
VCCO#	NA	Power supply pins for the I/O voltage of I/O BANK#.

Pin Name	I/O	Description
VCCX	NA	Power supply pins for auxiliary voltage.
VCCPLLL01	NA	LQFP: Power supply pins for left PLL0/1, only available for LQFP.
VCCPLLR0/1	NA	LQFP: Power supply pins for right PLL0/1, only available for LQFP.
VCCPLLL	NA	PBGA: Power supply pins for left PLL0/1.
VCCPLLR	NA	PBGA: Power supply pins for right PLL0/1.

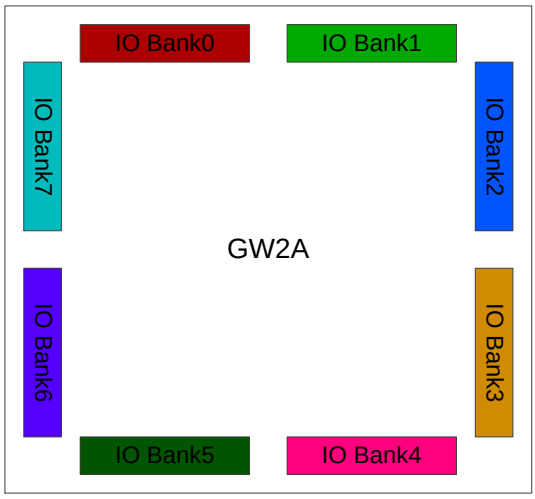
Note!

[1]When the input is single-ended, the GLKC_[x] pin is not a global clock pin.

2.6 Introduction to the I/O BANK

There are eight I/O Banks in the GW2A series of FPGA products, as shown in Figure 2-1.

Figure 2-1 GW2A I/O Bank Distribution



This manual provides an overview of the distribution view of the pins in the GW2A series of FPGA products. The eight I/O Banks that form the GW2A series of FPGA products are marked with eight different colors.

User I/O, power, and ground are marked with different symbols and colors. The various symbols and colors used for the various pins are defined as follows:

- "" denotes I/Os in BANK0. The filling color changes with the BANK;
- "" denotes I/Os in BANK1. The filling color changes with the BANK;
- "" denotes I/Os in BANK2. The filling color changes with the BANK;
- "" denotes I/Os in BANK3. The filling color changes with the BANK;
- "" denotes I/Os in BANK4. The filling color changes with the BANK;
- "" denotes I/Os in BANK5. The filling color changes with the BANK;
- "" denotes I/Os in BANK6. The filling color changes with the BANK;
- "" denotes I/Os in BANK7. The filling color changes with the BANK;

- "  " denotes VCC, VCCX, and VCCO. The filling color does not change;
- "  " denotes VSS. The filling color does not change;
- "  " denotes NC;
- "  " denotes dedicated pins EXTR.

3 View of Pin Distribution

3.1 View of GW2A-18 Pins Distribution

3.1.1 View of QN88 Pins Distribution

Figure 3-1 GW2A-18 QN88 View of Pins Distribution (Top View)

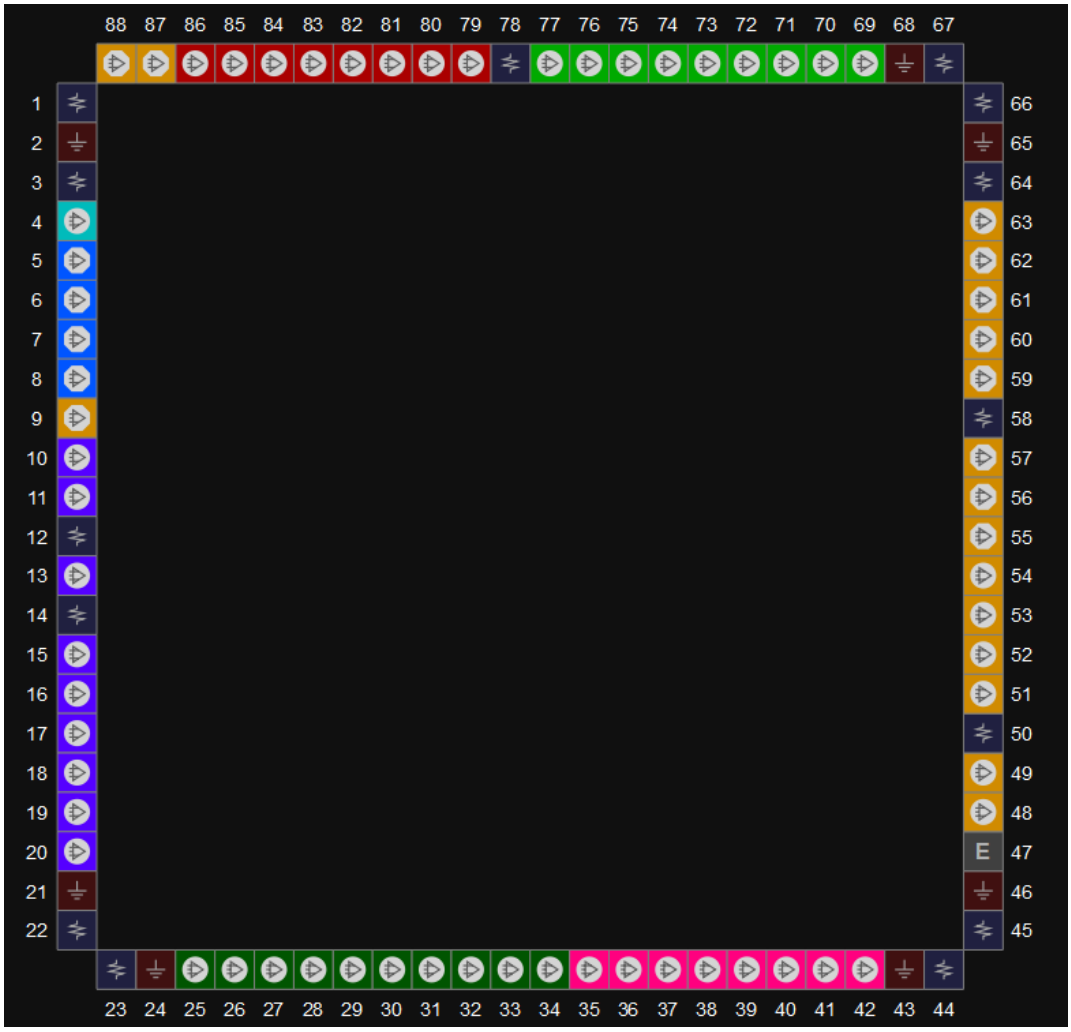


Table 3-1 Other Pins in GW2A-18 QN88

VCC	1, 22, 45, 66
VCCX/ VCCO2/ VCCO6	12, 64
VCCO0	78
VCCO1	67
VCCO3	58
VCCO4	44
VCCO5	23
VCCO7	3
VCCPLLL1	14
VCCPLLR1	50
VSS	2, 21, 24, 43, 46, 65, 68
EXTR	47
MODE	87, 88

3.1.2 View of LQ144 Pins Distribution

Figure 3-2 GW2A-18 LQ144 View of Pins Distribution

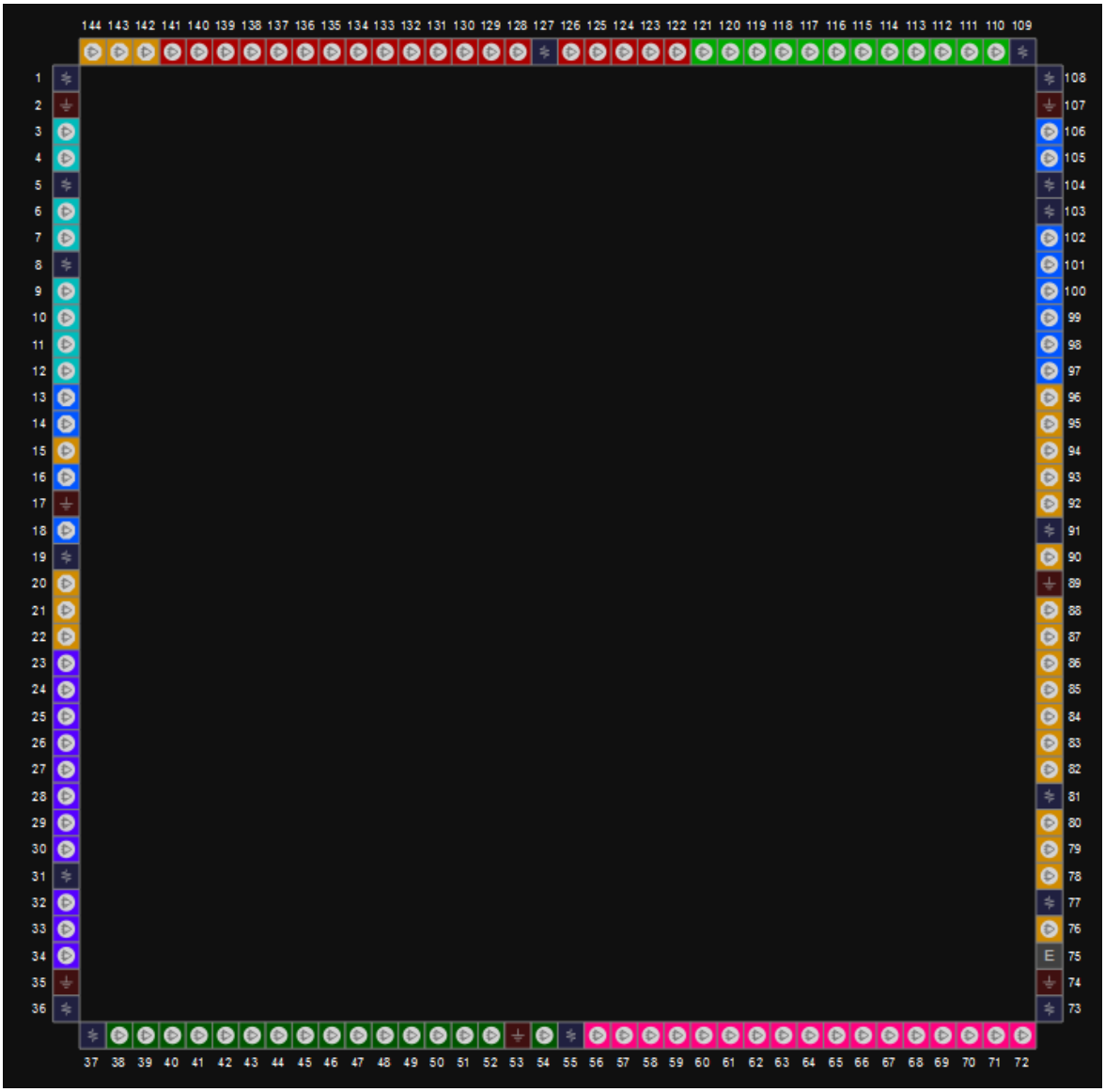


Table 3-2 Other Pins in GW2A-18 LQ144

VCC/VCCPLLL1	1, 36, 73, 108
VCCX/ VCCO2/ VCCO6	31, 103
VCCO0	127
VCCO1	109
VCCO3	77, 91
VCCO4	55
VCCO5	37
VCCO7	5,19
VCCPLLL0	8
VCCPLLR0	104
VCCPLLR1	81
VSS	2, 17, 35, 53, 74, 89, 107
EXTR	75
MODE	142, 143, 144

3.1.3 View of EQ144 Pins Distribution

Figure 3-3 GW2A-18 EQ144 View of Pins Distribution

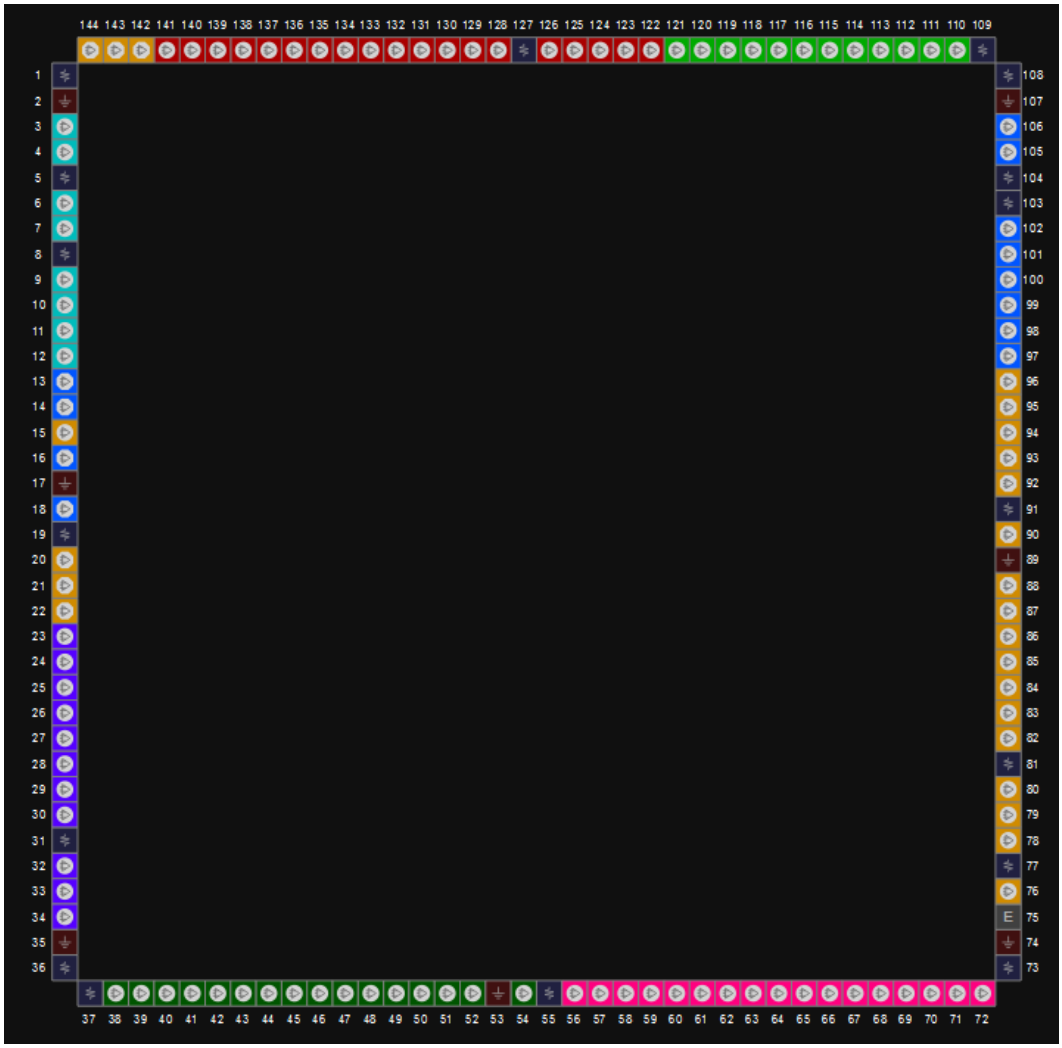


Table 3-3 Other Pins in GW2A-18 EQ144

VCC/VCCPLLL1	1, 36, 73, 108
VCCX/ VCCO2/ VCCO6	31, 103
VCCO0	127
VCCO1	109
VCCO3	77, 91
VCCO4	55
VCCO5	37
VCCO7	5,19
VCCPLLL0	8
VCCPLLR0	104
VCCPLLR1	81
VSS	2, 17, 35, 53, 74, 89, 107
EXTR	75
MODE	142, 143, 144

3.1.4 View of MG196 Pins Distribution

Figure 3-4 GW2A-18 MG196 View of Pins Distribution

Table 3-4 Other Pins in GW2A-18 MG196

VCC/VCCPLLL0/VCCPLLL1 /VCCPLLR0/VCCPLLR1	E10, E5, E6, E9, F10, F5, F6, F9, J5, J6, J9, K10, K5 K6, K9
VCCO0	C10, C4
VCCO1	C5, C9
VCCO2	D12, E12, G11
VCCO3	G12, K11, K12
VCCO4	M10, M5
VCCO5	M6, M9
VCCO6	E3, E4, G3
VCCO7	H3, K3, K4
VCCX	D7, E7, G10, G9, H5, H6, K7, L7
VSS	A1, A14, C2, C3, C6, C7, D10, D5, D6, D9, E11, E8, F7 F8, G4, G5, G6, G7, G8, H10, H4, H7, H8, H9, J10, J7 J8, K8, L10, L11, L3, L5, L6, L9, M11, M3, M7, P1, P14
MODE	N9, P13

3.1.5 View of PG256 Pins Distribution

Figure 3-5 GW2A-18 PG256View of Pins Distribution

Table 3-5 Other Pins in GW2A-18 PG256 (Power, MODE, and Ground, compatible with GW1N)

VCC	A1, A16, G7, K10, T1, T16
VCCO0	E13, H10
VCCO1	J10, M13
VCCO2	N12
VCCO3	K8, N5
VCCO4	M4, J7
VCCO5	E4, H7
VCCO6	D5
VCCO7	D12, G9
VCCX	G8, K9
VCCPLLL	G10
VCCPLLR	K7
VSS	B2, B15, C3, C14, D4, D13, E5, E12, F6, F11, H8, H9, J8, J9, L6, L11 M5, M12, N4, N13, P3, P14, R2, R15
EXTR	L7
MODE	B16, C15, M16

3.1.6 View of PG256S Pins Distribution

Figure 3-6 GW2A-18 PG256S View of Pins Distribution

Table 3-6 Other Pins in GW2A-18 PG256S

VCC	G7, G9, H8, J9, K10, K8
VCCO0	B4, B9, D7
VCCO1	B13, D10
VCCO2	D15, G13, J15
VCCO3	K13, N15, R13
VCCO4	N10， R8
VCCO5	R4， N7
VCCO6	J2, K4, N2
VCCO7	D2, G4
VCCX	E5, F11, F8, G10, H6, J10, L6, L9
VCCPLLL	J7
VCCPLLR	H10
VSS	A1, A16, B11, B7, D13, D4, E9, G15, G2, G8, H12, H7, H9, J5, J8, K7, K9, L15, L2, M8, N13, P3, R10, R6, T1, T16
NC	P14
MODE	T11, N11
JTAGSEL_N	D12

3.1.7 View of PG256C Pins Distribution

Figure 3-7 GW2A-18 PG256C View of Pins Distribution

Table 3-7 Other Pins in GW2A-18 PG256C

VCC/VCCPLLL/ VCCPLLR	D13, G10, G6, G7, G8, G9, H11, H6, K7, N4
VCCO0	A1, C4, C7
VCCO1	A16, C10, C13
VCCO2	E14, G14
VCCO3	K14, M14
VCCO4	P10, P13, T16
VCCO5	P4, P7, T1
VCCO6	K3, M3
VCCX /VCCO7	E3, G3
VCCPLLL	L5
VCCPLLR	F12
VSS	B15, B2, C12, C5, D10, D7, E12, E13, E2, E4, G13, G4, H10, H15 H16, H7, H8, H9, J10, J7, J8, J9, K13, K4, M13, M4, M5, N10, N7 P12, P5, R15, R2
NC	L5,F12
MODE	H13, H12, G12
JTAGSEL_N	C11

3.1.8 View of UG324 Pins Distribution

Figure 3-8 GW2A-18 UG324 View of Pins Distribution (Top View)

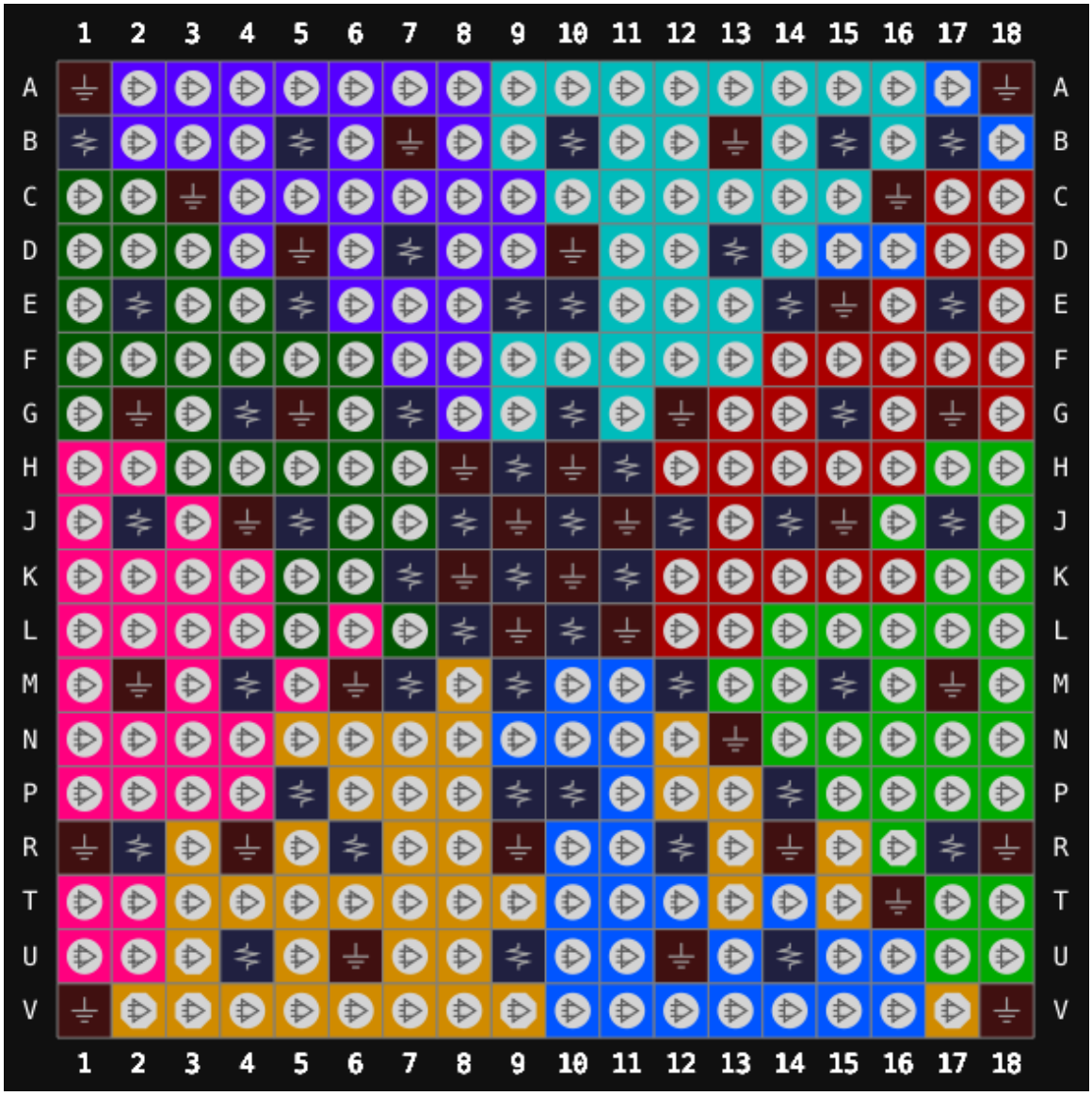


Table 3-8 Other Pins in GW2A-18 UG324

VCC/VCCPLLL/ VCCPLLR	G7,H11,H9 J10,J8,K11,K9,L10,L8,M12,M7
VCCO0	E17,G15,J14
VCCO1	J17,M15,R17
VCCO2	P9,R12,U14
VCCO3	R6,U4,U9
VCCO4	J5,M4,R2
VCCO5	E2,G4,J2
VCCO6	B10,B5,D7
VCCO7	B15,D13,E10
VSS	A1,A18,B13,B7,C16,C3,D10,D5,E15,G12,G17,G2,G5,H10,H8,J11,J1 ,J4,J9,K10,K8,L11,L9,M17,M2,M6,N13,R1,R14,R18,R4,R9,T16,U12, U6,V1
MODE	T15,N12
JTAGSEL_N	R16

3.1.9 View of PG484 Pins Distribution

Figure 3-9 GW2A-18 PG484 View of Pins Distribution (Top View)

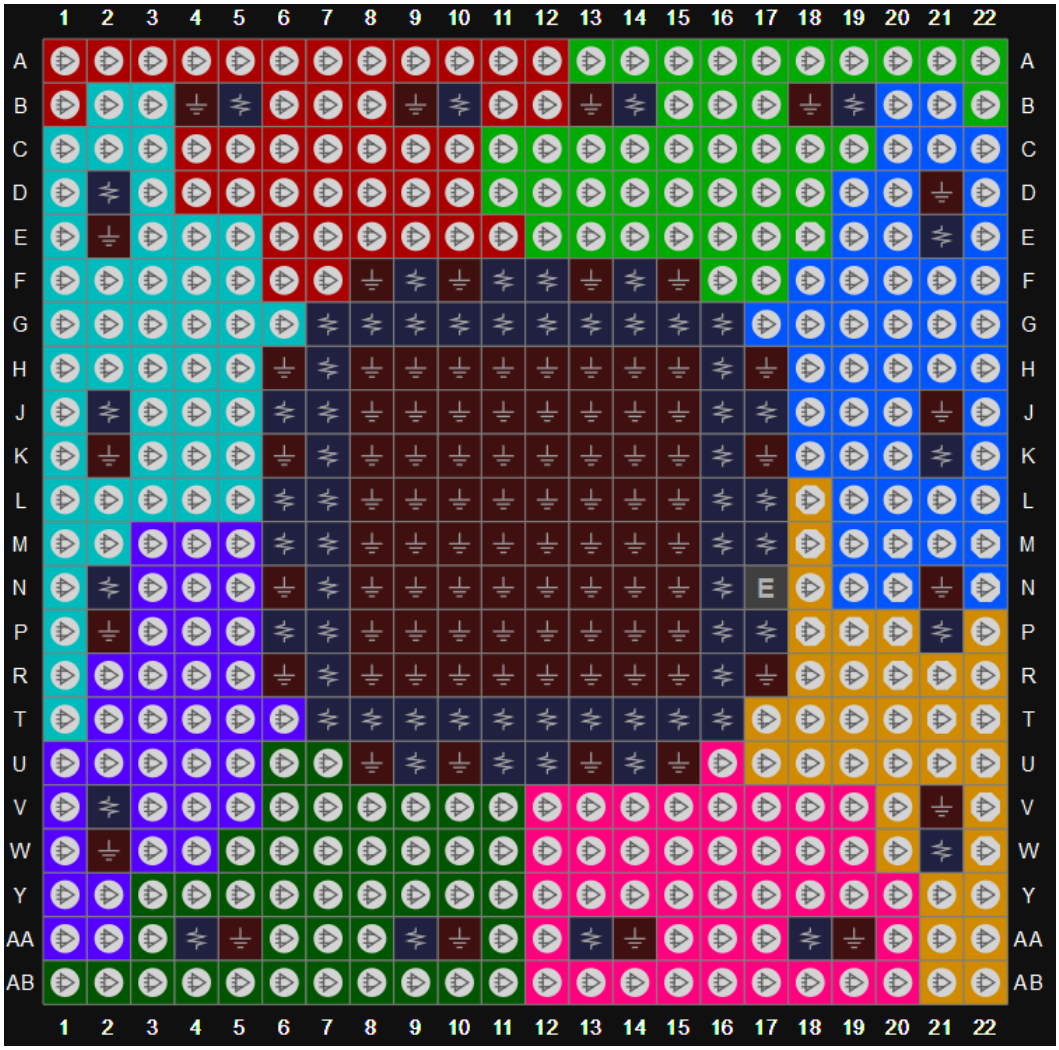


Table 3-9 Other Pins in GW2A-18 PG484

VCC	G10, G11, G12, G13, G14, G15, G16, G7, G8, G9, H16, H7, J16, J7 L16, L7, M16, M7, P16, P7, R16, R7, T10, T11, T12, T13, T14, T15, T16 T7, T8, T9
VCCO0	B5, B10, F11
VCCO1	B14, B19, F12
VCCO2	E21, K21, L17
VCCO3	M17, P21, W21
VCCO4	AA13, AA18, U12
VCCO5	U11, AA4, AA9
VCCO6	M6, N2, V2
VCCO7	D2, J2, L6
VCCX	F14, F9, J6, J17, P6, P17, U9, U14
VCCPLLL	N7, K7
VCCPLLR	N16, K16
VSS	AA10, AA14, AA19, AA5, B13, B18, B4, B9, D21, E2, F10, F13, F15, F8 H10, H11, H12, H13, H14, H15, H17, H6, H8, H9, J10, J11, J12, J13 J14, J15, J21, J8, J9, K10, K11, K12, K13, K14, K15, K17, K2, K6, K8 K9, L10, L11, L12, L13, L14, L15, L8, L9, M10, M11, M12, M13, M14 M15, M8, M9, N10, N11, N12, N13, N14, N15, N21, N6, N8, N9, P10 P11, P12, P13, P14, P15, P2, P8, P9, R10, R11, R12, R13, R14, R15 R17, R6, R8, R9, U10, U13, U15, U8, V21, W2
EXTR	N17
MODE	U22, U21, T22
JTAGSEL_N	E18

3.1.10 View of PG256E Pins Distribution

Figure 3-10 GW2A-18 PG256E View of Pins Distribution

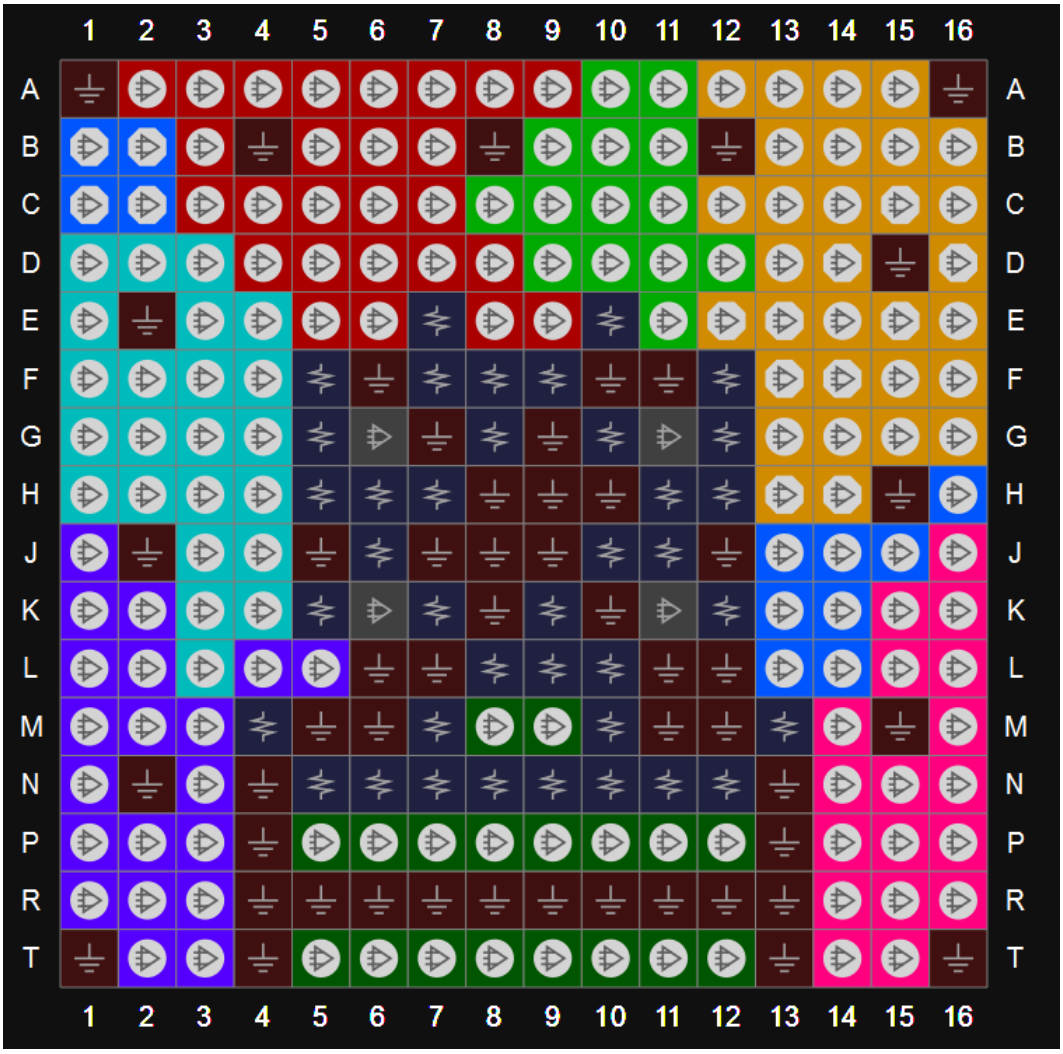


Table 3-10 Other Pins in GW2A-18 PG256E

VCC/VCCPLL/VCCPLLR	F5,G10,G8,H7,J10,K7,K9,L8,L9,M10,M7
VCCO0	E7,F7
VCCO1	E10,F9
VCCO2	G12,H11
VCCO3	F12,N7,N8
VCCO4	J11,M13
VCCO5	N10,N11,N12,N5,N6,N9
VCCO6	J6,M4
VCCO7	G5,H6
VCCX	F8,H12,H5,K12,K5,L10
VSS	A1,A16,B12,B4,B8,D15,E2,F10,F11,F6,G7,G9,H10,H15,H8,H9.J12,J2,J5,J7,J8,J9,K10,K8,L12,L6,L7,M11,M12,M15,M5,M6,N13,N2,N4,P13,P4,R10,R11,R12,R13,R4,R5,R6,R7,R8,R9,T1,T13,T16,T4, L11
NC	G6,G11,K11,K6

3.1.11 View of UG484 Pins Distribution

Figure 3-11 GW2A-18 UG484 View of Pins Distribution

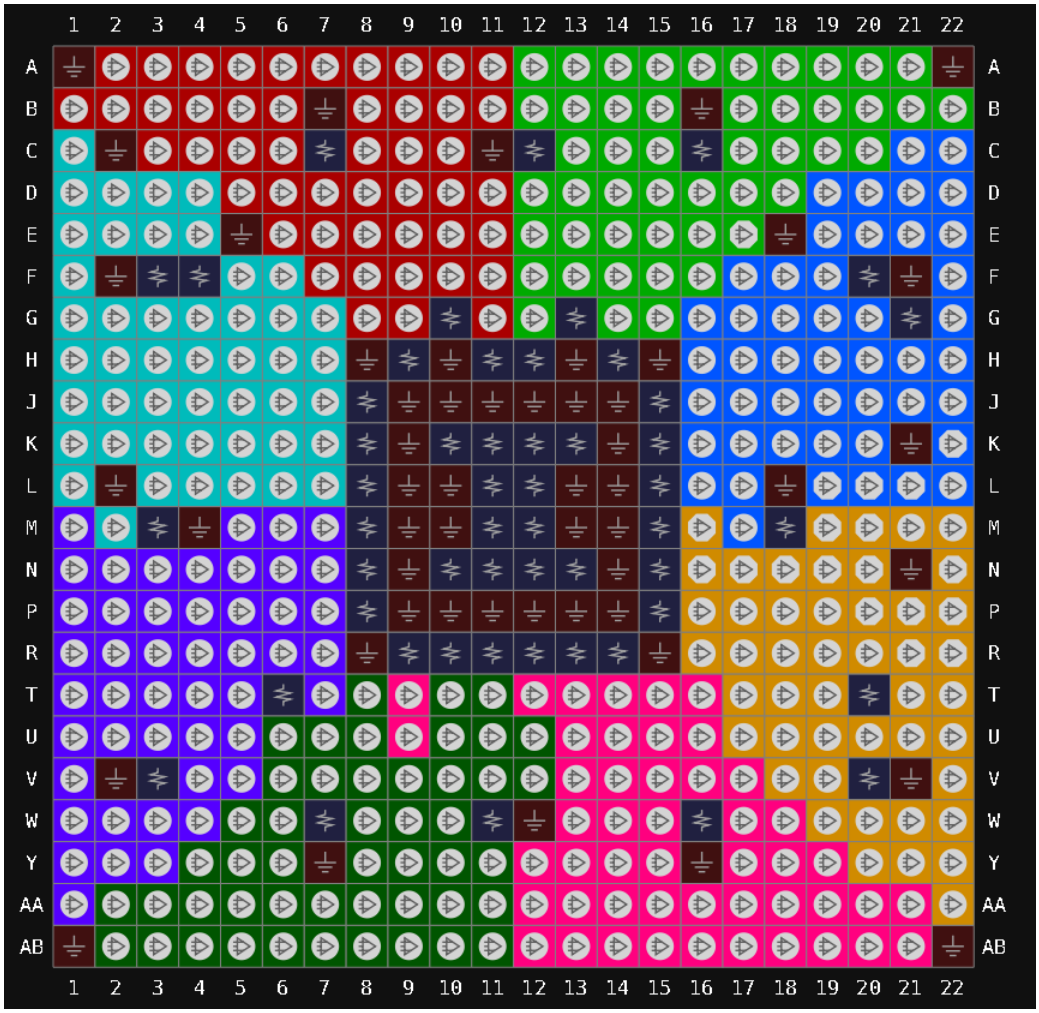


Table 3-11 Other Pins in GW2A-18 UG484

VCC	K10,K11,K12,K13,L11,L12,M11,M12,N10,N11,N12,N13
VCCO0	C7,G10,H11,H9
VCCO1	C12,C16,G13,H12,H14
VCCO3	M15,M18,N15,P15,V20
VCCO4	R12,R13,R14,W16
VCCO5	R10,R11,R9,W11,W7
VCCO6/VCCO7	F3,J8,K8,L8,M3,M8,N8,P8,V3
VCCX/VCCO2	F20,J15,K15,L15
VCCPLLL0	F4
VCCPLLL1	T6
VCCPLLR0	G21
VCCPLLR1	T20
VSS	A1,A22,AB1,AB22,B16,B7,C11,C2,E18,E5,F2,F21,H10,H13,H15,H8,J10,J11,J12,J13,J14,J9,K14,K21,K9,L10,L13,L14,L18,L2,L9,M10,M13,M14,M4,M9,N14,N21,N9,P10,P11,P12,P13,P14,P9,R15,R8,V2,V21,W12,Y16,Y7

3.1.12 View of PG256CF Pins Distribution

Figure 3-12 GW2A-18 PG256CF View of Pins Distribution

Table 3-12 Other Pins in GW2A-18 PG256CF

VCC/VCCPLLL/ VCCPLLR	D13, G10, G6, G7, G8, G9, H11, H6, K7, N4
VCCO0	A1, C4, C7
VCCO1	A16, C10, C13
VCCO2	E14, G14
VCCO3	K14, M14
VCCO4	P10, P13, T16
VCCO5	P4, P7, T1
VCCO6	K3, M3
VCCX /VCCO7	E3, G3
VSS	B15, B2, C12, C5, D10, D7, E12, E13, E2, E4, G13, G4, H10, H15, H16, H7, H8, H9, J10, J7, J8, J9, K13, K4, M13, M4, M5, N10, N7, P12, P5, R15, R2
NC	L5,F12
MODE	H13, H12, G12
JTAGSEL_N	C11

3.1.13 View of PG256SF Pins Distribution

Figure 3-13 GW2A-18 PG256SF View of Pins Distribution

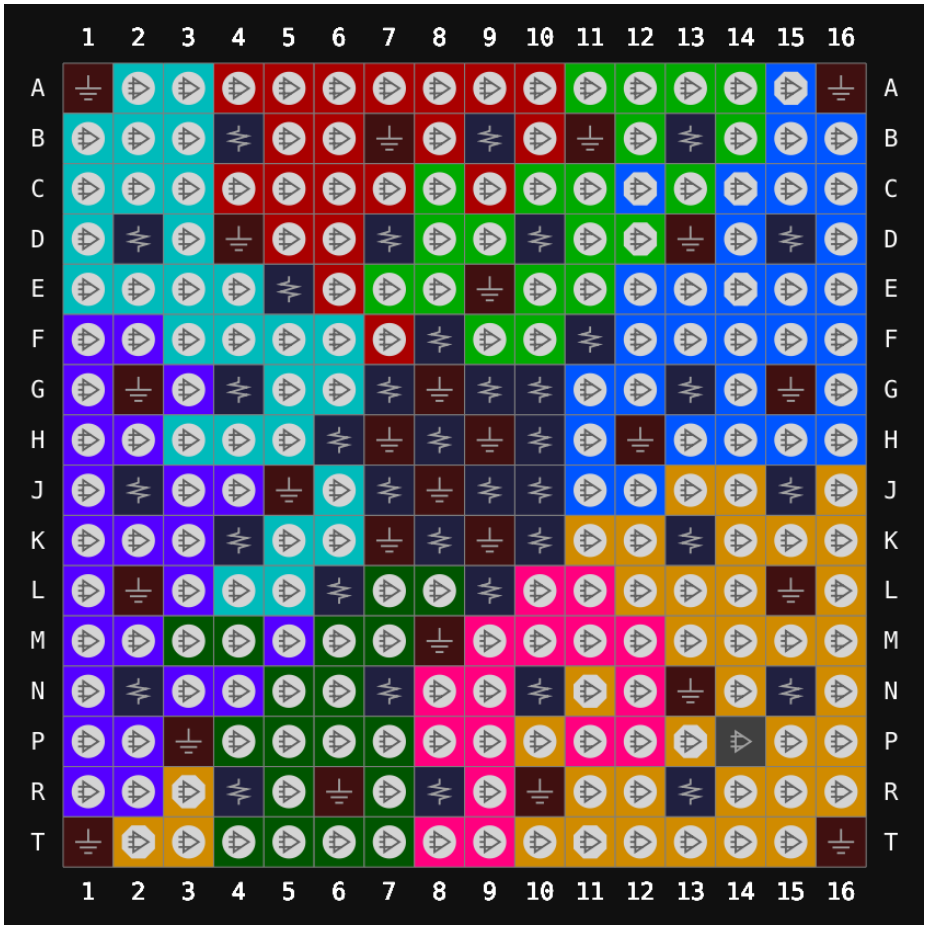


Table 3-13 Other Pins in GW2A-18 PG256SF

VCC	G7,G9,H8,J9,K10,K8
VCCO0	D7,B4,B9
VCCO1	D10,B13
VCCO2	D15,G13,J15
VCCO3	K13,N15,R13
VCCO4	N10,R8
VCCO5	N7,R4
VCCO6	K4,N2,J2
VCCO7	G4,D2
VCCPLLL	J7
VCCPLLR	H10
VCCX	E5,F11,F8,G10,H6,J10,L6,L9
VSS	A1,A16,B11,B7,D13,D4,E9,G15,G2,G8,H12,H7,H9,J5,J8,K7,K9,L15, L2,M8,N13,P3,R10,R6,T1,T16
NC	P14
MODE	T11,N11
JTAGSEL_N	D12

3.2 View of GW2A-55 Pin Distribution

3.2.1 View of UG324 Pin Distribution

Figure 3-14 View of GW2A-55 UG324 Pin Distribution

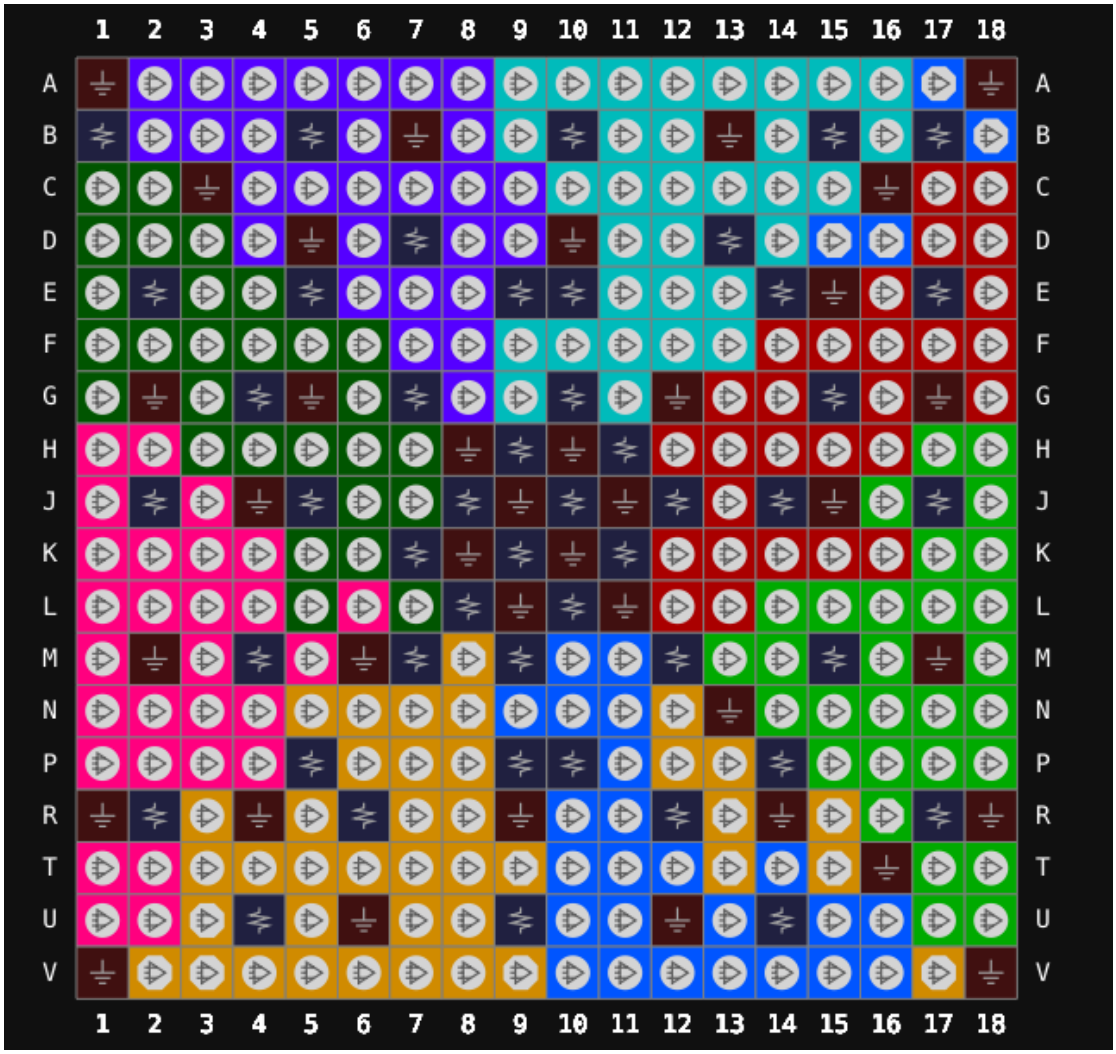


Table 3-14 Other Pins of GW2A-55 UG324

VCC/VCCPLLL/ VCCPLLR	G7,H11,H9,J10,J8,K11,K9,L10,L8,M12,M7
VCCO0	E17,J14,G15
VCCO1	J17,M15,R17
VCCO2	P9,R12,U14
VCCO3	R6,U4,U9
VCCO4	J5,M4,R2
VCCO5	E2,G4,J2
VCCO6	B10,B5,D7
VCCO7	B15,D13,E10
VCCX	B1,B17,E14,E5,E9,G10,J12,K7,M9,P10,P14,P5
VSS	A1,A18,B13,B7,C16,C3,D10,D5,E15,G12,G17,G2,G5,H10,H8,J11,J15,J4,J9,K10,K8,L11,L9,M17,M2,M6,N13,R1,R14,R18,R4,R9,T16,U12,U6,V1,V18
MODE	T15,N12

3.2.2 View of UG324D Pin Distribution

Figure 3-15 View of GW2A-55 UG324D Pin Distribution

Table 3-15 Other Pins of GW2A-55 UG324D

VCC/VCCPLLL/ VCCPLLR	M7,M12,L8,L10,K9,K11,J8,J10,H9,H11,G7
VCCO0	J14,G15,E17
VCCO1	J17,M15,R17
VCCO2	P9,R12,U14
VCCO3	R6,U4,U9
VCCO4	J5,M4,R2
VCCO5	E2,G4,J2
VCCO6	B10,B5,D7
VCCO7	B15,D13,E10
VCCX	B1,B17,E14,E5,E9,G10,J12,K7,M9,P10,P14,P5
VSS	A1,A18,B13,B7,C16,C3,D10,D5,E15,G12,G17,G2,G5,H10,H8,J11,J15,J4,J9,K10,K8,L11,L9,M17,M2,M6,N13,R1,R14,R18,R4,R9,T16,U12,U6,V1,V18
MODE	T15,N12

3.2.3 View of PG484 Pin Distribution

Figure 3-16 View of GW2A-55 PG484 Pin Distribution

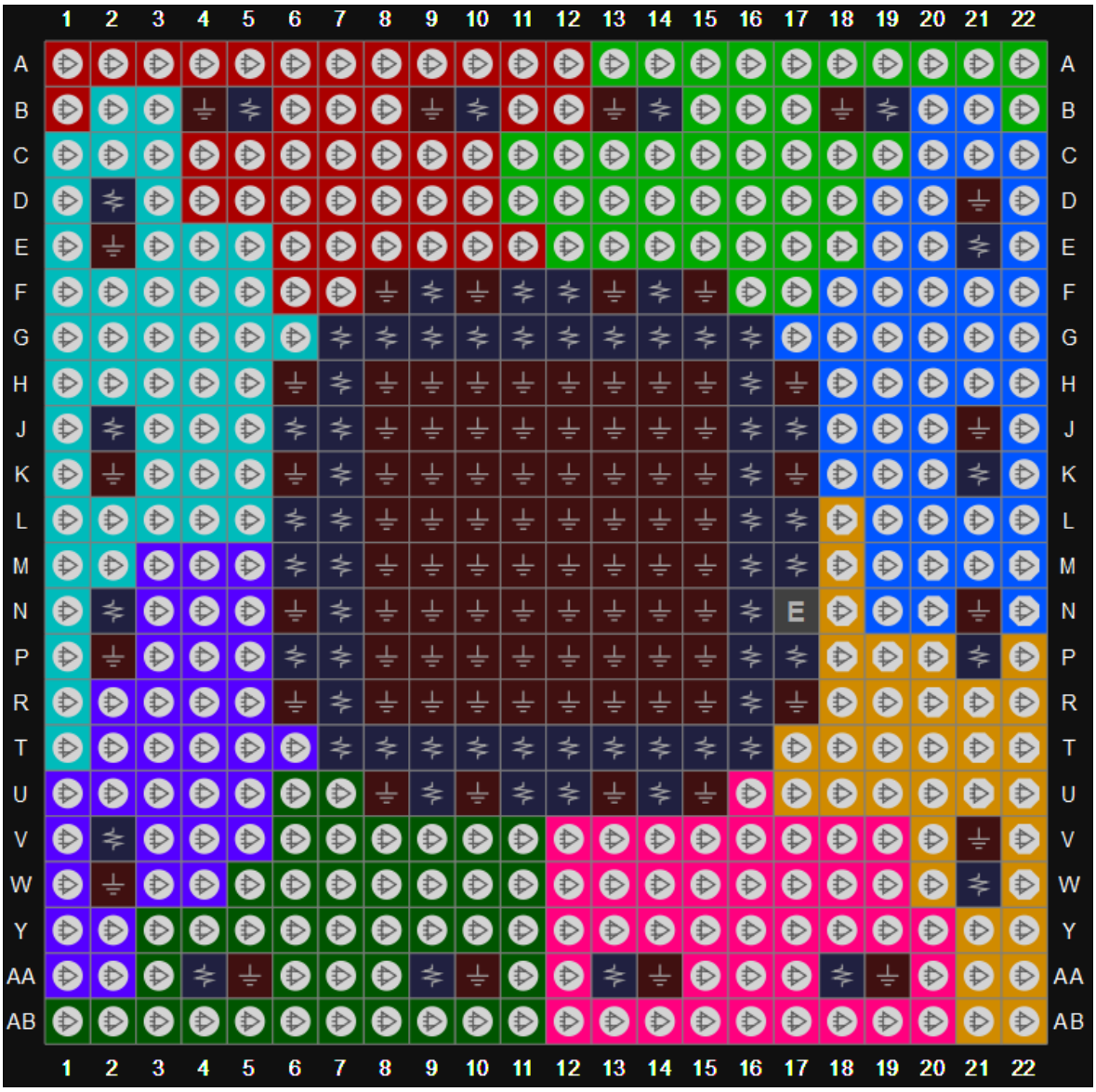


Table 3-16 Other Pins of GW2A-55 PG484

VCC	J7, M16, T7, L7, L16, H7, G9, T13, T14, G10, M7, G11, G12, G14, G13, G15 P16, P7, H16, G7, G16, G8, R16, J16, T12, T11, R7, T15, T9, T8, T10, T16
VCCO0	B5, B10, F11
VCCO1	B14, B19, F12
VCCO2	E21, K21, L17
VCCO3	M17, P21, W21
VCCO4	AA13, AA18, U12
VCCO5	U11, AA4, AA9
VCCO6	M6, N2, V2
VCCO7	D2, J2, L6
VCCX	F14, F9, J6, J17, P6, P17, U9, U14
VCCPLLL	N7, K7
VCCPLLR	N16, K16
VSS	AA10, AA14, AA19, AA5, B13, B18, B4, B9, D21, E2, F10, F13, F15, F8, H10 H11, H12, H13, H14, H15, H17, H6, H8, H9, J10, J11, J12, J13, J14, J15, J21 J8, J9, K10, K11, K12, K13, K14, K15, K17, K2, K6, K8, K9, L10, L11, L12, L13 L14, L15, L8, L9, M10, M11, M12, M13, M14, M15, M8, M9, N10, N11, N12 N13, N14, N15, N21, N6, N8, N9, P10, P11, P12, P13, P14, P15, P2, P8, P9 R10, R11, R12, R13, R14, R15, R17, R6, R8, R9, U10, U13, U15, U8, V21, W2
EXTR	N17
MODE	U22,U21,T22
JTAGSEL_N	E18

3.2.4 View of PG1156 Pin Distribution

Figure 3-17 View of GW2A-55 PG1156 Pin Distribution (Top View)

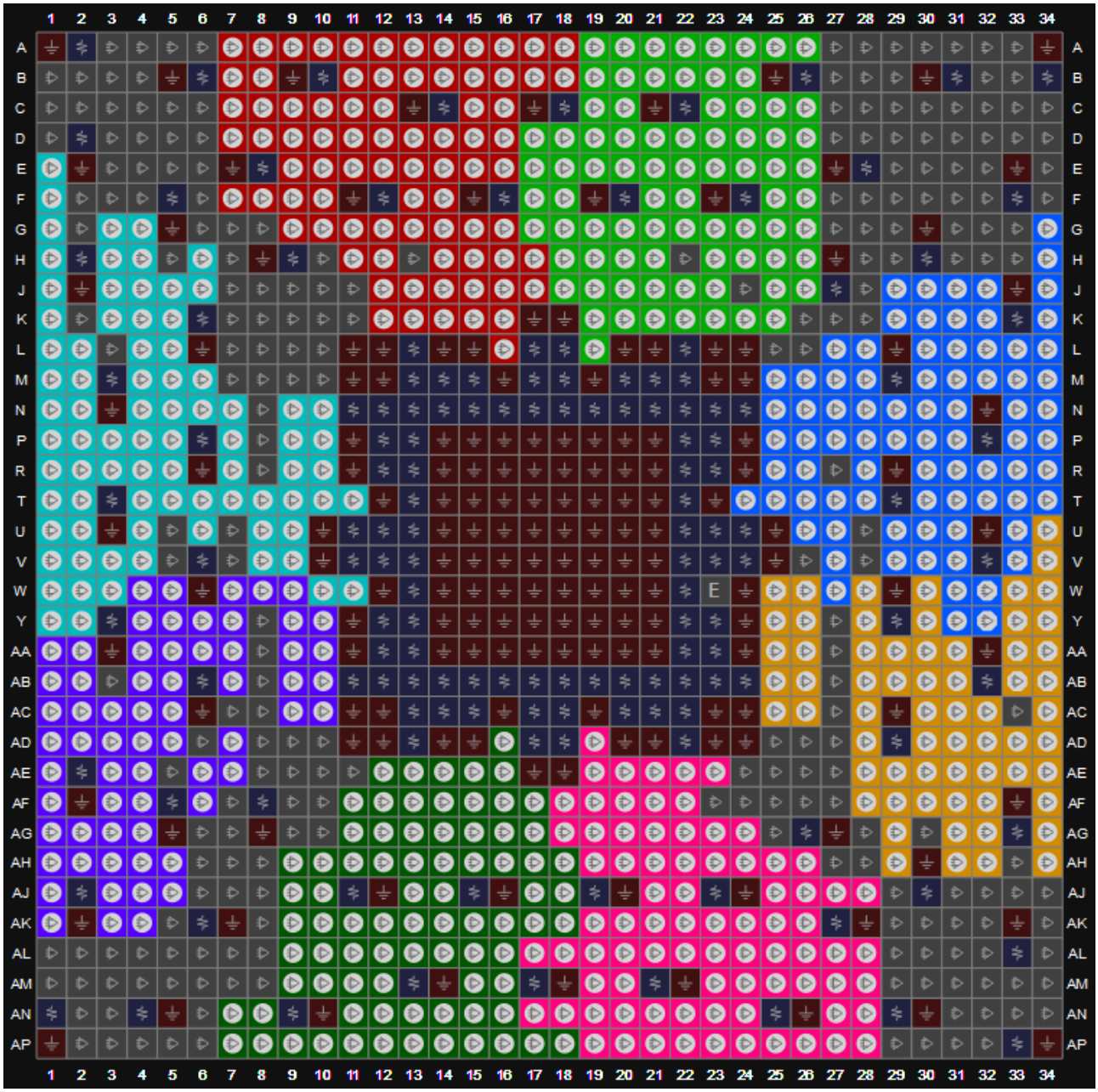


Table 3-17 Other Pins in GW2A-55 PG1156

VCC	AA13, AA22, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21 AB22, N13, N14, N15, N16, N17, N18, N19, N20, N21, N22, P13, P22, R13 R22, U13, U22, V13, V22, Y13, Y22
VCCO0	A2, B10, B6, C14, E8, F12, F16, H9, L13, L17, M13, M17
VCCO1	B26, B31, C18, C22, E28, F20, F24, L18, L22, M18, M22
VCCO2	B34, F33, H30, J27, K33, M29, N23, N24, P32, T29, U23, U24
VCCO3	AB23, AB24, AB32, AD29, AG33, AJ30, AL33, V23, V24, V32, Y29
VCCO4	AC18, AC22, AD18, AD22, AG26, AJ19, AJ23, AK27, AM21, AN25, AN29 AP33
VCCO5	AC13, AC17, AD13, AD17, AJ11, AJ15, AK6, AM13, AM17, AN4, AN9
VCCO6	AB11, AB12, AB6, AE2, AF5, AF8, AJ2, AN1, V11, V12, V6, Y3
VCCO7	D2, F5, H2, K6, M3, N11, N12, P6, T3, U11, U12
VCCX	AA12, AA23, AC14, AC15, AC20, AC21, M14, M15, M20, M21, P12, P23, R12 R23, Y12, Y23
VCCPLLL	T13,W13
VCCPLLR	T22,W22
VSS	A1, A34, AA11, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA24 AA3, AA32, AC11, AC12, AC16, AC19, AC23, AC24, AC29, AC6, AD11, AD12 AD14, AD15, AD20, AD21, AD23, AD24, AE17, AE18, AF2, AF33, AG27, AG5 AG8, AH30, AJ12, AJ16, AJ20, AJ24, AK2, AK28, AK33, AK7, AM14, AM18 AM22, AN10, AN26, AN30, AN5, AP1, AP34, B25, B30, B5, B9, C13, C17, C21 E2, E27, E33, E7, F11, F15, F19, F23, G30, G5, H27, H8, J2, J33, K17, K18 L11, L12, L14, L15, L20, L21, L23, L24, L29, L6, M11, M12, M16, M19, M23 M24, N3, N32, P11, P14, P15, P16, P17, P18, P19, P20, P21, P24, R11, R14 R15, R16, R17, R18, R19, R20, R21, R24, R29, R6, T12, T14, T15, T16, T17 T18, T19, T20, T21, T23, U10, U14, U15, U16, U17, U18, U19, U20, U21, U25 U3, U32, V10, V14, V15, V16, V17, V18, V19, V20, V21, V25, W12, W14, W15 W16, W17, W18, W19, W20, W21, W24, W29, W6, Y11, Y14, Y15, Y16, Y17 Y18, Y19, Y20, Y21, Y24
EXTR	W23
MODE	W28,V34,U34
JTAGSEL_N	G26
NC	A27, A28, A29, A3, A30, A31, A32, A33, A4, A5, A6, AA27, AA8, AB27, AB3 AB8, AC27, AC33, AC7, AC8, AD10, AD25, AD26, AD27, AD6, AD8, AD9 AE10, AE11, AE24, AE25, AE26, AE27, AE5, AE8, AE9, AF10, AF23, AF24 AF25, AF26, AF27, AF7, AF9, AG10, AG25, AG28, AG30, AG6, AG7, AG9 AH27, AH28, AH33, AH6, AH7, AH8, AJ29, AJ31, AJ32, AJ33, AJ34, AJ6, AJ7 AJ8, AK29, AK30, AK31, AK32, AK34, AK5, AK8, AL1, AL2, AL29, AL3, AL30 AL31, AL32, AL34, AL4, AL5, AL6, AL7, AL8, AM1, AM2, AM29, AM3, AM30 AM31, AM32, AM33, AM34, AM4, AM5, AM6, AM7, AM8, AN2, AN3, AN31 AN32, AN33, AN34, AN6, AP2, AP29, AP3, AP30, AP31, AP32, AP4, AP5 AP6, B1, B2, B27, B28, B29, B3, B32, B33, B4, C1, C2, C27, C28, C29, C3 C30, C31, C32, C33, C34, C4, C5, C6, D1, D27, D28, D29, D3, D30, D31, D32 D33, D34, D4, D5, D6, E29, E3, E30, E31, E32, E34, E4, E5, E6, F2, F27, F28 F29, F3, F30, F31, F32, F34, F4, F6, G2, G27, G28, G29, G31, G32, G33, G6 G7, G8, H10, H13, H22, H28, H29, H31, H32, H33, H5, H7, J10, J11, J24, J28 J7, J8, J9, K10, K11, K2, K26, K27, K28, K7, K8, K9, L10, L25, L26, L3, L7, L8 L9, M10, M7, M8, M9, N8, P8, R27, R8, U28, U5, U7, V26, V28, V5, V7, Y27 Y8

3.2.5 View of UG676 Pin Distribution

Figure 3-18 View of GW2A-55 UG676 Pin Distribution (Top View)

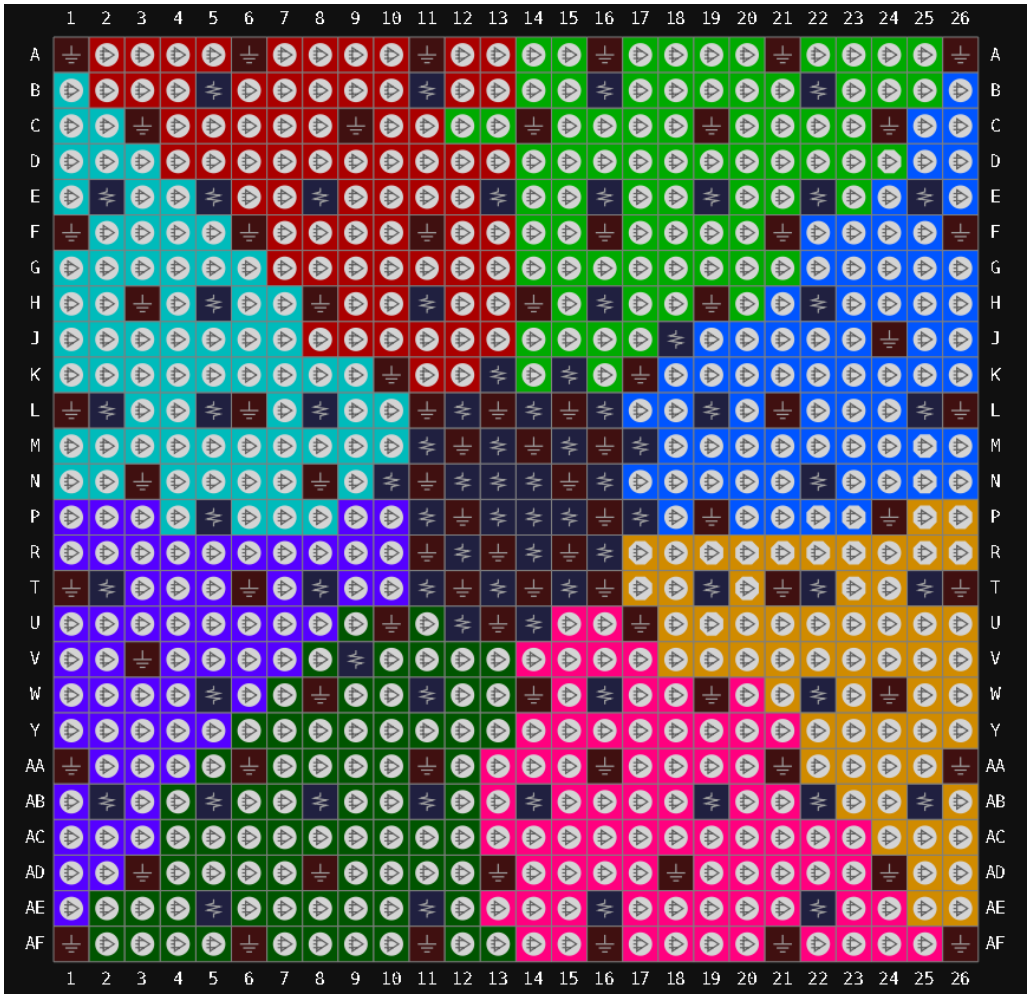


Table 3-18 Other Pins in GW2A-55 UG676

VCC	K15,L12,L14,L16,M13,M17,N12,N13,N14,N16,P11,P13,P14,P15,R12,R14,R1 ,T13,U12
VCCO0	B11,B5,E13,E8,H11
VCCO1	B16,B22,E19,H16
VCCO2	E25,H22,L19,L25,N22
VCCO3	AB25,T19,T25,W22
VCCO4	AB14,AB19,AE16,AE22,W16
VCCO5	AB8,AE11,AE5,W11
VCCO6	AB2,P5,T2,T8,W5
VCCO7	E2,H5,L2,L8
VCCX	AB11,AB22,AB5,E16,E22,E5,J18,K13,L5,N10,P17,T22,U14,V9
VCCPLLL	M11,M15
VCCPLLR	T11,T15
VSS	A1,A11,,A16,A21,A26,A6,AA1,AA11,AA16,,AA21,AA26,AA6,AD13,AD18,AD2 ,AD3,AD8,AF1,AF11,AF16,AF21,AF26,AF6,C14,C19,C24,C3,C9,F1,F11,F16, 21,F26,F6,H14,H19,H3,H8,J24,K10,K17,L1,L11,L13,L15,L21,L26,L6,M12,M1 M16,N11,N15,N3,N8,P12,P16,P19,P24,R11,R13,R15,T1,T12,T14,T16,T21,T2 6,T6,U10,U13,U17,V3,W14,W19,W24,W8
MODE	P26,R26,R23
JTAGSEL_N	D24

3.2.6 View of UG324F Pin Distribution

Figure 3-19 View of GW2A-55 UG324F Pin Distribution (Top View)

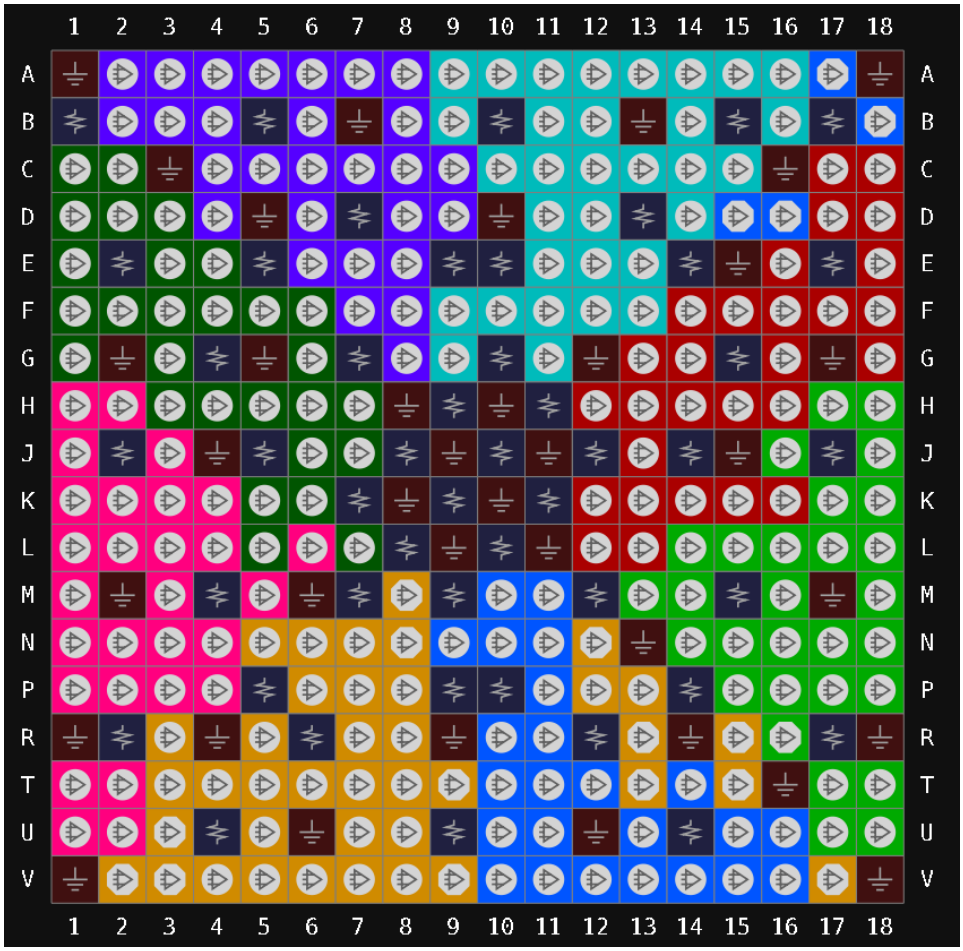


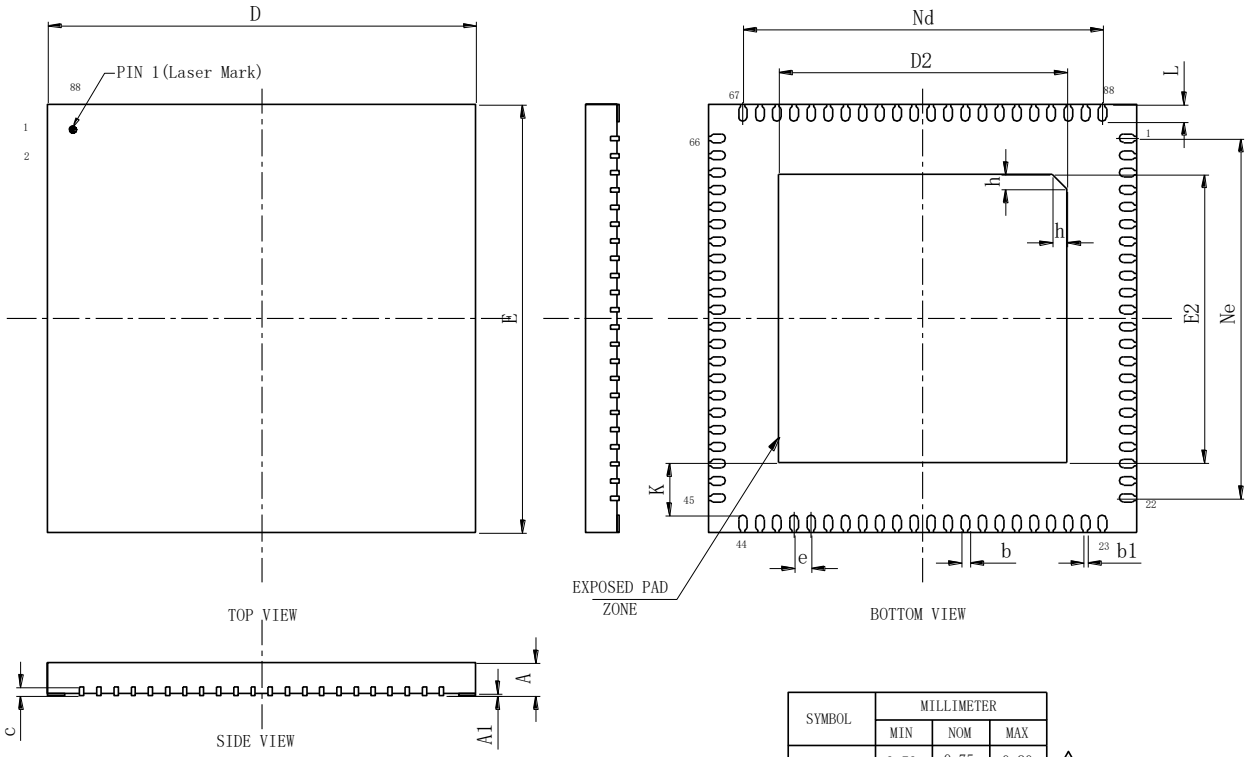
Table 3-19 Other Pins in GW2A-55 UG324F

VCC/VCCPLLL/ VCCPLLR	G7,H11,H9,J10,J8,K11,K9,L10,L8,M12,M7
VCCO0	E17,J14,G15
VCCO1	J17,M15,R17
VCCO2	P9,R12,U14
VCCO3	R6,U4,U9
VCCO4	J5,M4,R2
VCCO5	E2,G4,J2
VCCO6	B10,B5,D7
VCCO7	B15,D13,E10
VCCX	B1,B17,E14,E5,E9,G10,J12,K7,M9,P10,P14,P5
VSS	A1,A18,B13,B7,C16,C3,D10,D5,E15,G12,G17,G2,G5,H10,H8,J11,J 15,J4,J9,K10,K8,L11,L9,M17,M2,M6,N13,R1,R14,R18,R4,R9,T16, U12,U6,V1,V18
MODE	T15,N12

4 Package Diagrams

4.1 QN88 Package Outline (10mm x 10mm)

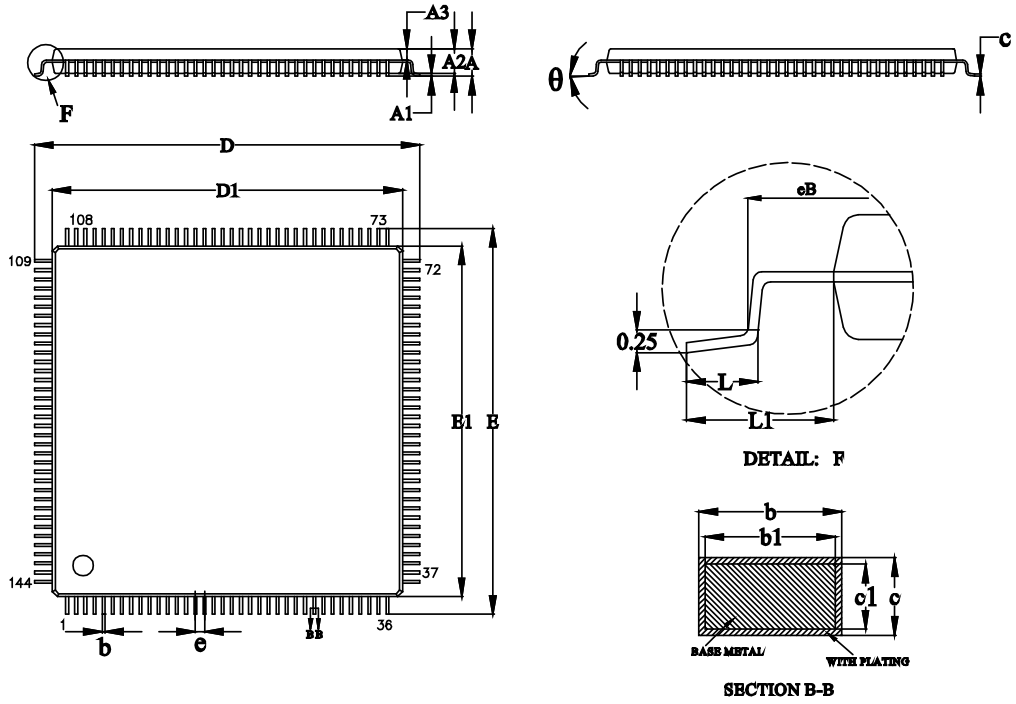
Figure 4-1 Package Outline QN88



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	⚠1
	0.80	0.85	0.90	
	0.85	0.90	0.95	⚠2
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
b1	0.10REF			⚠3
c	0.18	0.20	0.25	
D	9.90	10.00	10.10	
D2	6.64	6.74	6.84	
e	0.40BSC			
Nd	8.40REF			
E	9.90	10.00	10.10	
E2	6.64	6.74	6.84	
Ne	8.40REF			
L	0.30	0.40	0.50	
K	0.20	–	–	
h	0.30	0.35	0.40	
L/F载体尺寸 (mil)	300x300			

4.2 LQ144 Package Outline (20mm x 20mm)

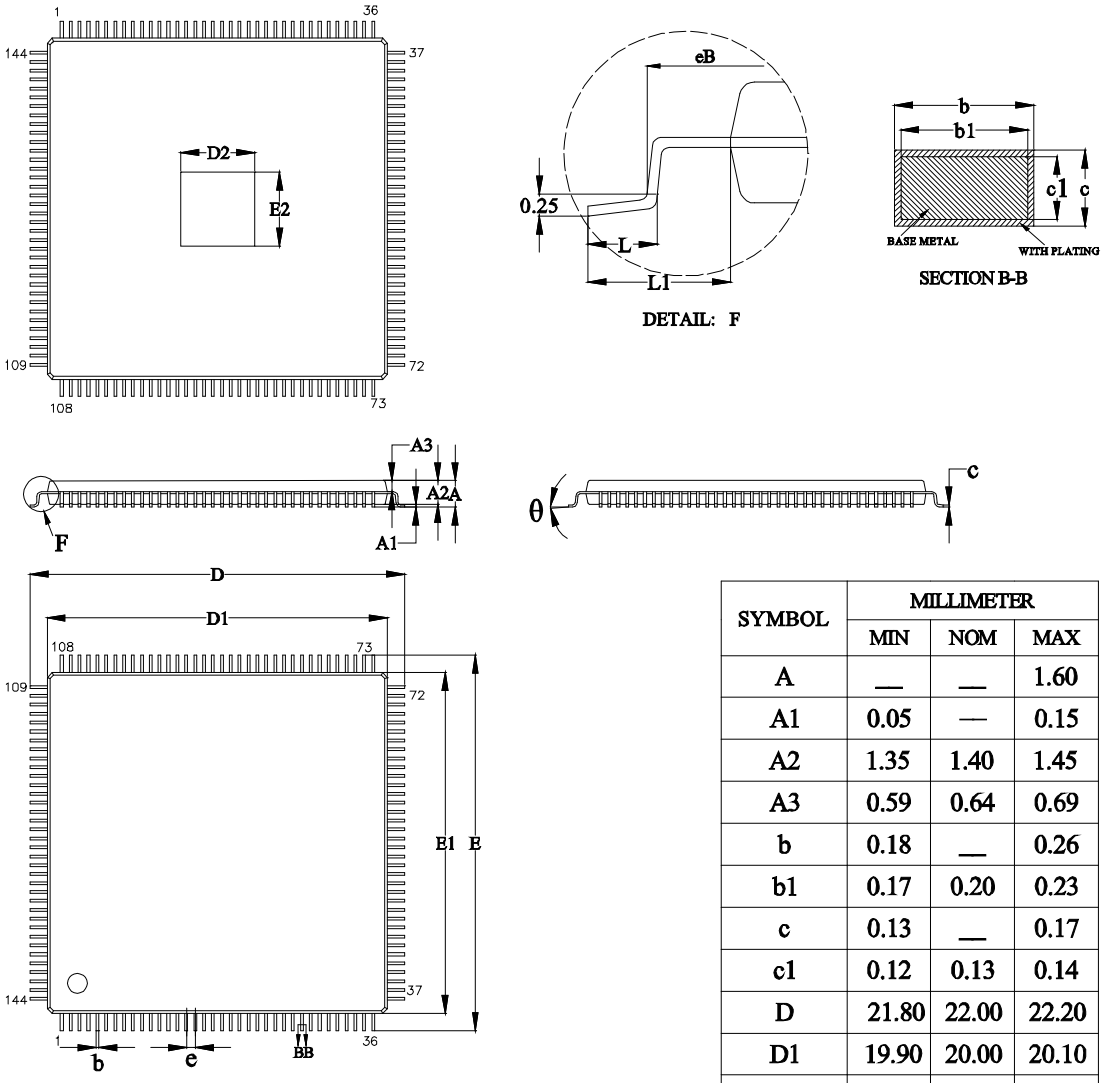
Figure 4-2 Package Outline LQ144



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

4.3 EQ144 Package Outline (20mm x 20mm)

Figure 4-3 Package Outline EQ144

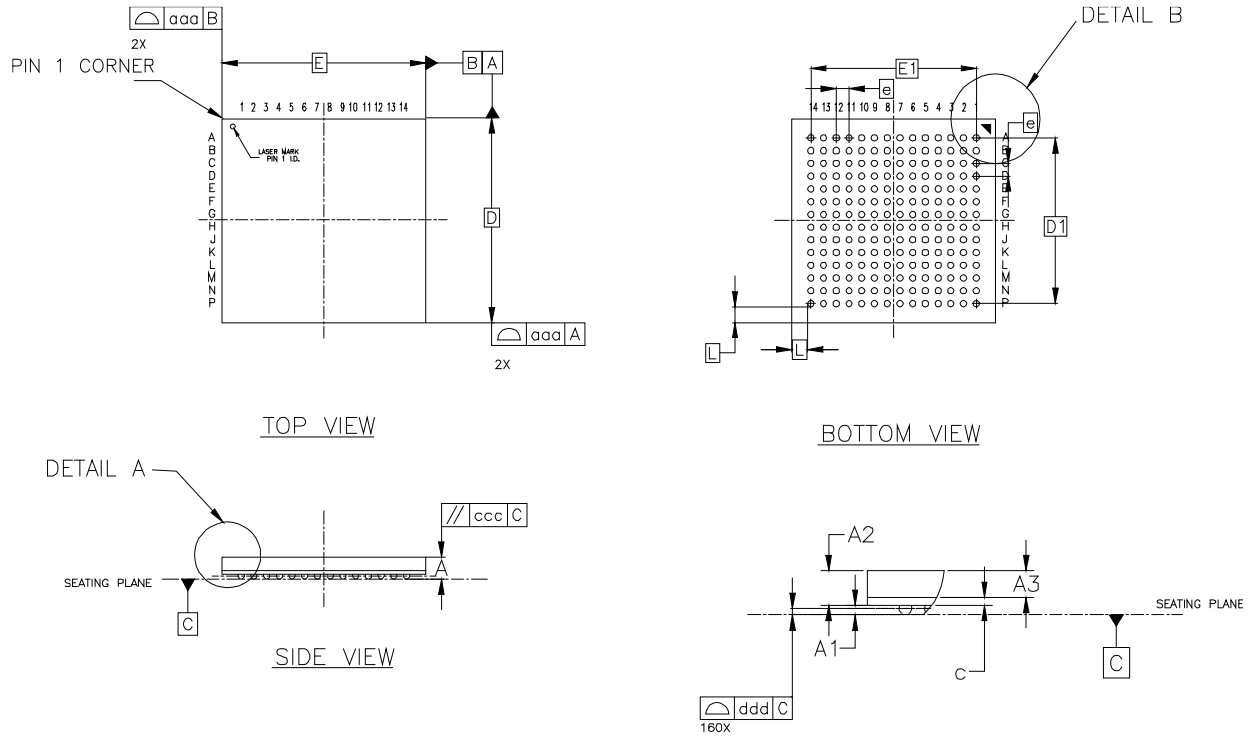


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
eB	21.15		21.40
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

L/F Size (mil) \ Size (mm)	D2	E2
383*383	9.74REF	9.74REF

4.4 MG196 Package Outline (8mm x 8mm)

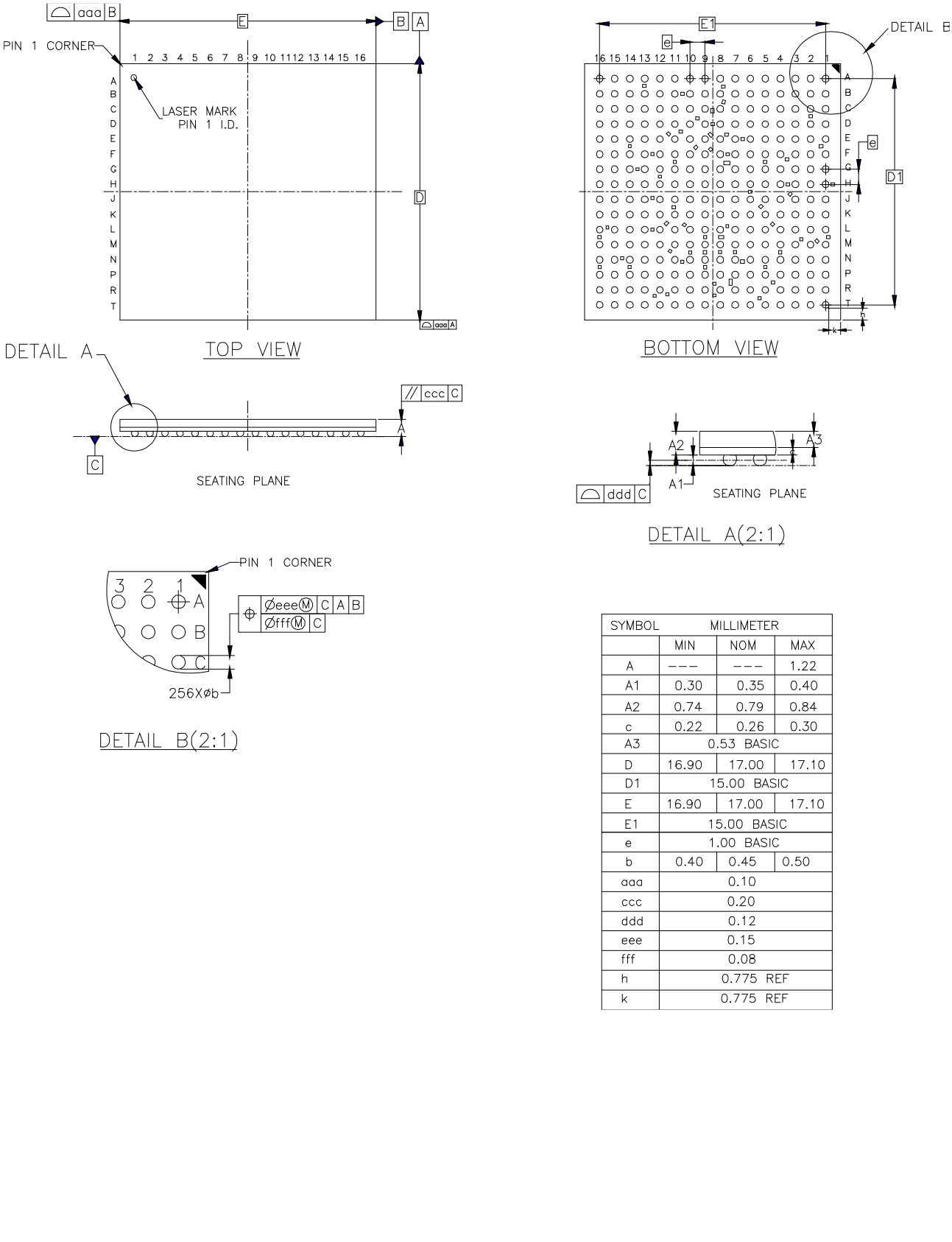
Figure 4-4 Package OutlineMG196



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	0.97
A1	0.13	0.18	0.23
A2	0.64	0.69	0.74
A3	0.53 BASIC		
c	0.13	0.16	0.19
D	7.90	8.00	8.10
D1	6.50 BASIC		
E	7.90	8.00	8.10
E1	6.50 BASIC		
L	0.625 BASIC		
e	0.50 BASIC		
b	0.20	0.25	0.30
aaa	0.15		
ccc	0.15		
ddd	0.08		
eee	0.15		
fff	0.05		

4.5 PG256 Package Outline (17mm x 17mm)

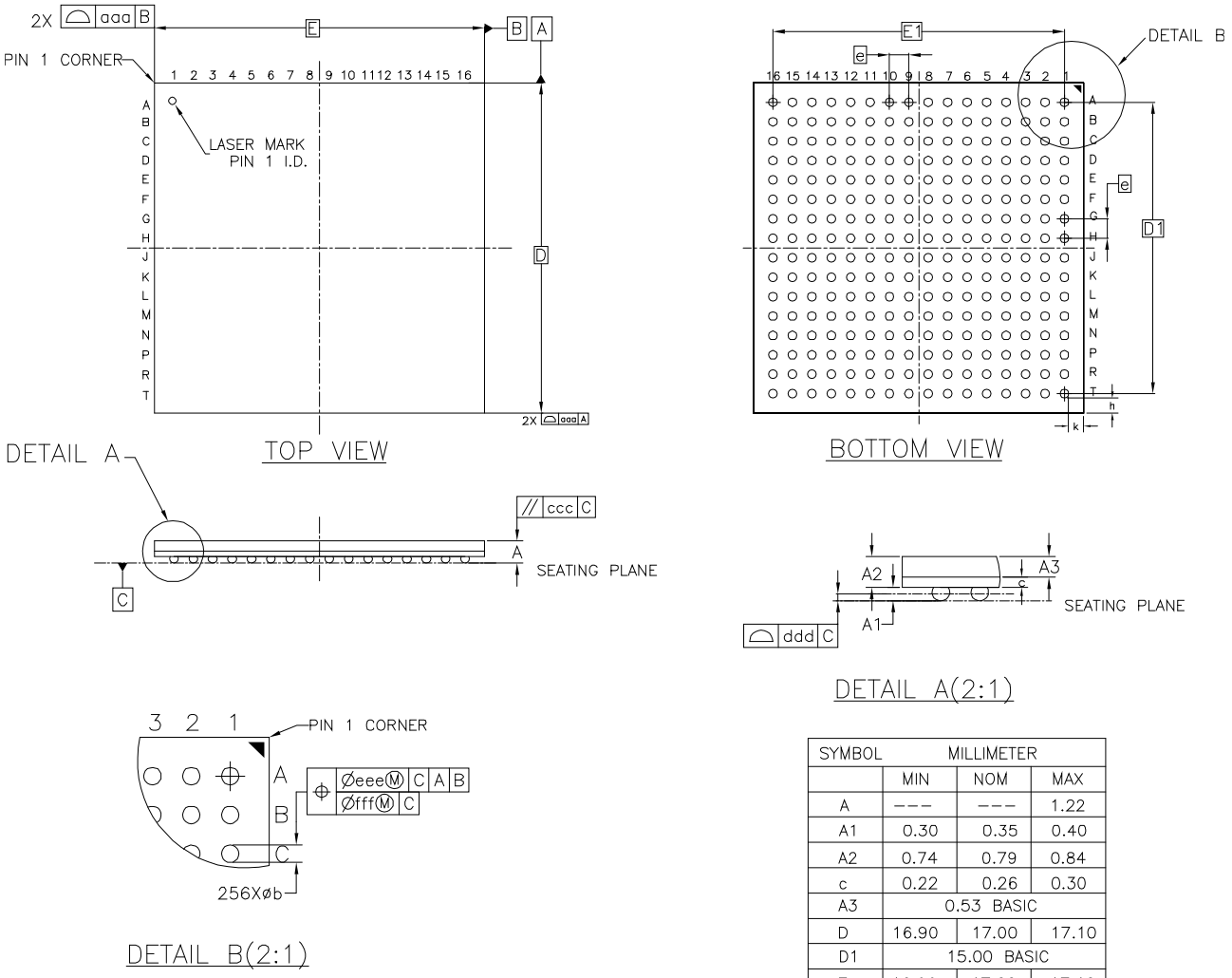
Figure 4-5 Package Outline PG256



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.22
A1	0.30	0.35	0.40
A2	0.74	0.79	0.84
c	0.22	0.26	0.30
A3	0.53 BASIC		
D	16.90	17.00	17.10
D1	15.00 BASIC		
E	16.90	17.00	17.10
E1	15.00 BASIC		
e	1.00 BASIC		
b	0.40	0.45	0.50
aaa	0.10		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		
h	0.775 REF		
k	0.775 REF		

4.6 PG256C/ PG256CF Package Outline (17mm x 17mm)

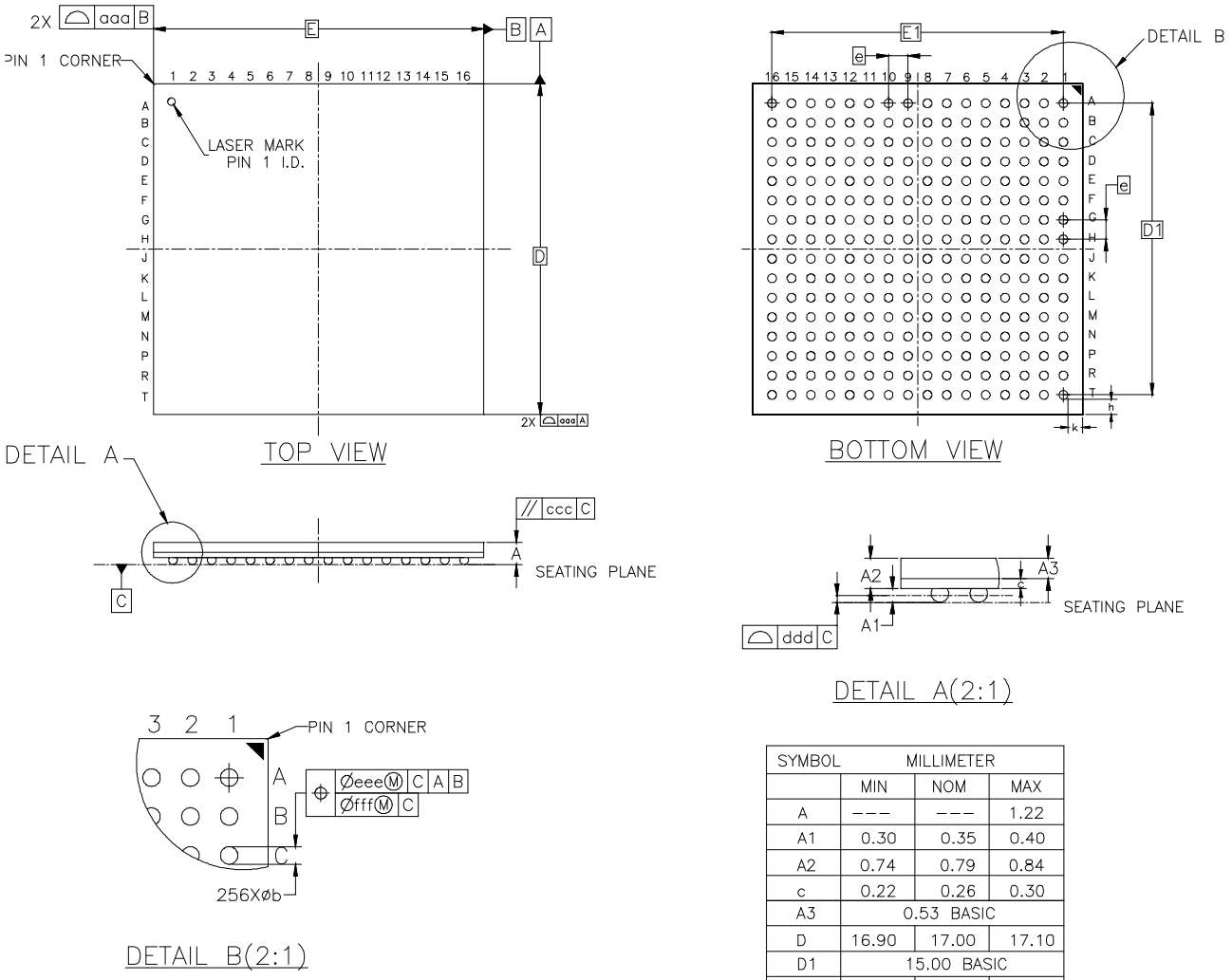
Figure 4-6 Package Outline PG256C



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.22
A1	0.30	0.35	0.40
A2	0.74	0.79	0.84
c	0.22	0.26	0.30
A3	0.53 BASIC		
D	16.90	17.00	17.10
D1	15.00 BASIC		
E	16.90	17.00	17.10
E1	15.00 BASIC		
e	1.00 BASIC		
b	0.40	0.45	0.50
aaa	0.10		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		
h	0.775 REF		
k	0.775 REF		

4.7 PG256S / PG256SF Package Outline (17mm x 17mm)

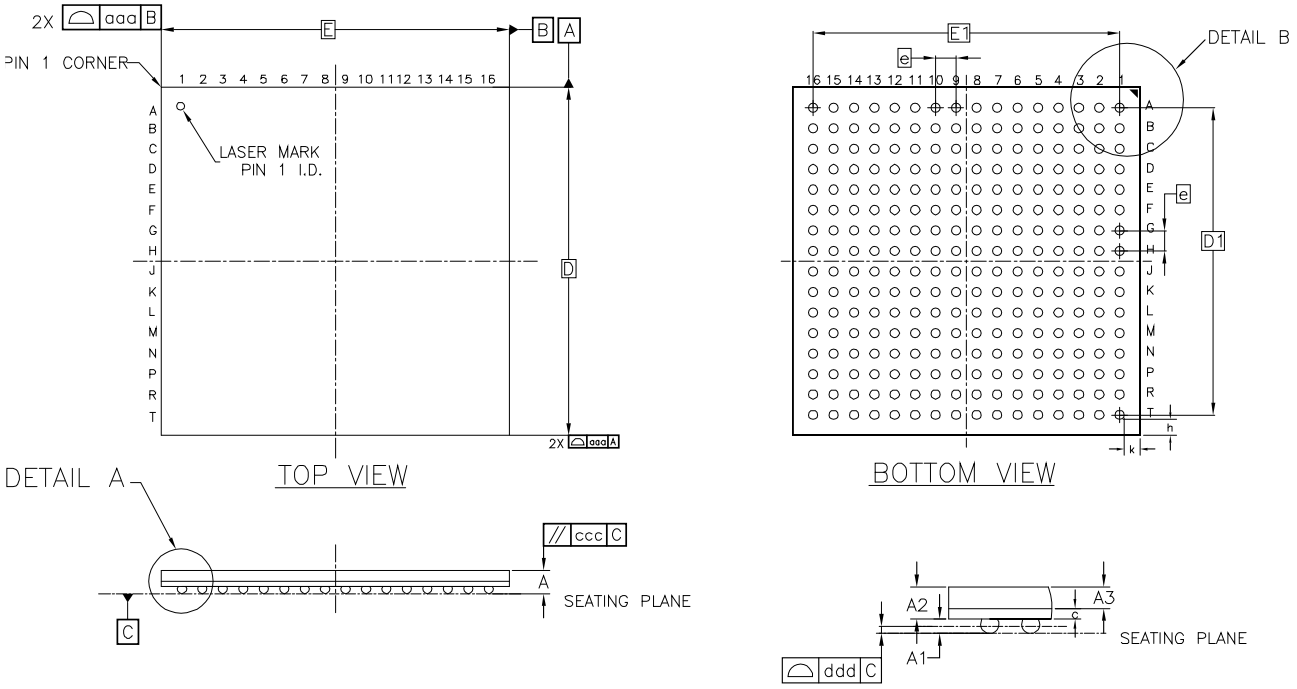
Figure 4-7 Package Outline PG256S / PG256SF



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.22
A1	0.30	0.35	0.40
A2	0.74	0.79	0.84
c	0.22	0.26	0.30
A3	0.53 BASIC		
D	16.90	17.00	17.10
D1	15.00 BASIC		
E	16.90	17.00	17.10
E1	15.00 BASIC		
e	1.00 BASIC		
b	0.40	0.45	0.50
aaa	0.10		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		
h	0.775 REF		
k	0.775 REF		

4.8 PG256E Package Outline (17mm x 17mm)

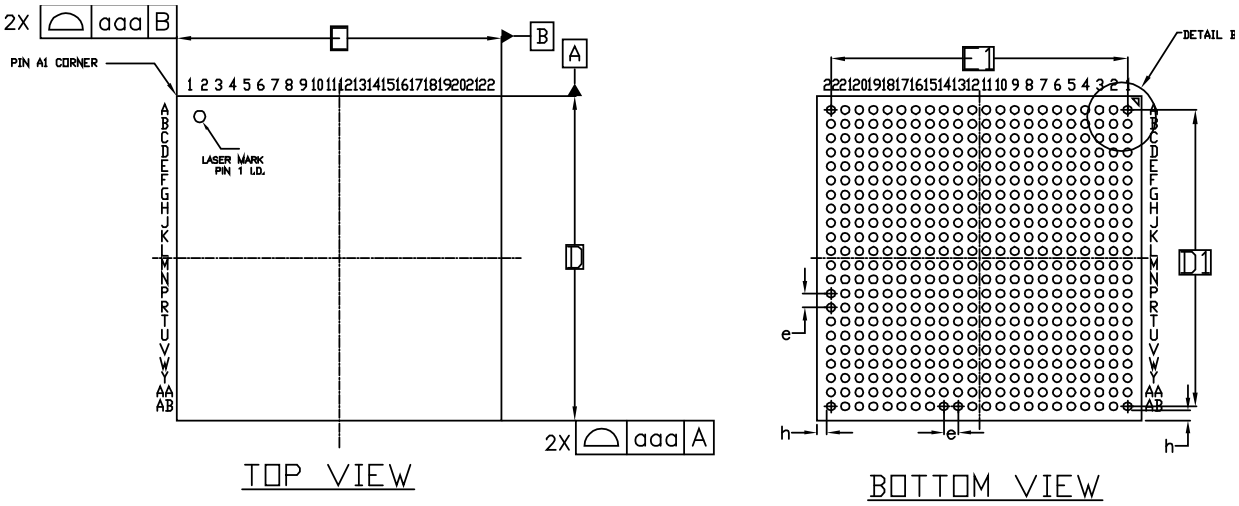
Figure 4-8 Package Outline PG256E



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.14	1.22
A1	0.30	0.35	0.40
A2	0.74	0.79	0.84
c	0.22	0.26	0.30
A3		0.53 BASIC	
D	16.90	17.00	17.10
D1		15.00 BASIC	
E	16.90	17.00	17.10
E1		15.00 BASIC	
e		1.00 BASIC	
b	0.40	0.45	0.50
aaa		0.10	
ccc		0.20	
ddd		0.12	
eee		0.15	
fff		0.08	
h		0.775 REF	
k		0.775 REF	

4.9 PG484 Package Outline (23mm x 23mm, GW2A-18)

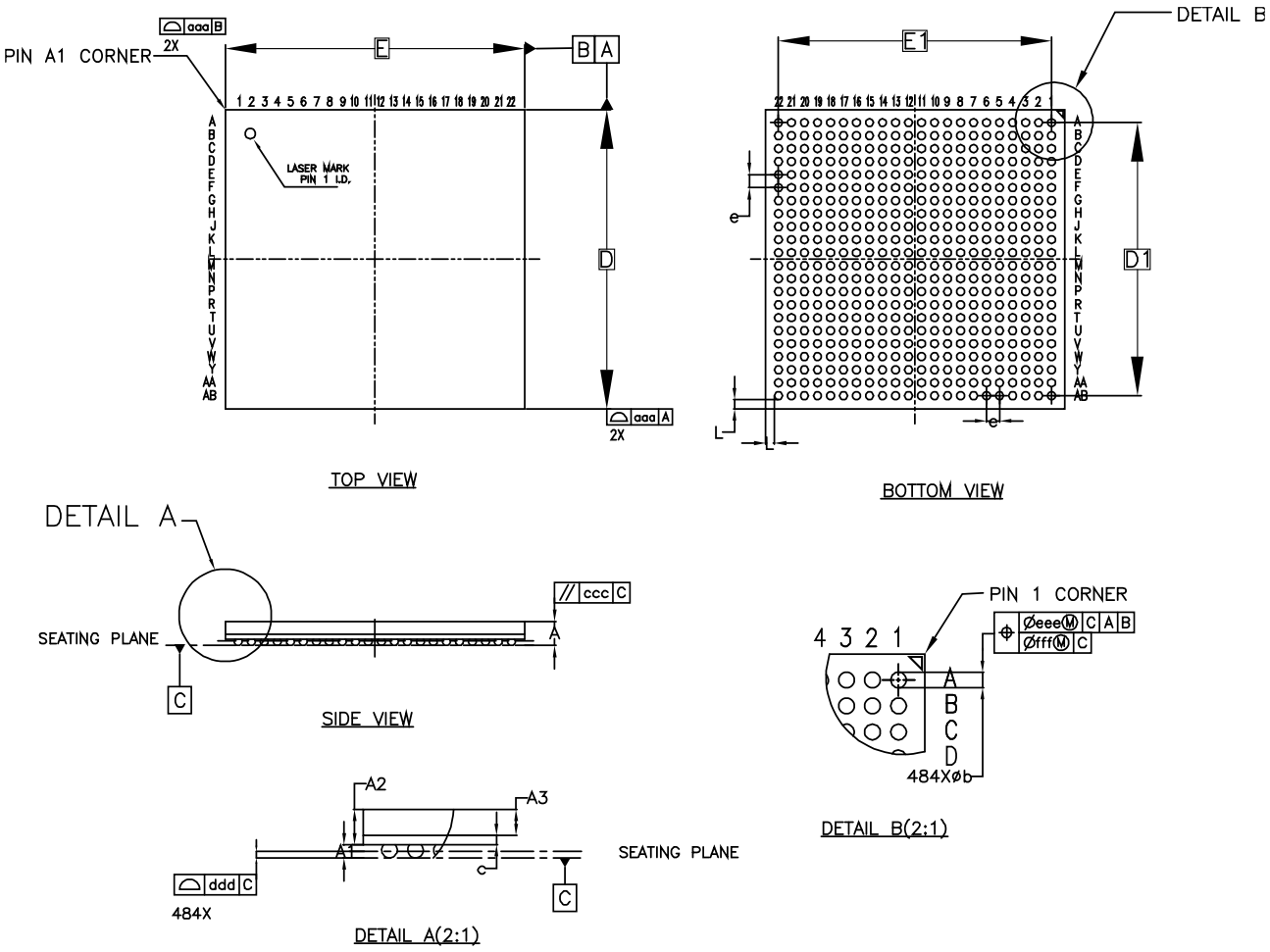
Figure 4-9 Package Outline PG484



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	2.06	2.15
A1	0.45	0.50	0.55
A2	1.51	1.56	1.61
A3	1.00 BASIC		
c	0.52	0.56	0.60
D	22.90	23.00	23.10
D1	21.00 BASIC		
E	22.90	23.00	23.10
E1	21.00 BASIC		
e	1.00 BASIC		
b	0.55	0.60	0.65
h	0.70 REF		
aaa	0.20		
ccc	0.35		
ddd	0.15		
eee	0.25		
fff	0.10		

4.10 PG484 Package Outline (23mm x 23mm, GW2A-55)

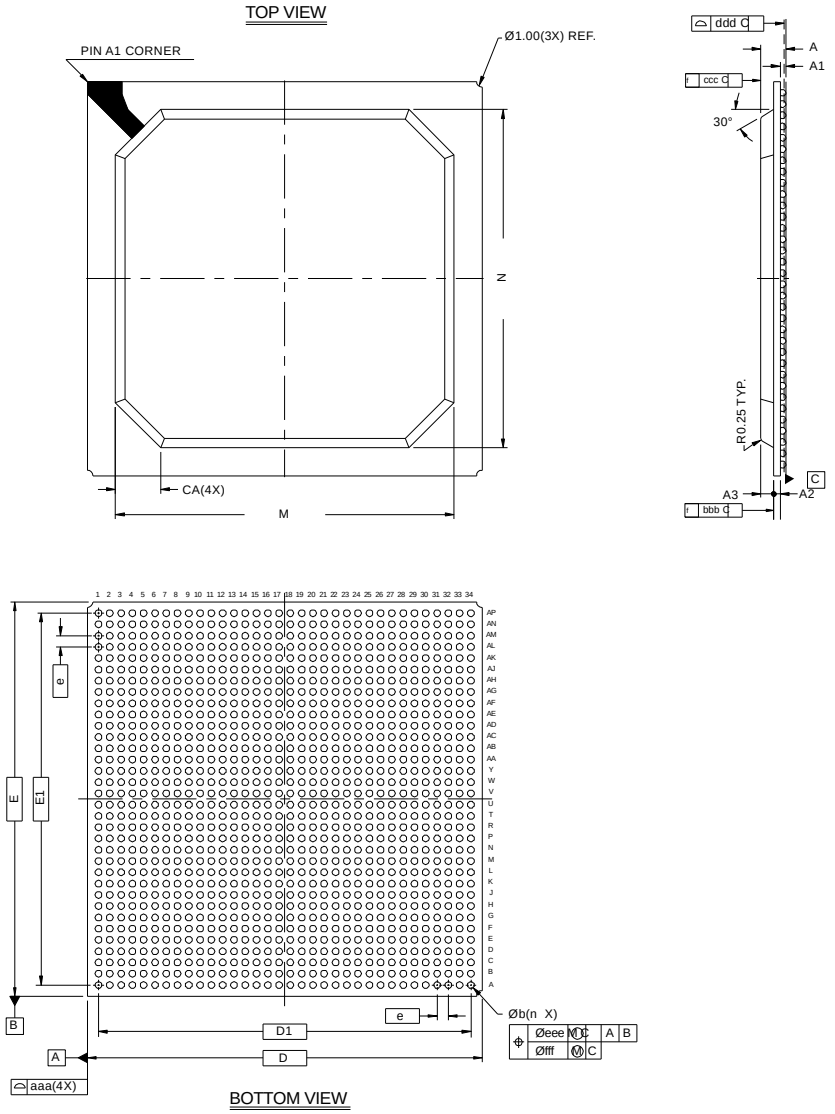
Figure 4-10 Package Outline PG484



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.76	1.86	1.96
A1	0.46	0.50	0.54
A2	1.28	1.36	1.44
A3		1.00 BASIC	
c	0.32	0.36	0.40
D	22.90	23.00	23.10
D1		21.00 BASIC	
E	22.90	23.00	23.10
E1		21.00 BASIC	
e		1.00 BASIC	
L		0.70 BASIC	
b	0.55	0.60	0.65
aaa		0.20	
ccc		0.25	
ddd		0.25	
eee		0.18	
fff		0.10	

4.11 PG1156 Package Outline (35mm x 35mm)

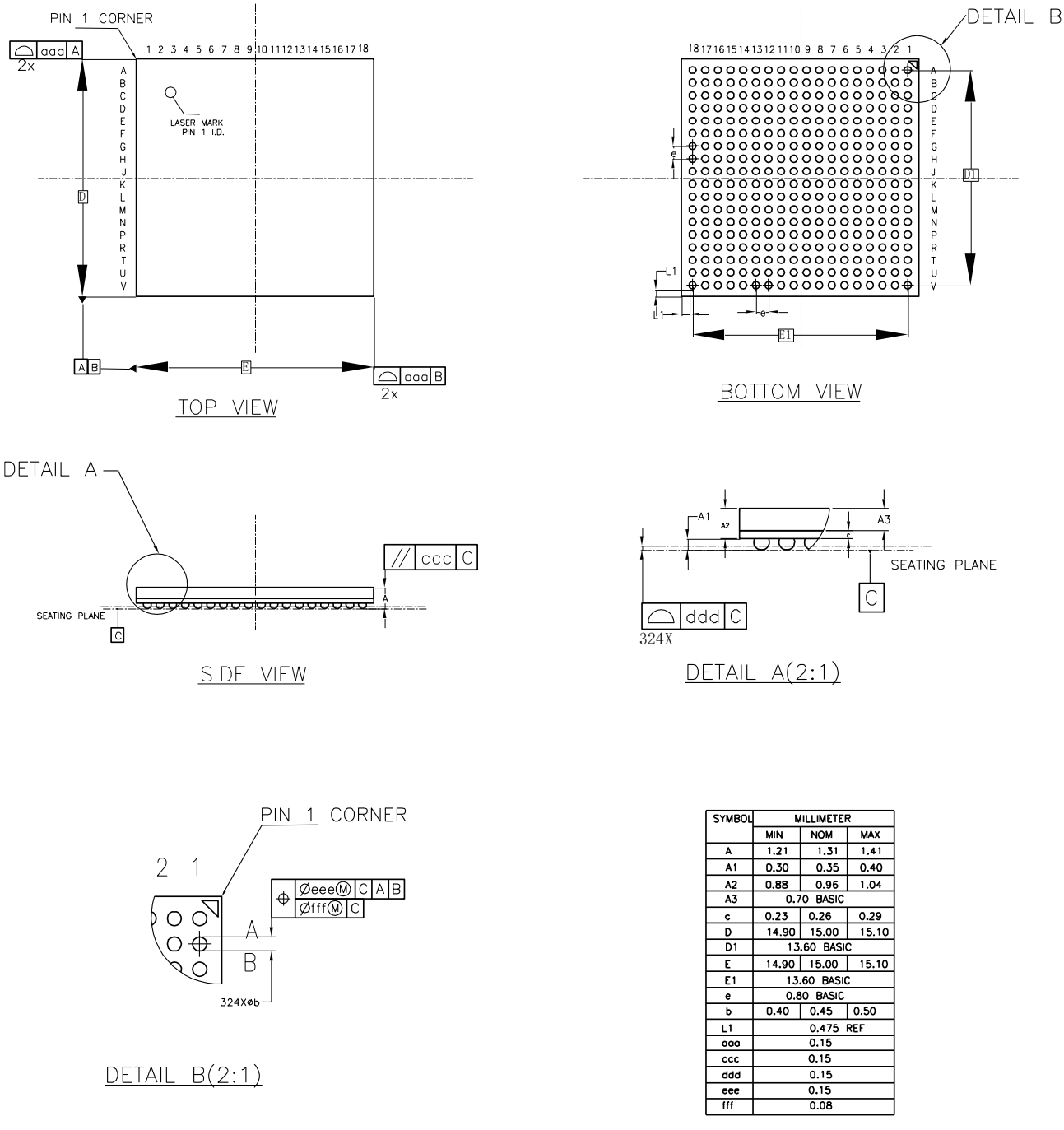
Figure 4-11 Package Outline PG1156



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :				PBGA	
Body Size:	X	D		35.000	
	Y	E		35.000	
Ball Pitch :		e		1.000	
Total Thickness :		A	2.108	2.230	2.352
Mold Thickness :		A3		1.170 Ref.	
Substrate Thickness :		A2		0.560 Ref.	
Ball Diameter :				0.600	
Stand Off :		A1	0.400	-	0.600
Ball Width :		b	0.500	-	0.700
Mold Area :	X	M		30.000	
	Y	N		30.000	
Chamfer		CA		4.000 Ref.	
Package Edge Tolerance :		aaa		0.200	
Substrate Parallelism :		bbb		0.250	
Mold Parallelism :		ccc		0.350	
Coplanarity:		ddd		0.150	
Ball Offset (Package) :		eee		0.250	
Ball Offset (Ball) :		fff		0.100	
Ball Count :		n		1156	
Edge Ball Center to Center :	X	D1		33.000	
	Y	E1		33.000	

4.12 UG324/UG324D/UG324F Package Outline (15mm x 15mm)

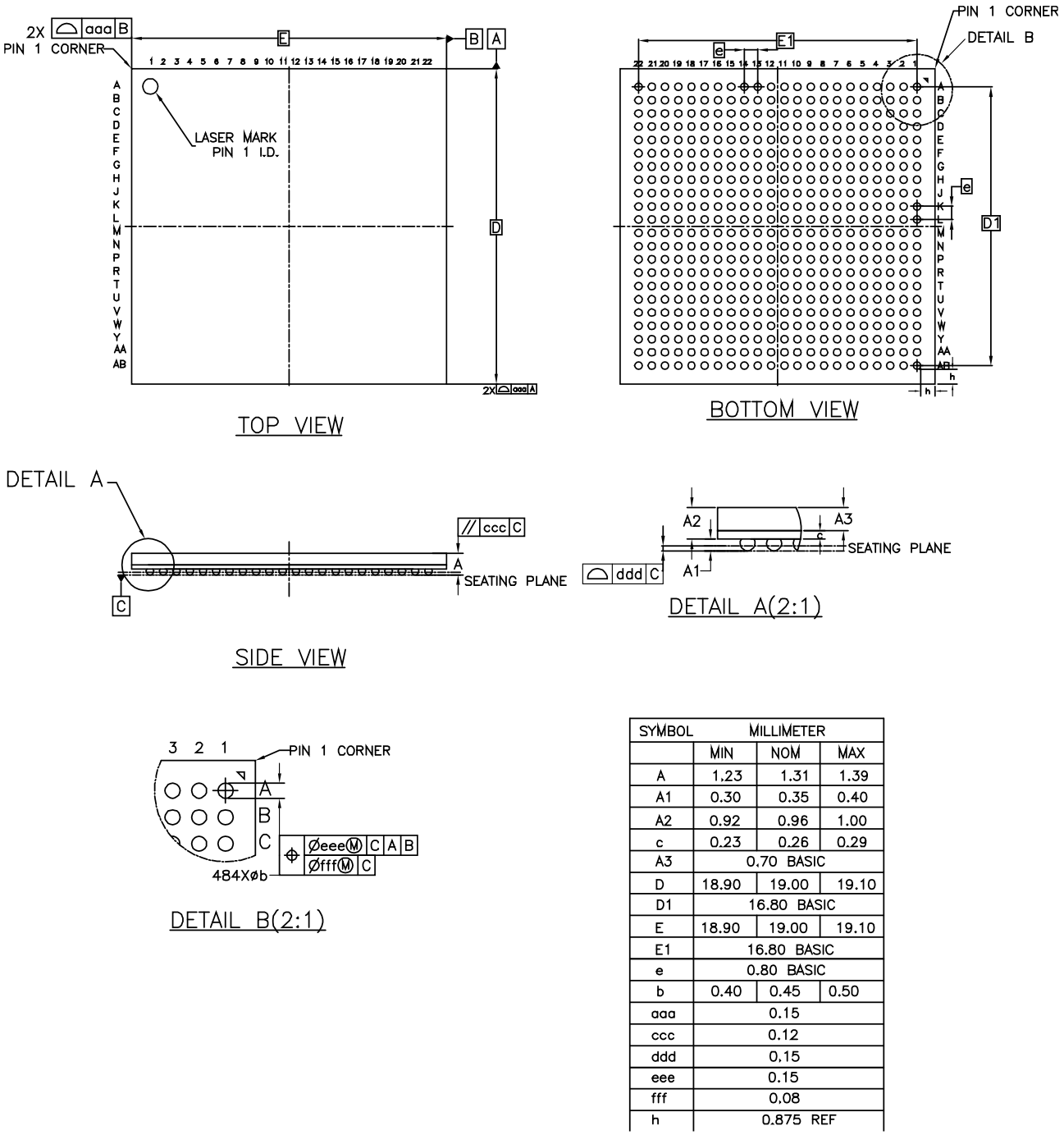
Figure 4-12 Package Outline UG324/UG324D/UG324F



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.21	1.31	1.41
A1	0.30	0.35	0.40
A2	0.88	0.96	1.04
A3		0.70 BASIC	
c	0.23	0.26	0.29
D	14.90	15.00	15.10
D1		13.60 BASIC	
E	14.90	15.00	15.10
E1		13.60 BASIC	
e		0.80 BASIC	
b	0.40	0.45	0.50
L1		0.475 REF	
aaa		0.15	
ccc		0.15	
ddd		0.15	
eee		0.15	
fff		0.08	

4.13 UG484 Package Outline (19mm x 19mm)

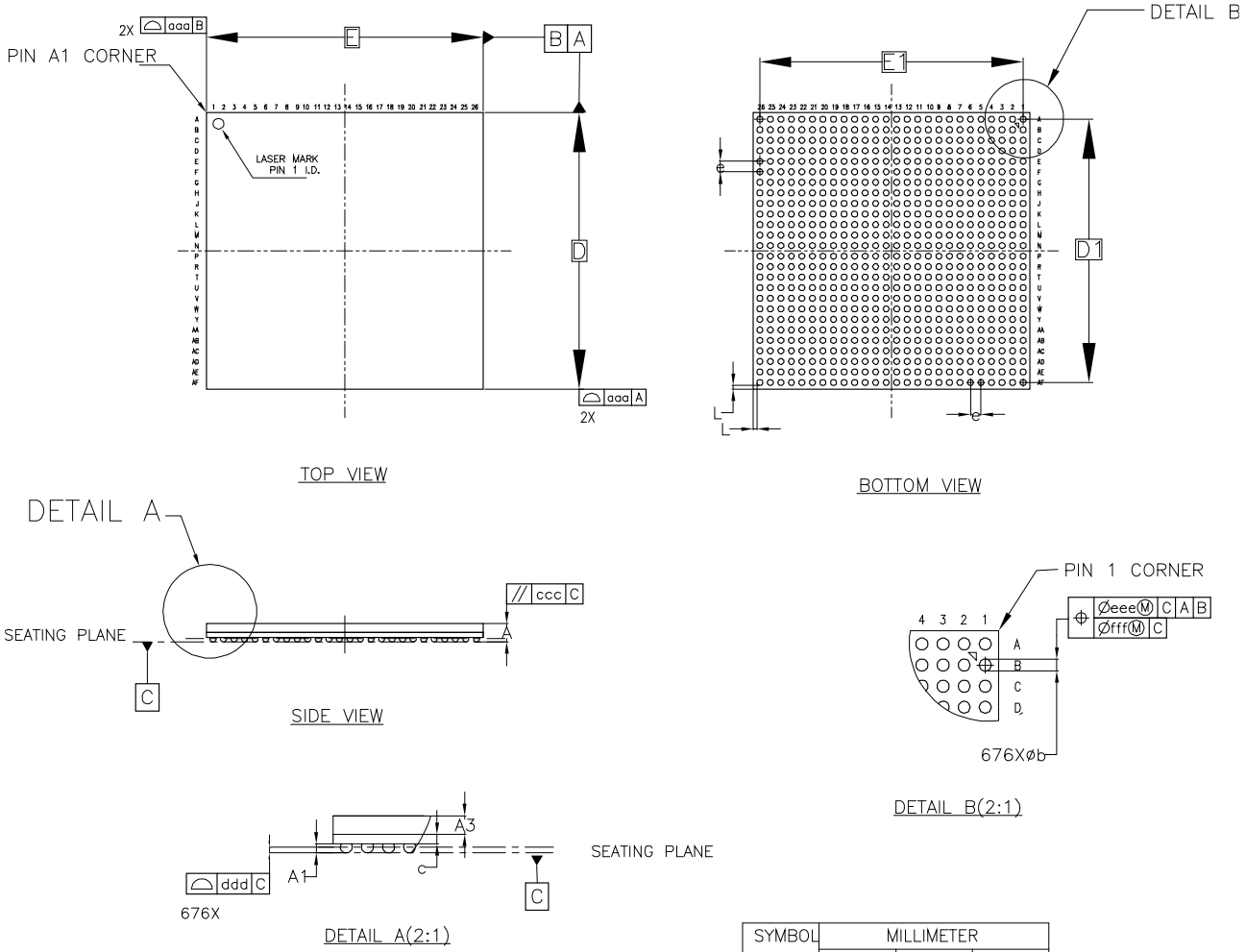
Figure 4-13 Package Outline UG484



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.23	1.31	1.39
A1	0.30	0.35	0.40
A2	0.92	0.96	1.00
c	0.23	0.26	0.29
A3	0.70 BASIC		
D	18.90	19.00	19.10
D1	16.80 BASIC		
E	18.90	19.00	19.10
E1	16.80 BASIC		
e	0.80 BASIC		
b	0.40	0.45	0.50
aaa	0.15		
ccc	0.12		
ddd	0.15		
eee	0.15		
fff	0.08		
h	0.875 REF		

4.14 UG676 Package Outline (21mm x 21mm)

Figure 4-14 Package Outline UG676



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.33	1.41	1.49
A1	0.30	0.35	0.40
A2	0.98	1.06	1.14
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	20.90	21.00	21.10
D1	20.00 BASIC		
E	20.90	21.00	21.10
E1	20.000 BASIC		
e	0.800 BASIC		
L	0.275 BASIC		
b	0.40	0.45	0.50
aaa	0.15		
ccc	0.17		
ddd	0.15		
eee	0.15		
fff	0.08		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