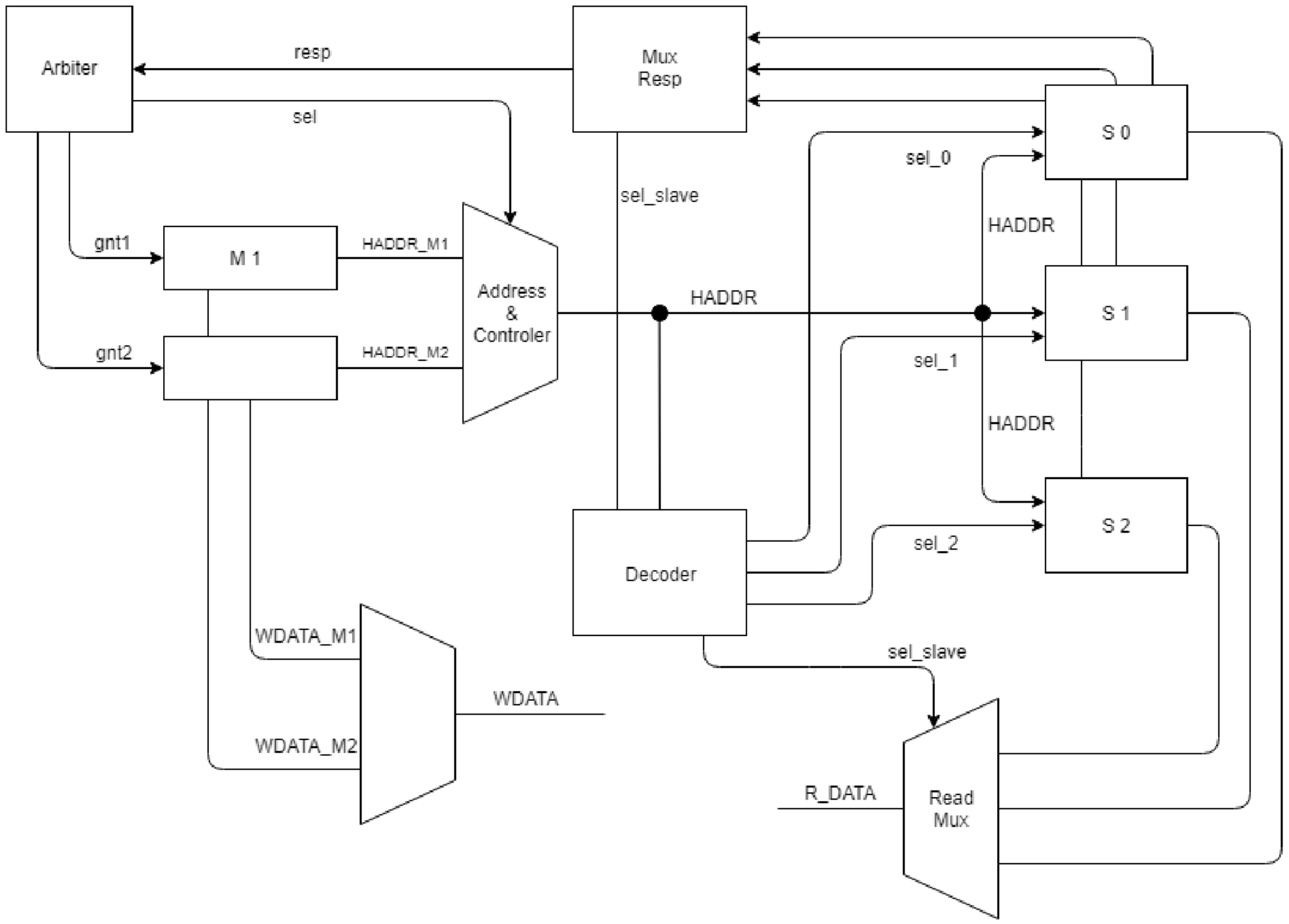
Signal	From	To	Task
clk		Bus	This clock times all bus transfers. All signal timings are related to the rising edge of HCLK
sb_lock_m1	Master 1	Arbiter	Lock request
req1	Master 1	Arbiter	Request for bus
req2	Master 2	Arbiter	Request for bus
Sb_lock_m2	Master 2	Arbiter	Lock request
resp0	Slave 0	Mux3-1_Resp	Response from slave 0
resp1	Slave 1	Mux3-1_Resp	Response from slave 1
resp2	Slave 2	Mux3-1_Resp	Response from slave 2
Resp	Mux3-1_Resp		
HADDR_M1 [14:0]	Master 1	ADD_mux (This is a 2 to 1 mux for address & control)	Address from master 1
HADDR_M2 [14:0]	Master 2	ADD_mux	Address from master 2
HADDR [14:0]	ADD_mux	Decoder	For slave selection first 2 bits specify the slave 00 - slave 0 01 - slave 1 10 - slave 2
RDATA_S0 [31:0]	Slave 0	Read mux (This is a 3-1 mux for read data)	Getting read data from slave 0
RDATA_S1 [31:0]	Slave 1	Read mux	Getting read data from slave 1

RDATA_S2 [31:0]	Slave 2	Read mux	Getting read data from slave 2
WDATA_M1 [31:0]	Master 1	Write data mux	Getting write data from master 1
WDATA_M2 [31:0]	Master 2	Write data mux	Getting write data from master 1
Sb_split_ar [1:0]	Slave	Arbiter	
sel_slave [1:0]	Decoder	Mux3-1_Resp Read mux	Sending slave selection data to mux
WDATA [31:0]	Write data mux	Slave	Sending write data to slave
gnt1	Arbiter	Master 1	Grant the master 1 (master 1 - granted master 2 - not granted)
gnt2	Arbiter	Master 2	Grant the master 2. (master 1 - not granted master 2 - granted)
Sb_masters [1:0]	Arbiter	ADD_mux (Address mux)	Specify the selected master. 00 - no master 01 - master 1 10 - master 2
Sb_mastlock	Arbiter	Slave	1 - lock 0 - no lock
RDATA [31:0]	Read mux	Master	Data bus carries read data from mux to master
sel_0	Decoder	Slave 0	1 - selected 0 - not selected
sel_1	Decoder	Slave 1	1 - selected 0 - not selected
sel_2	Decoder	Slave 2	1 - selected 0 - not selected
sel_slave [1:0]	Decoder	Mux3-1_Resp Read mux	Sending slave selected data to muxes 00 - slave 0

			01 - slave 1 10 - slave 2
WDATA [31:0]	Write data mux	Slave	Sending write data to slave



Bus architecture diagram

Top Module Architecture Diagram