Clock, counter/freq divider and FSM

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1 Clock

2 Counter/Frequency divider

2.1 50% DT

Counter upper limit:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity clkDiv is
  port (
    clk     : in  std_logic;
    rst     : in  std_logic;          -- 5 MHz clock
    clk_out : out std_logic);
end entity clkDiv;

architecture behavorial of clkDiv is
  signal cnt : integer   := 1;
  signal tmp : std_logic := '0';
begin  -- architecture behavorial

  -- purpose: divide the clock
  -- type   : sequential
  -- inputs : clk, rst
  -- outputs: clk_out
  process (clk, rst) is
  begin  -- process
```

```
   if rst = '0' then              -- asynchronous reset (active low)
      cnt <= 1;
      tmp <= '0';
   elsif clk'event and clk = '1' then  -- rising clock edge
      cnt <= cnt + 1;
      if (cnt = 2500000) then
        tmp <= not(tmp);
        cnt <= 1;
      end if;
    end if;
    clk_out <= tmp;
  end process;

end architecture behavorial;
```

3 FSM