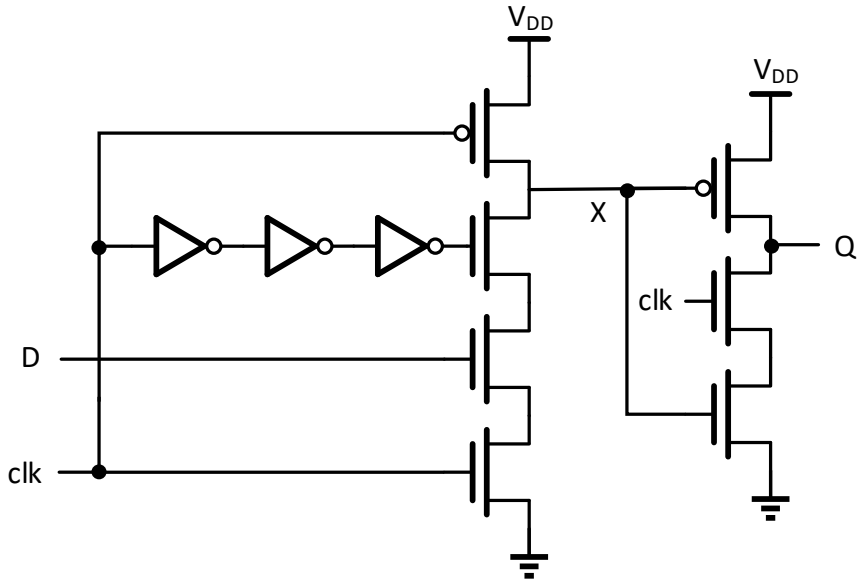
# ECEM216A Homework 4

**Instructor:** Hooman Darabi

**Sections covered:** Latches and flip flops, timing, pipelining, energy, FSMs.

Total of 5 questions, 20 points each. Due: 11:59PM Friday 12/5.

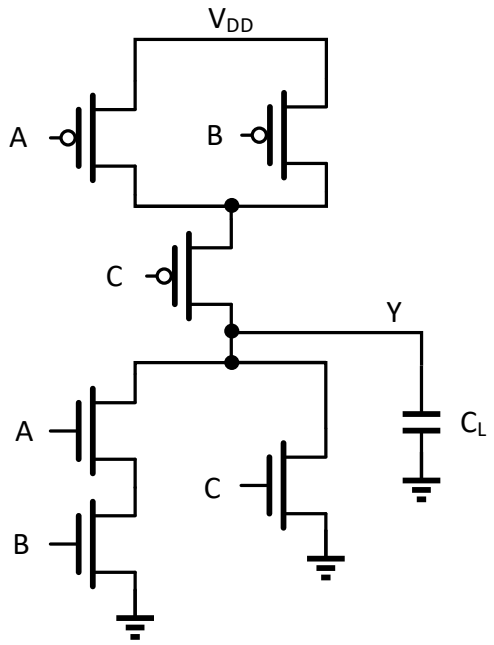
1. Consider the sequential circuit shown below.
   a. Would the sequential circuit from the figure above be considered a latch, a master-slave latch pair or a pulse-triggered latch? Briefly explain your answer.
   b. All transistors in this circuit are unit-sized, with equivalent resistances $R$ and gate capacitances $C$ (ignore diffusion capacitances). Calculate the propagation delay $t_{ddq}$ for high-to-low and low-to-high transitions. Load on the output Q is equal $10C$. Ignore the signal slopes in delay calculation.
   c. This circuit does not strictly follow the rules for designing sequential logic. List some major problems in the operation of this circuit.



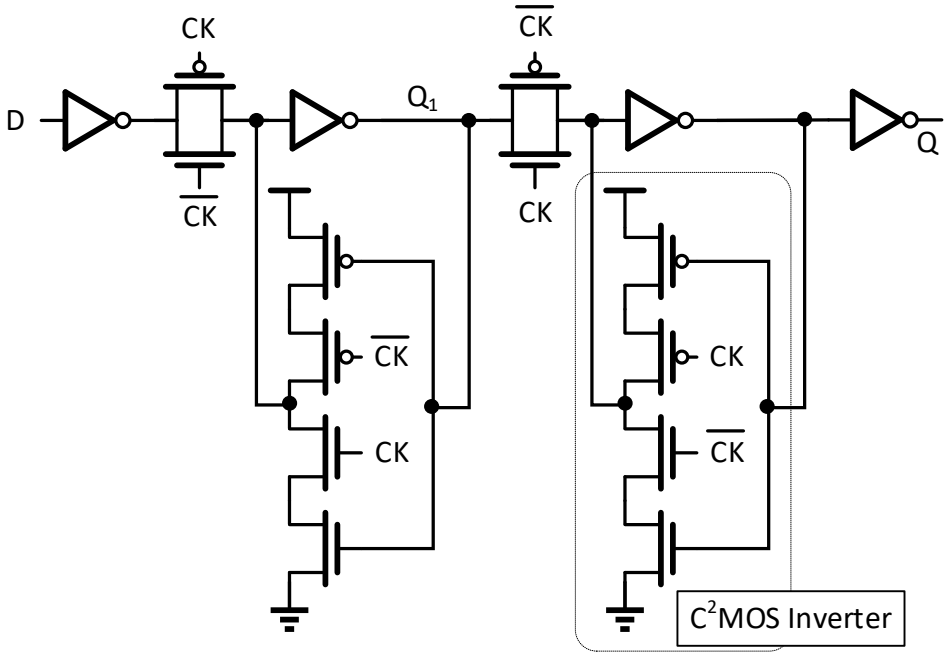

2. A datapath in a $1.2V$, $100-nm$ process has 10 million logic transistors. The average transistor width is $12\lambda$ ($\lambda = 25nm$). $|V_{TH}| = 180mV$ for both N and P devices. Subthreshold leakage for all OFF devices is $0.06nA/\mu m$. Assume $C_g = 2fF/\mu m$ and that half the transistors are OFF on average. $f_{clk} = 200MHz$, and the switching activity, $\alpha = 0.1$.
   a. Compute the dynamic power, leakage power, and total power.
   b. Consider the circuit shown below. $V_{DD} = 1V$, $C_L = 20fF$. Ignore any other capacitances. Let the drain current for each device be $1\mu A$ for NMOS at $V_{GS} = V_{THN}$, and PMOS at $V_{GS} = V_{THP}$. What input vectors cause the worst-case

leakage power for $Y = LOW$ and $Y = HIGH$? Provide input state(s), but do not calculate leakage.

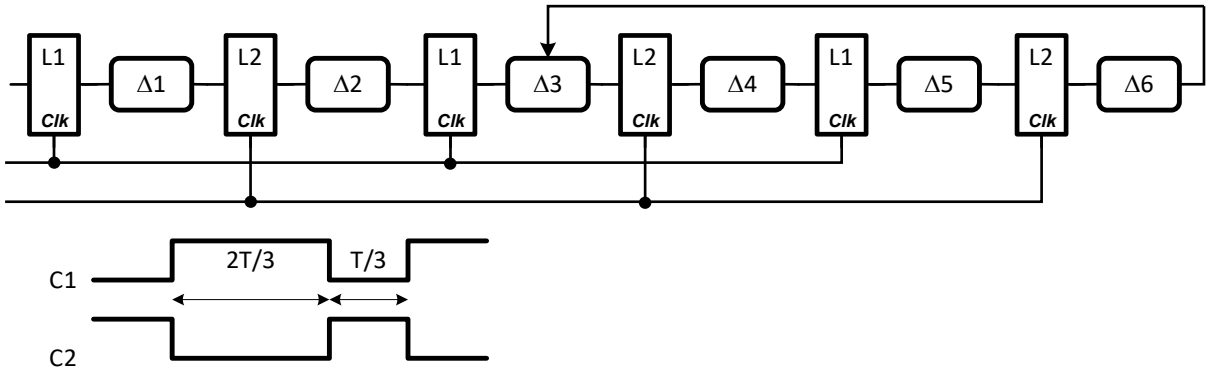
c. Suppose the circuit is active for a fraction of time $d$ and idle for $(1 - d)$. When the circuit is active, inputs arrive at $100MHz$. Assume inputs are uniformly distributed ($p(A = 1) = p(B = 1) = p(C = 1) = 0.5$), and independent. When the circuit is in the idle mode, inputs are in either of the states determined in part (b). Determine duty cycle $d$ where the dynamic and static power consumptions are equal. Assume $S = \ln(10)\, nV_T = 90mV/Dec$, where $I_{leakage} = I_0 \frac{W}{W_0} e^{\frac{V_{GS}-V_{TH}+\gamma V_{DS}}{nV_T}} = I_0 \frac{W}{W_0} 10^{\frac{V_{GS}-V_{TH}+\gamma V_{DS}}{nV_T}} \cong I_0 \frac{W}{W_0} 10^{\frac{V_{GS}-V_{TH}}{nV_T}}$ (DIBL ignored).




3. Consider the edge triggered flip-flop shown in the figure. Assume $clk$ and $\overline{clk}$ have negligible delay between them. If the static inverters, the transmission gates, and the $C^2$MOS inverters have all a propagation delay of $5pS$, find the flip flop propagation delay $t_{dcq}$, its setup time $t_s$, and the hold time $t_h$.




4. An example of pipeline is shown below. L1 latches are transparent when C1 is high, L2 latches are transparent when C2 is high. Data propagates from left to right, with last latch output fed back to Δ3. The pipeline is clocked by an asymmetric two-phase clock as shown. The clock edges are ideal and there is no skew or jitter. Assume that the latches have propagation delays, setup and hold times given as $t_{dcq} = t_{ddq} = t_s = t_h = 100pS$. Δ3 propagates its latest arriving input with the delay of $1.5ns$. Each of the logic blocks is built with static logic, with the following combinational logic delays: $\Delta 1 = 1\text{nS}$, $\Delta 2 = 1\text{nS}$, $\Delta 3 = 1.5\text{nS}$, $\Delta 4 = 1.5\text{nS}$, $\Delta 5 = 2\text{nS}$, $\Delta 6 = 1.2\text{nS}$. If input D is available $200ps$ before the falling edge of the clock C1, what is the minimum cycle time of this system? Show all delay constraints for this system.
**Hint**: Check the constraints of the input path first. That will set a lower bound for the clock period.



5. You are tasked to design a data pattern detector. Assume your input is a sequence of binary data (1 or 0). Design a finite state machine to detect the data pattern ("1101101"). Whenever such a pattern is found, the output should be high for 1 clock cycle.
   a. Draw the FSM transition diagram.
   b. Write the Verilog module FSM in a file named FSM.v, and a testbench for this module named FSM_tb in a file named FSM_tb.v.

   Submit the FSM transition diagram above and append FSM.v. Make sure that the signal names are called exactly how they are specified here.

| **Inputs** | **Bit Width** | **Description** |
|---|---|---|
| $clk$ | [0] | Clock |
| $rst$ | [0] | Asynchronous reset, active low |
| $data$ | [0] | Data input stream |
| **Output** | **Bit Width** | **Description** |
| $out$ | [0] | H: Pattern is found, high for one cycle<br>L: Pattern not found |