ECEM216A Homework 2

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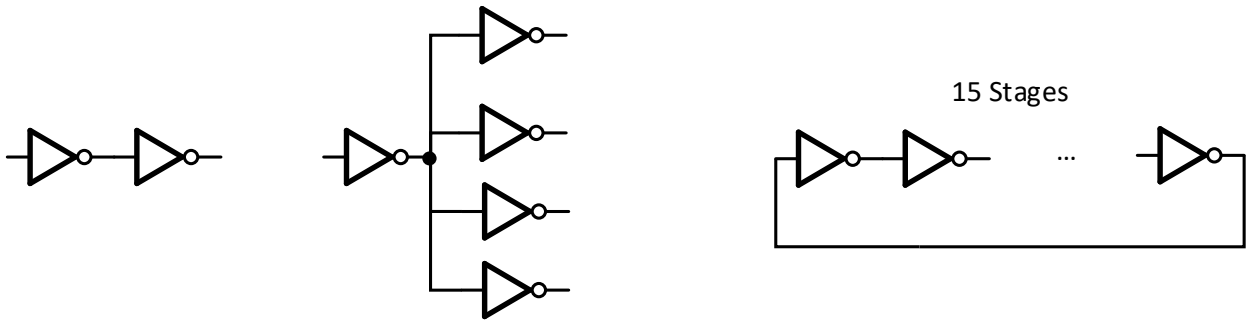
Sections covered: Delay and energy, gate sizing, logical effort, Verilog.

Total of 5 questions, 20 points each. Due: 11:59PM Friday 10/31.

For Cadence problems, make sure to take snapshots of your Cadence setup for each part, and any other simulation result you think is worth mentioning.

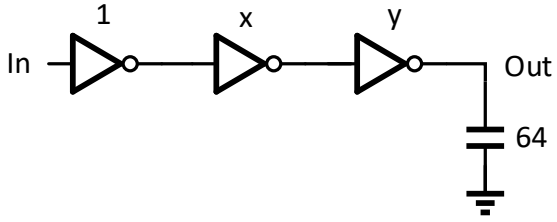
1. Using the simulation setups shown below, find:
   a. FO1 inverter delay.
   b. FO4 inverter delay.
   c. A 15-stage ring oscillator period of oscillation.
   d. Based on FO1 delay, can you justify the FO4 delay and the ring oscillator frequency of oscillation?

   For all the cases use lvt devices with INVX0 sizing with $V_{DD} = 0.8V$. Assume ideal pulses.



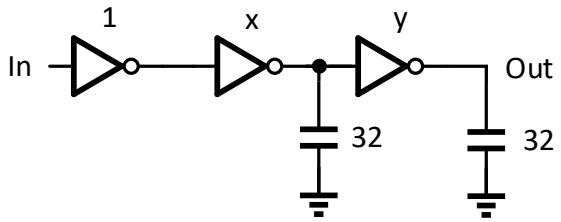
FO1 Test FO4 Test 15-Stage Ring Oscillator

2. Consider an inverter chain with wire-load as shown below. The numbers indicate size of the load relative to the reference inverter.



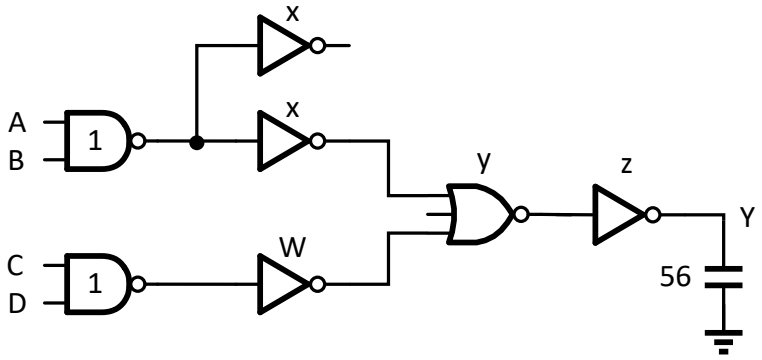
   a. Calculate x and y to minimize delay for the circuit above.
   b. What is the path delay from In to Out? Assume $\gamma = 0.5$ for the parasitic delay calculation.

c. Calculate x and y for minimum delay for the circuit below where the load capacitance is split between two stages.

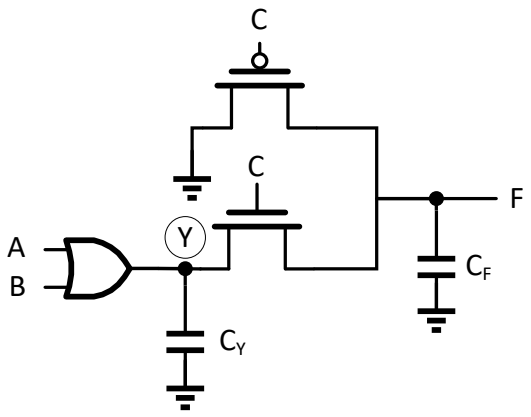


d. What is the minimum delay in this case ($\gamma = 0.5$)?

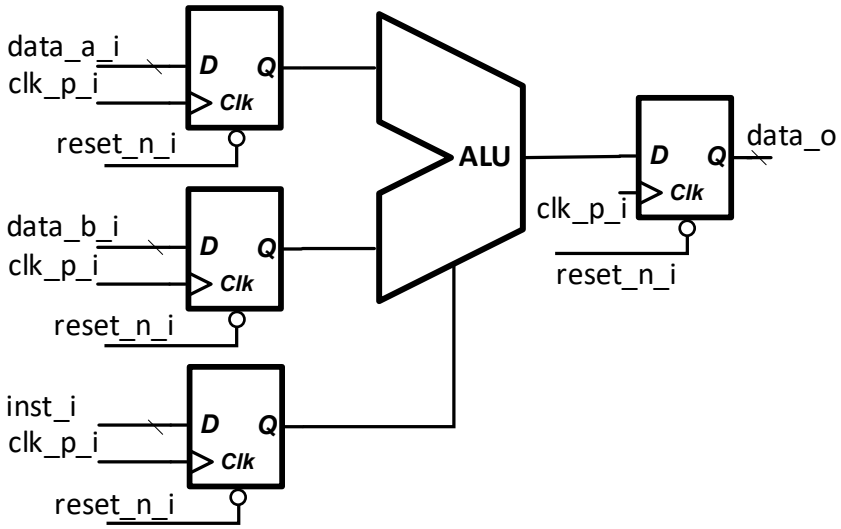
3. Assuming a reference unit-sized inverter with $W_P : W_N = 2 : 1$,
   a. Draw the schematic of the 3-input NOR gate, and size all the transistors such that the worst-case delay is equal to that of a unit-sized inverter. Find the logical effort (g_{NOR3}) and parasitic effort (p_{NOR3}) of the 3-input NOR gate.
   b. For the logic path from A to Y shown below, find the path logical effort (G), path branching effort (B), path electrical effort (H), path effort (F), path parasitic effort (P). What is the optimum effort per stage, f_{opt}, for minimum delay? What is the total path delay (D)?
   c. Find scaling factors (x, y, z) in order to minimize delay in the path A to Y.
   d. Is it possible to match the delay of path D to Y to the minimized delay of path A to Y? If yes, find scaling factors (w) that can achieve this.



4. For the logic circuit shown below, assume a clock frequency of 1GHz.
   a. What logic function is implemented by this circuit (inputs: A, B, C; output: F)?
   b. Consider the probability of logic 1 for inputs as follows: $P(A = 1) = 0.4$, $P(B = 1) = 0.35$, $P(C = 1) = 0.2$. Assuming $C_Y = 10fF$, $C_F = 30fF$, $V_{DD} = 1V$, $V_{THN} = 0.25V$, and $V_{THP} = -0.3V$, calculate the average switching power of the circuit (input C is a full swing signal).
   c. Calculate the heat energy dissipation for one cycle (charge + discharge) associated with C_Y and C_F.



5. An Arithmetic Logic Unit (ALU) is an atomic processing element in various applications. In this problem, you need to create an ALU with I/O registers using special instruction sets. The input registers prevent signal glitches propagating to the combinational circuits, and the output registers prevent signal glitches influencing the following stages. The ALU with I/O registers is shown below.



The 8-bit ALU 3-bit instruction is summarized in the table. Note that the output signal $\underline{data\_o}$ is 16-bit and uses 2's complement number representation and our input data of add/sub are positive unsigned values. You have to do zero-extension when output is positive and do sign-extension when output is negative. Please do zero-extension for AND as well as the XOR operations.

$inst\_i[2:0]$	**Operation**
000	Unsigned Addition
001	Unsigned Subtraction
010	Unsigned Multiplication
011	Bitwise AND
100	Bitwise XOR
101	Absolute Value of input a
110	Subtraction and Multiply by 4
111	Unused

An incomplete Verilog RTL code is provided. Modify the Verilog RTL to realize the above functions. A test bench is also provided for functional verification (see download links below). We will score your ALU design through the test bench.

Download the Verilog RTL file and the Testbench from:
$ cd ~/ee216a/
$ mkdir HW2/
$ cd HW2/
$ cp ../tool-setup .
$ cp /w/class.1/ee/ee216o/ee216ot2/fall25/CAD_Shared/HW2/HW2_alu.v .
$ cp /w/class.1/ee/ee216o/ee216ot2/fall25/CAD_Shared/HW2/HW2_test_alu.v .

Quick ModelSim Instructions
Once you finish writing your Verilog, follow these steps to work in ModelSim:

1) cd ~/ee216a/HW2/
2) bash
3) source tool-setup
4) Type **vsim &** to start ModelSim.
5) Click File -> New -> Project to create a new project and give it a name.
6) Add the Verilog files (it's probably better to reference the file rather than copy it).
7) In the Project tab (probably to the left of your screen), right click -> Compile -> Compile All. This will give you a message saying whether the compilation was

successful or not. If there are errors, double-click the red message to see what the errors were.

8) In the Transcript window (probably at bottom of your screen), type **vsim work.*xxx*** where xxx is the name of the testbench module (in our case, HW2_test_alu).

9) In the Objects window (looks blue), select everything -> right click -> Add to Wave -> Selected Signals. This should make these signals show up in the wave window (looks black).

10) In the Transcript window, type **restart** and then **run –all** to run the simulation.