ECEM216A Homework 1

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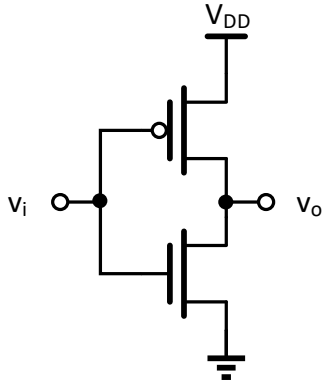
Sections covered: MOSFETs, wires, CMOS logic, delay.

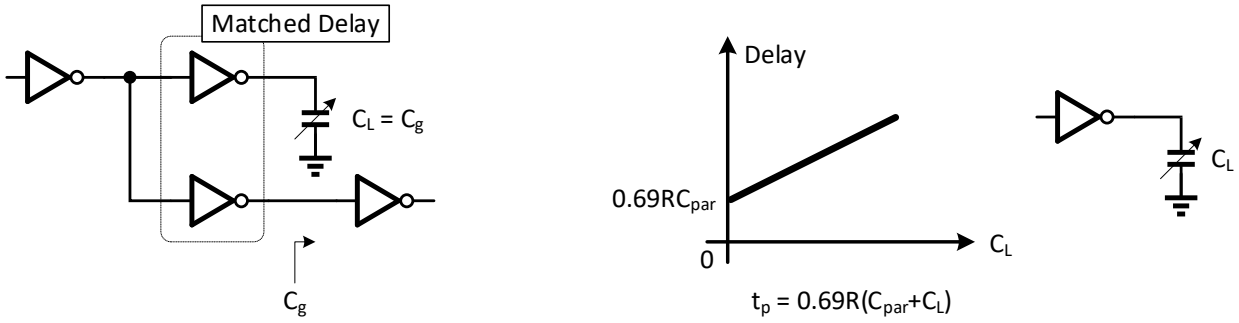
Total of 5 questions, 20 points each. Due: 11:59PM Sunday 10/19.

For Cadence problems, make sure to take snapshots of your Cadence setup for each part, and any other simulation result you think is worth mentioning.

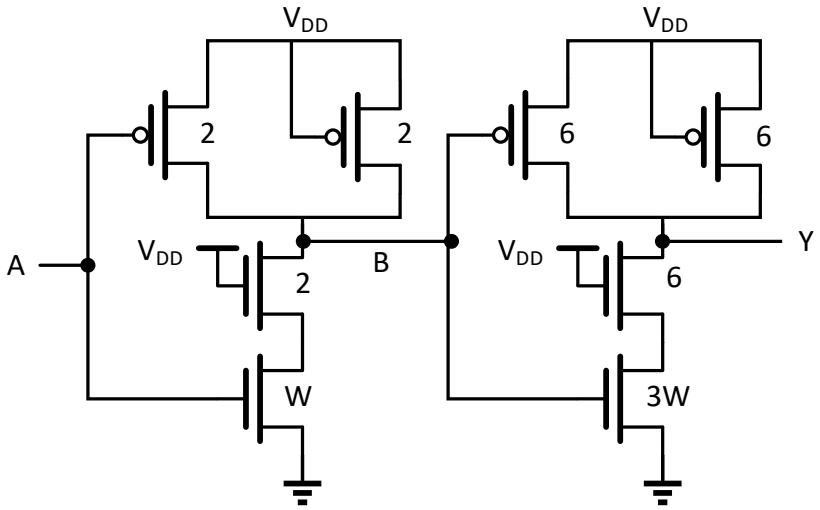
1. Use the following circuit to simulate the output-input characteristics (that is a plot of v_o with v_i going from 0 to V_{DD}) of a minimum sized inverter (INVX0).
   a. Use standard threshold transistors (svt) with number of fingers one, and number of fins 2 for both NMOS and PMOS. $V_{DD} = 0.8V$.
   b. Redo part a using low threshold (lvt) devices.
   c. For part b, find the low and high noise margins, and the midpoint voltage (the intersection of the $v_o - v_i$ curve with the line $v_o = v_i$). Noise margin low is the defined as V_{IL}, the input voltage for which the slope of $v_o - v_i$ curve is -1, and noise margin high is defined as $V_{DD} - V_{IH}$, where V_{IH} is the second input voltage for which the slope of $v_o - v_i$ curve is -1.
   d. How do the noise margins compare to the midpoint voltage? What does it say about the *robustness* of a CMOS inverter?



2. Using the setup below, simulate C_g, C_{par} and the effective resistance $R = \frac{t_p}{0.69(C_{par}+C_g)}$ for INVX0 as described in the previous problem. Use lvt devices, and $V_{DD} = 0.8V$.

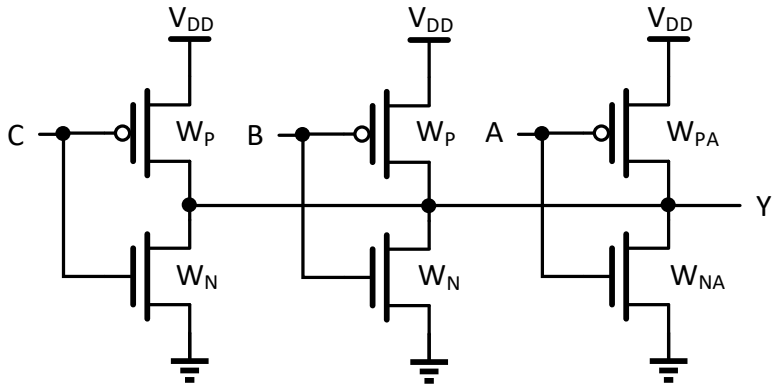


3. For the static CMOS circuit below, assume $C_{S/D} = 0.5C_0\ fF/\mu m$ for the diffusion capacitances, $C_g = C_0\ fF/\mu m$, and effective on resistance of $R_N = R_0\ k\Omega - \mu m$. All the sizes in the figure are in μm.
   a. What function this circuit performs (A is the input, Y is the output)?
   b. Assume no sharing of source/drain (S/D) of transistors. Find the time constant (*Elmore delay*) expressed in the given variables, and the width W that minimizes the delay of the gate from input A's rising edge to output B's falling edge.
   c. How does the answer change (the optimum W decreases or increases) if the sources and drains are shared as appropriate? Explain qualitatively.



4. Shown below is *ganged* CMOS logic circuit. Assuming 3 times higher mobility for N devices compared to P ($\beta = 3$), we wish to design an AND-OR-INV (AOI) gate such that: $Y = \overline{A + B.C}$.
   a. Given $W_{NA} = 3$, find the sizing constraints for other transistors to guarantee functional correctness.
   b. If the Ganged CMOS logic is sized such that $W_P = W_{PA} = W_{NA} = 3$, and $W_N = 1$, calculate the worst-case logical effort and parasitic effort.

c. Compare the logical effort and parasitic effort of Ganged CMOS logic with that of static CMOS logic (implementing the same function). What are the benefits of using Ganged CMOS logic instead of static CMOS logic?



5. Calculate the Elmore time constant from node A to node B of the following RC network.

$R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = 10\Omega$, and

$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = C_8 = 100fF$.