ECEM216A Homework 3

Instructor: Hooman Darabi

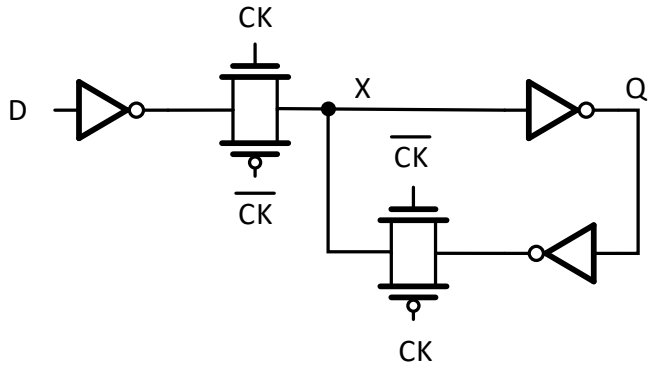
Sections covered: Latches and FFs, timing, Synthesis.

Total of 5 questions, 20 points each. Due: 11:59PM Sunday 11/23.

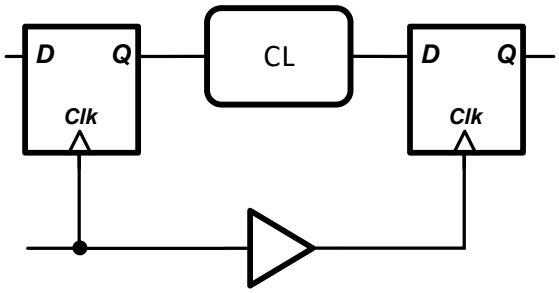
For Cadence problems, make sure to take snapshots of your Cadence setup for each part, and any other simulation result you think is worth mentioning.

1. We would like to find the setup time, hold time, and the $D \rightarrow Q$ propagation delay of the latch shown below. Assume an ideal $1 \rightarrow 0$ transition for the clock to force the latch into the hold mode. For simulations, assume a D input of 0, transitioning to 1, with edges arbitrarily close to (or passing) the clock edge.
   a. Find the t_s, t_p, and t_{dDQ}. Note that the hold time can be negative.
   b. Estimating the delay of the INVX0 inverters and passgates (you can assume them to be equal for simplicity), justify your findings.
   c. Clearly show in simulations the waveforms at nodes X and Q as the latch enters *metastability*.

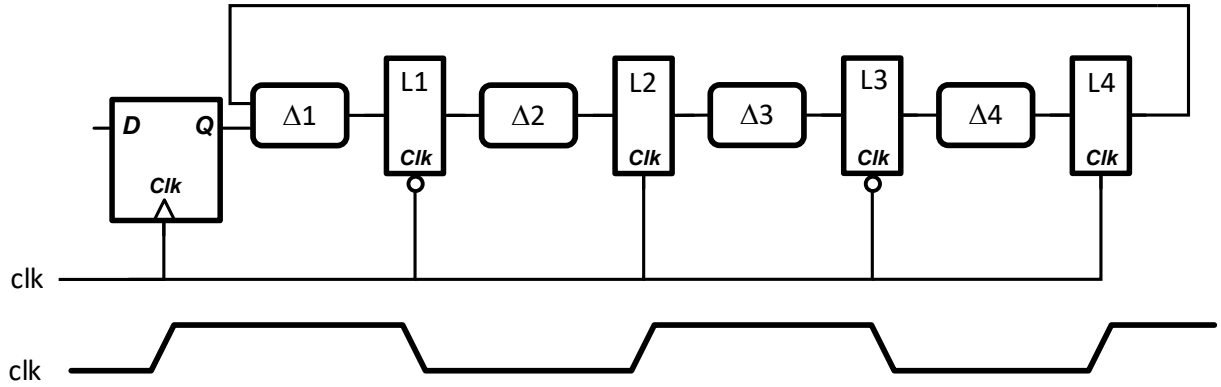
   Use lvt transistors for all the devices with one finger and two fins, and $V_{DD} = 0.8V$.



2. Analyze the figure below and determine if there is a setup and/or a hold time violation. Assume a clock period of $T_{clk} = 10nS$, a clock jitter of $1nS$, and the clock buffer delay of $1nS$. For the combinational circuit, the propagation delay is $4nS$ and the contamination delay is $3nS$. For the flipflops: $t_{dcq} = t_{ccq} = 2nS$, $t_s = 2nS$ and $t_h = 1nS$.



3. For the path in the figure, determine which latches borrow time and if any setup time violations occur. Calculate for cycle times of $1200pS$, $1000pS$, and $800pS$. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay of preceding-stage logic. $\Delta 1 = 550\text{pS}$, $\Delta 2 = 580\text{pS}$, $\Delta 3 = 480\text{pS}$, $\Delta 4 = 200\text{pS}$.



4. The goal of this exercise and the next is to introduce you to the Synopsys synthesis, timing, and power analysis tools. It also covers how to do a gate-level simulation in ModelSim for your synthesized design. You will be synthesizing the ALU from previous homework and analyzing its timing and power. To begin, you will need to source the included setup file:
   $ tcsh
   $ source tool-setup
   Included files: alu.v, alu_tb.v, saed32nm.v, lab2_synthesis.tcl, lab2_prime.tcl, tool-setup

   You will first synthesize the ALU. Run Synopsys Design Compiler:
   $ dc_shell -f lab2_synthesis.tcl
   It will generate the gate-level netlist (alu.vg) and a standard delay format file (alu.sdf), which you will need to do a gate-level accurate simulation in ModelSim. Also created is alu.sdc, which we will need for place and route (which we are not doing in this lab). Finally, several reports are generated, covering power, area, and timing. Using these reports, answer the questions below:

a. Report the synthesized design areas of Combinational, Buf/Inv, Non-combinational, and Net Interconnect blocks.
b. Report the synthesized design power for Switch Power, Int Power, Leak Power, and the Total Power.
c. Report the slack from the 5 worst hold times (paths 1 to 5).
d. Report the slack from the 5 worst setup times (paths 1 to 5).

5. Next, to check the timing of the ALU, run Synopsys PrimeTime/PrimePower:
   $ pt_shell -file lab2_prime.tcl
   The PrimePower of the script file has been commented out for now. We will need to run a gate-level ModelSim simulation to generate alu.vcd, a switching activity file, before we can run the PrimePower portion.
   a. Report the timing slack for the 2 paths reported by PrimeTime (paths 1 and 2).
   b. To generate alu.vcd, you will need to run alu_tb.v in ModelSim. Create a new project with alu_tb.v, alu.vg (created by synthesis), and the included Verilog technology file: saed32nm.v. Run the testbench for $10\mu S$ to create a switching activity file. Now open lab2_prime.tcl and uncomment the PrimePower sections. You will also need to add some code to the script to set the power analysis mode. For this lab, we will only look at the average power. Save and rerun the script. Fill out the following table for each ALU operation's power. The values for the case 000 (addition) have been provided so that you can verify your work. Generate a switching activity file of only $10\mu S$ for each operation when calculating the power. Provide the line(s) of code added to lab2_prime.tcl for PrimePower.
   c. Report the design power for each ALU operation, in the format shown in the table below:

ALU Operation	Switching Power	Int. Power	Leak Power	Total Power
000	4.65µW	32.08µW	164µW	168µW
001				
010				
011				
100				
101				
110				
111				