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| Branch(A53) | Immediate | Indirect | Mispredicted | PC change | Potential prediction | Taken |  |  |  |  |  |
| Branch(A73) | Immediate | Indirect | Mispredicted | PC change | Potential prediction |  |  |  |  |  |  |
| Bus(A53) | Access |  |  |  | Cycle | Read | Write |  |  |  |  |
| Bus(A73) | Access | Access normal | Access not shared | Access shared | Cycle |  |  | Peripheral |  |  |  |
| Cache(A53) |  | Allocate mode | Allocate mode enter | Data access | Data refill | Data TLB refill | - | Inst TLB refill | Instruction refill |  |  |
| Cache(A73) | BATC read | - | - | Data access | Data refill | Data TLB refill | Data ways | Inst TLB refill | Instruction refill |  |  |
| Cache L1 (A53) |  |  |  | Data error | Data write | Inst access | Inst error |  |  |  |  |
| Cache L1 (A73) | CP15 TLB refill | Data access write | Data read |  | Data write | Inst access | - | PLD TLB refill | TLB flush |  |  |
| Cache L2 (A53) | Data access |  |  |  |  | Data refill |  | Data write |  |  |  |
| Cache L2 (A73) | Data access | Data access write | Data clean | Data invalidate | Data read | Data refill | Data victim | Data write | TLB access | TLB miss |  |
| Cache (A53) | Linefill | Throttle | TLB eror |  |  |  |  |  |  |  |  |
| Cache (A73) | - | - | - |  |  |  |  |  |  |  |  |
| Clock(A53) | Cycles |  |  |  |  |  |  |  |  |  |  |
| Clock(A73) | Cycles |  |  |  |  |  |  |  |  |  |  |
| Counter chain(A53) | Odd performance |  |  |  |  |  |  |  |  |  |  |
| Counter chain(A73) | Odd performance |  |  |  |  |  |  |  |  |  |  |
| Exception(A53) | Return | Taken |  |  |  |  |  |  |  |  |  |
| Exception(A73) | Return | Taken | Hypervisor |  |  |  |  |  |  |  |  |
| ETM (A53) |  |  |  |  |  |  |  |  |  |  |  |
| ETM (A73) | Output 0 | Output 1 |  |  |  |  |  |  |  |  |  |
| Hypervisor (A53) |  |  |  |  |  |  |  |  |  |  |  |
| Hypervisor (A73) | Traps |  |  |  |  |  |  |  |  |  |  |

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| Interrupts(A73) |  |  |  |  |  |  |  |  |  |  |  |
| Memory(A53) | Error | External request | Memory access |  |  |  |  | Non-cacheable ext req | Snoop | Unaligned access | Write stall |
| Memory(A73) |  |  | Memory access | Read | Translation table | Unaligned | write |  |  |  |  |
| Pre-decoder(A53) | Error |  |  |  |  |  |  |  |  |  |  |
| Pre-decoder(A73) |  |  |  |  |  |  |  |  |  |  |  |
| Procedure(A53) | Return |  |  |  |  |  |  |  |  |  |  |
| Procedure(A73) | Return |  |  |  |  |  |  |  |  |  |  |
| MMU (A53) |  |  |  |  |  |  |  |  |  |  |  |
| MMU (A73) |  |  |  |  |  |  |  |  |  |  |  |
| Slots (A53) |  |  |  |  |  |  |  |  |  |  |  |
| Slots (A73) | Data engine issue Q | Data processing issue Q | Load/store issue Q | Load/store unit |  |  |  |  |  |  |  |
| Software(A53) | Increment |  |  |  |  |  |  |  |  |  |  |
| Software(A73) |  |  |  |  |  |  |  |  |  |  |  |
| Stall(A53) | Cache miss | DPU IP empty | Interlock address | Interlock other | SIMD/FPU | Load miss | Pre-decoder error | Store | TLB miss |  |  |
| Stall(A73) |  |  |  |  |  |  |  |  |  |  |  |

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| Instruction(A53) |  | CONTEXTIDR | Data read | Data executed | Memory write |  |  |  |  |  |  |
| Instruction(A73) | Advanced SIMD | CONTEXTIDR |  | Data executed |  | Crypto | DMB | DSB | Integer | ISB |  |
| Instruction (A53) |  |  |  |  |  |  |  |  |  |  |  |
| Instruction (A73) | Load | Load/store | Speculative | Stalled lindfill | Stalled page table walk | Store | VFP |  |  |  |  |
| Intrinsic (A53) |  |  |  |  |  |  |  |  |  |  |  |
| Intrinsic (A73) | LDREX | STREX fail |  |  |  |  |  |  |  |  |  |
| Interrupts(A53) | FIQ | IRQ |  |  |  |  |  |  |  |  |  |