ECE385

Fall 2021

Experiment #1

Introductory Experiment

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Section AB1

1. Introduction

The purpose of this lab is to design a 2-to-1 multiplexor using a 4 x 2 input NAND gate chip and observe the function of the circuit through oscilloscope. By noticing the glitches in original design, further improve the implementation by adding additional logics to circumvent the satic-1 hazard phenomenon.

2. Description of Circuit

The circuit in part A of pre-lab realized the logic function: Z=((BA)’(B’C)’)’. Since we want B to be the switch and when B=1, Z outputs A and when B=0, outputs C, according to the required performance, we have the following K-map:

Z		BC			
		00	01	11	10
A	0	0	1	0	0
	1	0	1	1	1

And that results in the original version target logic expression: Z=BA+B’C. To implement the circuit using NAND gates, we apply the De Morgan’s Law and get our final expression.

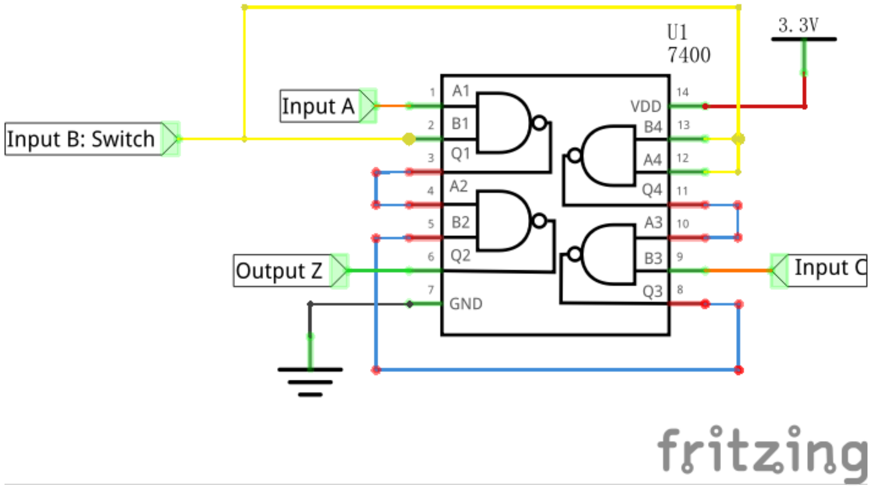
The circuit in part B implemented the logic function: Z=((((BA)’(B’C)’)’)’(AC)’)’. Since we are trying to avoid the static-1 hazard, we are going to cover all adjacent min-terms in the K-map:

Z		BC			
		00	01	11	10
A	0	0	1	0	0
	1	0	1	1	1

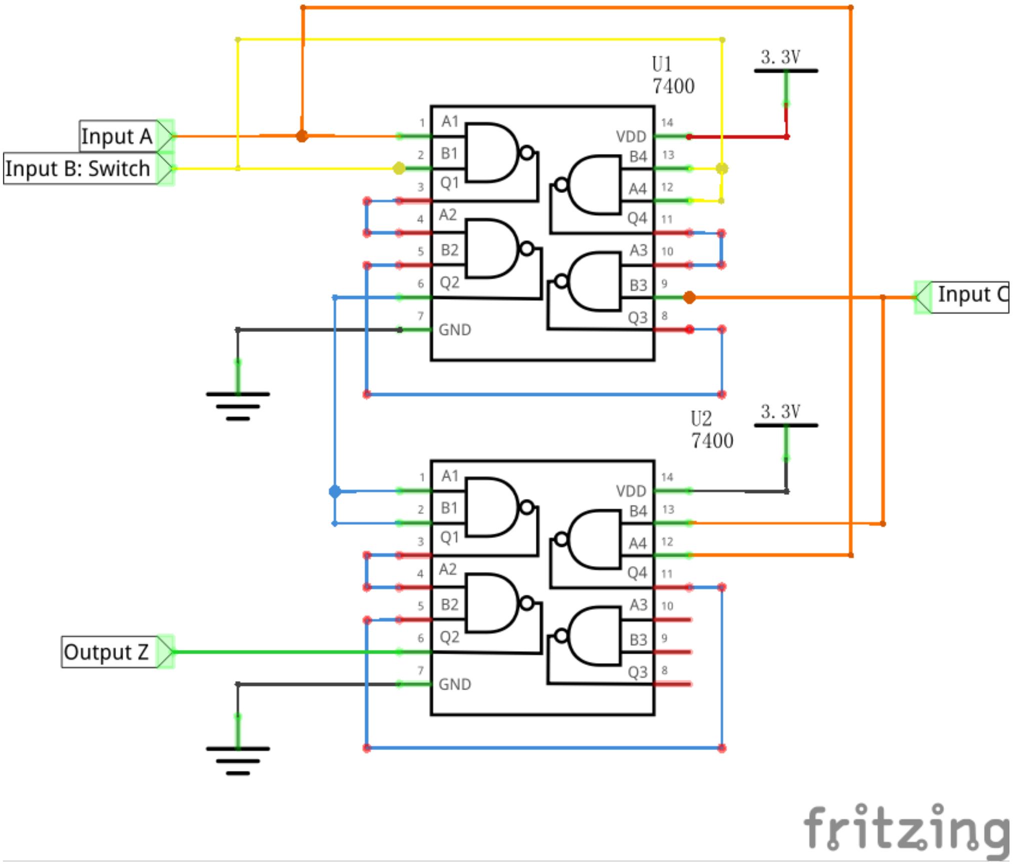
Thus, we have the logic expression: Z=BA+B’C+AC. Then we need to translate into NAND expression using De Morgan’s Law and get our final result.

3. Layout Sheet

a) Part A Circuit:

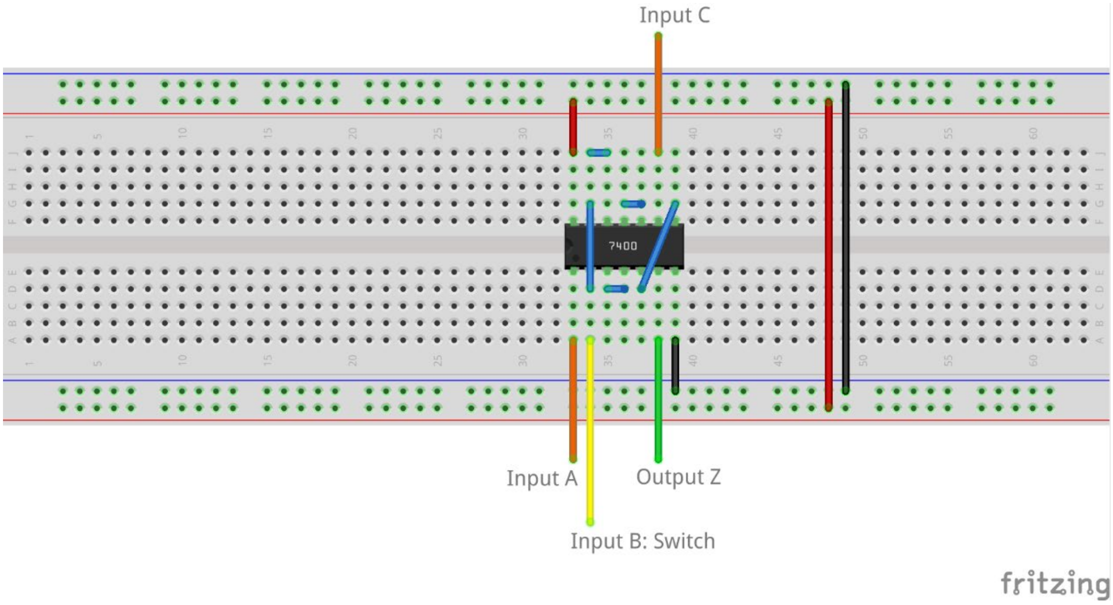


b) Part B Circuit:

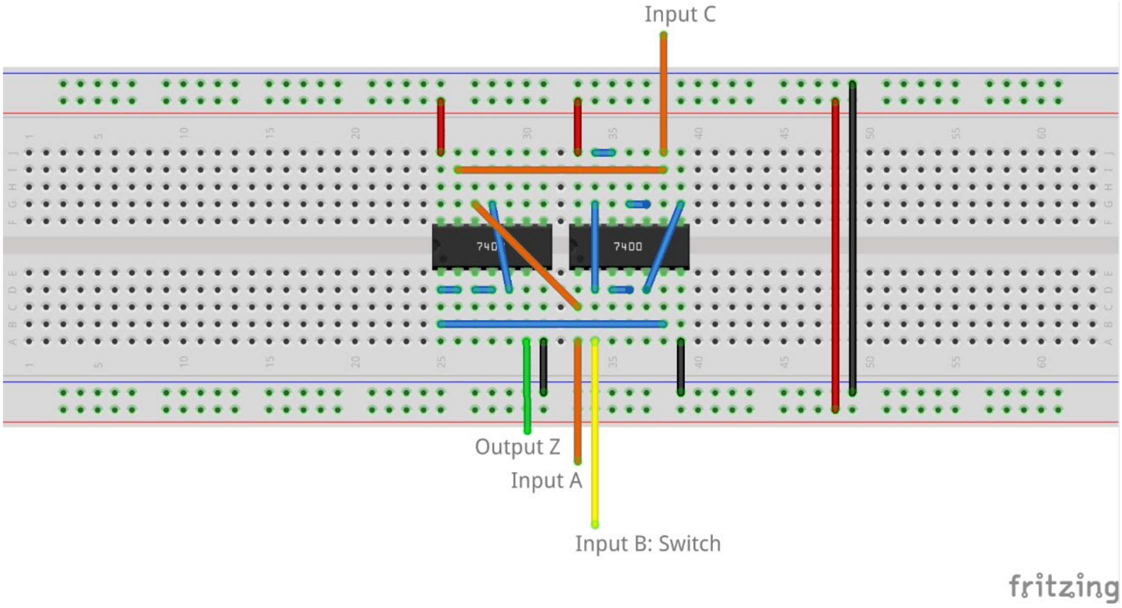


4. Component Diagram

a) Part A Diagram:



b) Part B Diagram:

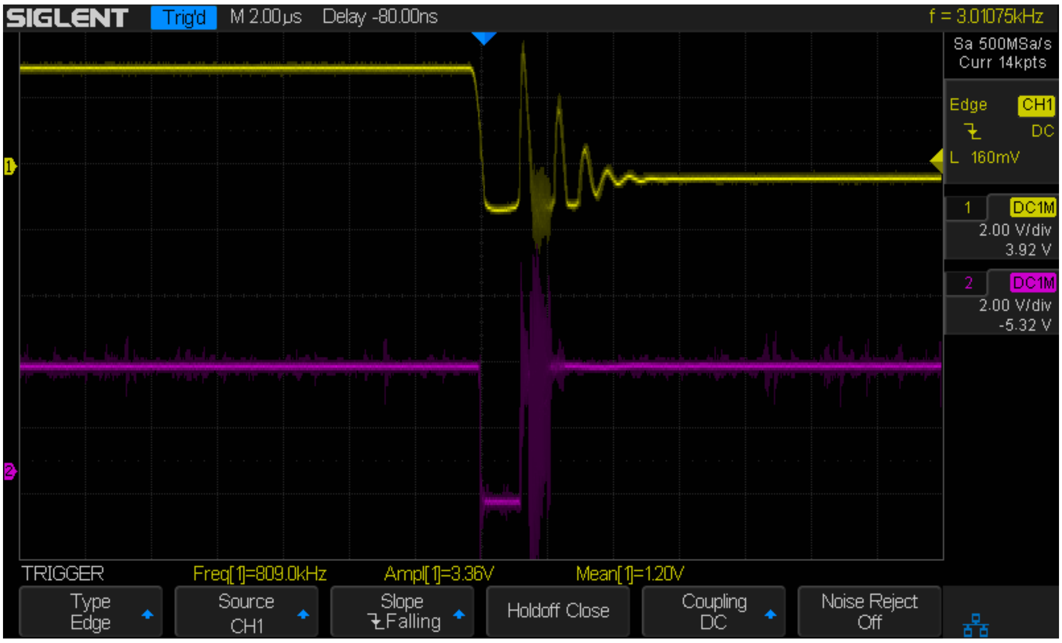


5. Lab Documentation

1. Truth Table for Part A:

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

2. Wave Form for Part A Circuit:



M 2.00μs Delay -80.00ns f = 3.01075kHz

Sa 500MSa/s
Curr 14kpts

Edge CH1
DC
L 160mV

1 DC1M
2.00 V/div
3.92 V

2 DC1M
2.00 V/div
-5.32 V

TRIGGER Freq[1]=809.0kHz Ampl[1]=3.36V Mean[1]=1.20V

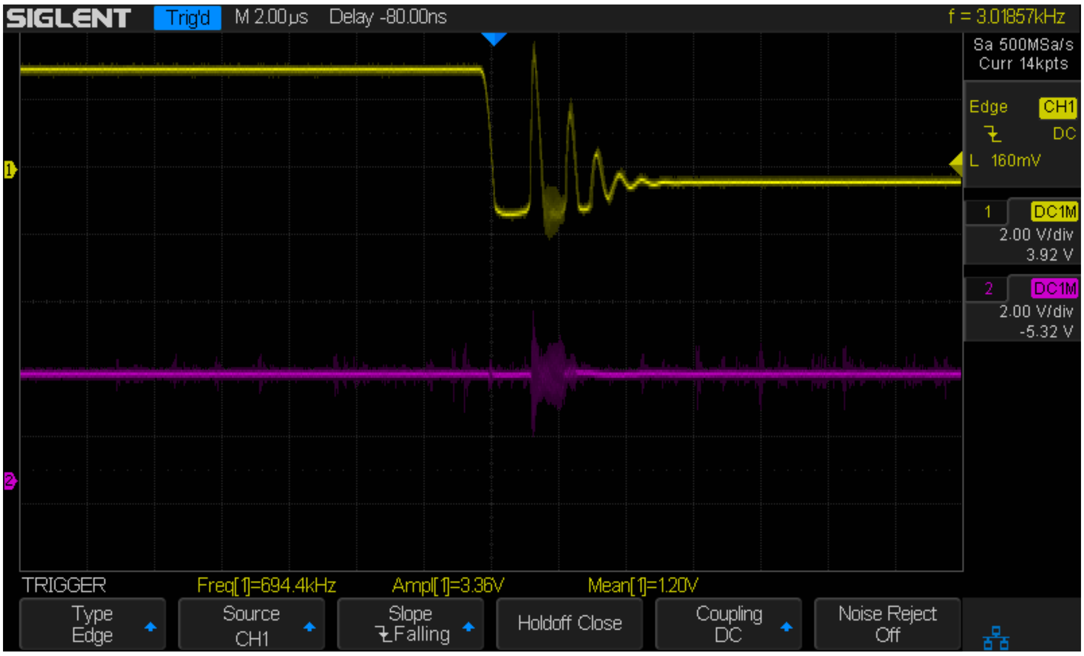
Type Edge
Source CH1
Slope Falling
Holdoff Close
Coupling DC
Noise Reject Off

3. Truth Table for Part B:

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The circuit responses exactly the same as the one of part A.

4. Wave Form for Part B Circuit:



Trig'd M 2.00μs Delay -80.00ns f = 3.01857kHz

Sa 500MSa/s
Curr 14kpts

Edge CH1
DC
L 160mV

1 DC1M
2.00 V/div
3.92 V

2 DC1M
2.00 V/div
-5.32 V

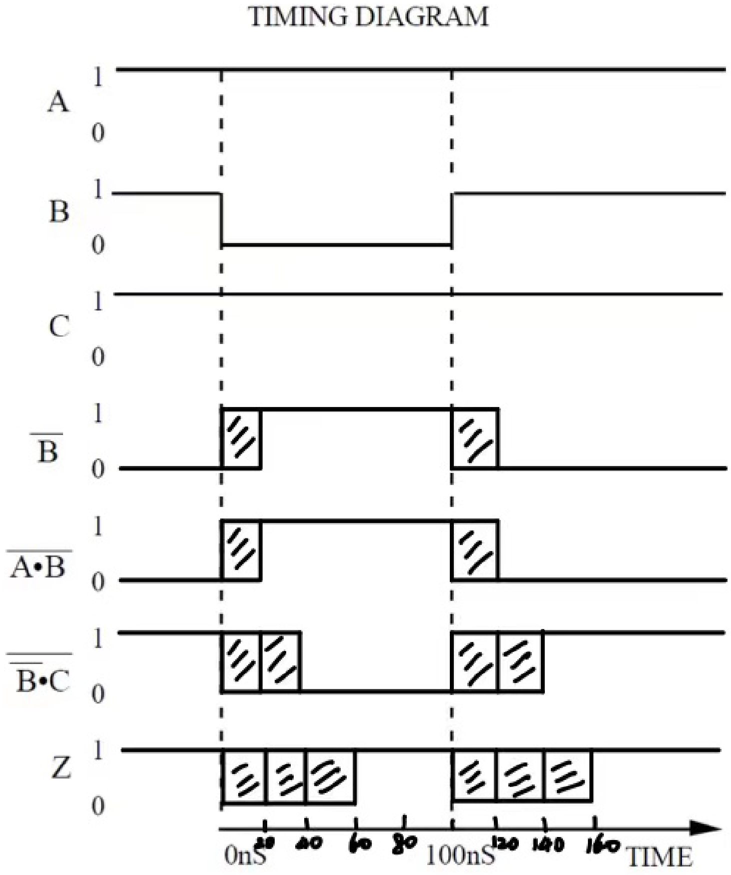
TRIGGER Freq[1]=694.4kHz Ampl[1]=3.36V Mean[1]=1.20V

Type Edge
Source CH1
Slope Falling
Holdoff Close
Coupling DC
Noise Reject Off

Given both A and C are logical high and the switch signal flipped, the output has tiny turbulence that may due to the switch signal bouncing, but no obvious glitch. Comparing to the result from Part A, the glitch is successfully avoided by adding the additional logic components. The glitches are more likely to be observed at the **falling edge** of the input B in part A. This is because the glitch is caused by the delay of transistors. Given the logic expression Z=BA+B'C, the B' signal goes into the OR gate calculating B'C will go through one more transistor than the B signal for BA. Since both A and C are logical high, when B transferred from high to low, the result of BA will become low first while B'C will still be low for several nano-seconds. OR-ing the two logical low signals will make Z low as will, and that causes the glitch. However, when B goes from low to high, BA goes low to high first while B'C keeps being logical high due to the delay. OR-ing the two logical highs will keep the output Z being high, and no glitch occurs at the rising edge.

6. Post-Lab Questions

1. The timing diagram is as below:



Z will stablize in 60ns both for rising and falling edges of B. There are potential glitches in the output. This is because each components has a delay which will accumulate. The logic expression of the output Z is ((AB)’(B’C)’)’. Assuming every component has a delay of 60ns. Given B, as the input, changes, (AB)’ and (B’C)’ will take different time to stablize due the extra delay introduced by B’. Therefore, the glicth will appear when (AB)’ is stablized while (B’C)’ is not. Such delay is inevitable and unpredictable. Thus, such glicthes will always potentially exist.

2. The debouncer circuit consists of a normal switch and two NAND gates connected in a flipflop-like way. One foot of the NAND gate is connected to logical high when the switch is open on that side and logical low when the switch is closed since it is grounded. If the switch is closed, one input of the NAND will be logical low, and the out put of the NAND gate will then be logical high. The output of this NAND gate will connect to the other NAND gate, while the other input of that NAND gate is logical high according to the switch position. Therefore, the output of the NAND gate will be logical low, which will connect to the first NAND gated. That is how the debouncer circuit functioning as a switch. The ill effect of machinal connect bounce means when the switch

connects the one side, it may bounce back and cause disconnection. Then, the input to a NAND gate will be logical low initially, then bouncing between logical low and high, and finally stable at logical low. However, with the debouncer circuit, we know that the output of the other NAND gate, which will be logical low when the switch is connected to the other side, is connected to the first NAND gate, making the output stable at logical high as soon as it outputs logical high in the first place. That is how the circuit eliminate the ill effect of machinal connect bounce.

7. General Guide Problems

1. GG.6

   The larger noise immunity means the component will have a stable logic output even if the input is noisy, this will result in a robust circuit whose logical level will not change even if the input fluctuates in small scale. We want to measure the noise immunity after is passing through several inverters because we want to manually introduce some noise to the circuit, then the measurement of noise immunity is more meaningful then measuring it under a stable input. From the graph, we can see that the noise immunity for logical “1” is 3.5-1.35=2.15V while the one for logical “0” is 1.15-0.35=0.8V.

2. GG.31

   If many LEDs connects in parallel and shares one resistor, the total amount of the current passing through the resistor will be the same as one LED connect with one resistor. However, since the resistor is shared, the current will be divided between the LEDs, which will result in the circuit having lower current then necessary and may finally lead to malfunctioning.

8. Conclusion

Although we did not finish experiment #1 on hand, we observed the static-1 hazard if we build the circuit in the naïve way. We also find out that by adding one more term, we can eliminate the hazard and make the circuit more robust.