**RS Flip-flop**

**Set the pins in the following order and record the states for Q and Q’**

|  |  |  |  |
| --- | --- | --- | --- |
| **S** | **R** | **Q** | **Q’** |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 |

A diagram of a circuit

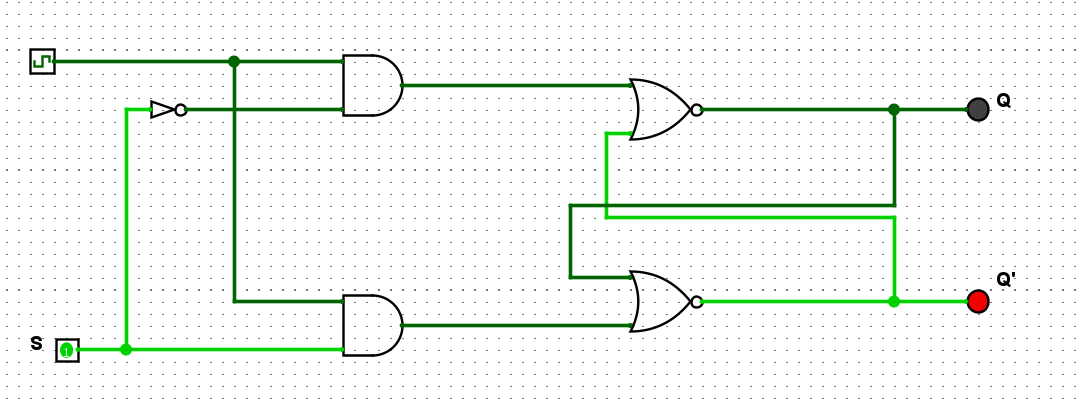
Description automatically generated

**Describe in a sentence, the behavior of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.**

* When the S is 1, the Q is 0, and the Q’ is 1. When the R is 1, the Q is 1, and the Q’ is 0. This is useful for digital circuit design since it stores the current state of the circuit.

**What do you notice about the two times you set both inputs to? Briefly explain what is happening here and why this is an issue for digital circuit design.**

* When both inputs are 1, both of Q and Q’ are 0. Since Q and Q’ must maintain opposite state for the flip-flop to work, this is a illegal state and an issue for digital circuit.

**D Flip-flop**

|  |  |  |  |
| --- | --- | --- | --- |
| **Clock** | **Pin** | **Q** | **Q’** |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |

**Briefly explain the behavior of a D Flip Flop and how it is useful for digital circuit design.**

* When the clock signal is one, it unlocks the S signal to go in the circuit to change the states of the output. When the clock signal is 0, it will lock the states of the output therefore the states of the output cannot be changed by the S. This is helpful for the digital circuit as it allows to store bits on the other side of the signal.

**What is the role of the clock? How does it impact the changing state of Q and Q’?**

* The clock's role is to unlock and lock the states of the output, when the clock signal is 1, it will allow the states of the output to be changed by the S signal. When the clock signal is 0, it will lock the states of the output therefore the output can’t be changed by the S signal.

**Why is it generally preferred over the R-S Flip Flop?**

* Because thanks to the clock and the AND gates, there is no illegal states in this flip flop.

**J-K Flip flop**

|  |  |  |  |
| --- | --- | --- | --- |
| **J** | **K** | **Q (when clocked)** | **Q’ (when clocked)** |
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

A diagram of a circuit

Description automatically generated

**How can a J-K Flip Flop be made to behave like a D Flip Flop?**

* To make a J-K flip flop behave like a D flip flop, the J and K input can be tied into 1 input with a not gate in the middle so the signal goes in J and K will always be different and It will be the S input in the D flip flop.

**How can a J-K Flip Flop be made to behave like a toggle (T Flip Flop)?**

* To make a J-K flip-flop behave like a T flip-flop, the J and K inputs can be tied into 1 input and act as T input in the T flip-flop.

A computer screen shot of a diagram

Description automatically generated**Register**

|  |  |  |
| --- | --- | --- |
| **Ox** | **Input Binary** | **Output Binary** |
| 0 | 0000 | 0000 |
| 1 | 0001 | 0001 |
| 2 | 0010 | 0010 |
| 3 | 0011 | 0011 |
| 4 | 0100 | 0100 |
| 5 | 0101 | 0101 |
| A | 1010 | 1010 |
| B | 1011 | 1011 |
| C | 1100 | 1100 |
| D | 1101 | 1101 |
| E | 1110 | 1110 |
| F | 1111 | 1111 |