Document Number: MMA8451Q
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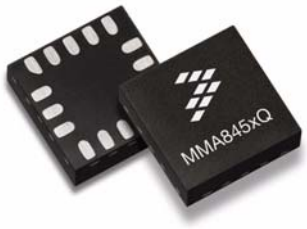
RoHS

Xtrinsic MMA8451Q 3-Axis, 14-bit/8-bit Digital Accelerometer

MMA8451Q

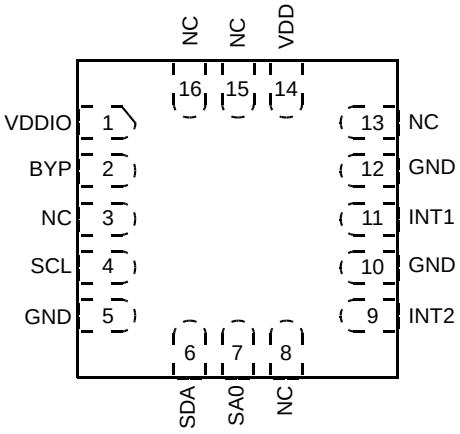
The MMA8451Q is a smart, low-power, three-axis, capacitive, micromachined accelerometer with 14 bits of resolution. This accelerometer is packed with embedded functions with flexible user programmable options, configurable to two interrupt pins. Embedded interrupt functions allow for overall power savings relieving the host processor from continuously polling data. There is access to both low-pass filtered data as well as high-pass filtered data, which minimizes the data analysis required for jolt detection and faster transitions. The device can be configured to generate inertial wakeup interrupt signals from any combination of the configurable embedded functions allowing the MMA8451Q to monitor events and remain in a low-power mode during periods of inactivity. The MMA8451Q is available in a 3 mm by 3 mm by 1 mm QFN package.

Top and Bottom View



16 PIN QFN
3 mm by 3 mm by 1 mm
CASE 2077-02

Top View



Pin Connections

Features

- 1.95V to 3.6V supply voltage
- 1.6V to 3.6V interface voltage
- ±2g/±4g/±8g dynamically selectable full-scale
- Output Data Rates (ODR) from 1.56 Hz to 800 Hz
- 99 µg/√Hz noise
- 14-bit and 8-bit digital output
- I^2C digital output interface (operates to 2.25 MHz with 4.7 kΩ pullup)
- Two programmable interrupt pins for seven interrupt sources
- Three embedded channels of motion detection
- Freefall or Motion Detection: 1 channel
- Pulse Detection: 1 channel
- Jolt Detection: 1 channel
- Orientation (Portrait/Landscape) detection with programmable hysteresis
- Automatic ODR change for Auto-WAKE and return to SLEEP
- 32-sample FIFO
- High-Pass Filter Data available per sample and through the FIFO
- Self-Test
- RoHS compliant
- Current Consumption: 6 µA to 165 µA

Typical Applications

- E-Compass applications
- Static orientation detection (Portrait/Landscape, Up/Down, Left/Right, Back/Front position identification)
- Notebook, e-reader, and Laptop Tumble and Freefall Detection
- Real-time orientation detection (virtual reality and gaming 3D user position feedback)
- Real-time activity analysis (pedometer step counting, freefall drop detection for HDD, dead-reckoning GPS backup)
- Motion detection for portable product power saving (Auto-SLEEP and Auto-WAKE for cell phone, PDA, GPS, gaming)
- Shock and vibration monitoring (mechatronic compensation, shipping and warranty usage logging)
- User interface (menu scrolling by orientation change, tap detection for button replacement)

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package Description**	**Shipping**
MMA8451QT	-40°C to +85°C	QFN-16	Tray
MMA8451QR1	-40°C to +85°C	QFN-16	Tape and Reel

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freescale Xtrinsic

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Related Documentation

The MMA8451Q device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number MMA8451Q.
3. In the Refine Your Result pane on the left, click on the Documentation link.

1 Block Diagram and Pin Description

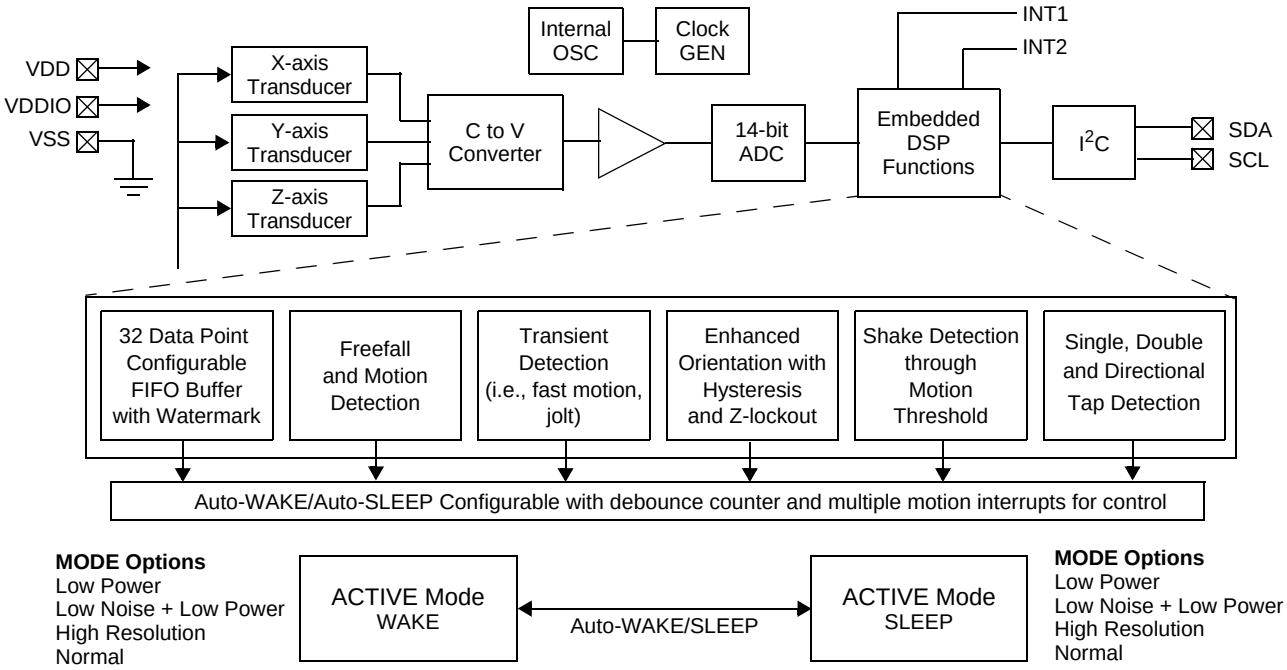


Figure 1. Block Diagram

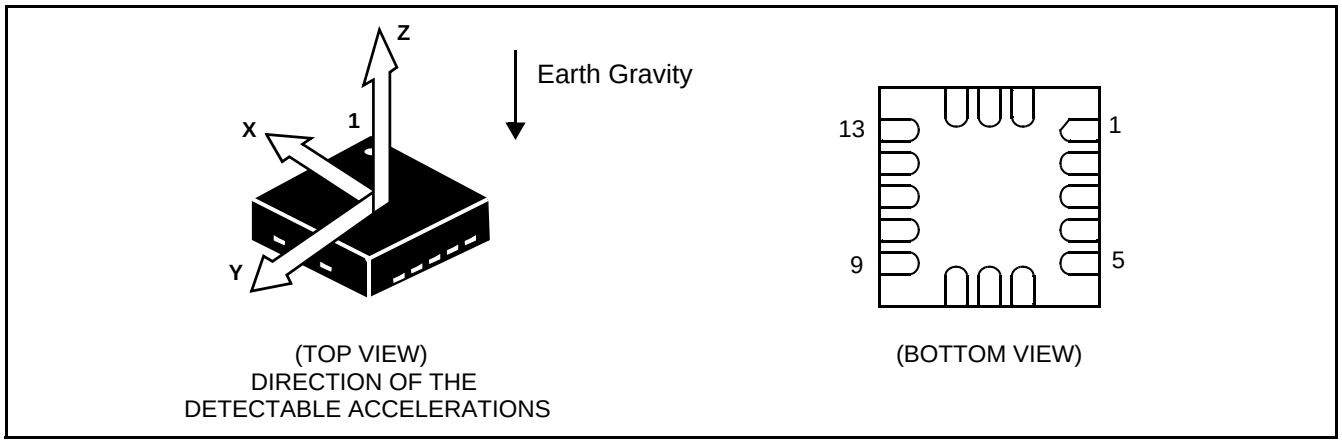


Figure 2. Direction of the Detectable Accelerations

Figure 3 shows the device configuration in the 6 different orientation modes. These orientations are defined as the following: PU = Portrait Up, LR = Landscape Right, PD = Portrait Down, LL = Landscape Left, BACK and FRONT side views. There are several registers to configure the orientation detection and are described in detail in the register setting section.

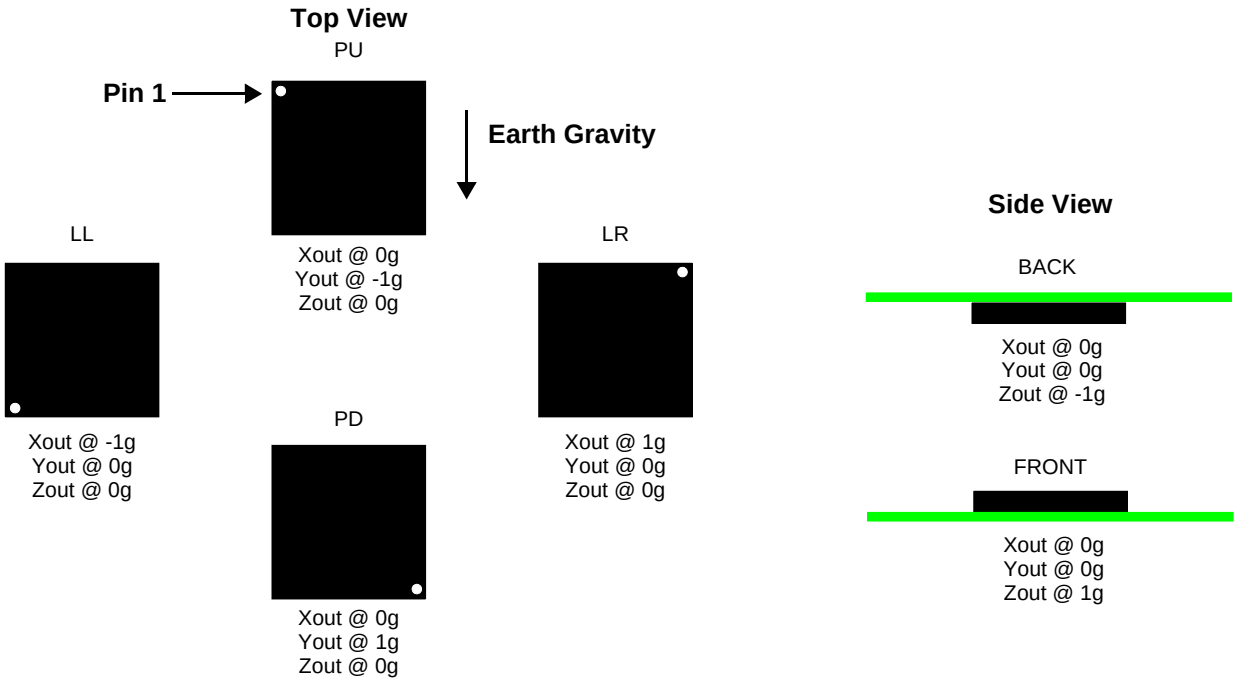


Figure 3. Landscape/Portrait Orientation

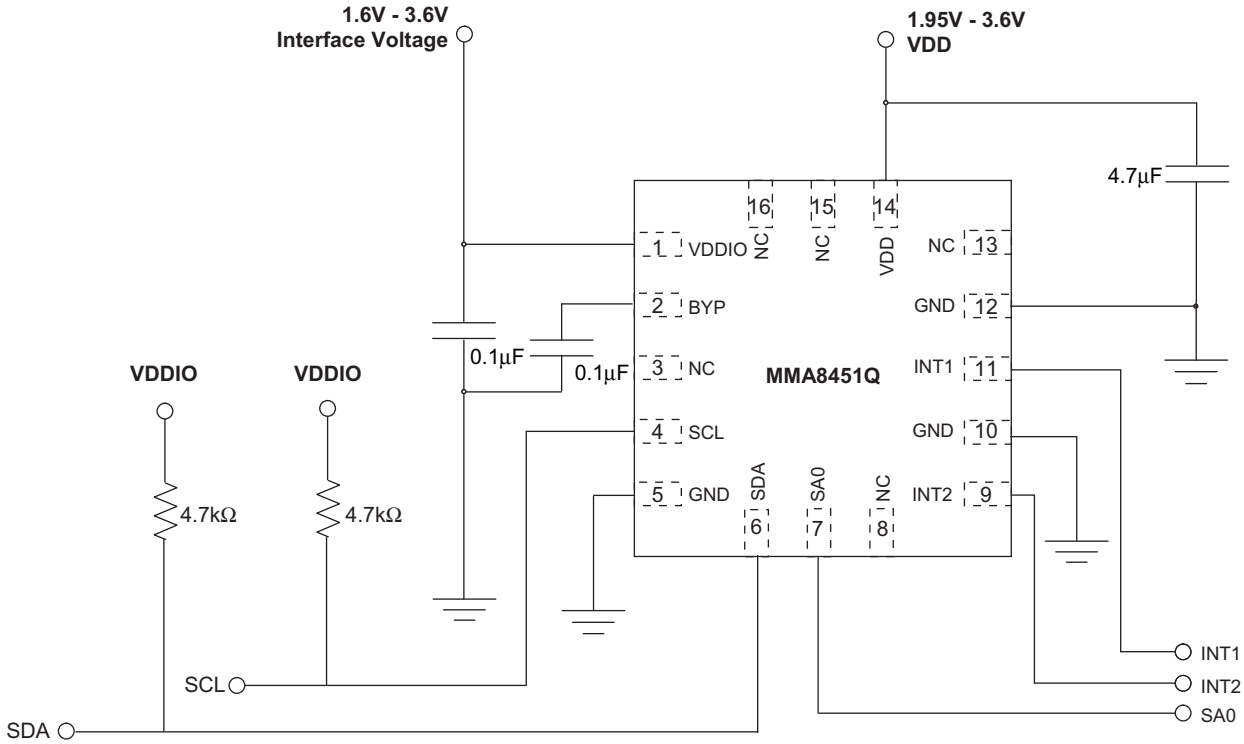


Figure 4. Application Diagram

Table 1. Pin Description

Pin #	Pin Name	Description	Pin Status
1	VDDIO	Internal Power Supply (1.62V - 3.6V)	Input
2	BYP	Bypass capacitor (0.1 µF)	Input
3	NC	Leave open. Do not connect	Open
4	SCL	I^2C Serial Clock	Open Drain
5	GND	Connect to Ground	Input
6	SDA	I^2C Serial Data	Open Drain
7	SA0	I^2C Least Significant Bit of the Device I^2C Address	Input
8	NC	Internally not connected (can be GND or VDD)	Input
9	INT2	Inertial Interrupt 2	Output
10	GND	Connect to Ground	Input
11	INT1	Inertial Interrupt 1	Output
12	GND	Connect to Ground	Input
13	NC	Internally not connected (can be GND or VDD)	Input
14	VDD	Power Supply (1.95V to 3.6V)	Input
15	NC	Internally not connected (can be GND or VDD)	Input
16	NC	Internally not connected (can be GND or VDD)	Input

The device power is supplied through VDD line. Power supply decoupling capacitors (100 nF ceramic plus 4.7 µF bulk, or a single 4.7 µF ceramic) should be placed as near as possible to the pins 1 and 14 of the device.

The control signals SCL, SDA, and SA0 are not tolerant of voltages more than VDDIO + 0.3V. If VDDIO is removed, the control signals SCL, SDA, and SA0 will clamp any logic signals with their internal ESD protection diodes.

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) are user programmable through the I^2C interface. The SDA and SCL I^2C connections are open drain and therefore require a pullup resistor as shown in the application diagram in Figure 4.

1.1 Soldering Information

The QFN package is compliant with the RoHS standard. Please refer to AN4077.

2 Mechanical and Electrical Specifications

2.1 Mechanical Characteristics

Table 2. Mechanical Characteristics @ VDD = 2.5V, VDDIO = 1.8V, T = 25°C unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Measurement Range(1)	FS[1:0] set to 00 2g Mode	FS		±2		g
	FS[1:0] set to 01 4g Mode			±4		
	FS[1:0] set to 10 8g Mode			±8		
Sensitivity	FS[1:0] set to 00 2g Mode	So		4096		counts/g
	FS[1:0] set to 01 4g Mode			2048		
	FS[1:0] set to 10 8g Mode			1024		
Sensitivity Accuracy(2)		Soa		±2.64		%
Sensitivity Change vs. Temperature	FS[1:0] set to 00 2g Mode	TCSo		±0.008		%/°C
	FS[1:0] set to 01 4g Mode					
	FS[1:0] set to 10 8g Mode					
Zero-g Level Offset Accuracy(3)	FS[1:0] 2g, 4g, 8g	TyOff		±17		mg
Zero-g Level Offset Accuracy Post Board Mount(4)	FS[1:0] 2g, 4g, 8g	TyOffPBM		±20		mg
Zero-g Level Change vs. Temperature	-40°C to 85°C	TCOff		±0.15		mg/°C
Self-Test Output Change(5) X Y Z	FS[1:0] set to 0 4g Mode	Vst		+181 +255 +1680		LSB
ODR Accuracy 2 MHz Clock				±2		%
Output Data Bandwidth		BW	ODR/3		ODR/2	Hz
Output Noise	Normal Mode ODR = 400 Hz	Noise		126		µg/√Hz
Output Noise Low Noise Mode(1)	Normal Mode ODR = 400 Hz	Noise		99		µg/√Hz
Operating Temperature Range		Top	-40		+85	°C

1. Dynamic Range is limited to 4g when the Low Noise bit in Register 0x2A, bit 2 is set.
2. Sensitivity remains in spec as stated, but changing Oversampling mode to Low Power causes 3% sensitivity shift. This behavior is also seen when changing from 800 Hz to any other data rate in the Normal, Low Noise + Low Power or High Resolution mode.
3. Before board mount.
4. Post Board Mount Offset Specifications are based on an 8 Layer PCB, relative to 25°C.
5. Self-Test is one direction only.

2.2 Electrical Characteristics

Table 3. Electrical Characteristics @ VDD = 2.5V, VDDIO = 1.8V, T = 25°C unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage		VDD(1)	1.95	2.5	3.6	V
Interface Supply Voltage		VDDIO(1)	1.62	1.8	3.6	V
Low Power Mode	ODR = 1.56 Hz	I_{dd}LP		6		µA
	ODR = 6.25 Hz			6		
	ODR = 12.5 Hz			6		
	ODR = 50 Hz			14		
	ODR = 100 Hz			24		
	ODR = 200 Hz			44		
	ODR = 400 Hz			85		
	ODR = 800 Hz			165		
Normal Mode	ODR = 1.56 Hz	I_{dd}		24		µA
	ODR = 6.25 Hz			24		
	ODR = 12.5 Hz			24		
	ODR = 50 Hz			24		
	ODR = 100 Hz			44		
	ODR = 200 Hz			85		
	ODR = 400 Hz			165		
	ODR = 800 Hz			165		
Current during Boot Sequence, 0.5 mSec max duration using recommended Bypass Cap	VDD = 2.5V	Idd Boot			1	mA
Value of Capacitor on BYP Pin	-40°C 85°C	Cap	75	100	470	nF
STANDBY Mode Current @25°C	VDD = 2.5V, VDDIO = 1.8V STANDBY Mode	I_{dd}Stby		1.8	5	µA
Digital High Level Input Voltage SCL, SDA, SA0		VIH	0.75*VDDIO			V
Digital Low Level Input Voltage SCL, SDA, SA0		VIL			0.3*VDDIO	V
High Level Output Voltage INT1, INT2	I_O = 500 µA	VOH	0.9*VDDIO			V
Low Level Output Voltage INT1, INT2	I_O = 500 µA	VOL			0.1*VDDIO	V
Low Level Output Voltage SDA	I_O = 500 µA	VOLS			0.1*VDDIO	V
Power on Ramp Time			0.001		1000	ms
Time from VDDIO on and VDD > Vmin until I^2C ready for operation	Cbyp = 100 nF	BT	—	350	500	µs
Turn-on time (STANDBY to ACTIVE)		Ton		2/ODR + 1 ms		s
Turn-on time (Power Down to ACTIVE Mode)		Ton		2/ODR + 2 ms		s
Operating Temperature Range		Top	-40		+85	°C

1. There is no requirement for power supply sequencing. The VDDIO input voltage can be higher than the VDD input voltage.

2.3 I²C interface characteristics

Table 4. I²C slave timing values(1)

Parameter	Symbol	I²C Fast Mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	0	400	kHz
Bus-free time between STOP and START condition	t_{BUF}	1.3		µs
(Repeated) START hold time	$t_{HD;STA}$	0.6		µs
Repeated START setup time	$t_{SU;STA}$	0.6		µs
STOP condition setup time	$t_{SU;STO}$	0.6		µs
SDA data hold time	$t_{HD;DAT}$	0.05	0.9 (2)	µs
SDA setup time	$t_{SU;DAT}$	100		ns
SCL clock low time	t_{LOW}	1.3		µs
SCL clock high time	t_{HIGH}	0.6		µs
SDA and SCL rise time	t_r	20 + 0.1 C_b(3)	300	ns
SDA and SCL fall time	t_f	20 + 0.1 C_b(3)	300	ns
SDA valid time (4)	$t_{VD;DAT}$		0.9 (2)	µs
SDA valid acknowledge time (5)	$t_{VD;ACK}$		0.9 (2)	µs
Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter	t_{SP}	0	50	ns
Capacitive load for each bus line	Cb		400	pF

1.All values referred to $V_{IH(min)}$ (0.3V_{DD}) and $V_{IL(max)}$ (0.7V_{DD}) levels.
2.This device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3.C_b = total capacitance of one bus line in pF.
4.$t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5.$t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

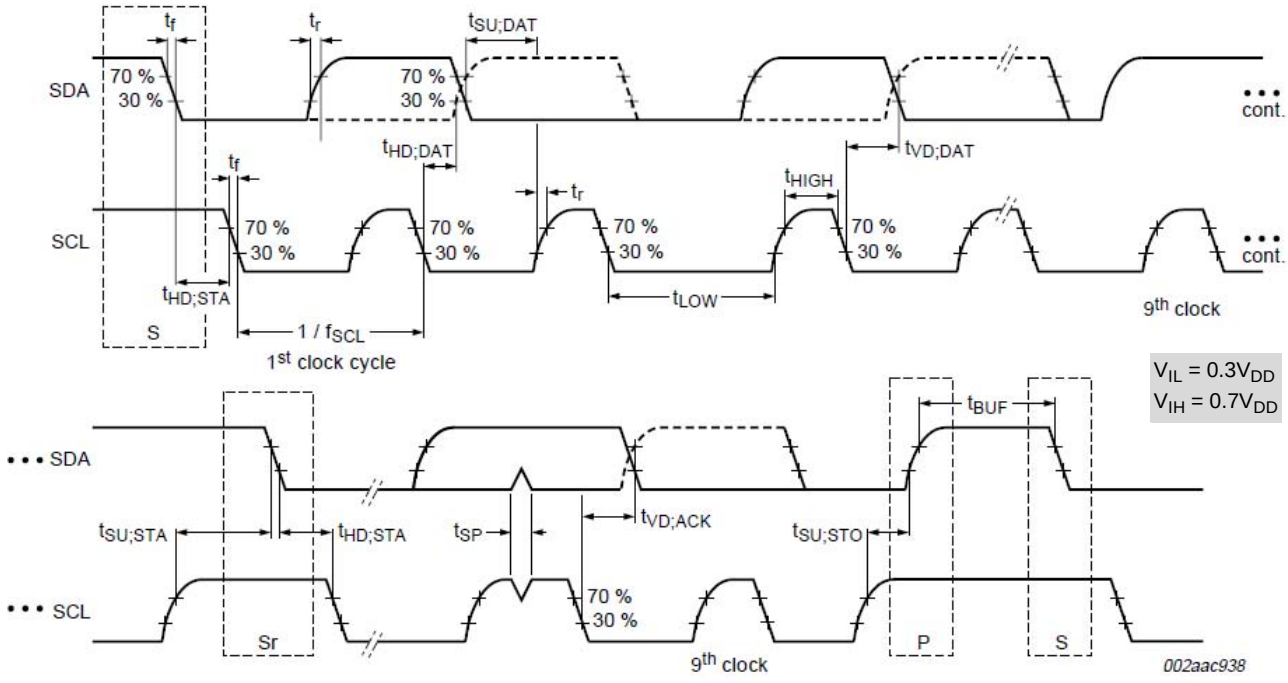


Figure 5. I²C slave timing diagram

2.4 Absolute Maximum Ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Acceleration (all axes, 100 μs)	g_{max}	5,000	g
Supply Voltage	VDD	-0.3 to + 3.6	V
Input voltage on any control pin (SA0, SCL, SDA)	Vin	-0.3 to VDDIO + 0.3	V
Drop Test	D_{drop}	1.8	m
Operating Temperature Range	T_{OP}	-40 to +85	°C
Storage Temperature Range	T_{STG}	-40 to +125	°C

Table 6. ESD and Latchup Protection Characteristics

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latchup Current at T = 85°C	—	±100	mA

This device is sensitive to mechanical shock. Improper handling can cause permanent damage of the part or cause the part to otherwise fail.

This device is sensitive to ESD, improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

The sensitivity is represented in counts/g. In 2g mode the sensitivity is 4096 counts/g. In 4g mode the sensitivity is 2048 counts/g and in 8g mode the sensitivity is 1024 counts/g.

3.2 Zero-g Offset

Zero-g Offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if the sensor is stationary. A sensor stationary on a horizontal surface will measure 0g in X-axis and 0g in Y-axis whereas the Z-axis will measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT Registers 0x00, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress on the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.

3.3 Self-Test

Self-Test checks the transducer functionality without external mechanical stimulus. When Self-Test is activated, an electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case, the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When Self-Test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

4 Modes of Operation

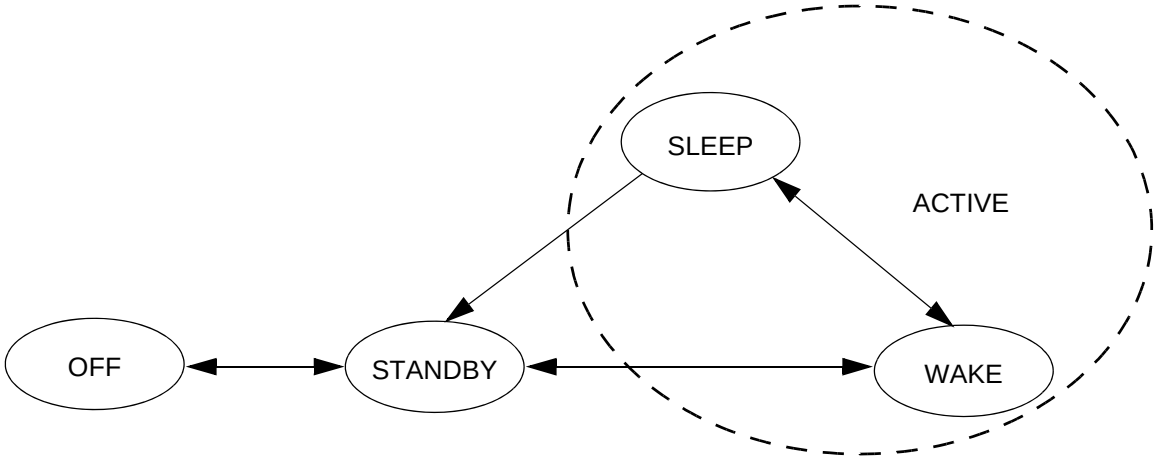


Figure 6. MMA8451Q Mode Transition Diagram

Table 7. Mode of Operation Description

Mode	I^2C Bus State	VDD	VDDIO	Function Description
OFF	Powered Down	<1.8V	VDDIO Can be > VDD	The device is powered off. All analog and digital blocks are shutdown. I^2C bus inhibited.
STANDBY	I^2C communication with MMA8451Q is possible	ON	VDDIO = High VDD = High ACTIVE bit is cleared	Only digital blocks are enabled. Analog subsystem is disabled. Internal clocks disabled.
ACTIVE (WAKE/SLEEP)	I^2C communication with MMA8451Q is possible	ON	VDDIO = High VDD = High ACTIVE bit is set	All blocks are enabled (digital, analog).

All register contents are preserved when transitioning from ACTIVE to STANDBY mode. Some registers are reset when transitioning from STANDBY to ACTIVE. These are all noted in the device memory map register table. The SLEEP and WAKE modes are ACTIVE modes. For more information on how to use the SLEEP and WAKE modes and how to transition between these modes, please refer to the functionality section of this document.

5 Functionality

The MMA8451Q is a low-power, digital output 3-axis linear accelerometer with a I^2C interface and embedded logic used to detect events and notify an external microprocessor over interrupt lines. The functionality includes the following:

- 8-bit or 14-bit data, High-Pass Filtered data, 8-bit or 14-bit configurable 32 sample FIFO
- Four different oversampling options for compromising between resolution and current consumption based on application requirements
- Additional Low Noise mode that functions independently of the Oversampling modes for higher resolution
- Low Power and Auto-WAKE/SLEEP modes for conservation of current consumption
- Single/Double tap with directional information 1 channel
- Motion detection with directional information or Freefall 1 channel
- Transient/Jolt detection based on a high-pass filter and settable threshold for detecting the change in acceleration above a threshold with directional information 1 channel
- Flexible user configurable portrait landscape detection algorithm addressing many use cases for screen orientation

All functionality is available in 2g, 4g or 8g dynamic ranges. There are many configuration settings for enabling all the different functions. Separate application notes have been provided to help configure the device for each embedded functionality.

Table 8. Features of the MMA845xQ devices

Feature List	MMA8451	MMA8452	MMA8453
Digital Resolution (Bits)	14	12	10
Digital Sensitivity (Counts/g)	4096	1024	256
Data-Ready Interrupt	Yes	Yes	Yes
Single-Pulse Interrupt	Yes	Yes	Yes
Double-Pulse Interrupt	Yes	Yes	Yes
Directional-Pulse Interrupt	Yes	Yes	Yes
Auto-WAKE	Yes	Yes	Yes
Auto-SLEEP	Yes	Yes	Yes
Freefall Interrupt	Yes	Yes	Yes
32 Level FIFO	Yes	No	No
High-Pass Filter	Yes	Yes	Yes
Low-Pass Filter	Yes	Yes	Yes
Orientation Detection Portrait/Landscape = 30°, Landscape to Portrait = 60°, and Fixed 45° Threshold	Yes	Yes	Yes
Programmable Orientation Detection	Yes	No	No
Motion Interrupt with Direction	Yes	Yes	Yes
Transient Detection with High-Pass Filter	Yes	Yes	Yes
Low Power Mode	Yes	Yes	Yes

5.1 Device Calibration

The device interface is factory calibrated for sensitivity and Zero-g offset for each axis. The trim values are stored in Non Volatile Memory (NVM). On power-up, the trim parameters are read from NVM and applied to the circuitry. In normal use, further calibration in the end application is not necessary. However, the MMA8451Q allows the user to adjust the Zero-g offset for each axis after power-up, changing the default offset values. The user offset adjustments are stored in 6 volatile registers. For more information on device calibration, refer to Freescale application note, AN4069.

5.2 8-bit or 14-bit Data

The measured acceleration data is stored in the OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB registers as 2's complement 14-bit numbers. The most significant 8-bits of each axis are stored in OUT_X (Y, Z)_MSB, so applications needing only 8-bit results can use these 3 registers and ignore OUT_X,Y, Z_LSB. To do this, the F_READ bit in CTRL_REG1 must be set. When the F_READ bit is cleared, the fast read mode is disabled.

When the full-scale is set to 2g, the measurement range is -2g to +1.99975g, and each count corresponds to 1g/4096 (0.25 mg) at 14-bits resolution. When the full-scale is set to 8g, the measurement range is -8g to +7.999g, and each count corresponds to 1g/1024 (0.98 mg) at 14-bits resolution. The resolution is reduced by a factor of 64 if only the 8-bit results are used. For more information on the data manipulation between data formats and modes, refer to Freescale application.

5.3 Internal FIFO Data Buffer

MMA8451Q contains a 32 sample internal FIFO data buffer minimizing traffic across the I^2C bus. The FIFO can also provide power savings of the system by allowing the host processor/MCU to go into a SLEEP mode while the accelerometer independently stores the data, up to 32 samples per axis. The FIFO can run at all output data rates. There is the option of accessing the full 14-bit data or for accessing only the 8-bit data. When access speed is more important than high resolution the 8-bit data read is a better option.

The FIFO contains four modes (Fill Buffer Mode, Circular Buffer Mode, Trigger Mode, and Disabled Mode) described in the F_SETUP Register 0x09. Fill Buffer Mode collects the first 32 samples and asserts the overflow flag when the buffer is full and another sample arrives. It does not collect any more data until the buffer is read. This benefits data logging applications where all samples must be collected. The Circular Buffer Mode allows the buffer to be filled and then new data replaces the oldest sample in the buffer. The most recent 32 samples will be stored in the buffer. This benefits situations where the processor is waiting for an specific interrupt to signal that the data must be flushed to analyze the event. The trigger mode will hold the last data up to the point when the trigger occurs and can be set to keep a selectable number of samples after the event occurs.

The MMA8451Q FIFO Buffer has a configurable watermark, allowing the processor to be triggered after a configurable number of samples has filled in the buffer (1 to 32).

For details on the configurations for the FIFO buffer as well as more specific examples and application benefits, refer to Freescale application note, AN4073.

5.4 Low Power Modes vs. High Resolution Modes

The MMA8451Q can be optimized for lower power modes or for higher resolution of the output data. High resolution is achieved by setting the LNOISE bit in Register 0x2A. This improves the resolution but be aware that the dynamic range is limited to 4g when this bit is set. This will affect all internal functions and reduce noise. Another method for improving the resolution of the data is by oversampling. One of the oversampling schemes of the data can activated when MODS = 10 in Register 0x2B which will improve the resolution of the output data only. The highest resolution is achieved at 1.56 Hz.

There is a trade-off between low power and high resolution. Low Power can be achieved when the oversampling rate is reduced. The lowest power is achieved when MODS = 11 or when the sample rate is set to 1.56 Hz. For more information on how to configure the MMA8451Q in Low Power mode or High Resolution mode and to realize the benefits, refer to Freescale application note, AN4075.

5.5 Auto-WAKE/SLEEP Mode

The MMA8451Q can be configured to transition between sample rates (with their respective current consumption) based on four of the interrupt functions of the device. The advantage of using the Auto-WAKE/SLEEP is that the system can automatically transition to a higher sample rate (higher current consumption) when needed but spends the majority of the time in the SLEEP mode (lower current) when the device does not require higher sampling rates. Auto-WAKE refers to the device being triggered by one of the interrupt functions to transition to a higher sample rate. This may also interrupt the processor to transition from a SLEEP mode to a higher power mode.

SLEEP mode occurs after the accelerometer has not detected an interrupt for longer than the user definable time-out period. The device will transition to the specified lower sample rate. It may also alert the processor to go into a lower power mode to save on current during this period of inactivity.

The Interrupts that can WAKE the device from SLEEP are the following: Tap Detection, Orientation Detection, Motion/Freefall, and Transient Detection. The FIFO can be configured to hold the data in the buffer until it is flushed if the FIFO Gate bit is set in Register 0x2C but the FIFO cannot WAKE the device from SLEEP.

The interrupts that can keep the device from falling asleep are the same interrupts that can wake the device with the addition of the FIFO. If the FIFO interrupt is enabled and data is being accessed continually servicing the interrupt then the device will remain in the WAKE mode. Refer to AN4074, for more detailed information for configuring the Auto-WAKE/SLEEP.

5.6 Freefall and Motion Detection

MMA8451Q has flexible interrupt architecture for detecting either a Freefall or a Motion. Freefall can be enabled where the set threshold must be less than the configured threshold, or motion can be enabled where the set threshold must be greater than the threshold. The motion configuration has the option of enabling or disabling a high-pass filter to eliminate tilt data (static offset). The freefall does not use the high-pass filter. For details on the Freefall and Motion detection with specific application examples and recommended configuration settings, refer to Freescale application note, AN4070.

5.6.1 Freefall Detection

The detection of “Freefall” involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is **below** a user specified threshold for a user definable amount of time. Normally, the usable threshold ranges are between ±100 mg and ±500 mg.

5.6.2 Motion Detection

Motion is often used to simply alert the main processor that the device is currently in use. When the acceleration exceeds a set threshold the motion interrupt is asserted. A motion can be a fast moving shake or a slow moving tilt. This will depend on the threshold and timing values configured for the event. The motion detection function can analyze static acceleration changes or faster jolts. For example, to detect that an object is spinning, all three axes would be enabled with a threshold detection of > 2g. This condition would need to occur for a minimum of 100 ms to ensure that the event wasn't just noise. The timing value is set by a configurable debounce counter. The debounce counter acts like a filter to determine whether the condition exists for configurable set of time (i.e., 100 ms or longer). There is also directional data available in the source register to detect the direction of the motion. This is useful for applications such as directional shake or flick, which assists with the algorithm for various gesture detections.

5.7 Transient Detection

The MMA8451Q has a built-in high-pass filter. Acceleration data goes through the high-pass filter, eliminating the offset (DC) and low frequencies. The high-pass filter cutoff frequency can be set by the user to four different frequencies which are dependent on the Output Data Rate (ODR). A higher cutoff frequency ensures the DC data or slower moving data will be filtered out, allowing only the higher frequencies to pass. The embedded Transient Detection function uses the high-pass filtered data allowing the user to set the threshold and debounce counter. The transient detection feature can be used in the same manner as the motion detection by bypassing the high-pass filter. There is an option in the configuration register to do this. This adds more flexibility to cover various customer use cases.

Many applications use the accelerometer’s static acceleration readings (i.e., tilt) which measure the change in acceleration due to gravity only. These functions benefit from acceleration data being filtered with a low-pass filter where high frequency data is considered noise. However, there are many functions where the accelerometer must analyze dynamic acceleration. Functions such as tap, flick, shake and step counting are based on the analysis of the change in the acceleration. It is simpler to interpret these functions dependent on dynamic acceleration data when the static component has been removed. The Transient Detection function can be routed to either interrupt pin through bit 5 in CTRL_REG5 register (0x2E). Registers 0x1D – 0x20 are the dedicated Transient Detection configuration registers. The source register contains directional data to determine the direction of the acceleration, either positive or negative. For details on the benefits of the embedded Transient Detection function along with specific application examples and recommended configuration settings, please refer to Freescale application note, AN4071.

5.8 Tap Detection

The MMA8451Q has embedded single/double and directional tap detection. This function has various customizing timers for setting the pulse time width and the latency time between pulses. There are programmable thresholds for all three axes. The tap detection can be configured to run through the high-pass filter and also through a low-pass filter, which provides more customizing and tunable tap detection schemes. The status register provides updates on the axes where the event was detected and the direction of the tap. For more information on how to configure the device for tap detection please refer to Freescale application note, AN4072.

5.9 Orientation Detection

The MMA8451Q incorporates an advanced algorithm for orientation detection (ability to detect all 6 orientations) with configurable trip points. The embedded algorithm allows the selection of the mid point with the desired hysteresis value.

The MMA8451Q Orientation Detection algorithm confirms the reliability of the function with a configurable Z-lockout angle. Based on known functionality of linear accelerometers, it is not possible to rotate the device about the Z-axis to detect change in acceleration at slow angular speeds. The angle at which the device no longer detects the orientation change is referred to as the “Z-Lockout angle”. The device operates down to 14° from the flat position.

For further information on the configuration settings of the orientation detection function, including recommendations for configuring the device to support various application use cases, refer to Freescale application note, AN4068.

Figure 8 shows the definitions of the trip angles going from Landscape to Portrait (A) and then also from Portrait to Landscape (B).

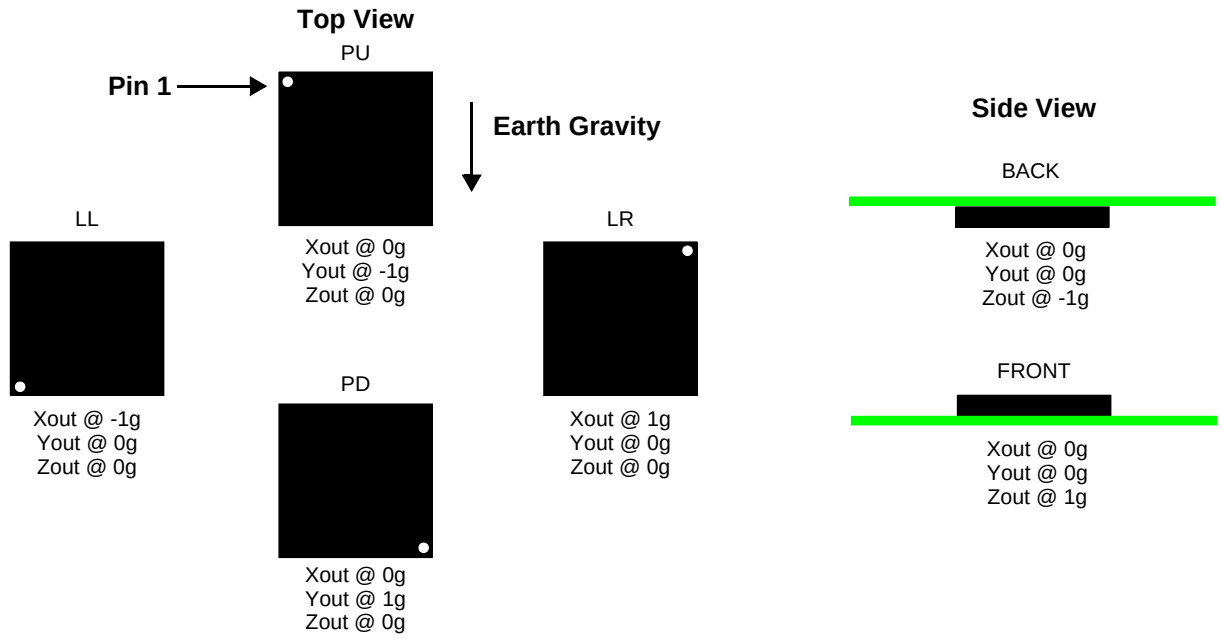


Figure 7. Landscape/Portrait Orientation

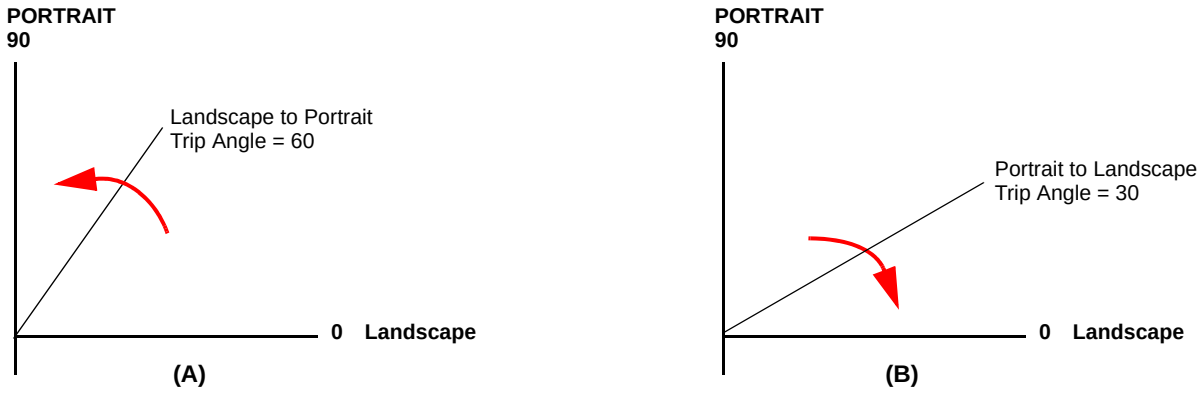


Figure 8. Illustration of Landscape to Portrait Transition (A) and Portrait to Landscape Transition (B)

Figure 9 illustrates the Z-angle lockout region. When lifting the device upright from the flat position it will be active for orientation detection as low as14° from flat. This is user configurable. The default angle is 29° but it can be set as low as 14°.
.

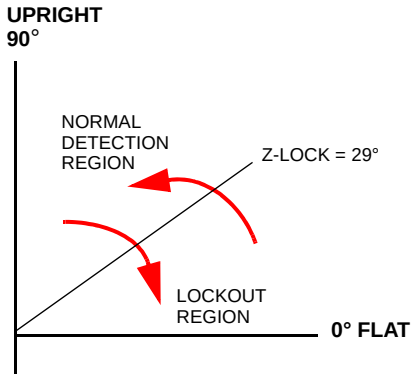


Figure 9. Illustration of Z-Tilt Angle Lockout Transition

5.10 Interrupt Register Configurations

There are seven configurable interrupts in the MMA8451Q: Data Ready, Motion/Freefall, Tap (Pulse), Orientation, Transient, FIFO and Auto-SLEEP events. These seven interrupt sources can be routed to one of two interrupt pins. The interrupt source must be enabled and configured. If the event flag is asserted because the event condition is detected, the corresponding interrupt pin, INT1 or INT2, will assert.

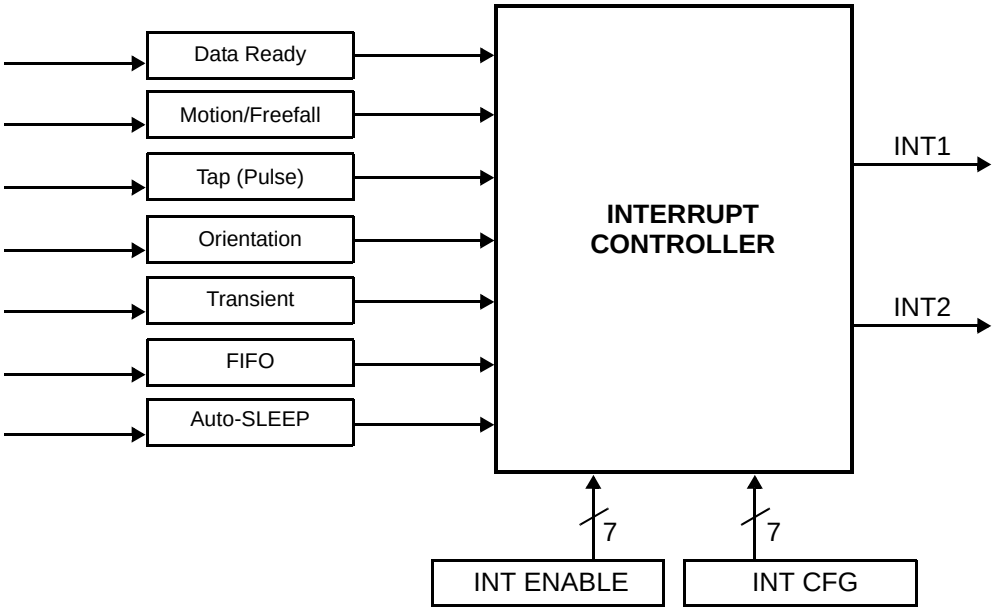


Figure 10. System Interrupt Generation Block Diagram

5.11 Serial I²C Interface

Acceleration data may be accessed through an I²C interface thus making the device particularly suitable for direct interfacing with a microcontroller. The MMA8451Q features an interrupt signal which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device. The MMA8451Q may also be configured to generate other interrupt signals accordingly to the programmable embedded functions of the device for Motion, Freefall, Transient, Orientation, and Tap.

The registers embedded inside the MMA8451Q are accessed through the I²C serial interface (Table 9). To enable the I²C interface, VDDIO line must be tied high (i.e., to the interface supply voltage). If VDD is not present and VDDIO is present, the

MMA8451Q is in off mode and communications on the I^2C interface are ignored. The I^2C interface may be used for communications between other I^2C devices and the MMA8451Q does not affect the I^2C bus.

Table 9. Serial Interface Pin Description

Pin Name	Pin Description
SCL	I^2C Serial Clock
SDA	I^2C Serial Data
SA0	I^2C least significant bit of the device address

There are two signals associated with the I^2C bus; the Serial Clock Line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are expected for SDA and SCL. When the bus is free both the lines are high. The I^2C interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) I^2C standards (Table 4).

5.11.1 I^2C Operation

The transaction on the bus is started through a start condition (START) signal. START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After START has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after START contains the slave address in the first 7 bits, and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master. The 9th clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

A LOW to HIGH transition on the SDA line while the SCL line is high is defined as a stop condition (STOP). A data transfer is always terminated by a STOP. A Master may also issue a repeated START during a data transfer. The MMA8451Q expects repeated STARTs to be used to randomly read from specific registers.

The MMA8451Q's standard slave address is a choice between the two sequential addresses 0011100 and 0011101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are factory programmed and alternate addresses are available at customer request. The format is shown in Table 10.

Table 10. I^2C Address Selection Table

Slave Address (SA0 = 0)	Slave Address (SA0 = 1)	Comment
0011100 (0x1C)	0011101 (0x1D)	Factory Default

Single Byte Read

The MMA8451Q has an internal ADC that can sample, convert and return sensor data on request. The transmission of an 8-bit command begins on the falling edge of SCL. After the eight clock cycles are used to send the command, note that the data returned is sent with the MSB first once the data is received. Figure 11 shows the timing diagram for the accelerometer 8-bit I^2C read operation. The Master (or MCU) transmits a start condition (ST) to the MMA8451Q, slave address ($1D), with the R/W bit set to “0” for a write, and the MMA8451Q sends an acknowledgement. Then the Master (or MCU) transmits the address of the register to read and the MMA8451Q sends an acknowledgement. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA8451Q ($1D) with the R/W bit set to “1” for a read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

Multiple Byte Read

When performing a multi-byte read or “burst read”, the MMA8451Q automatically increments the received register address commands after a read command is received. Therefore, after following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each MMA8451Q acknowledgment (AK) is received until a no acknowledge (NAK) occurs from the Master followed by a stop condition (SP) signaling an end of transmission.

Single Byte Write

To start a write command, the Master transmits a start condition (ST) to the MMA8451Q, slave address ($1D) with the R/W bit set to “0” for a write, the MMA8451Q sends an acknowledgement. Then the Master (MCU) transmits the address of the register to write to, and the MMA8451Q sends an acknowledgement. Then the Master (or MCU) transmits the 8-bit data to write to the designated register and the MMA8451Q sends an acknowledgement that it has received the data. Since this transmission is

complete, the Master transmits a stop condition (SP) to the data transfer. The data sent to the MMA8451Q is now stored in the appropriate register.

Multiple Byte Write

The MMA8451Q automatically increments the received register address commands after a write command is received. Therefore, after following the steps of a single byte write, multiple bytes of data can be written to sequential registers after each MMA8451Q acknowledgment (ACK) is received.

Table 11. I²C Device Address Sequence

Command	[6:1] Device Address	[0] SA0	[6:0] Device Address	R/W	8-bit Final Value
Read	001110	0	0x1C	1	0x39
Write	001110	0	0x1C	0	0x38
Read	001110	1	0x1D	1	0x3B
Write	001110	1	0x1D	0	0x3A

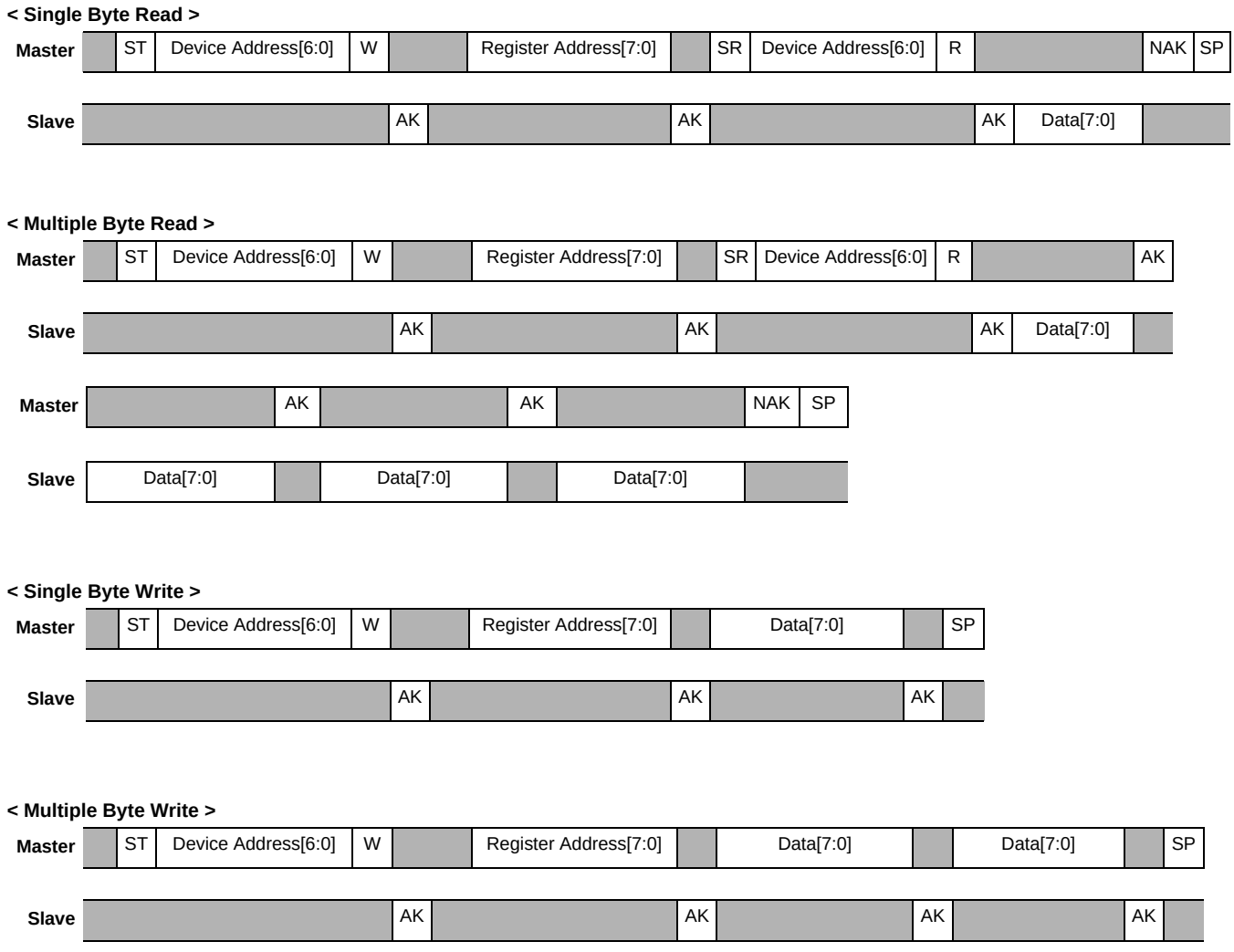


Figure 11. I²C Timing Diagram

6 Register Descriptions

Table 12. Register Address Map

Name	Type	Register Address	Auto-Increment Address				Default	Hex Value	Comment
			FMODE = 0 F_READ = 0	FMODE > 0 F_READ = 0	FMODE = 0 F_READ = 1	FMODE > 0 F_READ = 1			
STATUS/F_STATUS(1)(2)	R	0x00	0x01				00000000	0x00	FMODE = 0, real time status FMODE > 0, FIFO status
OUT_X_MSB(1)(2)	R	0x01	0x02	0x01	**0x03**	**0x01**	Output	—	[7:0] are 8 MSBs of 14-bit sample. / Root pointer to XYZ FIFO data.
OUT_X_LSB(1)(2)	R	0x02	0x03		**0x00**		Output	—	[7:2] are 6 LSBs of 14-bit real-time sample
OUT_Y_MSB(1)(2)	R	0x03	0x04		**0x05**	**0x00**	Output	—	[7:0] are 8 MSBs of 14-bit real-time sample
OUT_Y_LSB(1)(2)	R	0x04	0x05		**0x00**		Output	—	[7:2] are 6 LSBs of 14-bit real-time sample
OUT_Z_MSB(1)(2)	R	0x05	0x06		**0x00**		Output	—	[7:0] are 8 MSBs of 14-bit real-time sample
OUT_Z_LSB(1)(2)	R	0x06	**0x00**				Output	—	[7:2] are 6 LSBs of 14-bit real-time sample
Reserved	R	0x07	—	—	—	—	—	—	Reserved. Read return 0x00.
Reserved	R	0x08	—	—	—	—	—	—	Reserved. Read return 0x00.
F_SETUP(1)(3)	R/W	0x09	0x0A				00000000	0x00	FIFO setup
TRIG_CFG(1)(4)	R/W	0x0A	0x0B				00000000	0x00	Map of FIFO data capture events
SYSMOD(1)(2)	R	0x0B	0x0C				00000000	0x00	Current System Mode
INT_SOURCE(1)(2)	R	0x0C	0x0D				00000000	0x00	Interrupt status
WHO_AM_I(1)	R	0x0D	0x0E				00011010	0x1A	Device ID (0x1A)
XYZ_DATA_CFG(1)(4)	R/W	0x0E	0x0F				00000000	0x00	Dynamic Range Settings
HP_FILTER_CUTOFF(1)(4)	R/W	0x0F	0x10				00000000	0x00	Cutoff frequency is set to 16 Hz @ 800 Hz
PL_STATUS(1)(2)	R	0x10	0x11				00000000	0x00	Landscape/Portrait orientation status
PL_CFG (1)(4)	R/W	0x11	0x12				10000000	0x80	Landscape/Portrait configuration.
PL_COUNT(1)(3)	R/W	0x12	0x13				00000000	0x00	Landscape/Portrait debounce counter
PL_BF_ZCOMP(1)(4)	R/W	0x13	0x14				01000100	0x44	Back/Front, Z-Lock Trip threshold
P_L_THS_REG(1)(4)	R/W	0x14	0x15				10000100	0x84	Portrait to Landscape Trip Angle is 29°
FF_MT_CFG(1)(4)	R/W	0x15	0x16				00000000	0x00	Freefall/Motion functional block configuration
FF_MT_SRC(1)(2)	R	0x16	0x17				00000000	0x00	Freefall/Motion event source register
FF_MT_THS(1)(3)	R/W	0x17	0x18				00000000	0x00	Freefall/Motion threshold register
FF_MT_COUNT(1)(3)	R/W	0x18	0x19				00000000	0x00	Freefall/Motion debounce counter
Reserved	R	0x19	—	—	—	—	—	—	Reserved. Read return 0x00.
Reserved	R	0x1A	—	—	—	—	—	—	Reserved. Read return 0x00.
Reserved	R	0x1B	—	—	—	—	—	—	Reserved. Read return 0x00.
Reserved	R	0x1C	—	—	—	—	—	—	Reserved. Read return 0x00.
TRANSIENT_CFG(1)(4)	R/W	0x1D	0x1E				00000000	0x00	Transient functional block configuration
TRANSIENT_SCR(1)(2)	R	0x1E	0x1F				00000000	0x00	Transient event status register

Table 12. Register Address Map

TRANSIENT_THS(1)(3)	R/W	0x1F	0x20	00000000	0x00	Transient event threshold
TRANSIENT_COUNT(1)(3)	R/W	0x20	0x21	00000000	0x00	Transient debounce counter
PULSE_CFG(1)(4)	R/W	0x21	0x22	00000000	0x00	ELE, Double_XYZ or Single_XYZ
PULSE_SRC(1)(2)	R	0x22	0x23	00000000	0x00	EA, Double_XYZ or Single_XYZ
PULSE_THSX(1)(3)	R/W	0x23	0x24	00000000	0x00	X pulse threshold
PULSE_THSY(1)(3)	R/W	0x24	0x25	00000000	0x00	Y pulse threshold
PULSE_THSZ(1)(4)	R/W	0x25	0x26	00000000	0x00	Z pulse threshold
PULSE_TMLT(1)(4)	R/W	0x26	0x27	00000000	0x00	Time limit for pulse
PULSE_LTCY(1)(4)	R/W	0x27	0x28	00000000	0x00	Latency time for 2nd pulse
PULSE_WIND(1)(4)	R/W	0x28	0x29	00000000	0x00	Window time for 2nd pulse
ASLP_COUNT(1)(4)	R/W	0x29	0x2A	00000000	0x00	Counter setting for Auto-SLEEP
CTRL_REG1(1)(4)	R/W	0x2A	0x2B	00000000	0x00	ODR = 800 Hz, STANDBY Mode.
CTRL_REG2(1)(4)	R/W	0x2B	0x2C	00000000	0x00	Sleep Enable, OS Modes, RST, ST
CTRL_REG3(1)(4)	R/W	0x2C	0x2D	00000000	0x00	Wake from Sleep, IPOL, PP_OD
CTRL_REG4(1)(4)	R/W	0x2D	0x2E	00000000	0x00	Interrupt enable register
CTRL_REG5(1)(4)	R/W	0x2E	0x2F	00000000	0x00	Interrupt pin (INT1/INT2) map
OFF_X(1)(4)	R/W	0x2F	0x30	00000000	0x00	X-axis offset adjust
OFF_Y(1)(4)	R/W	0x30	0x31	00000000	0x00	Y-axis offset adjust
OFF_Z(1)(4)	R/W	0x31	**0x0D**	00000000	0x00	Z-axis offset adjust
Reserved (do not modify)		0x40 – 7F	—	—	—	Reserved. Read return 0x00.

1. Register contents are preserved when transition from ACTIVE to STANDBY mode occurs.
2. Register contents are reset when transition from STANDBY to ACTIVE mode occurs.
3. Register contents can be modified anytime in STANDBY or ACTIVE mode. A write to this register will cause a reset of the corresponding internal system debounce counter.
4. Modification of this register's contents can only occur when device is STANDBY mode except CTRL_REG1 ACTIVE bit and CTRL_REG2 RST bit.

Note: Auto-increment addresses which are not a simple increment are highlighted in **bold**. The auto-increment addressing is only enabled when device registers are read using I^2C burst read mode. Therefore the internal storage of the auto-increment address is cleared whenever a stop-bit is detected.

6.1 Data Registers

The following are the data registers for the MMA8451Q. For more information on data manipulation of the MMA8451Q, refer to application note, AN4076.

When the F_MODE bits found in Register 0x09 (F_SETUP), bits 7 and 6 are both cleared (the FIFO is not on). Register 0x00 reflects the real-time status information of the X, Y and Z sample data. When the F_MODE value is greater than zero the FIFO is on (in either Fill, Circular or Trigger mode). In this case Register 0x00 will reflect the status of the FIFO. It is expected when the FIFO is on that the user will access the data from Register 0x01 (X_MSB) for either the 14-bit or 8-bit data. When accessing the 8-bit data the F_READ bit (Register 0x2A) is set which modifies the auto-incrementing to skip over the LSB data. When F_READ bit is cleared the 14-bit data is read accessing all 6 bytes sequentially (X_MSB, X_LSB, Y_MSB, Y_LSB, Z_MSB, Z_LSB).

F_MODE = 00: 0x00 STATUS: Data Status Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR

Table 13. STATUS Description

ZYXOW	X, Y, Z-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous X, Y, or Z data was overwritten by new X, Y, or Z data before it was read
ZOW	Z-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous Z-axis data was overwritten by new Z-axis data before it was read
YOW	Y-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous Y-axis data was overwritten by new Y-axis data before it was read
XOW	X-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous X-axis data was overwritten by new X-axis data before it was read
ZYXDR	X, Y, Z-axis new Data Ready. Default value: 0 0: No new set of data ready 1: A new set of data is ready
ZDR	Z-axis new Data Available. Default value: 0 0: No new Z-axis data is ready 1: A new Z-axis data is ready
YDR	Y-axis new Data Available. Default value: 0 0: No new Y-axis data ready 1: A new Y-axis data is ready
XDR	X-axis new Data Available. Default value: 0 0: No new X-axis data ready 1: A new X-axis data is ready

ZYXOW is set whenever a new acceleration data is produced before completing the retrieval of the previous set. This event occurs when the content of at least one acceleration data register (i.e., OUT_X, OUT_Y, OUT_Z) has been overwritten. ZYXOW is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the active channels are read.

ZOW is set whenever a new acceleration sample related to the Z-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. ZOW is cleared anytime OUT_Z_MSB register is read.

YOW is set whenever a new acceleration sample related to the Y-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. YOW is cleared anytime OUT_Y_MSB register is read.

XOW is set whenever a new acceleration sample related to the X-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. XOW is cleared anytime OUT_X_MSB register is read.

ZYXDR signals that a new sample for any of the enabled channels is available. ZYXDR is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the enabled channels are read.

ZDR is set whenever a new acceleration sample related to the Z-axis is generated. ZDR is cleared anytime OUT_Z_MSB register is read.

YDR is set whenever a new acceleration sample related to the Y-axis is generated. YDR is cleared anytime OUT_Y_MSB register is read.

XDR is set whenever a new acceleration sample related to the X-axis is generated. XDR is cleared anytime OUT_X_MSB register is read.

Data Registers: 0x01 OUT_X_MSB, 0x02 OUT_X_LSB, 0x03 OUT_Y_MSB, 0x04 OUT_Y_LSB, 0x05 OUT_Z_MSB, 0x06 OUT_Z_LSB

These registers contain the X-axis, Y-axis, and Z-axis14-bit output sample data expressed as 2's complement numbers.

Note: The sample data output registers store the current sample data if the FIFO data output register driver is disabled, but if the FIFO data output register driver is enabled (F_MODE > 00) the sample data output registers point to the head of the FIFO buffer (Register 0x01 X_MSB) which contains the previous 32 X, Y, and Z data samples. Data Registers F_MODE = 00

0x01: OUT_X_MSB: X_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD13	XD12	XD11	XD10	XD9	XD8	XD7	XD6

0x02: OUT_X_LSB: X_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD5	XD4	XD3	XD2	XD1	XD0	0	0

0x03: OUT_Y_MSB: Y_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD13	YD12	YD11	YD10	YD9	YD8	YD7	YD6

0x04: OUT_Y_LSB: Y_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD5	YD4	YD3	YD2	YD1	YD0	0	0

0x05: OUT_Z_MSB: Z_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD13	ZD12	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6

0x06: OUT_Z_LSB: Z_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD5	ZD4	ZD3	ZD2	ZD1	ZD0	0	0

OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the auto-incrementing address range of 0x01 to 0x06 to reduce reading the status followed by 14-bit axis data to 7 bytes. If the F_READ bit is set (0x2A bit 1), auto increment will skip over LSB registers. This will shorten the data acquisition from 7 bytes to 4 bytes. The LSB registers can only be read immediately following the read access of the corresponding MSB register. A random read access to the LSB registers is not possible. Reading the MSB register and then the LSB register in sequence ensures that both bytes (LSB and MSB) belong to the same data sample, even if a new data sample arrives between reading the MSB and the LSB byte.

6.2 32 Sample FIFO

The following registers are used to configure the FIFO. For more information on the FIFO please refer to AN4073.

F_MODE > 0 0x00: F_STATUS FIFO Status Register

When F_MODE > 0, Register 0x00 becomes the FIFO Status Register which is used to retrieve information about the FIFO. This register has a flag for the overflow and watermark. It also has a counter that can be read to obtain the number of samples stored in the buffer when the FIFO is enabled.

0x00: F_STATUS: FIFO STATUS Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_OVF	F_WMRK_FLAG	F_CNT5	F_CNT4	F_CNT3	F_CNT2	F_CNT1	F_CNT0

Table 14. FIFO Flag Event Description

F_OVF	F_WMRK_FLAG	Event Description
0	—	No FIFO overflow events detected.
1	—	FIFO event detected; FIFO has overflowed.
—	0	No FIFO watermark events detected.
—	1	FIFO Watermark event detected. FIFO sample count is greater than watermark value. If F_MODE = 11, Trigger Event detected.

The F_OVF and F_WMRK_FLAG flags remain asserted while the event source is still active, but the user can clear the FIFO interrupt bit flag in the interrupt source register (INT_SOURCE) by reading the F_STATUS register. In this case, the SRC_FIFO bit in the INT_SOURCE register will be set again when the next data sample enters the FIFO. Therefore the F_OVF bit flag will remain asserted while the FIFO has overflowed and the F_WMRK_FLAG bit flag will remain asserted while the F_CNT value is equal to or greater than then F_WMRK value. If the FIFO overflow flag is cleared and if F_MODE = 11 then the FIFO overflow flag will remain 0 before the trigger event even if the FIFO is full and overflows. If the FIFO overflow flag is set and if F_MODE is = 11, the FIFO has stopped accepting samples.

Table 15. FIFO Sample Count Description

F_CNT[5:0]	FIFO sample counter. Default value: 00_0000. (00_0001 to 10_0000 indicates 1 to 32 samples stored in FIFO

F_CNT[5:0] bits indicate the number of acceleration samples currently stored in the FIFO buffer. Count 000000 indicates that the FIFO is empty.

0x09: F_SETUP FIFO Setup Register

0x09 F_SETUP: FIFO Setup Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_MODE1	F_MODE0	F_WMRK5	F_WMRK4	F_WMRK3	F_WMRK2	F_WMRK1	F_WMRK0

Table 16. F_SETUP Description

BITS	Description
F_MODE[1:0](1)(2)	FIFO buffer overflow mode. Default value: 0. **00:** FIFO is disabled. **01:** FIFO contains the most recent samples when overflowed (circular buffer). Oldest sample is discarded to be replaced by new sample. **10:** FIFO stops accepting new samples when overflowed. **11:** Trigger mode. The FIFO will be in a circular mode up to the number of samples in the watermark. The FIFO will be in a circular mode until the trigger event occurs after that the FIFO will continue to accept samples for 32-WMRK samples and then stop receiving further samples. This allows data to be collected both before and after the trigger event and it is definable by the watermark setting. The FIFO is flushed whenever the FIFO is disabled, during an automatic ODR change (Auto-WAKE/SLEEP), or transitioning from STANDBY mode to ACTIVE mode. Disabling the FIFO (F_MODE = 00) resets the F_OVF, F_WMRK_FLAG, F_CNT to zero. A FIFO overflow event (i.e., F_CNT = 32) will assert the F_OVF flag and a FIFO sample count equal to the sample count watermark (i.e., F_WMRK) asserts the F_WMRK_FLAG event flag.
F_WMRK[5:0](2)	FIFO Event Sample Count Watermark. Default value: 00_0000. These bits set the number of FIFO samples required to trigger a watermark interrupt. A FIFO watermark event flag is raised when FIFO sample count F_CNT[5:0] ≥ F_WMRK[5:0] watermark. Setting the F_WMRK[5:0] to 00_0000 will disable the FIFO watermark event flag generation. Also used to set the number of pre-trigger samples in Trigger mode.

1. Bit field can be written in ACTIVE mode.
2. Bit field can be written in STANDBY mode.

The FIFO mode can be changed while in the active state. The mode must first be disabled F_MODE = 00 then the mode can be switched between Fill mode, Circular mode and Trigger mode.

A FIFO sample count exceeding the watermark event does not stop the FIFO from accepting new data. The FIFO update rate is dictated by the selected system ODR. In ACTIVE mode the ODR is set by the DR bits in the CTRL_REG1 register. When Auto-SLEEP is active the ODR is set by the ASLP_RATE field in the CTRL_REG1 register.

When a byte is read from the FIFO buffer the oldest sample data in the FIFO buffer is returned and also deleted from the front of the FIFO buffer, while the FIFO sample count is decremented by one. It is assumed that the host application shall use the I^2C multi-byte read transaction to empty the FIFO.

0x0A: TRIG_CFG

In the trigger configuration register the bits that are set (logic ‘1’) control which function may trigger the FIFO to its interrupt and conversely bits that are cleared (logic ‘0’) indicate which function has not asserted its interrupt.

The bits set are rising edge sensitive, and are set by a low to high state change and reset by reading the appropriate source register.

0x0A: TRIG_CFG Trigger Configuration Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	Trig_TRANS	Trig_LNDPRT	Trig_PULSE	Trig_FF_MT	—	—

Table 17. Trigger Configuration Description

INT_SOURCE	Description
Trig_TRANS	Transient interrupt trigger bit. Default value: 0
Trig_LNDPRT	Landscape/Portrait Orientation interrupt trigger bit. Default value: 0
Trig_PULSE	Pulse interrupt trigger bit. Default value: 0
Trig_FF_MT	Freefall/Motion trigger bit. Default value: 0

0x0B: SYSMOD System Mode Register

The System mode register indicates the current device operating mode. Applications using the Auto-SLEEP/WAKE mechanism should use this register to synchronize the application with the device operating mode transitions. The System mode register also indicates the status of the FIFO gate error and number of samples since the gate error occurred.

0x0B: SYSMOD: System Mode Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FGERR	FGT_4	FGT_3	FGT_2	FGT_1	FGT_0	SYSMOD1	SYSMOD0

Table 18. SYSMOD Description

FGERR	FIFO Gate Error. Default value: 0. 0: No FIFO Gate Error detected. 1: FIFO Gate Error was detected. Emptying the FIFO buffer clears the FGERR bit in the SYS_MOD register. See section 0x2C: CTRL_REG3 Interrupt Control Register for more information on configuring the FIFO Gate function.
FGT[4:0]	Number of ODR time units since FGERR was asserted. Reset when FGERR Cleared. Default value: 0_0000
SYSMOD[1:0]	System Mode. Default value: 00. 00: STANDBY mode 01: WAKE mode 10: SLEEP mode

0x0C: INT_SOURCE System Interrupt Status Register

In the interrupt source register the status of the various embedded features can be determined. The bits that are set (logic '1') indicate which function has asserted an interrupt and conversely the bits that are cleared (logic '0') indicate which function has not asserted or has deasserted an interrupt. **The bits are set by a low to high transition and are cleared by reading the appropriate interrupt source register.** The SRC_DRDY bit is cleared by reading the X, Y and Z data. It is not cleared by simply reading the Status Register (0x00).

0x0C: INT_SOURCE: System Interrupt Status Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRC_ASLP	SRC_FIFO	SRC_TRANS	SRC_LNDPRT	SRC_PULSE	SRC_FF_MT	—	SRC_DRDY

Table 19. INT_SOURCE Description

INT_SOURCE	Description
SRC_ASLP	Auto-SLEEP/WAKE interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt event that can cause a WAKE to SLEEP or SLEEP to WAKE system mode transition has occurred. Logic '0' indicates that no WAKE to SLEEP or SLEEP to WAKE system mode transition interrupt event has occurred. **WAKE to SLEEP** transition occurs when no interrupt occurs for a time period that exceeds the user specified limit (ASLP_COUNT). This causes the system to transition to a user specified low ODR setting. **SLEEP to WAKE** transition occurs when the user specified interrupt event has woken the system; thus causing the system to transition to a user specified high ODR setting. Reading the SYSMOD register clears the SRC_ASLP bit.
SRC_FIFO	FIFO interrupt status bit. Default value: 0. Logic '1' indicates that a FIFO interrupt event such as an overflow event or watermark has occurred. Logic '0' indicates that no FIFO interrupt event has occurred. FIFO interrupt event generators: FIFO Overflow, or (Watermark: F_CNT = F_WMRK) and the interrupt has been enabled. This bit is cleared by reading the F_STATUS register.
SRC_TRANS	Transient interrupt status bit. Default value: 0. Logic '1' indicates that an acceleration transient value greater than user specified threshold has occurred. Logic '0' indicates that no transient event has occurred. This bit is asserted whenever **"**EA**"** bit in the TRANS_SRC is asserted and the interrupt has been enabled. This bit is cleared by reading the TRANS_SRC register.
SRC_LNDPRT	Landscape/Portrait Orientation interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt was generated due to a change in the device orientation status. Logic '0' indicates that no change in orientation status was detected. This bit is asserted whenever **"**NEWLP**"** bit in the PL_STATUS is asserted and the interrupt has been enabled. This bit is cleared by reading the PL_STATUS register.
SRC_PULSE	Pulse interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt was generated due to single and/or double pulse event. Logic '0' indicates that no pulse event was detected. This bit is asserted whenever "EA" bit in the PULSE_SRC is asserted and the interrupt has been enabled. This bit is cleared by reading the PULSE_SRC register.
SRC_FF_MT	Freefall/Motion interrupt status bit. Default value: 0. Logic '1' indicates that the Freefall/Motion function interrupt is active. Logic '0' indicates that no Freefall or Motion event was detected. This bit is asserted whenever "EA" bit in the FF_MT_SRC register is asserted and the FF_MT interrupt has been enabled. This bit is cleared by reading the FF_MT_SRC register.
SRC_DRDY	Data Ready Interrupt bit status. Default value: 0. Logic '1' indicates that the X, Y, Z data ready interrupt is active indicating the presence of new data and/or data overrun. Otherwise if it is a logic '0' the X, Y, Z interrupt is not active. This bit is asserted when the ZYXOW and/or ZYXDR is set and the interrupt has been enabled. This bit is cleared by reading the X, Y, and Z data.

0x0D: WHO_AM_I Device ID Register

The device identification register identifies the part. The default value is 0x1A. This value is factory programmed. Consult the factory for custom alternate values.

0x0D: WHO_AM_I Device ID Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	1	0	1	0

0x0E: XYZ_DATA_CFG Register

The XYZ_DATA_CFG register sets the dynamic range and sets the high-pass filter for the output data. When the HPF_OUT bit is set, both the FIFO and DATA registers will contain high-pass filtered data.

0x0E: XYZ_DATA_CFG (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	HPF_OUT	0	0	FS1	FS0

Table 20. XYZ Data Configuration Descriptions

HPF_OUT	Enable High-pass output data 1 = output data High-pass filtered. Default value: 0.
FS[1:0]	Output buffer data format full scale. Default value: 00 (2g).

The default full scale value range is 2g and the high-pass filter is disabled.

Table 21. Full Scale Range

FS1	FS0	Full Scale Range
0	0	2
0	1	4
1	0	8
1	1	Reserved

0x0F: HP_FILTER_CUTOFF High-Pass Filter Register

This register sets the high-pass filter cutoff frequency for removal of the offset and slower changing acceleration data. The output of this filter is indicated by the data registers (0x01-0x06) when bit 4 (HPF_OUT) of Register 0x0E is set. The filter cutoff options change based on the data rate selected as shown in Table 23. For details of implementation on the high-pass filter, refer to Freescale application note, AN4071.

0x0F: HP_FILTER_CUTOFF: High-Pass Filter Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	Pulse_HPF_BYP	Pulse_LPF_EN	0	0	SEL1	SEL0

Table 22. High-Pass Filter Cutoff Register Descriptions

Pulse_HPF_BYP	Bypass High-Pass Filter (HPF) for Pulse Processing Function. 0: HPF enabled for Pulse Processing, 1: HPF Bypassed for Pulse Processing Default value: 0.
Pulse_LPF_EN	Enable Low-Pass Filter (LPF) for Pulse Processing Function. 0: LPF disabled for Pulse Processing, 1: LPF Enabled for Pulse Processing Default value: 0.
SEL[1:0]	HPF Cutoff frequency selection. Default value: 00 (see Table 23).

Table 23. High-Pass Filter Cutoff Options

Oversampling Mode = Normal									
SEL1	SEL0	800 Hz	400 Hz	200 Hz	100 Hz	50 Hz	12.5 Hz	6.25 Hz	1.56 Hz
0	0	16 Hz	16 Hz	8 Hz	4 Hz	2 Hz	2 Hz	2 Hz	2 Hz
0	1	8 Hz	8 Hz	4 Hz	2 Hz	1 Hz	1 Hz	1 Hz	1 Hz
1	0	4 Hz	4 Hz	2 Hz	1 Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz
1	1	2 Hz	2 Hz	1 Hz	0.5 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz
Oversampling Mode = Low Noise Low Power									
0	0	16 Hz	16 Hz	8 Hz	4 Hz	2 Hz	0.5 Hz	0.5 Hz	0.5 Hz
0	1	8 Hz	8 Hz	4 Hz	2 Hz	1 Hz	0.25 Hz	0.25 Hz	0.25 Hz
1	0	4 Hz	4 Hz	2 Hz	1 Hz	0.5 Hz	0.125 Hz	0.125 Hz	0.125 Hz
1	1	2 Hz	2 Hz	1 Hz	0.5 Hz	0.25 Hz	0.063 Hz	0.063 Hz	0.063 Hz
Oversampling Mode = High Resolution									
0	0	16 Hz	16 Hz	16 Hz	16 Hz	16 Hz	16 Hz	16 Hz	16 Hz
0	1	8 Hz	8 Hz	8 Hz	8 Hz	8 Hz	8 Hz	8 Hz	8 Hz
1	0	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz
1	1	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz
Oversampling Mode = Low Power									
0	0	16 Hz	8 Hz	4 Hz	2 Hz	1 Hz	0.25 Hz	0.25 Hz	0.25 Hz
0	1	8 Hz	4 Hz	2 Hz	1 Hz	0.5 Hz	0.125 Hz	0.125 Hz	0.125 Hz
1	0	4 Hz	2 Hz	1 Hz	0.5 Hz	0.25 Hz	0.063 Hz	0.063 Hz	0.063 Hz
1	1	2 Hz	1 Hz	0.5 Hz	0.25 Hz	0.125 Hz	0.031 Hz	0.031 Hz	0.031 Hz

6.3 Portrait/Landscape Embedded Function Registers

For more details on the meaning of the different user configurable settings and for example code refer to Freescale application note, AN4068.

0x10: PL_STATUS Portrait/Landscape Status Register

This status register can be read to get updated information on any change in orientation by reading Bit 7, or on the specifics of the orientation by reading the other bits. For further understanding of Portrait Up, Portrait Down, Landscape Left, Landscape Right, Back and Front orientations please refer to Figure 3. The interrupt is cleared when reading the PL_STATUS register.

0x10: PL_STATUS Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NEWLP	LO	—	—	—	LAPO[1]	LAPO[0]	BAFRO

Table 24. PL_STATUS Register Description

NEWLP	Landscape/Portrait status change flag. Default value: 0. 0: No change, 1: BAFRO and/or LAPO and/or Z-Tilt lockout value has changed
LO	Z-Tilt Angle Lockout. Default value: 0. 0: Lockout condition has not been detected. 1: Z-Tilt lockout trip angle has been exceeded. Lockout has been detected.
LAPO[1:0](1)	Landscape/Portrait orientation. Default value: 00 00: Portrait Up: Equipment standing vertically in the normal orientation 01: Portrait Down: Equipment standing vertically in the inverted orientation 10: Landscape Right: Equipment is in landscape mode to the right 11: Landscape Left: Equipment is in landscape mode to the left.
BAFRO	Back or Front orientation. Default value: 0 0: Front: Equipment is in the front facing orientation. 1: Back: Equipment is in the back facing orientation.

1. *The default power up state is BAFRO = 0, LAPO = 0, and LO = 0.*

NEWLP is set to 1 after the first orientation detection after a STANDBY to ACTIVE transition, and whenever a change in LO, BAFRO, or LAPO occurs. NEWLP bit is cleared anytime PL_STATUS register is read. The Orientation mechanism state change is limited to a maximum 1.25g. LAPO BAFRO and LO continue to change when NEWLP is set. The current position is locked if the absolute value of the acceleration experienced on any of the three axes is greater than 1.25g.

0x11: Portrait/Landscape Configuration Register

This register enables the Portrait/Landscape function and sets the behavior of the debounce counter.

0x11: PL_CFG Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	PL_EN	—	—	—	—	—	—

Table 25. PL_CFG Description

DBCNTM	Debounce counter mode selection. Default value: 1 0: Decrements debounce whenever condition of interest is no longer valid. 1: Clears counter whenever condition of interest is no longer valid.
PL_EN	Portrait/Landscape Detection Enable. Default value: 0 0: Portrait/Landscape Detection is Disabled. 1: Portrait/Landscape Detection is Enabled.

0x12: Portrait/Landscape Debounce Counter

This register sets the debounce count for the orientation state transition. The minimum debounce latency is determined by the data rate set by the product of the selected system ODR and PL_COUNT registers. Any transition from WAKE to SLEEP or vice versa resets the internal Landscape/Portrait debounce counter. **Note:** The debounce counter weighting (time step) changes based on the ODR and the Oversampling mode. Table 27 explains the time step value for all sample rates and all Oversampling modes.

0x12: PL_COUNT Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBNCE[7]	DBNCE[6]	DBNCE[5]	DBNCE[4]	DBNCE[3]	DBNCE[2]	DBNCE[1]	DBNCE[0]

Table 26. PL_COUNT Description

DBCNE[7:0]	Debounce Count value. Default value: 0000_0000.

Table 27. PL_COUNT Relationship with the ODR

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

0x13: PL_BF_ZCOMP Back/Front and Z Compensation Register

The Z-Lock angle compensation bits allow the user to adjust the Z-lockout region from 14° up to 43°. The default Z-lockout angle is set to the default value of 29° upon power up. The Back to Front trip angle is set by default to ±75° but this angle also can be adjusted from a range of 65° to 80° with 5° step increments.

0x13: PL_BF_ZCOMP Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BKFR[1]	BKFR[0]	—	—	—	ZLOCK[2]	ZLOCK[1]	ZLOCK[0]

Table 28. PL_BF_ZCOMP Description

BKFR[7:6]	Back/Front Trip Angle Threshold. Default: **01** ≥ **±75°**. Step size is 5°. Range: ±(65° to 80°).
ZLOCK[2:0]	Z-Lock Angle Threshold. Range is from 14° to 43°. Step size is 4°. Default value: **100** ≥ **29°**. Maximum value: **111** ≥ **43°**.

Note: All angles are accurate to ±2°.

Table 29. Z-Lock Threshold Angles

Z-Lock Value	Threshold Angle
0x00	14°
0x01	18°
0x02	21°
0x03	25°
0x04	29°
0x05	33°
0x06	37°
0x07	42°

Table 30. Back/Front Orientation Definition

BKFR	Back/Front Transition	Front/Back Transition
00	Z < 80° or Z > 280°	Z > 100° and Z < 260°
01	Z < 75° or Z > 285°	Z > 105° and Z < 255°
10	Z < 70° or Z > 290°	Z > 110° and Z < 250°
11	Z < 65° or Z > 295°	Z > 115° and Z < 245°

0x14: P_L_THS_REG Portrait/Landscape Threshold and Hysteresis Register

This register represents the Portrait to Landscape trip threshold register used to set the trip angle for transitioning from Portrait to Landscape and Landscape to Portrait. This register includes a value for the hysteresis.

0x14: P_L_THS_REG Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]	HYS[2]	HYS[1]	HYS[0]

Table 31. P_L_THS_REG Description

P_L_THS[7:3]	Portrait/Landscape trip threshold angle from 15° to 75°. See Table 32 for the values with the corresponding approximate threshold angle. Default value: 1_0000 (45°).
HYS[2:0]	This angle is added to the threshold angle for a smoother transition from Portrait to Landscape and Landscape to Portrait. This angle ranges from 0° to ±24°. The default is 100 (±14°).

Table 32 is a lookup table to set the threshold. This is the center value that will be set for the trip point from Portrait to Landscape and Landscape to Portrait. The default Trip Angle is 45° (0x10). The default hysteresis is ±14°.

Note: The condition THS + HYS > 0 and THS + HYS < 32 must be met in order for Landscape/Portrait detection to work properly. The value of 32 represents the sum of both P_L_THS and HYS register values in decimal. For example, THS angle = 75°, P_L_THS = 25(dec) then max HYS must be set to 6 to meet the condition THS+HYS < 32. To configure correctly the hysteresis (HYS) angle must be smaller than the threshold angle (P_L_THS).

Table 32. Threshold Angle Thresholds Lookup Table

Threshold Angle (approx.)	5-bit Register value
15°	0x07
20°	0x09
30°	0x0C
35°	0x0D
40°	0x0F
45°	**0x10**
55°	0x13
60°	0x14
70°	0x17
75°	0x19

Table 33. Trip Angles with Hysteresis for 45° Angle

Hysteresis Register Value	Hysteresis ± Angle Range	Landscape to Portrait Trip Angle	Portrait to Landscape Trip Angle
0	±0	45°	45°
1	±4	49°	41°
2	±7	52°	38°
3	±11	56°	34°
4	**±14**	**59°**	**31°**

Table 33. Trip Angles with Hysteresis for 45° Angle

5	±17	62°	28°
6	±21	66°	24°
7	±24	69°	21°

6.4 Motion and Freefall Embedded Function Registers

The freefall/motion function can be configured in either Freefall or Motion Detection mode via the **OAE** configuration bit (0x15 bit 6). The freefall/motion detection block can be disabled by setting all three bits ZEFE, YEFE, and XEFE to zero.

Depending on the register bits **ELE** (0x15 bit 7) and **OAE** (0x15 bit 6), each of the freefall and motion detection block can operate in four different modes:

Mode 1: Freefall Detection with ELE = 0, OAE = 0

In this mode, the **EA** bit (0x16 bit 7) indicates a freefall event after the debounce counter is complete. The ZEFE, YEFE, and XEFE control bits determine which axes are considered for the freefall detection. Once the EA bit is set, and DBCNTM = 0, the EA bit can get cleared only after the delay specified by FF_MT_COUNT. This is because the counter is in decrement mode. If DBCNTM = 1, the EA bit is cleared as soon as the freefall condition disappears, and will not be set again before the delay specified by FF_MT_COUNT has passed. Reading the FF_MT_SRC register does not clear the EA bit. The event flags (0x16) ZHE, ZHP, YHE, YHP, XHE, and XHP reflect the motion detection status (i.e. high g event) without any debouncing, provided that the corresponding bits ZEFE, YEFE, and/or XEFE are set.

Mode 2: Freefall Detection with ELE = 1, OAE = 0

In this mode, the **EA** event bit indicates a freefall event after the debounce counter. Once the debounce counter reaches the time value for the set threshold, the EA bit is set, and remains set until the FF_MT_SRC register is read. When the FF_MT_SRC register is read, the EA bit and the debounce counter are cleared and a new event can only be generated after the delay specified by FF_MT_CNT. The ZEFE, YEFE, and XEFE control bits determine which axes are considered for the freefall detection. While EA = 0, the event flags ZHE, ZHP, YHE, YHP, XHE, and XHP reflect the motion detection status (i.e., high g event) without any debouncing, provided that the corresponding bits ZEFE, YEFE, and/or XEFE are set. The event flags ZHE, ZHP, YHE, YHP, XHE, and XHP are latched when the EA event bit is set. The event flags ZHE, ZHP, YHE, YHP, XHE, and XHP will start changing only after the FF_MT_SRC register has been read.

Mode 3: Motion Detection with ELE = 0, OAE = 1

In this mode, the **EA** bit indicates a motion event after the debounce counter time is reached. The ZEFE, YEFE, and XEFE control bits determine which axes are taken into consideration for motion detection. Once the **EA** bit is set, and DBCNTM = 0, the EA bit can get cleared only after the delay specified by FF_MT_COUNT. If DBCNTM = 1, the **EA** bit is cleared as soon as the motion high g condition disappears. The event flags ZHE, ZHP, YHE, YHP, XHE, and XHP reflect the motion detection status (i.e., high g event) without any debouncing, provided that the corresponding bits ZEFE, YEFE, and/or XEFE are set. Reading the FF_MT_SRC does not clear any flags, nor is the debounce counter reset.

Mode 4: Motion Detection with ELE = 1, OAE = 1

In this mode, the EA bit indicates a motion event after debouncing. The ZEFE, YEFE, and XEFE control bits determine which axes are taken into consideration for motion detection. Once the debounce counter reaches the threshold, the EA bit is set, and remains set until the FF_MT_SRC register is read. When the FF_MT_SRC register is read, all register bits are cleared and the debounce counter are cleared and a new event can only be generated after the delay specified by FF_MT_CNT. While the bit EA is zero, the event flags ZHE, ZHP, YHE, YHP, XHE, and XHP reflect the motion detection status (i.e., high g event) without any debouncing, provided that the corresponding bits ZEFE, YEFE, and/or XEFE are set. When the EA bit is set, these bits keep their current value until the FF_MT_SRC register is read.

0x15: FF_MT_CFG Freefall/Motion Configuration Register

This is the Freefall/Motion configuration register for setting up the conditions of the freefall or motion function.

0x15: FF_MT_CFG Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ELE	OAE	ZEFE	YEFE	XEFE	—	—	—

Table 34. FF_MT_CFG Description

ELE	Event Latch Enable: Event flags are latched into FF_MT_SRC register. Reading of the FF_MT_SRC register clears the event flag EA and all FF_MT_SRC bits. Default value: 0. 0: Event flag latch disabled; 1: event flag latch enabled
OAE	Motion detect / Freefall detect flag selection. Default value: 0. (Freefall Flag) 0: Freefall Flag (Logical AND combination) 1: Motion Flag (Logical OR combination)
ZEFE	Event flag enable on Z Default value: 0. 0: event detection disabled; 1: raise event flag on measured acceleration value beyond preset threshold
YEFE	Event flag enable on Y event. Default value: 0. 0: Event detection disabled; 1: raise event flag on measured acceleration value beyond preset threshold
XEFE	Event flag enable on X event. Default value: 0. 0: event detection disabled; 1: raise event flag on measured acceleration value beyond preset threshold

OAE bit allows the selection between Motion (logical OR combination) and Freefall (logical AND combination) detection.
ELE denotes whether the enabled event flag will to be latched in the FF_MT_SRC register or the event flag status in the FF_MT_SRC will indicate the real-time status of the event. If ELE bit is set to a logic '1', then the event flags are frozen when the EA bit gets set, and are cleared by reading the FF_MT_SRC source register.
ZHFE, YEFE, XEFE enable the detection of a motion or freefall event when the measured acceleration data on X, Y, Z channel is beyond the threshold set in FF_MT_THS register. If the ELE bit is set to logic '1' in the FF_MT_CFG register new event flags are blocked from updating the FF_MT_SRC register.
FF_MT_THS is the threshold register used to detect freefall motion events. The unsigned 7-bit **FF_MT_THS** threshold register holds the threshold for the freefall detection where the magnitude of the X and Y and Z acceleration values is lower or equal than the threshold value. Conversely, the **FF_MT_THS** also holds the threshold for the motion detection where the magnitude of the X or Y or Z acceleration value is higher than the threshold value.

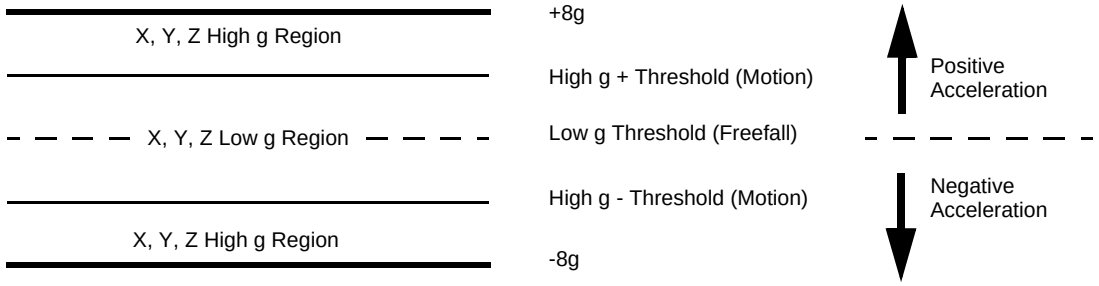


Figure 12. FF_MT_CFG High and Low g Level

0x16: FF_MT_SRC Freefall/Motion Source Register

0x16: FF_MT_SRC Freefall and Motion Source Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EA	—	ZHE	ZHP	YHE	YHP	XHE	XHP

Table 35. Freefall/Motion Source Description

EA	Event Active Flag. Default value: 0. 0: No event flag has been asserted; 1: one or more event flag has been asserted. See the description of the OAE bit to determine the effect of the 3-axis event flags on the EA bit.
ZHE	Z Motion Flag. Default value: 0. 0: No Z Motion event detected, 1: Z Motion has been detected This bit reads always zero if the ZEFE control bit is set to zero
ZHP	Z Motion Polarity Flag. Default value: 0. 0: Z event was Positive g, 1: Z event was Negative g This bit read always zero if the ZEFE control bit is set to zero
YHE	Y Motion Flag. Default value: 0. 0: No Y Motion event detected, 1: Y Motion has been detected This bit read always zero if the YEFE control bit is set to zero
YHP	Y Motion Polarity Flag. Default value: 0 0: Y event detected was Positive g, 1: Y event was Negative g This bit reads always zero if the YEFE control bit is set to zero
XHE	X Motion Flag. Default value: 0 0: No X Motion event detected, 1: X Motion has been detected This bit reads always zero if the XEFE control bit is set to zero
XHP	X Motion Polarity Flag. Default value: 0 0: X event was Positive g, 1: X event was Negative g This bit reads always zero if the XEFE control bit is set to zero

This register keeps track of the acceleration event which is triggering (or has triggered, in case of ELE bit in FF_MT_CFG register being set to 1) the event flag. In particular EA is set to a logic ‘1’ when the logical combination of acceleration events flags specified in FF_MT_CFG register is true. This bit is used in combination with the values in INT_EN_FF_MT and INT_CFG_FF_MT register bits to generate the freefall/motion interrupts.

An X,Y, or Z motion is true when the acceleration value of the X or Y or Z channel is higher than the preset threshold value defined in the FF_MT_THS register.

Conversely an X, Y, and Z low event is true when the acceleration value of the X and Y and Z channel is lower than or equal to the preset threshold value defined in the FF_MT_THS register.

0x17: FF_MT_THS Freefall and Motion Threshold Register

0x17: FF_MT_THS Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 36. FF_MT_THS Description

DBCNTM	Debounce counter mode selection. Default value: 0. 0: increments or decrements debounce, 1: increments or clears counter.
THS[6:0]	Freefall /Motion Threshold: Default value: 000_0000.

The threshold resolution is 0.063g/LSB and the threshold register has a range of 0 to 127 counts. The maximum range is to 8g. Note that even when the full scale value is set to 2g or 4g the motion detects up to 8g. If the Low Noise bit is set in Register 0x2A then the maximum threshold will be limited to 4g regardless of the full scale range.

DBCNTM bit configures the way in which the debounce counter is reset when the inertial event of interest is momentarily not true.

When DBCNTM bit is a logic ‘1’, the debounce counter is cleared to 0 whenever the inertial event of interest is no longer true as shown in Figure 13, (b). While the DBCNTM bit is set to logic ‘0’ the debounce counter is decremented by 1 whenever the inertial event of interest is no longer true (Figure 13, (c)) until the debounce counter reaches 0 or the inertial event of interest becomes active.

Decrementing the debounce counter acts as a median enabling the system to filter out irregular spurious events which might impede the detection of inertial events.

0x18: FF_MT_COUNT Debounce Register

This register sets the number of debounce sample counts for the event trigger.

0x18: FF_MT_COUNT_Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 37. FF_MT_COUNT Description

D[7:0]	Count value. Default value: 0000_0000

This register sets the minimum number of debounce sample counts of continuously matching the detection condition user selected for the freefall, motion event.

When the internal debounce counter reaches the FF_MT_COUNT value a Freefall/Motion event flag is set. The debounce counter will never increase beyond the FF_MT_COUNT value. Time step used for the debounce sample count depends on the ODR chosen and the Oversampling mode as shown in Table 38.

Table 38. FF_MT_COUNT Relationship with the ODR

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

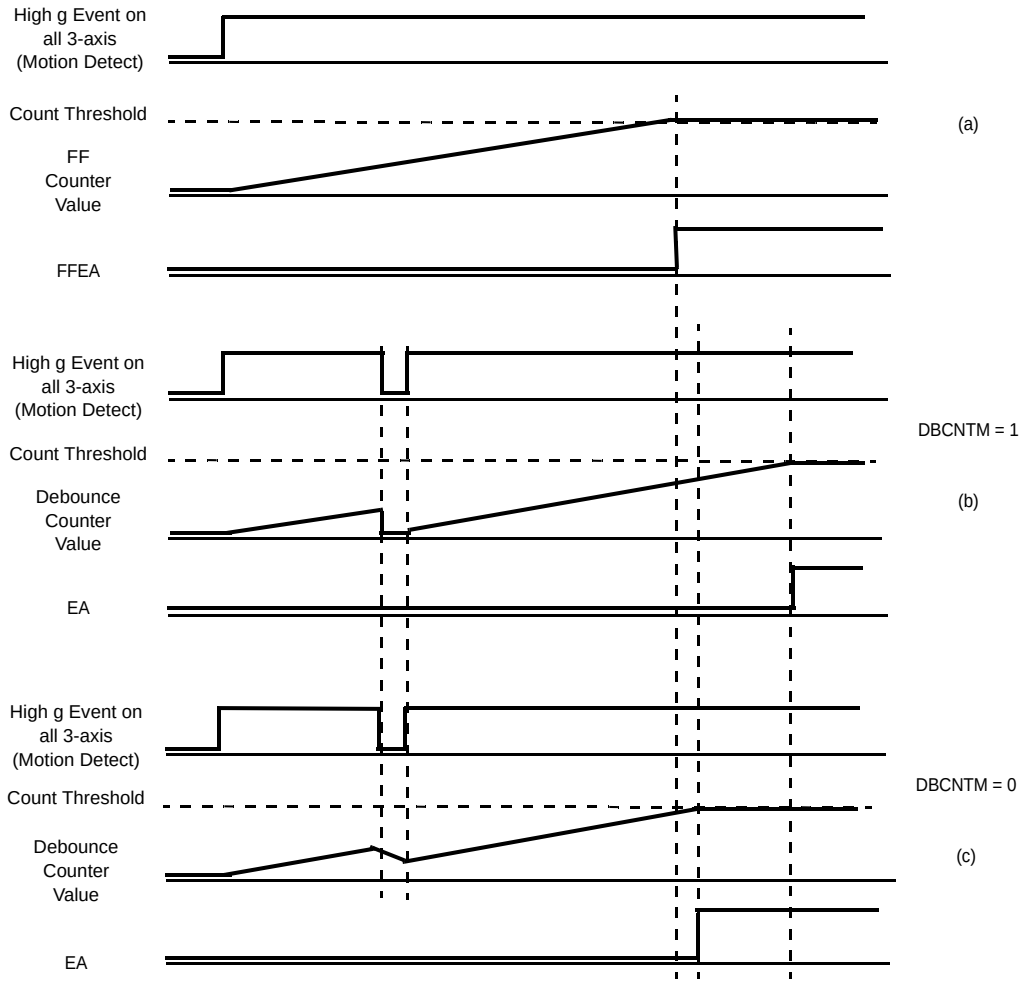


Figure 13. DBCNTM Bit Function

6.5 Transient (HPF) Acceleration Detection

For more information on the uses of the transient function please review Freescale application note, AN4071. This function is similar to the motion detection except that high-pass filtered data is compared. There is an option to disable the high-pass filter through the function. In this case the behavior is the same as the motion detection. This allows for the device to have 2 motion detection functions.

0x1D: Transient_CFG Register

The transient detection mechanism can be configured to raise an interrupt when the magnitude of the high-pass filtered acceleration threshold is exceeded. The TRANSIENT_CFG register is used to enable the transient interrupt generation mechanism for the 3 axes (X, Y, Z) of acceleration. There is also an option to bypass the high-pass filter. When the high-pass filter is bypassed, the function behaves similar to the motion detection.

0x1D: TRANSIENT_CFG Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	ELE	ZTEFE	YTEFE	XTEFE	HPF_BYP

Table 39. TRANSIENT_CFG Description

ELE	Transient event flags are latched into the TRANSIENT_SRC register. Reading of the TRANSIENT_SRC register clears the event flag. Default value: 0. 0: Event flag latch disabled; 1: Event flag latch enabled
ZTEFE	Event flag enable on Z transient acceleration greater than transient threshold event. Default value: 0. 0: Event detection disabled; 1: Raise event flag on measured acceleration delta value greater than transient threshold.
YTEFE	Event flag enable on Y transient acceleration greater than transient threshold event. Default value: 0. 0: Event detection disabled; 1: Raise event flag on measured acceleration delta value greater than transient threshold.
XTEFE	Event flag enable on X transient acceleration greater than transient threshold event. Default value: 0. 0: Event detection disabled; 1: Raise event flag on measured acceleration delta value greater than transient threshold.
HPF_BYP	Bypass High-Pass filter Default value: 0. 0: Data to transient acceleration detection block is through HPF 1: Data to transient acceleration detection block is NOT through HPF (similar to motion detection function)

0x1E: TRANSIENT_SRC Register

The Transient Source register provides the status of the enabled axes and the polarity (directional) information. When this register is read it clears the interrupt for the transient detection. When new events arrive while EA = 1, additional *TRANSE bits may get set, and the corresponding *_Trans_Pol flag become updated. However, no *TRANSE bit may get cleared before the TRANSIENT_SRC register is read.

0x1E: TRANSIENT_SRC Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	EA	ZTRANSE	Z_Trans_Pol	YTRANSE	Y_Trans_Pol	XTRANSE	X_Trans_Pol

Table 40. TRANSIENT_SRC Description

EA	Event Active Flag. Default value: 0. 0: no event flag has been asserted; 1: one or more event flag has been asserted.
ZTRANSE	Z transient event. Default value: 0. 0: no interrupt, 1: Z Transient acceleration greater than the value of TRANSIENT_THS event has occurred
Z_Trans_Pol	Polarity of Z Transient Event that triggered interrupt. Default value: 0. 0: Z event was Positive g, 1: Z event was Negative g
YTRANSE	Y transient event. Default value: 0. 0: no interrupt, 1: Y Transient acceleration greater than the value of TRANSIENT_THS event has occurred
Y_Trans_Pol	Polarity of Y Transient Event that triggered interrupt. Default value: 0. 0: Y event was Positive g, 1: Y event was Negative g
XTRANSE	X transient event. Default value: 0. 0: no interrupt, 1: X Transient acceleration greater than the value of TRANSIENT_THS event has occurred
X_Trans_Pol	Polarity of X Transient Event that triggered interrupt. Default value: 0. 0: X event was Positive g, 1: X event was Negative g

When the EA bit gets set while ELE = 1, all other status bits get frozen at their current state. By reading the TRANSIENT_SRC register, all bits get cleared.

0x1F: TRANSIENT_THS Register

The Transient Threshold register sets the threshold limit for the detection of the transient acceleration. The value in the TRANSIENT_THS register corresponds to a g value which is compared against the values of High-Pass Filtered Data. If the High-Pass Filtered acceleration value exceeds the threshold limit, an event flag is raised and the interrupt is generated if enabled.

0x1F: TRANSIENT_THS Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 41. TRANSIENT_THS Description

DBCNTM	Debounce counter mode selection. Default value: 0. 0: increments or decrements debounce; 1: increments or clears counter.
THS[6:0]	Transient Threshold: Default value: 000_0000.

The threshold THS[6:0] is a 7-bit unsigned number, 0.063g/LSB. The maximum threshold is 8g. Even if the part is set to full scale at 2g or 4g this function will still operate up to 8g. If the Low Noise bit is set in Register 0x2A, the maximum threshold to be reached is 4g.

0x20: TRANSIENT_COUNT

The TRANSIENT_COUNT sets the minimum number of debounce counts continuously matching the condition where the unsigned value of high-pass filtered data is greater than the user specified value of TRANSIENT_THS.

0x20: TRANSIENT_COUNT Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 42. TRANSIENT_COUNT Description

D[7:0]	Count value. Default value: 0000_0000.

The time step for the transient detection debounce counter is set by the value of the system ODR and the Oversampling mode.

Table 43. TRANSIENT_COUNT Relationship with the ODR

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

6.6 Single, Double and Directional Tap Detection Registers

For more details of how to configure the tap detection and sample code, please refer to Freescale application note, AN4072. The tap detection registers are referred to as “Pulse”.

0x21: PULSE_CFG Pulse Configuration Register

This register configures the event flag for the tap detection for enabling/disabling the detection of a single and double pulse on each of the axes.

0x21: PULSE_CFG Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPA	ELE	ZDPEFE	ZSPEFE	YDPEFE	YSPEFE	XDPEFE	XSPEFE

Table 44. PULSE_CFG Description

DPA	Double Pulse Abort. Default value: 0. 0: Double Pulse detection is not aborted if the start of a pulse is detected during the time period specified by the PULSE_LTCY register. 1: Setting the DPA bit momentarily suspends the double tap detection if the start of a pulse is detected during the time period specified by the PULSE_LTCY register and the pulse ends before the end of the time period specified by the PULSE_LTCY register.
ELE	Pulse event flags are latched into the PULSE_SRC register. Reading of the PULSE_SRC register clears the event flag. Default value: 0. 0: Event flag latch disabled; 1: Event flag latch enabled
ZDPEFE	Event flag enable on double pulse event on Z-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
ZSPEFE	Event flag enable on single pulse event on Z-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
YDPEFE	Event flag enable on double pulse event on Y-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
YSPEFE	Event flag enable on single pulse event on Y-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
XDPEFE	Event flag enable on double pulse event on X-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
XSPEFE	Event flag enable on single pulse event on X-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled

0x22: PULSE_SRC Pulse Source Register

This register indicates a double or single pulse event has occurred and also which direction. The corresponding axis and event must be enabled in Register 0x21 for the event to be seen in the source register.

0x22: PULSE_SRC Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EA	AxZ	AxY	AxX	DPE	PolZ	PolY	PolX

Table 45. PULSE_SRC Description

EA	Event Active Flag. Default value: 0. (0: No interrupt has been generated; 1: One or more interrupt events have been generated)
AxZ	Z-axis event. Default value: 0. (0: No interrupt; 1: Z-axis event has occurred)
AxY	Y-axis event. Default value: 0. (0: No interrupt; 1: Y-axis event has occurred)
AxX	X-axis event. Default value: 0. (0: No interrupt; 1: X-axis event has occurred)
DPE	Double pulse on first event. Default value: 0. (0: Single Pulse Event triggered interrupt; 1: Double Pulse Event triggered interrupt)
PolZ	Pulse polarity of Z-axis Event. Default value: 0. (0: Pulse Event that triggered interrupt was Positive; 1: Pulse Event that triggered interrupt was negative)
PolY	Pulse polarity of Y-axis Event. Default value: 0. (0: Pulse Event that triggered interrupt was Positive; 1: Pulse Event that triggered interrupt was negative)
PolX	Pulse polarity of X-axis Event. Default value: 0. (0: Pulse Event that triggered interrupt was Positive; 1: Pulse Event that triggered interrupt was negative)

When the EA bit gets set while ELE = 1, all status bits (AxZ, AxY, AxZ, DPE, and PolX, PolY, PolZ) are frozen. Reading the PULSE_SRC register clears all bits. Reading the source register will clear the interrupt.

0x23 - 0x25: PULSE_THSX, Y, Z Pulse Threshold for X, Y & Z Registers

The pulse threshold can be set separately for the X, Y and Z axes. The PULSE_THSX, PULSE_THSY and PULSE_THSZ registers define the threshold which is used by the system to start the pulse detection procedure.

0x23: PULSE_THSX Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 46. PULSE_THSX Description

THSX[6:0]	Pulse Threshold on X-axis. Default value: 000_0000.

0x24: PULSE_THSY Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 47. PULSE_THSY Description

THSY[6:0]	Pulse Threshold on Y-axis. Default value: 000_0000.

0x25: PULSE_THSZ Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 48. PULSE_THSZ Description

THSZ[6:0]	Pulse Threshold on Z-axis. Default value: 000_0000.

The threshold values range from 1 to 127 with steps of 0.63g/LSB at a fixed 8g acceleration range, thus the minimum resolution is always fixed at 0.063g/LSB. If the Low Noise bit in Register 0x2A is set then the maximum threshold will be 4g. The PULSE_THSX, PULSE_THSY and PULSE_THSZ registers define the threshold which is used by the system to start the pulse detection procedure. The threshold value is expressed over 7-bits as an unsigned number.

0x26: PULSE_TMLT Pulse Time Window 1 Register

0x26: PULSE_TMLT Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMLT7	TMLT6	TMLT5	TMLT4	TMLT3	TMLT2	TMLT1	TMLT0

Table 49. PULSE_TMLT Description

TMLT[7:0]	Pulse Time Limit. Default value: 0000_0000.

The bits TMLT7 through TMLT0 define the maximum time interval that can elapse between the start of the acceleration on the selected axis exceeding the specified threshold and the end when the acceleration on the selected axis must go below the specified threshold to be considered a valid pulse.

The minimum time step for the pulse time limit is defined in Table 50 and Table 51. Maximum time for a given ODR and Oversampling mode is the time step pulse multiplied by 255. The time steps available are dependent on the Oversampling mode and whether the Pulse Low-Pass Filter option is enabled or not. The Pulse Low Pass Filter is set in Register 0x0F.

Table 50. Time Step for PULSE Time Limit (Reg 0x0F) Pulse_LPF_EN = 1

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

Table 51. Time Step for PULSE Time Limit (Reg 0x0F) Pulse_LPF_EN = 0

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.159	0.159	0.159	0.159	0.625	0.625	0.625	0.625
400	0.159	0.159	0.159	0.319	0.625	0.625	0.625	1.25
200	0.319	0.319	0.159	0.638	1.25	1.25	0.625	2.5
100	0.638	0.638	0.159	1.28	2.5	2.5	0.625	5
50	1.28	1.28	0.159	2.55	5	5	0.625	10
12.5	1.28	5.1	0.159	10.2	5	20	0.625	40
6.25	1.28	5.1	0.159	10.2	5	20	0.625	40
1.56	1.28	5.1	0.159	10.2	5	20	0.625	40

0x27: PULSE_LTCY Pulse Latency Timer Register

0x27: PULSE_LTCY Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LTCY7	LTCY6	LTCY5	LTCY4	LTCY3	LTCY2	LTCY1	LTCY0

Table 52. PULSE_LTCY Description

LTCY[7:0]	Latency Time Limit. Default value: 0000_0000

The bits LTCY7 through LTCY0 define the time interval that starts after the first pulse detection. During this time interval, all pulses are ignored. **Note:** This timer must be set for single pulse and for double pulse.

The minimum time step for the pulse latency is defined in Table 53 and Table 54. The maximum time is the time step at the ODR and Oversampling mode multiplied by 255. The timing also changes when the Pulse LPF is enabled or disabled.

Table 53. Time Step for PULSE Latency @ ODR and Power Mode (Reg 0x0F) Pulse_LPF_EN = 1

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
400	1.276	1.276	1.276	1.276	5	5	5	5
200	2.56	2.56	1.276	2.56	10	10	5	10
100	5.1	5.1	1.276	5.1	20	20	5	20
50	10.2	10.2	1.276	10.2	40	40	5	40
12.5	10.2	40.8	1.276	40.8	40	160	5	160
6.25	10.2	40.8	1.276	81.6	40	160	5	320
1.56	10.2	40.8	1.276	81.6	40	160	5	320

Table 54. Time Step for PULSE Latency @ ODR and Power Mode (Reg 0x0F) Pulse_LPF_EN = 0

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.318	0.318	0.318	0.318	1.25	1.25	1.25	1.25
400	0.318	0.318	0.318	0.638	1.25	1.25	1.25	2.5
200	0.638	0.638	0.318	1.276	2.5	2.5	1.25	5
100	1.276	1.276	0.318	2.56	5	5	1.25	10
50	2.56	2.56	0.318	5.1	10	10	1.25	20
12.5	2.56	10.2	0.318	20.4	10	40	1.25	80
6.25	2.56	10.2	0.318	20.4	10	40	1.25	80
1.56	2.56	10.2	0.318	20.4	10	40	1.25	80

0x28: PULSE_WIND Register (Read/Write)

0x28: PULSE_WIND Second Pulse Time Window Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WIND7	WIND6	WIND5	WIND4	WIND3	WIND2	WIND1	WIND0

Table 55. PULSE_WIND Description

WIND[7:0]	Second Pulse Time Window. Default value: 0000_0000.

The bits WIND7 through WIND0 define the maximum interval of time that can elapse after the end of the latency interval in which the start of the second pulse event must be detected provided the device has been configured for double pulse detection. The detected second pulse width must be shorter than the time limit constraints specified by the PULSE_TMLT register, but the end of the double pulse need not finish within the time specified by the PULSE_WIND register.

The minimum time step for the pulse window is defined in Table 56 and Table 57. The maximum time is the time step at the ODR, Oversampling mode and LPF Filter Option multiplied by 255.

Table 56. Time Step for PULSE Detection Window @ ODR and Power Mode (Reg 0x0F) Pulse_LPF_EN = 1

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
400	1.276	1.276	1.276	1.276	5	5	5	5
200	2.56	2.56	1.276	2.56	10	10	5	10
100	5.1	5.1	1.276	5.1	20	20	5	20
50	10.2	10.2	1.276	10.2	40	40	5	40
12.5	10.2	40.8	1.276	40.8	40	160	5	160
6.25	10.2	40.8	1.276	81.6	40	160	5	320
1.56	10.2	40.8	1.276	81.6	40	160	5	320

Table 57. Time Step for PULSE Detection Window @ ODR and Power Mode (Reg 0x0F) Pulse_LPF_EN = 0

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.318	0.318	0.318	0.318	1.25	1.25	1.25	1.25
400	0.318	0.318	0.318	0.638	1.25	1.25	1.25	2.5
200	0.638	0.638	0.318	1.276	2.5	2.5	1.25	5
100	1.276	1.276	0.318	2.56	5	5	1.25	10
50	2.56	2.56	0.318	5.1	10	10	1.25	20
12.5	2.56	10.2	0.318	20.4	10	40	1.25	80
6.25	2.56	10.2	0.318	20.4	10	40	1.25	80
1.56	2.56	10.2	0.318	20.4	10	40	1.25	80

6.7 Auto-WAKE/SLEEP Detection

The ASLP_COUNT register sets the minimum time period of inactivity required to change current ODR value from the value specified in the **DR[2:0]** register to **ASLP_RATE** register value, provided the **SLPE** bit is set to a logic ‘1’ in the **CTRL_REG2** register. See Table 59 for functional blocks that may be monitored for inactivity in order to trigger the “return to SLEEP” event.

0x29: ASLP_COUNT Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 58. ASLP_COUNT Description

D[7:0]	Duration value. Default value: 0000_0000.

D7-D0 defines the minimum duration time to change current ODR value from **DR** to **ASLP_RATE**. Time step and maximum value depend on the ODR chosen as shown in Table 59.

Table 59. ASLP_COUNT Relationship with ODR

Output Data Rate (ODR)	Duration	ODR Time Step	ASLP_COUNT Step
800 Hz	0 to 81s	1.25 ms	320 ms
400 Hz	0 to 81s	2.5 ms	320 ms
200 Hz	0 to 81s	5 ms	320 ms
100 Hz	0 to 81s	10 ms	320 ms
50 Hz	0 to 81s	20 ms	320 ms
12.5 Hz	0 to 81s	80 ms	320 ms
6.25 Hz	0 to 81s	160 ms	320 ms
1.56 Hz	0 to 162s	640 ms	640 ms

Table 60. SLEEP/WAKE Mode Gates and Triggers

Interrupt Source	Event restarts timer and delays Return to SLEEP	Event will WAKE from SLEEP
FIFO_GATE	Yes	No
SRC_TRANS	Yes	Yes
SRC_LNDPRT	Yes	Yes
SRC_PULSE	Yes	Yes
SRC_FF_MT	Yes	Yes
SRC_ASLP	No*	No*
SRC_DRDY	No	No

* If the FIFO_GATE bit is set to logic ‘1’, the assertion of the SRC_ASLP interrupt does not prevent the system from transitioning to SLEEP or from WAKE mode; instead it prevents the FIFO buffer from accepting new sample data until the host application flushes the FIFO buffer.

In order to wake the device, the desired function or functions must be enabled in CTRL_REG4 and set to WAKE to SLEEP in CTRL_REG3. All enabled functions will still function in SLEEP mode at the SLEEP ODR. Only the functions that have been selected for WAKE from SLEEP will **WAKE** the device.

MMA8451Q has four functions that can be used to keep the sensor from falling asleep; Transient, Orientation, Tap and Motion/Freefall. One or more of these functions can be enabled. In order to WAKE the device, four functions are provided; Transient, Orientation, Tap, and the Motion/Freefall. Note that the FIFO does not WAKE the device. The Auto-WAKE/SLEEP interrupt does not affect the WAKE/SLEEP, nor does the data ready interrupt. The FIFO gate (bit 7) in Register 0x2C, when set, will hold the last data in the FIFO before transitioning to a different ODR. After the buffer is flushed, it will accept new sample data at the current ODR. See Register 0x2C for the WAKE from SLEEP bits.

If the Auto-SLEEP bit is disabled, then the device can only toggle between STANDBY and WAKE mode. If Auto-SLEEP interrupt is enabled, transitioning from ACTIVE mode to Auto-SLEEP mode and vice versa generates an interrupt.

6.8 Control Registers

Note: Except for STANDBY mode selection, the device must be in STANDBY mode to change any of the fields within CTRL_REG1 (0x2A).

0x2A: CTRL_REG1 System Control 1 Register

0x2A: CTRL_REG1 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ASLP_RATE1	ASLP_RATE0	DR2	DR1	DR0	LNOISE	F_READ	ACTIVE

Table 61. CTRL_REG1 Description

ASLP_RATE[1:0]	Configures the Auto-WAKE sample frequency when the device is in SLEEP Mode. Default value: 00. See Table 62 for more information.
DR[2:0]	Data rate selection. Default value: 000. See Table 63 for more information.
LNOISE	Reduced noise reduced Maximum range mode. Default value: 0. (0: Normal mode; 1: Reduced Noise mode)
F_READ	Fast Read mode: Data format limited to single Byte Default value: 0. (0: Normal mode 1: Fast Read Mode)
ACTIVE	Full Scale selection. Default value: 00. (0: STANDBY mode; 1: ACTIVE mode)

Table 62. SLEEP Mode Rate Description

ASLP_RATE1	ASLP_RATE0	Frequency (Hz)
0	0	50
0	1	12.5
1	0	6.25
1	1	1.56

It is important to note that when the device is Auto-SLEEP mode, the system ODR and the data rate for all the system functional blocks are overridden by the data rate set by the **ASLP_RATE** field.

DR[2:0] bits select the Output Data Rate (ODR) for acceleration samples. The default value is **000 for a data rate of 800 Hz.**

Table 63. System Output Data Rate Selection

DR2	DR1	DR0	ODR	Period
0	0	0	800 Hz	1.25 ms
0	0	1	400 Hz	2.5 ms
0	1	0	200 Hz	5 ms
0	1	1	100 Hz	10 ms
1	0	0	50 Hz	20 ms
1	0	1	12.5 Hz	80 ms
1	1	0	6.25 Hz	160 ms
1	1	1	1.56 Hz	640 ms

ACTIVE bit selects between STANDBY mode and ACTIVE mode. The default value is 0 for STANDBY mode.

Table 64. Full Scale Selection

Active	Mode
0	STANDBY
1	ACTIVE

LNOISE bit selects between normal full dynamic range mode and a high sensitivity, Low Noise mode. In Low Noise mode, the maximum signal that can be measured is ±4g. **Note:** Any thresholds set above 4g will not be reached.

F_READ bit selects between normal and Fast Read mode. When selected, the auto increment counter will skip over the LSB data bytes. Data read from the FIFO will skip over the LSB data, reducing the acquisition time. Note F_READ can only be changed when FMODE = 00. The F_READ bit applies for both the output registers and the FIFO.

0x2B: CTRL_REG2 System Control 2 Register

0x2B: CTRL_REG2 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ST	RST	0	SMODS1	SMODS0	SLPE	MODS1	MODS0

Table 65. CTRL_REG2 Description

ST	Self-Test Enable. Default value: 0. 0: Self-Test disabled; 1: Self-Test enabled
RST	Software Reset. Default value: 0. 0: Device reset disabled; 1: Device reset enabled.
SMODS[1:0]	SLEEP mode power scheme selection. Default value: 00. See Table 66 and Table 67
SLPE	Auto-SLEEP enable. Default value: 0. 0: Auto-SLEEP is not enabled; 1: Auto-SLEEP is enabled.
MODS[1:0]	ACTIVE mode power scheme selection. Default value: 00. See Table 66 and Table 67

ST bit activates the self-test function. When ST is set, X, Y, and Z outputs will shift. **RST** bit is used to activate the software reset. The reset mechanism can be enabled in STANDBY and ACTIVE mode.

When the reset bit is enabled, all registers are rest and are loaded with default values. Writing '1' to the RST bit immediately resets the device, no matter whether it is in ACTIVE/WAKE, ACTIVE/SLEEP, or STANDBY mode.

The I^2C communication system is reset to avoid accidental corrupted data access.

At the end of the boot process, the RST bit is deasserted to 0. Reading this bit will return a value of zero.

The **(S)MODS[1:0]** bits select which Oversampling mode is to be used shown in Table 66. The Oversampling modes are available in both WAKE Mode MOD[1:0] and also in the SLEEP Mode SMOD[1:0].

Table 66. MODS Oversampling Modes

(S)MODS1	(S)MODS0	Power Mode
0	0	Normal
0	1	Low Noise Low Power
1	0	High Resolution
1	1	Low Power

Table 67. MODS Oversampling Modes Current Consumption and Averaging Values at each ODR

Mode	Normal (00)		Low Noise Low Power (01)		High Resolution (10)		Low Power (11)	
ODR	Current µA	OS Ratio	Current µA	OS Ratio	Current µA	OS Ratio	Current µA	OS Ratio
1.56 Hz	24	128	8	32	165	1024	6	16
6.25 Hz	24	32	8	8	165	256	6	4
12.5 Hz	24	16	8	4	165	128	6	2
50 Hz	24	4	24	4	165	32	14	2
100 Hz	44	4	44	4	165	16	24	2
200 Hz	85	4	85	4	165	8	44	2
400 Hz	165	4	165	4	165	4	85	2
800 Hz	165	2	165	2	165	2	165	2

0x2C: CTRL_REG3 Interrupt Control Register

0x2C: CTRL_REG3 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO_GATE	WAKE_TRANS	WAKE_LNDPRT	WAKE_PULSE	WAKE_FF_MT	—	IPOL	PP_OD

Table 68. CTRL_REG3 Description

FIFO_GATE	0: FIFO gate is bypassed. FIFO is flushed upon the system mode transitioning from WAKE to SLEEP mode or from SLEEP to WAKE mode. Default value: 0. 1: The FIFO input buffer is blocked when transitioning from WAKE to SLEEP mode or from SLEEP to WAKE mode until the FIFO is flushed. Although the system transitions from WAKE to SLEEP or from SLEEP to WAKE the contents of the FIFO buffer are preserved, new data samples are ignored until the FIFO is emptied by the host application. If the FIFO_GATE bit is set to logic '1' and the FIFO buffer is not emptied before the arrival of the next sample, then the FGERR bit in the SYS_MOD register (0x0B) will be asserted. The FGERR bit remains asserted as long as the FIFO buffer remains un-emptied. Emptying the FIFO buffer clears the FGERR bit in the SYS_MOD register.
WAKE_TRANS	0: Transient function is bypassed in SLEEP mode. Default value: 0. 1: Transient function interrupt can wake up system
WAKE_LNDPRT	0: Orientation function is bypassed in SLEEP mode. Default value: 0. 1: Orientation function interrupt can wake up system
WAKE_PULSE	0: Pulse function is bypassed in SLEEP mode. Default value: 0. 1: Pulse function interrupt can wake up system
WAKE_FF_MT	0: Freefall/Motion function is bypassed in SLEEP mode. Default value: 0. 1: Freefall/Motion function interrupt can wake up
IPOL	Interrupt polarity ACTIVE high, or ACTIVE low. Default value: 0. 0: ACTIVE low; 1: ACTIVE high
PP_OD	Push-Pull/Open Drain selection on interrupt pad. Default value: 0. 0: Push-Pull; 1: Open Drain

IPOL bit selects the polarity of the interrupt signal. When IPOL is '0' (default value) any interrupt event will signaled with a logical 0.
PP_OD bit configures the interrupt pin to Push-Pull or in Open Drain mode. The default value is 0 which corresponds to Push-Pull mode. The Open Drain configuration can be used for connecting multiple interrupt signals on the same interrupt line.

0x2D: CTRL_REG4 Register (Read/Write)

0x2D: CTRL_REG4 Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EN_ASLP	INT_EN_FIFO	INT_EN_TRANS	INT_EN_LNDPR	INT_EN_PULSE	INT_EN_FF_MT	—	INT_EN_DRDY

Table 69. Interrupt Enable Register Description

Interrupt Enable	Description
INT_EN_ASLP	Interrupt Enable. Default value: 0. 0: Auto-SLEEP/WAKE interrupt disabled; 1: Auto-SLEEP/WAKE interrupt enabled.
INT_EN_FIFO	Interrupt Enable. Default value: 0. 0: FIFO interrupt disabled; 1: FIFO interrupt enabled.
INT_EN_TRANS	Interrupt Enable. Default value: 0. 0: Transient interrupt disabled; 1: Transient interrupt enabled.
INT_EN_LNDPRT	Interrupt Enable. Default value: 0. 0: Orientation (Landscape/Portrait) interrupt disabled. 1: Orientation (Landscape/Portrait) interrupt enabled.
INT_EN_PULSE	Interrupt Enable. Default value: 0. 0: Pulse Detection interrupt disabled; 1: Pulse Detection interrupt enabled
INT_EN_FF_MT	Interrupt Enable. Default value: 0. 0: Freefall/Motion interrupt disabled; 1: Freefall/Motion interrupt enabled
INT_EN_DRDY	Interrupt Enable. Default value: 0. 0: Data Ready interrupt disabled; 1: Data Ready interrupt enabled

The corresponding functional block interrupt enable bit allows the functional block to route its event detection flags to the system's interrupt controller. The interrupt controller routes the enabled functional block interrupt to the INT1 or INT2 pin.

0x2E: CTRL_REG5 Register (Read/Write)

0x2E: CTRL_REG5 Interrupt Configuration Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_CFG_ASLP	INT_CFG_FIFO	INT_CFG_TRANS	INT_CFG_LNDPRT	INT_CFG_PULSE	INT_CFG_FF_MT	—	INT_CFG_DRDY

Table 70. Interrupt Configuration Register Description

Interrupt Configuration	Description
INT_CFG_ASLP	INT1/INT2 Configuration. Default value: 0. 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_FIFO	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_TRANS	INT1/INT2 Configuration. Default value: 0. 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_LNDPRT	INT1/INT2 Configuration. Default value: 0. 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_PULSE	INT1/INT2 Configuration. Default value: 0. 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_FF_MT	INT1/INT2 Configuration. Default value: 0. 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin
INT_CFG_DRDY	INT1/INT2 Configuration. Default value: 0. 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1 pin

The system's interrupt controller shown in Figure 10 uses the corresponding bit field in the CTRL_REG5 register to determine the routing table for the INT1 and INT2 interrupt pins. If the bit value is logic '0', the functional block's interrupt is routed to INT2, and if the bit value is logic '1', then the interrupt is routed to INT1. One or more functions can assert an interrupt pin; therefore a host application responding to an interrupt should read the INT_SOURCE (0x0C) register to determine the appropriate sources of the interrupt.

6.9 User Offset Correction Registers

For more information on how to calibrate the 0g offset, refer to application note AN4069. The 2's complement offset correction registers values are used to realign the Zero-g position of the X, Y, and Z-axis after device board mount. The resolution of the offset registers is 2 mg per LSB. The 2's complement 8-bit value would result in an offset compensation range ±256 mg.

0x2F: OFF_X Offset Correction X Register

0x2F: OFF_X Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 71. OFF_X Description

D[7:0]	X-axis offset value. Default value: 0000_0000.

0x30: OFF_Y Offset Correction Y Register

0x30: OFF_Y Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 72. OFF_Y Description

D[7:0]	Y-axis offset value. Default value: 0000_0000.

0x31: OFF_Z Offset Correction Z Register

0x31: OFF_Z Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Table 73. OFF_Z Description

D[7:0]	Z-axis offset value. Default value: 0000_0000.

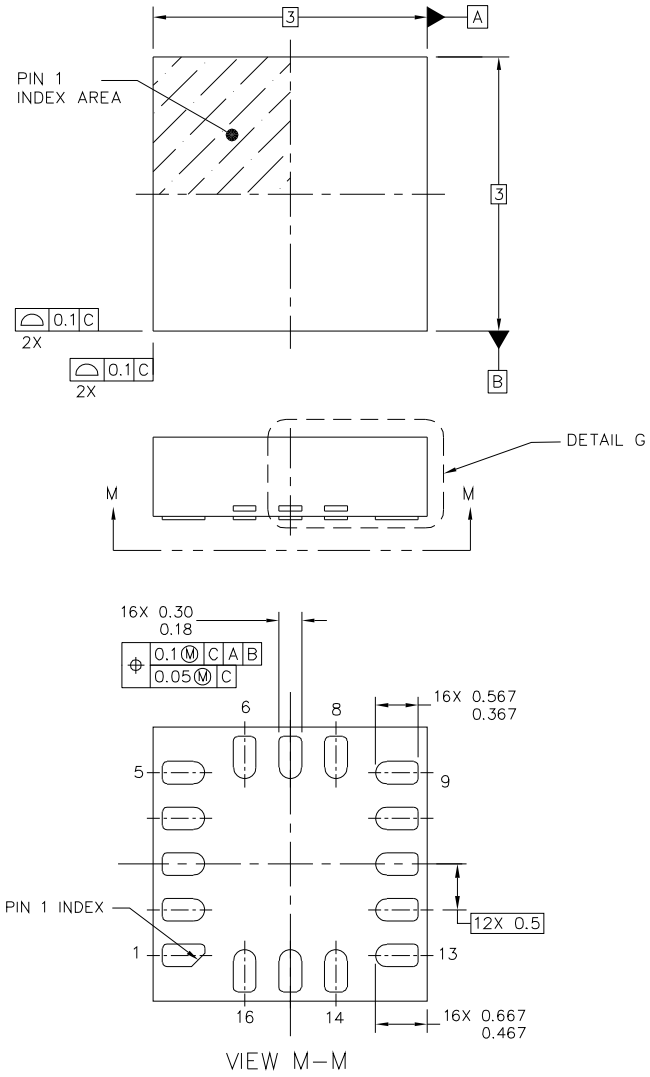
Table 74. MMA8451Q Register Map

Reg	Name	Definition	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	STATUS/F_STATUS	Data Status R	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
01	OUT_X_MSB	14 bit X Data R	XD13	XD12	XD11	XD10	XD9	XD8	XD7	XD6
02	OUT_X_LSB	14 bit X Data R	XD5	XD4	XD3	XD2	XD1	XD0	0	0
03	OUT_Y_MSB	14 bit Y Data R	YD13	YD12	YD11	YD10	YD9	YD8	YD7	YD6
04	OUT_Y_LSB	14 bit Y Data R	YD5	YD4	YD3	YD2	YD1	YD0	0	0
05	OUT_Z_MSB	14 bit Z Data R	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6
06	OUT_Z_LSB	14 bit Z Data R	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0	0	0
09	F_SETUP	FIFO Setup R/W	F_MODE1	F_MODE0	F_WMRK5	F_WMRK4	F_WMRK3	F_WMRK2	F_WMRK1	F_WMRK0
0A	TRIG_CFG	FIFO Triggers R/W	—	—	Trig_TRANS	Trig_LNDPRT	Trig_PULSE	Trig_FF_MT	—	—
0B	SYSMOD	System Mode R	FGERR	FGT_4	FGT_3	FGT_2	FGT_1	FGT_0	SYSMOD1	SYSMOD0
0C	INT_SOURCE	Interrupt Status R	SRC_ASLP	SRC_FIFO	SRC_TRANS	SRC_LNDPRT	SRC_PULSE	SRC_FF_MT	—	SRC_DRDY
0D	WHO_AM_I	ID Register R	0	0	0	1	1	0	1	0
0E	XYZ_DATA_CFG	Data Config R/W	—	—	—	HPF_Out	—	—	FS1	FS0
0F	HP_FILTER_CUTOFF	HP Filter Setting R/W	—	—	Pulse_HPF_BYP	Pulse_LPF_EN	—	—	SEL1	SEL0
10	PL_STATUS	PL Status R	NEWLP	LO	—	—	—	LAPO[1]	LAPO[0]	BAFRO
11	PL_CFG	PL Configuration R/W	DBCNTM	PL_EN	—	—	—	—	—	—
12	PL_COUNT	PL DEBOUNCE R/W	DBNCE[7]	DBNCE[6]	DBNCE[5]	DBNCE[4]	DBNCE[3]	DBNCE[2]	DBNCE[1]	DBNCE[0]
13	PL_BF_ZCOMP	PL Back/Front Z Comp R/W	BKFR[1]	BKFR[0]	—	—	—	ZLOCK[2]	ZLOCK[1]	ZLOCK[0]
14	P_L_THS_REG	PL THRESHOLD R/W	P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]	HYS[2]	HYS[1]	HYS[0]
15	FF_MT_CFG	Freefall/Motion Config R/W	ELE	OAE	ZEFE	YEFE	XEFE	—	—	—
16	FF_MT_SRC	Freefall/Motion Source R	EA	—	ZHE	ZHP	YHE	YHP	XHE	XHP
17	FF_MT_THS	Freefall/Motion Threshold R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
18	FF_MT_COUNT	Freefall/Motion Debounce R/W	D7	D6	D5	D4	D3	D2	D1	D0
1D	TRANSIENT_CFG	Transient Config R/W	—	—	—	ELE	ZTEFE	YTEFE	XTEFE	HPF_BYP
1E	TRANSIENT_SRC	Transient Source R	—	EA	ZTRANSE	Z_Trans_Pol	YTRANSE	Y_Trans_Pol	XTRANSE	X_Trans_Pol
1F	TRANSIENT_THS	Transient Threshold R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
20	TRANSIENT_COUNT	Transient Debounce R/W	D7	D6	D5	D4	D3	D2	D1	D0
21	PULSE_CFG	Pulse Config R/W	DPA	ELE	ZDPEFE	ZSPEFE	YDPEFE	YSPEFE	XDPEFE	XSPEFE
22	PULSE_SRC	Pulse Source R	EA	AxZ	AxY	AxX	DPE	Pol_Z	Pol_Y	Pol_X
23	PULSE_THSX	Pulse X Threshold R/W	—	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0
24	PULSE_THSY	Pulse Y Threshold R/W	—	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0
25	PULSE_THSZ	Pulse Z Threshold R/W	—	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0
26	PULSE_TMLT	Pulse First Timer R/W	TMLT7	TMLT6	TMLT5	TMLT4	TMLT3	TMLT2	TMLT1	TMLT0
27	PULSE_LTCY	Pulse Latency R/W	LTCY7	LTCY6	LTCY5	LTCY4	LTCY3	LTCY2	LTCY1	LTCY0
28	PULSE_WIND	Pulse 2nd Window R/W	WIND7	WIND6	WIND5	WIND4	WIND3	WIND2	WIND1	WIND0
29	ASLP_COUNT	Auto-SLEEP Counter R/W	D7	D6	D5	D4	D3	D2	D1	D0
2A	CTRL_REG1	Control Reg1 R/W	ASLP_RATE1	ASLP_RATE0	DR2	DR1	DR0	LNOISE	F_READ	ACTIVE
2B	CTRL_REG2	Control Reg2 R/W	ST	RST	—	SMODS1	SMODS0	SLPE	MODS1	MODS0
2C	CTRL_REG3	Control Reg3 (WAKE Interrupts from SLEEP) R/W	FIFO_GATE	WAKE_TRANS	WAKE_LNDPRT	WAKE_PULSE	WAKE_FF_MT	—	IPOL	PP_OD
2D	CTRL_REG4	Control Reg4 (Interrupt Enable Map) R/W	INT_EN_ASLP	INT_EN_FIFO	INT_EN_TRANS	INT_EN_LNDPRT	INT_EN_PULSE	INT_EN_FF_MT	—	INT_EN_DRDY
2E	CTRL_REG5	Control Reg5 (Interrupt Configuration) R/W	INT_CFG_ASLP	INT_CFG_FIFO	INT_CFG_TRANS	INT_CFG_LNDPRT	INT_CFG_PULSE	INT_CFG_FF_MT	—	INT_CFG_DRDY
2F	OFF_X	X 8-bit offset R/W	D7	D6	D5	D4	D3	D2	D1	D0
30	OFF_Y	Y 8-bit offset R/W	D7	D6	D5	D4	D3	D2	D1	D0
31	OFF_Z	Z 8-bit offset R/W	D7	D6	D5	D4	D3	D2	D1	D0

Table 75. Accelerometer Output Data

14-bit Data	Range ±2g (0.25 mg)	Range ±4g (0.5 mg)	Range ±8g (1.0 mg)
01 1111 1111 1111	1.99975g	+3.9995g	+7.999g
01 1111 1111 1110	1.99950g	+3.9990g	+7.998g
…	…	…	…
00 0000 0000 0001	0.00025g	+0.0005g	+0.001g
00 0000 0000 0000	0.00000g	0.00000g	0.000g
11 1111 1111 1111	-0.00025g	-0.0005g	-0.001g
…	…	…	…
10 0000 0000 0001	-1.99975g	-3.9995g	-7.999g
10 0000 0000 0000	-2.00000g	-4.0000g	-8.000g
8-bit Data	**Range ±2g (15.6 mg)**	**Range ±4g (31.25 mg)**	**Range ±8g (62.5 mg)**
0111 1111	1.9844g	+3.9688g	+7.9375g
0111 1110	1.9688g	+3.9375g	+7.8750g
…	…	…	…
0000 0001	+0.0156g	+0.0313g	+0.0625g
0000 0000	0.000g	0.0000g	0.0000g
1111 1111	-0.0156g	-0.0313g	-0.0625g
…	…	…	…
1000 0001	-1.9844g	-3.9688g	-7.9375g
1000 0000	-2.0000g	-4.0000g	-8.0000g

PACKAGE DIMENSIONS



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	CASE NUMBER: 2077–02	20 OCT 2011
	STANDARD: NON JEDEC	

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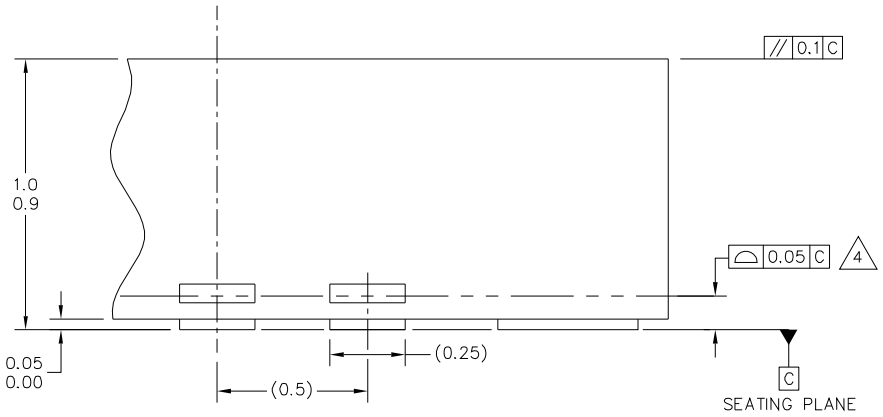

DETAIL G

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16-LEAD QFN

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THIS IS NON JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO ALL LEADS.
5. MIN. METAL GAP SHOULD BE 0.2MM.

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: QUAD FLAT NO LEAD COL PACKAGE (QFN–COL) 16 TERMINAL, 0.5 PITCH (3 X 3 X 1.0)	DOCUMENT NO: 98ASA00063D	REV: A
	CASE NUMBER: 2077–02	20 OCT 2011
	STANDARD: NON JEDEC	

CASE 2077-02
ISSUE A
16-LEAD QFN

Table 76. Revision History

Revision number	Revision date	Description of changes
7	03/2012	• Table 2. Updated Typ values for Sensitivity Accuracy from 2.5% to 2.64%; Zero-g Level Offset Accuracy from ±20 mg to ±17 mg and Zero-g Level Offset Accuracy Post Board Mount from ±30 mg to ±20 mg. • Table 4. Updated Min value from 50 µs to 0.05 µs and added Max value of 0.9 µs • Added Table 8. Features of the MMA845xQ devices. • Removed FIFO paragraph at the end of Section 6.1. • Updated Note preceding Table 32 from "THS + HYS > 0 and THS + HYS < 49... " to "The condition THS + HYS > 0 and THS + HYS < 32 must be met in order for Landscape/Portrait detection to work properly...." • Updated Case outline with current version.
7.1	05/2012	• Updated Figure 5 to correspond to table.
8	02/2013	• Replaced Section 2.3 I^2C interface characteristics, including Table 4 and Figure 5.

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