CMOS Circuit Design Spice Simulation

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Contents

1 Day 1

1.1 NMOS Analysis

1.1.1 Structure of NMOS

A typical MOS transistor is a majority-carrier device in which the current in a conducting channel between the source and drain is controlled by a voltage applied to the gate. In nMOS transistor the majority carriers are electrons; in a pMOS transistor the majority carriers are holes.

A typical nMOS transistor is

- 4-terminal device called Gate-G, Source-S, Drain-D, Body-B
- A P-substrate which is light-moderately doped
- Isolation region which is used isolate other transistor so that they don't interfere and operate as a single unit.
- n^+ diffusion region which is heavily doped etched into the P-Substrate.
- Gate oxide placed over the p-substrate, this is the Metal Oxide
- Poly-Si or metal gate placed on top of the Gate oxide

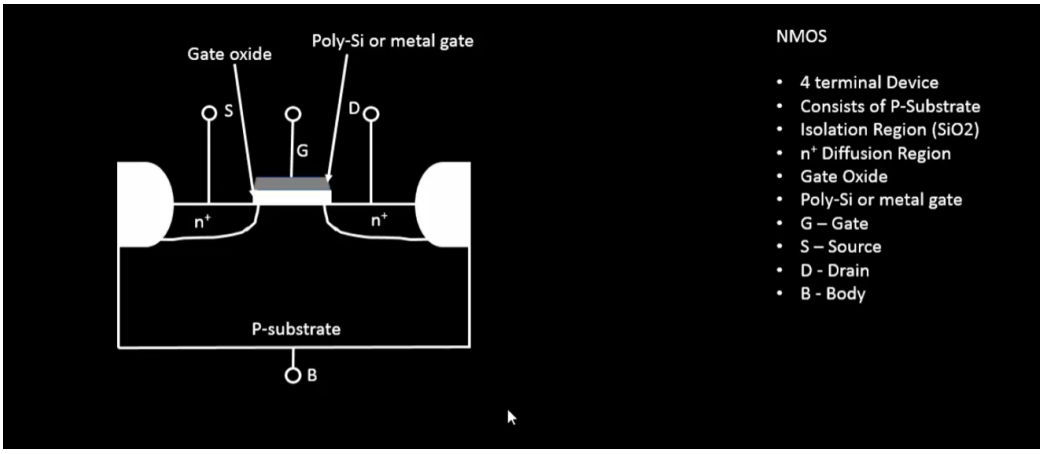

Figure 1: nMOS Structure

1.1.2 I-V Characteristics

nMOS transistors have 3 modes of operation.

- Cutoff or subthreshold mode
- Linear mode
- Saturation mode

1.1.3 Cutoff Mode

We will analyze two scenarios:

1. When $V_{SB} = 0$ (source-to-body voltage is zero). As V_{GS} increases, the h^+ carriers are repelled from the gate region, creating a depletion layer that merges with the existing depletion regions. With further increase in V_{GS}, charge accumulation leads to **strong inversion**. The gate voltage at which this occurs is the **threshold voltage** V_{T0}.
2. When both the source and drain are connected to a voltage source (source positive, drain negative). In this case, a higher V_{GS} is required for strong inversion. The threshold voltage is given by:

$$V_T = V_{T0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

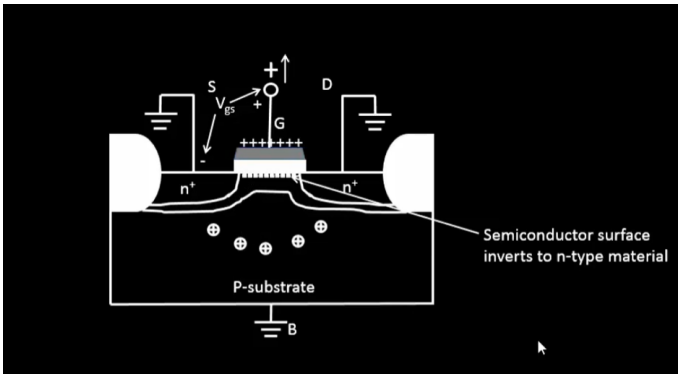

Figure 2: $V_{SB} = 0$

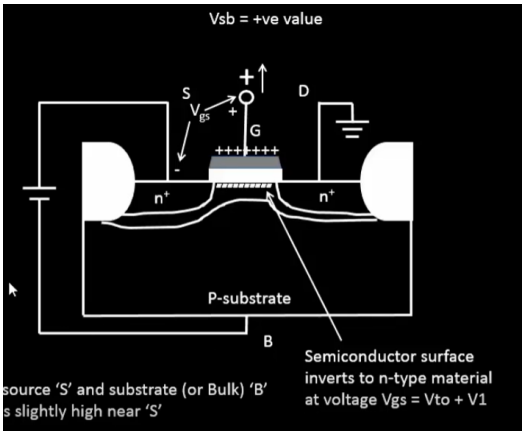

Figure 3: $V_{SB} > 0$

1.1.4 Linear Mode

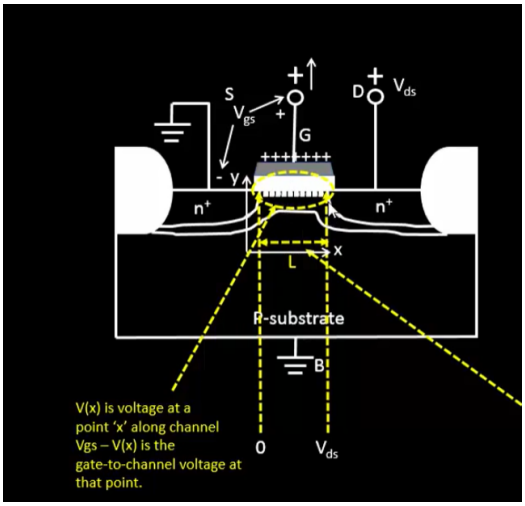

Figure 4: Linear Mode: $V_{ds} < V_{gs} - V_t$

Applying a small V_{DS} voltage at the drain causes a current I_D (drain current) to flow from drain to source. The drain current equation is given by:

$$I_D = \mu_n C_{\text{ox}} \left(\frac{W}{L} \right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

1.1.5 Saturation Mode

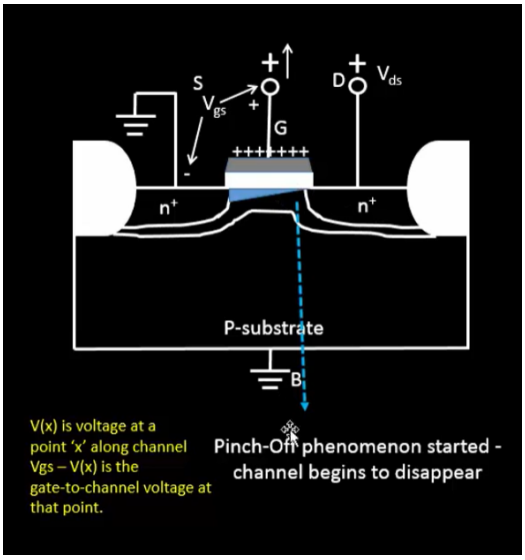

Figure 5: Saturation Mode: $V_{ds} > V_{gs} - V_t$

At higher values of V_{DS}, V_{GS} no longer has full control over channel modulation, and I_D remains almost constant (though not entirely). When $V_{GS} - V_{DS} = V_T$, the transistor reaches the **pinch-off condition**.

The drain current in this region is given by:

$$I_D = \mu_n C_{\text{ox}} \left(\frac{W}{L}\right) \frac{(V_{GS} - V_T)^2}{2}$$

However, in reality, there is a slight dependence of I_D on V_{DS}, expressed as:

$$I_D = \mu_n C_{\text{ox}} \left(\frac{W}{L}\right) \frac{(V_{GS} - V_T)^2}{2} (1 + \lambda V_{DS})$$

where λ is the **channel length modulation parameter**.

1.2 SPICE Simulation

1.2.1 SPICE Model for NMOS

Now, we will create a SPICE model for the NMOS transistor using the following region-wise equations:

$$I_D = \begin{cases} 0, & \text{Cutoff Region: } V_{GS} < V_T \\ k'_n \left(\frac{W}{L}\right) \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right], & \text{Linear Region: } V_{DS} < V_{GS} - V_T \\ k'_n \left(\frac{W}{L}\right) \frac{(V_{GS} - V_T)^2}{2} (1 + \lambda V_{DS}), & \text{Saturation Region: } V_{DS} \geq V_{GS} - V_T \end{cases}$$

The threshold voltage including the body effect is given by:

$$V_T = V_{T0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

where the model parameters are:

- k'_n — Process transconductance parameter ($k'_n = \mu_n C_{\text{ox}}$)
- V_{T0} — Zero-bias threshold voltage
- γ — Body effect coefficient
- ϕ_F — Fermi potential
- λ — Channel length modulation parameter

1.2.2 SPICE Setup

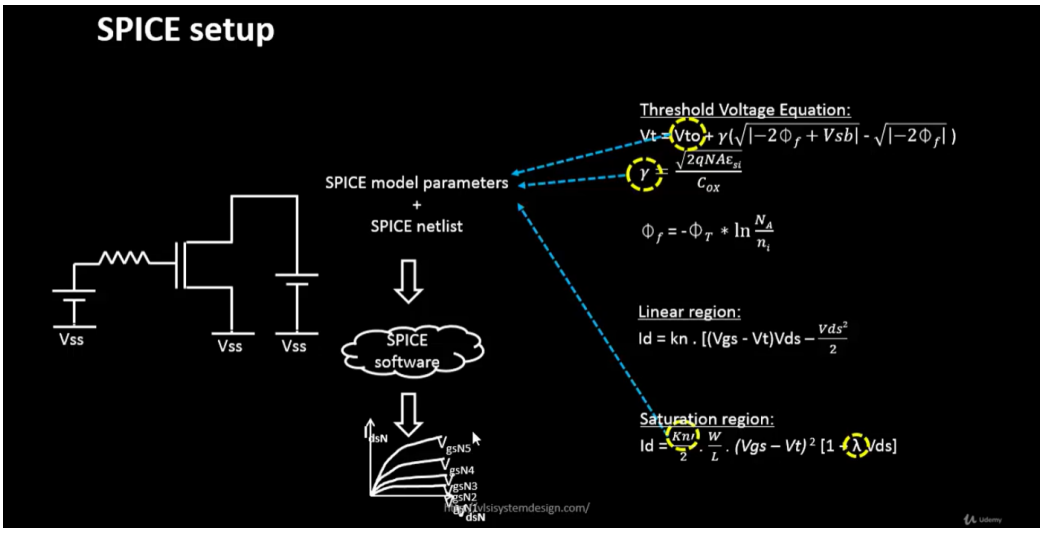

Figure 6: SPICE Setup

1.2.3 Netlist Description

Consider the circuit below.

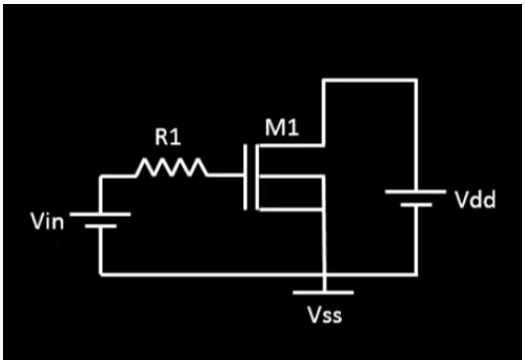

Figure 7: NMOSFET Circuit

The full SPICE description of the circuit includes the node assignments, transistor models, and voltage sources. Each figure below shows the schematic,

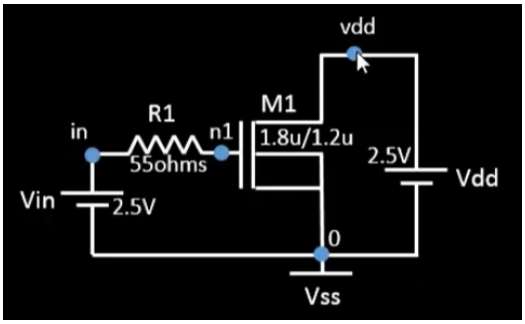

Figure 8: Circuit with nodes labeled

```
*Netlist Description


XM1 Vdd n1 0 0 sky130_fd_pr__nfet_01v8 w=1.8 l=1.2

R1 n1 in 55

Vdd vdd 0 2.5V
Vin in 0 2.5V
```

Figure 9: SPICE Netlist for the above circuit

labeled nodes, and corresponding netlist to simulate the NMOSFET operation.

```
*Model Description
.param temp=27


*Including sky130 library files
.lib "sky130_fd_pr/models/sky130.lib.spice" tt


*Netlist Description



XM1 Vdd n1 0 0 sky130_fd_pr__nfet_01v8 w=1.8 l=1.2

R1 n1 in 55

Vdd vdd 0 2.5V
Vin in 0 2.5V

*simulation commands

.op
.dc Vdd 0 2.5 0.1 Vin 0 2.5 0.2

.control

run
display
setplot dc1
.endc

.end
```

Figure 10: Circuit including model files

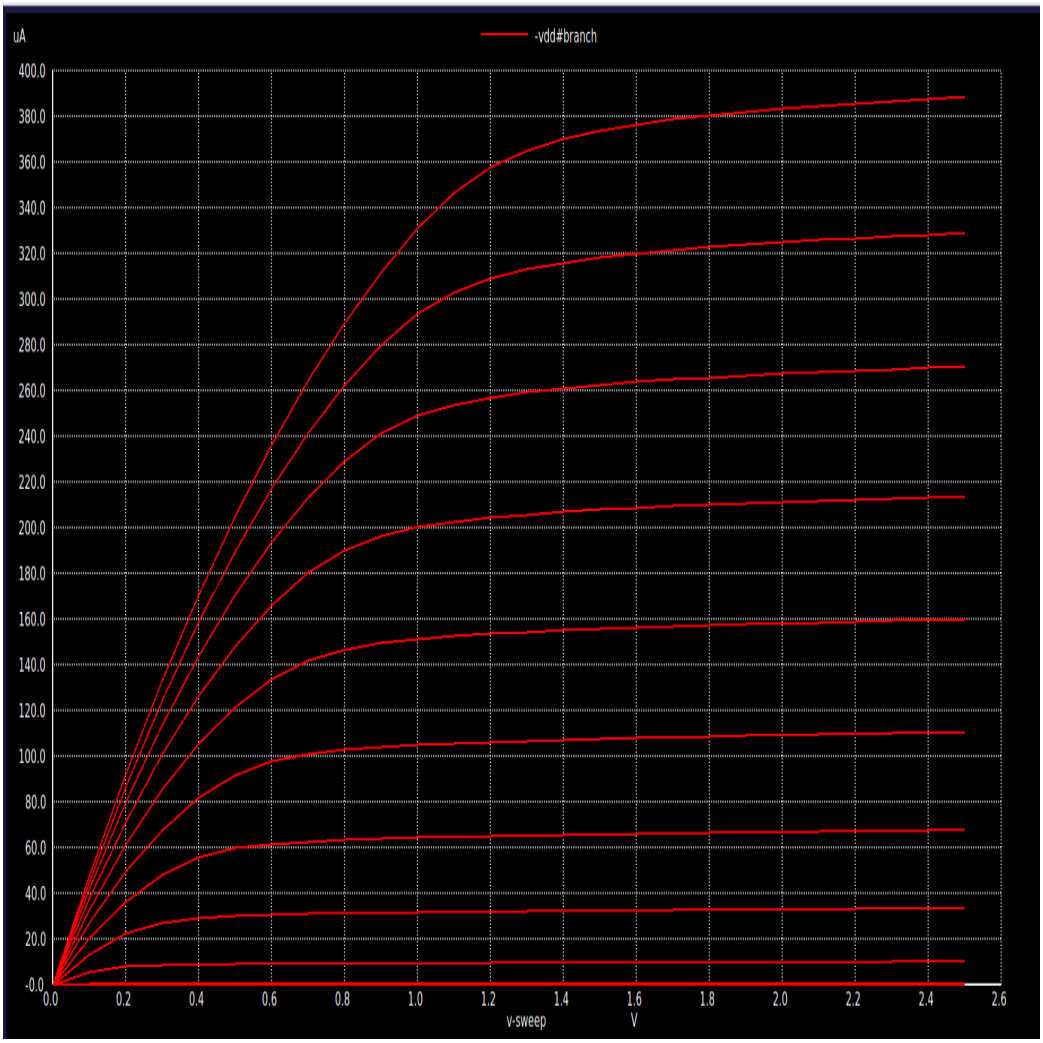

Figure 11: I-V Charactersitics of nMOSFET

2 Day 2

2.1 Velocity Saturation Effect

2.1.1 Long Channel vs Short Channel Effects

For a **long-channel device**, the drain current I_D in the saturation region has a quadratic dependence on V_{GS} for a particular V_{DS}. This is reflected in the drain current equation:

$$I_D = k'_n \left(\frac{W}{L}\right) \frac{(V_{GS} - V_T)^2}{2} (1 + \lambda V_{DS})$$

For a **short-channel device**, I_D shows quadratic dependence at lower V_{GS}, but at higher V_{GS}, it exhibits a linear dependence. This linear behavior is due to the **velocity saturation effect**.

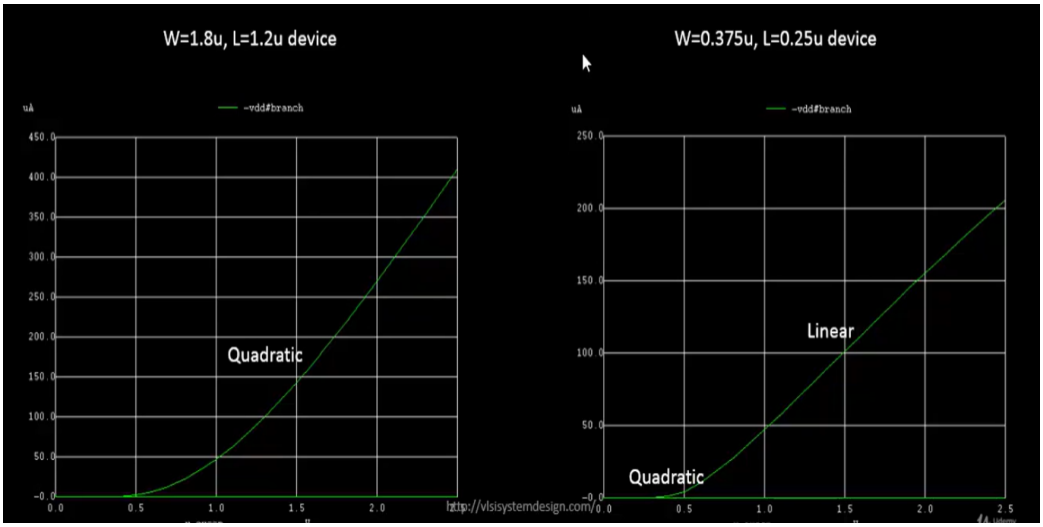

Figure 12: $I_D vs V_{GS}$ for long and short channel

2.1.2 Velocity Saturation Mode

Velocity saturation effect occurs at higher electric fields, where the carrier drift velocity reaches a maximum (saturation) value. At lower electric fields, the drift velocity varies linearly with the electric field.

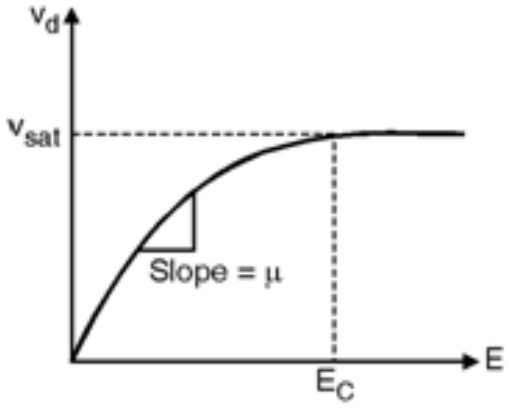

Figure 13: velocity saturation at higher fields

We need to re-derive the drain current equation which includes the velocity saturation effect. We will use a model that makes the **velocity saturation effect as a mode of operation**. The modes of operation for long channel and short channel is given below:

Long Channel (>250nm)	Short Channel (<250nm)
Cutoff	Cutoff
Resistive	Resistive
	Velocity Saturation
Saturation	Saturation

Figure 14: Modes Of Operation

The model we use for the drain current:

$$I_D = k_n \left[(V_{GT}) V_{\min} - \frac{V_{\min}^2}{2} \right] (1 + \lambda V_{DS})$$

where

$$V_{\min} = \min(V_{GT}, V_{DS}, V_{DSAT}), \quad V_{GT} = V_{GS} - V_T$$

Here, V_{DSAT} is the drain-source voltage at which velocity saturation occurs.

Note: V_{DSAT} is a model parameter in SPICE simulations.

- if $V_{\min}$=V_{GT}, it represents Saturation Region.

$$I_D = k_n' \left(\frac{W}{L}\right) (V_{GT})^2 (1 + \lambda V_{DS})$$

- if $V_{\min}$=V_{DS}, it represents Linear Region.

$$I_D = k_n \left[(V_{GT})V_{DS} - \frac{V_{DS}^2}{2}\right] (1 + \lambda V_{DS})$$

  V_{DS} is very less so λV_{DS}<<1

- if $V_{\min}$=V_{DSAT}, it represents Velocity Saturation Region.

$$I_D = k_n \left[(V_{GT})V_{DSAT} - \frac{V_{DSAT}^2}{2}\right] (1 + \lambda V_{DS})$$

As the effective **channel length decreases** I_D **also decreases.** this is due to velocity saturation effect.

2.2 CMOS Inverter

2.2.1 MOS-Transistor as a switch

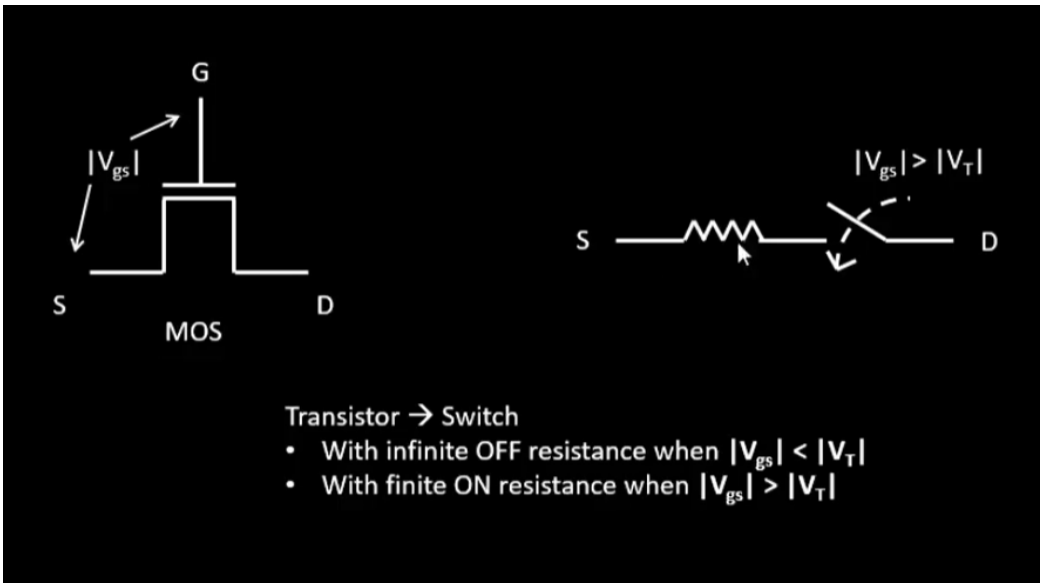

Figure 15: MOSFET modeled as a switch

The MOS transistor can be modeled as an electronic switch. Its behavior depends on the gate-to-source voltage (V_{GS}) relative to the threshold voltage (V_T):

- It behaves as an **open switch** (infinite OFF resistance) when $|V_{GS}| < |V_T|$.
- It behaves as a **closed switch** (finite ON resistance) when $|V_{GS}| > |V_T|$.

2.2.2 CMOS Inverter Operation

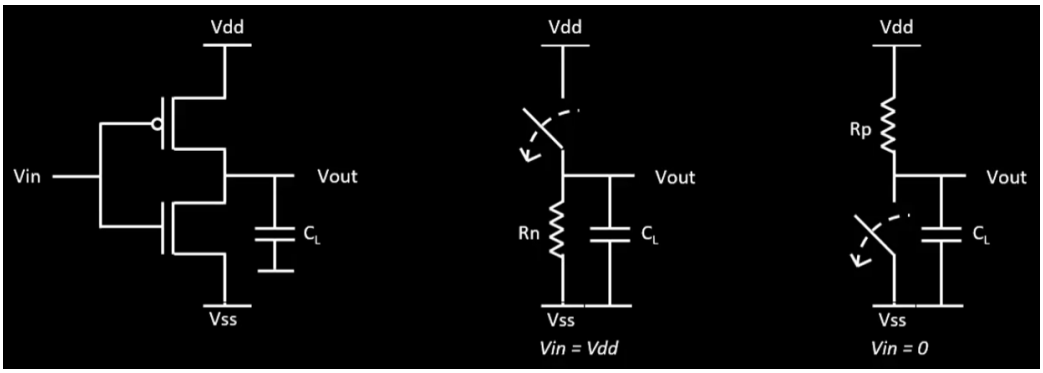

Figure 16: cmos inverter switch model

When the input voltage V_{in} is high ($V_{in} = V_{DD}$), the nMOS transistor turns ON while the pMOS transistor turns OFF. As a result, the output node is connected to ground through the conducting pMOS, producing a **logic LOW output** ($V_{out} \approx 0$).

When the input voltage V_{in} is low ($V_{in} = 0$), the pMOS transistor turns ON and the nMOS transistor turns OFF. The output node is then connected to V_{DD} through the conducting pMOS, producing a **logic HIGH output** ($V_{out} \approx V_{DD}$).

2.3 CMOS Transfer Characteristics

Consider the following circuit below.

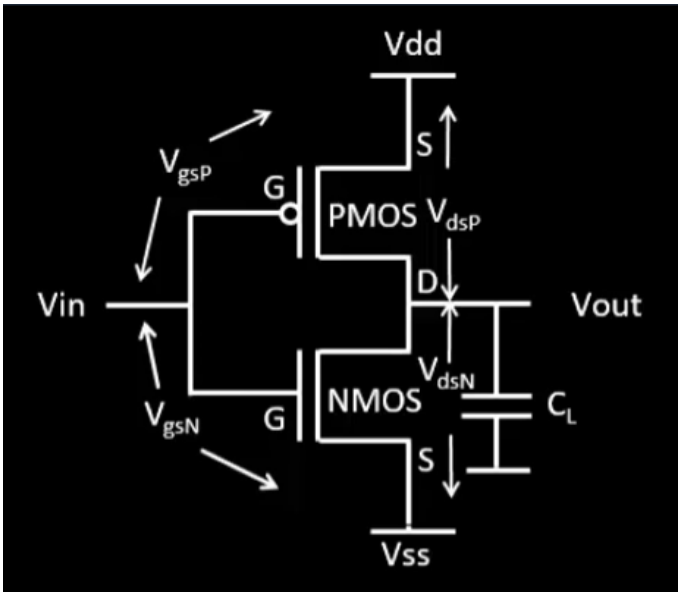

Figure 17: CMOS Inverter

The Voltage Transfer Characteristics is defined as the relation between the output voltage V_{out} and input voltage V_{in}

From the Plot of VTC below:

1. Low Input Region:
For small values of V_{in} (near 0 V), the pMOS transistor operates in the *linear region* and conducts strongly, while the nMOS transistor remains OFF. Consequently, the output voltage stays close to V_{DD}, representing a logic HIGH.

2. Transition Region:
As V_{in} increases, the nMOS begins to turn ON and enters *saturation*, while the pMOS gradually moves toward saturation. In this region, both transistors conduct simultaneously, and the output voltage V_{out} falls rapidly. This steep portion of the curve corresponds to the switching region of the inverter, where the circuit exhibits high voltage gain.

3. High Input Region:
When V_{in} approaches V_{DD}, the nMOS enters the *linear region* (acting as a strong pull-down path), and the pMOS turns OFF. As a result, the output voltage drops close to 0 V, producing a logic LOW.

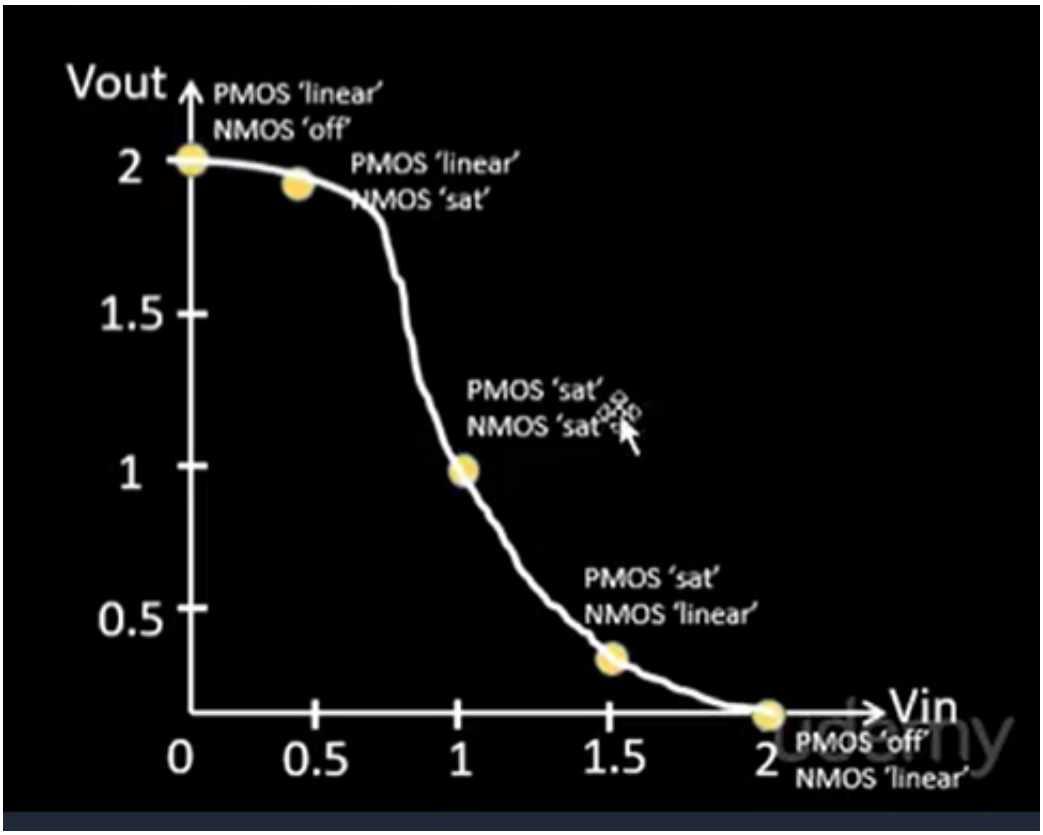

Figure 18: Voltage Transfer Characteristics

3 Day 3

3.1 Static behavior-CMOS inverter robustness – Switching Threshold

3.1.1 Swithcing Threshold

The **switching threshold** is the point on the Voltage Transfer Characteristic (VTC) curve where the input voltage equals the output voltage ($V_{in} = V_{out}$). It represents the transition point of the CMOS inverter from the logic HIGH state to the logic LOW state.

Below, we have plotted the VTCs of two CMOS inverters with different (W/L) ratios for the PMOS and NMOS transistors.

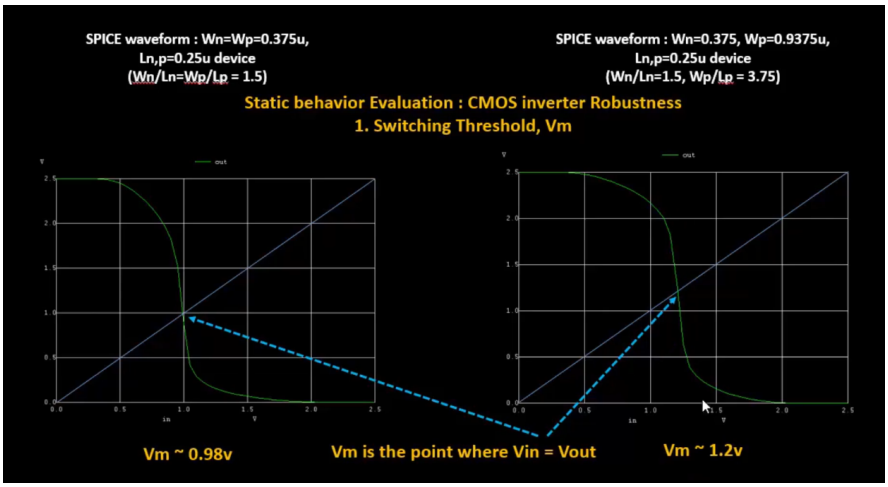

Figure 19: Swithcing Threshold

From the plots, it can be inferred that the switching threshold voltage depends on the relative (W/L) ratios of the PMOS and NMOS devices. By adjusting these ratios, the switching point can be shifted closer to either V_{DD} or ground, allowing control over the inverter's noise margins and switching behavior.

3.1.2 Expression for Switching Threshold V_m

3.1.3 Calculation of Switching Threshold Voltage V_m

- When the ratios $(W/L)_n$ and $(W/L)_p$ are known, the switching threshold voltage V_m can be determined using the following conditions and equations.

  1. At the switching point, both transistors conduct equally:

  $$I_{dsp} + I_{dsn} = 0$$

  2. The drain current equation for each transistor is given by:

  $$I_D = k_n \left[(V_{GS} - V_t) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right]$$

  The resulting expression for the switching threshold voltage is:

  $$V_m = V_{DD} \cdot \frac{R}{1+R}$$

  where

  $$R = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

  The transconductance parameters for each device are defined as:

  $$k_p = (W/L)_p \, k'_p \quad \text{and} \quad k_n = (W/L)_n \, k'_n$$

- Another Expression when V_m is known. Using the same steps as above we get the following expression:

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSATn} \left[(V_m - V_{tn}) - \frac{V_{DSATn}}{2} \right]}{k'_p V_{DSATp} \left[(V_{DD} - V_m + V_{tp}) - \frac{V_{DSATp}}{2} \right]}$$

3.1.4 Effects of (W/L) ratios

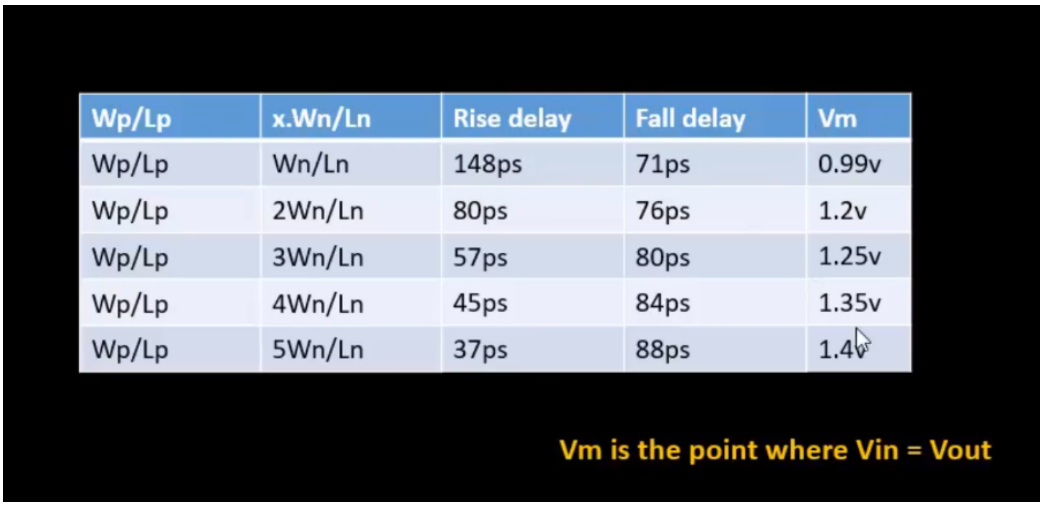

Figure 20: Rise and fall delay for different ratios

Key Observations about the CMOS Inverter:

- The switching threshold voltage (V_m) shows minimal variation with changes in pMOS size relative to nMOS. This insensitivity is advantageous during fabrication, as small process variations have limited impact on V_m.
- Increasing $(W/L)_p$ reduces the rise delay since a stronger pMOS transistor charges the load capacitance more rapidly.
- The rise and fall delays become nearly equal when $(W/L)_p = 2(W/L)_n$. This ratio is preferred in clock inverter design for achieving symmetrical transition characteristics.
- Other (W/L) ratios are selected based on design requirements in data path circuits, where unequal rise and fall times may be advantageous for optimizing read and write operations.

4 Day 4

4.1 Static behavior evaluation – CMOS inverter robustness – Noise margin

4.1.1 Noise Margins

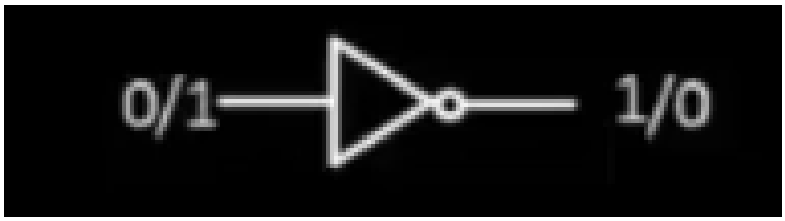

Figure 21: Inverter

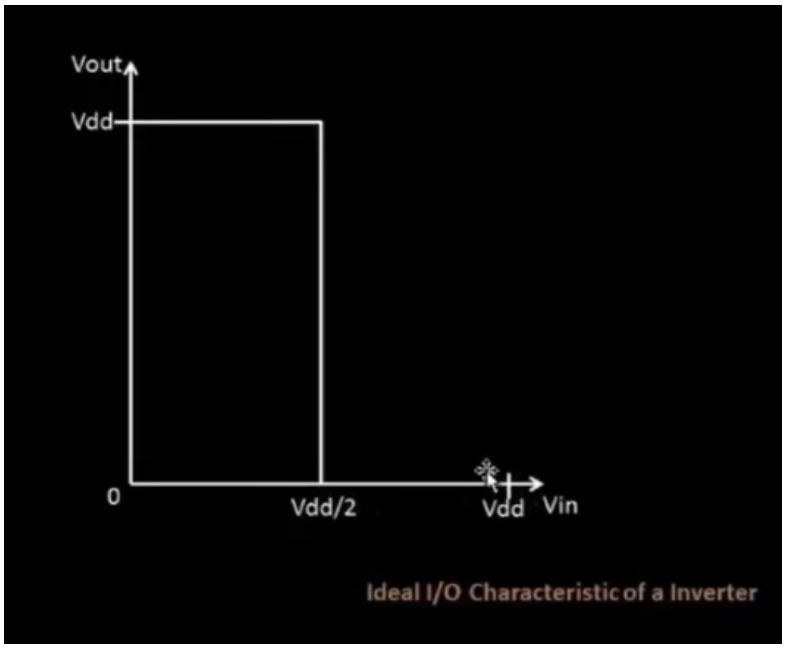

Figure 22: Ideal I/O characteristics

Consider the inverter circuit above and the ideal I/O characteristics.
When V_{in} is in range$[0, \frac{V_{DD}}{2}]$, we consider it as **logic '0'**. When V_{in} is in

range[$\frac{V_{DD}}{2}$,V_{DD}], we consider it as **logic '1'**.

Similarly, when $V_{out} = V_{DD}$ output is **logic '1'**.
When $V_{out} = 0$ output is **logic '0'**.

Now considering the actual I/O Characteristics Of CMOS Inverter

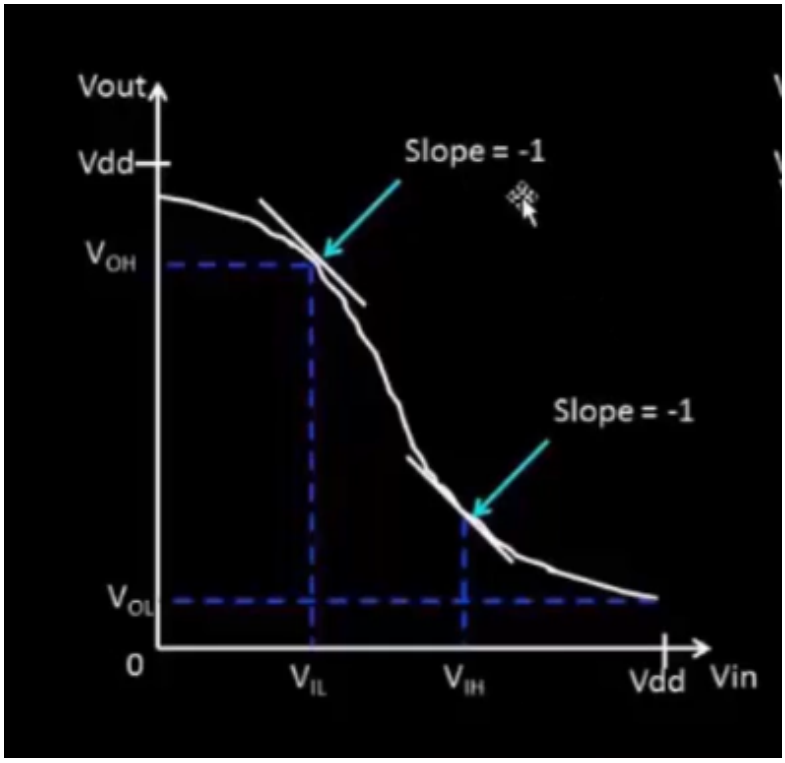

Figure 23: Real I/O characteristics

Figure 23 shows the voltage transfer characteristic (VTC) of a digital inverter, plotting output voltage V_{out} against input voltage V_{in}. This curve reveals how the inverter switches between logic high (1) and low (0) states. The key voltage levels are:

V_{OL}: Maximum output for logic low (near 0 V). V_{OH}: Minimum output for logic high (near V_{DD}). V_{IL}: Maximum input recognized as logic low. V_{IH}: Minimum input recognized as logic high.

The points where the slope equals -1 (unity gain) define the transition region's boundaries, ensuring sharp switching. Noise margins measure the

inverter's tolerance to voltage noise or interference, preventing logic errors. They are defined as:

$NM_L = V_{IL} - V_{OL}$ (low-state margin), $NM_H = V_{OH} - V_{IH}$ (high-state margin).

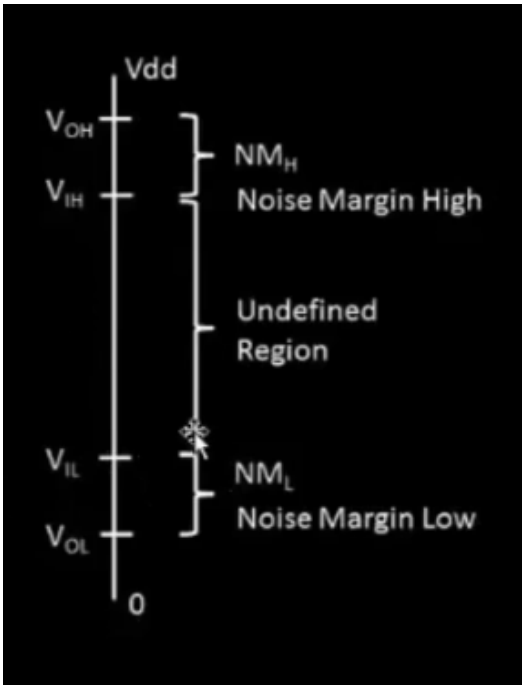

Figure 24: Noise Margins

4.1.2 Importance Of Noise Margins

Noise can be viewed as small unwanted variations or "bumps" in the input and output voltage signals. By defining a **noise margin**, the CMOS inverter establishes a tolerance level for such disturbances, ensuring that small voltage glitches do not cause unintended logic state changes.

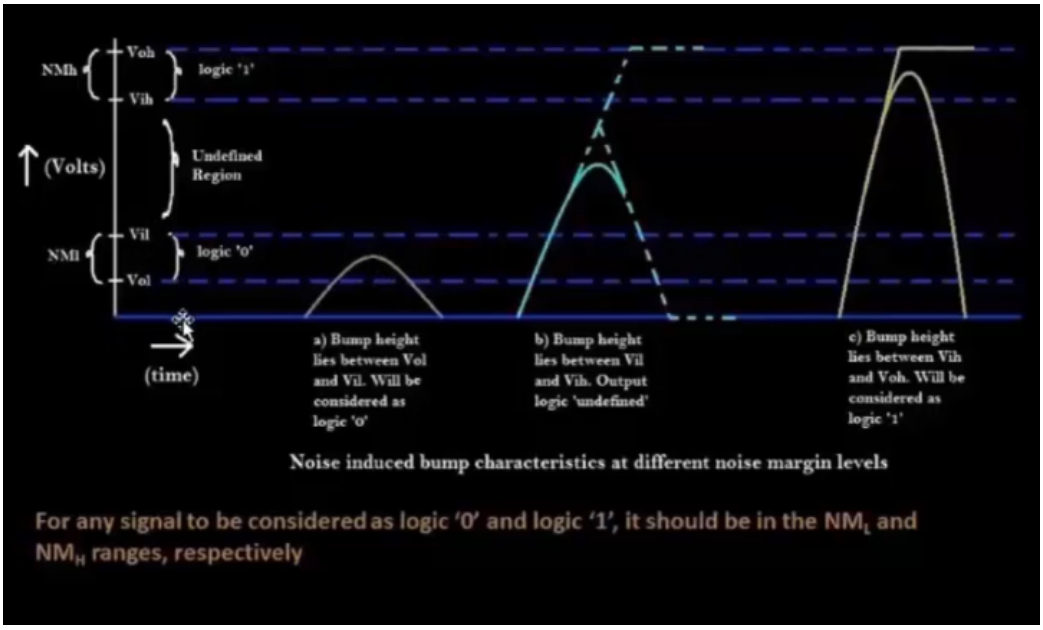

Figure 25: Summary Of Noise Margin

4.1.3 Variation Of Noise Margin with p-MOS width

Wp/Lp	x.Wn/Ln	NM_H	NM_L	Vm
Wp/Lp	Wn/Ln	0.3	0.3	0.99v
Wp/Lp	2Wn/Ln	0.35	0.3	1.2v
Wp/Lp	3Wn/Ln	0.4	0.3	1.25v
Wp/Lp	4Wn/Ln	0.42	0.27	1.35v
Wp/Lp	5Wn/Ln	0.42	0.27	1.4v

Figure 26:

We observe that variations in NM_H and NM_L remain within a range of approximately 50 mV as the pMOS width is varied. This characteristic is highly advantageous during the fabrication process, where slight deviations in the actual transistor width may occur due to process imperfections. Despite these variations, the noise margins exhibit only minimal change, ensuring robust inverter performance.

4.1.4 Preferred Region of Operation

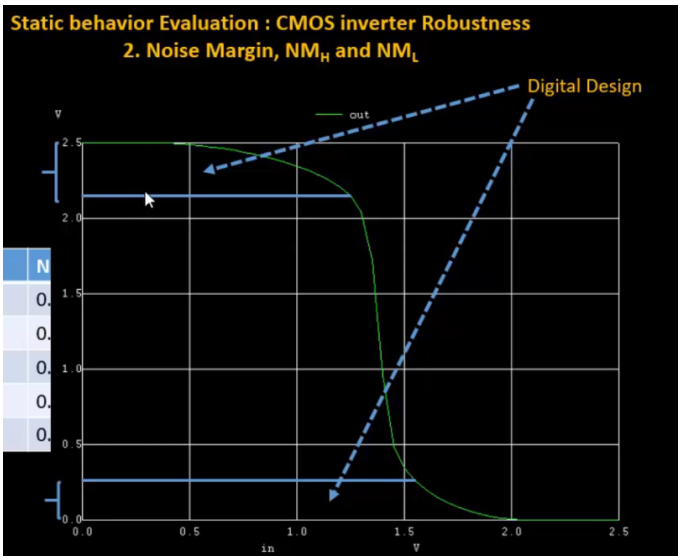

Figure 27: Digital Designs

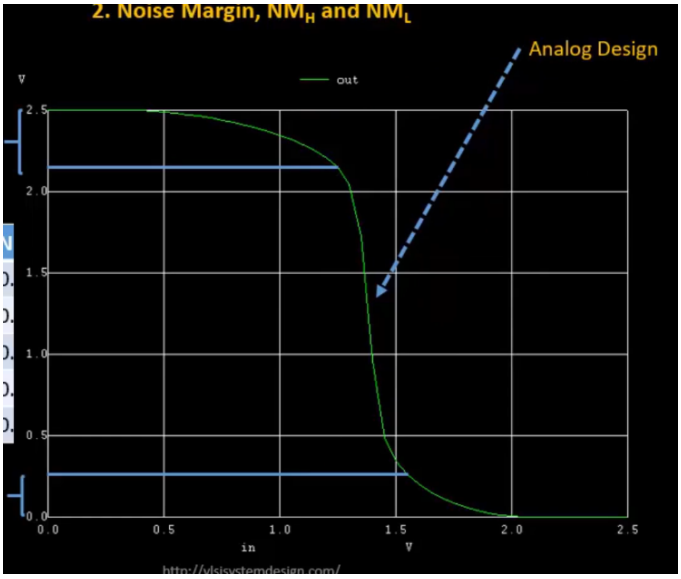

Figure 28: Analog Designs

5 Day 5

5.1 Static behavior evaluation – CMOS inverter robustness

5.1.1 Power Supply Variation

We will Study the VTC of CMOS inverter for different power supply voltage values

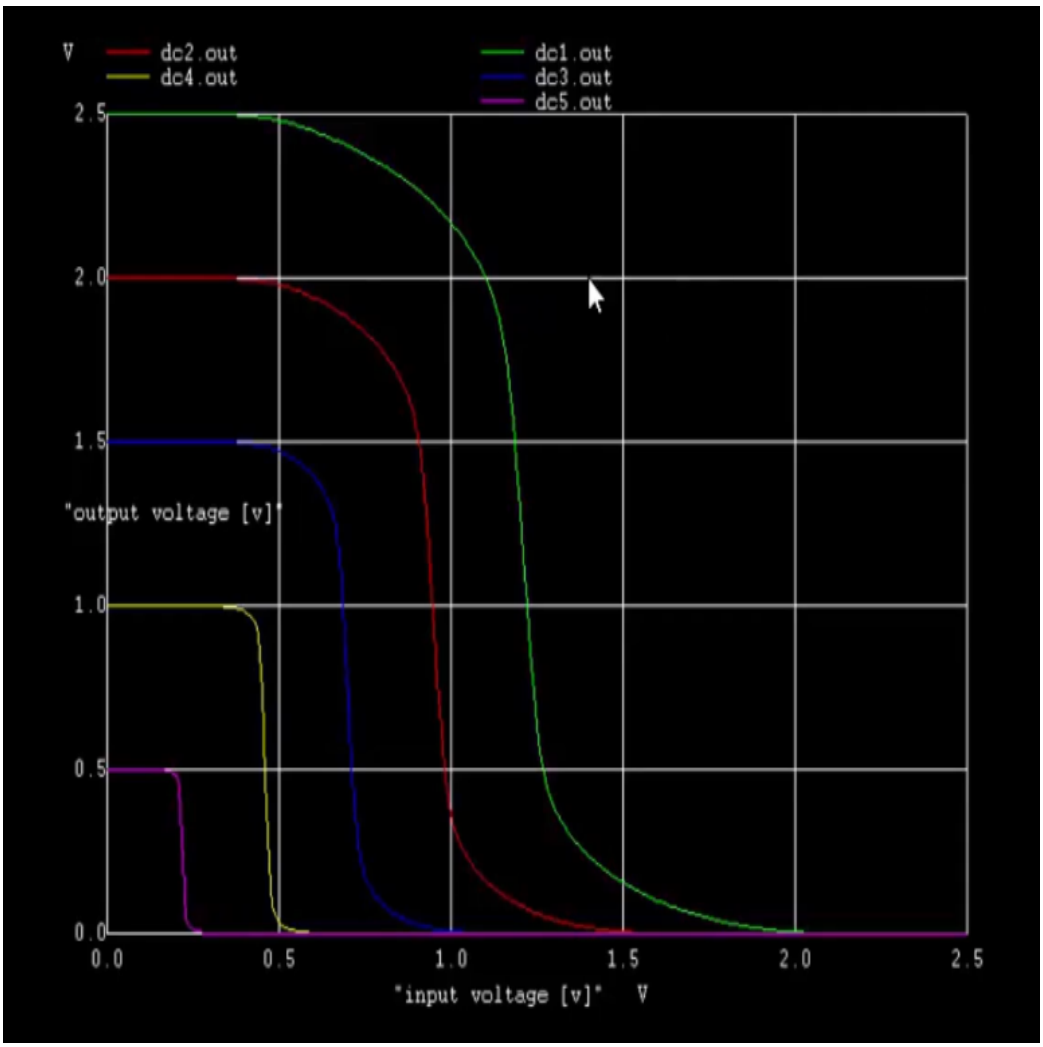

Figure 29: I/O Characteristics with different Power Supply

Key Observations

- Even with variation of Power Supply, we see that the inverter operation is still intact, showcasing its robustness towards power supply variation.
- Advantages of low power supply operation
    1. Increased gain close to **50 percent**
    2. Significant reduction in energy close to **90 percent**
- Disadvantages of low power supply operation.
    1. There is a significant increase in Rise time and Fall delay times. Leading to performance issues.
    2. Transient Response for $V_{DD} = 2.5V$

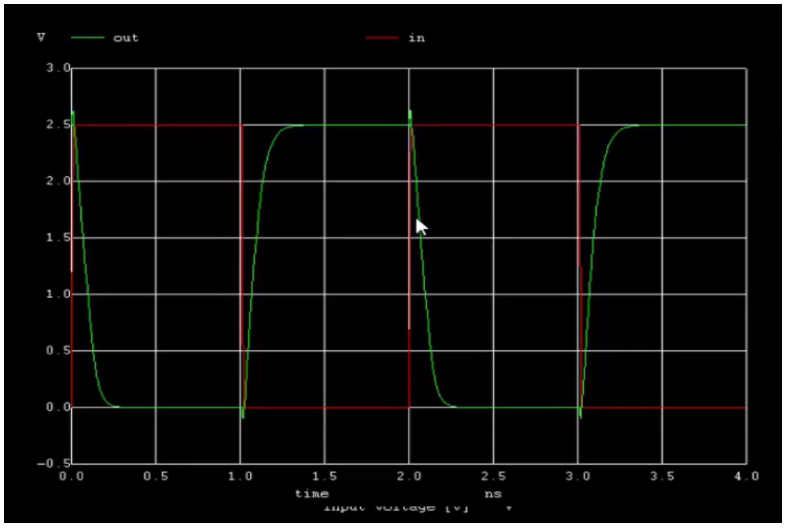

Figure 30: Less rise and fall delay time.

3. Transient Response for $V_{DD} = 0.5V$

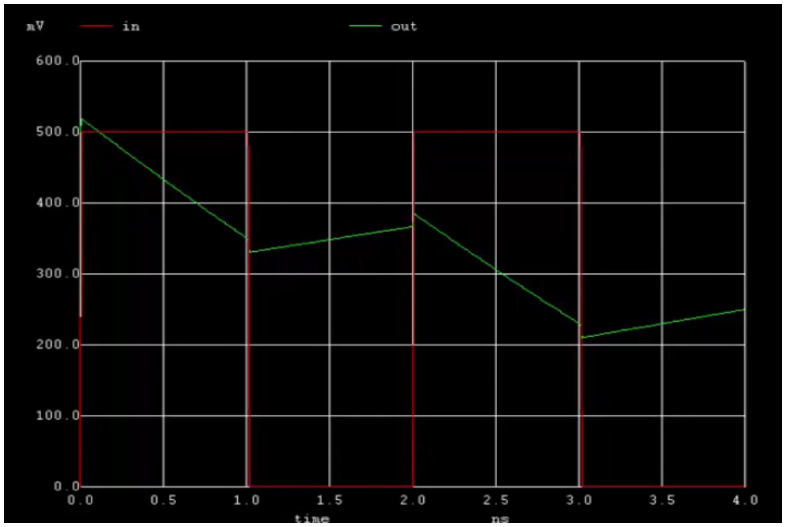

Figure 31: More rise and fall delay time.

5.1.2 Device Variation

Source Of Variation-Etching Process Consider the circuit below. If we go closer and we can see its layout which is given below.

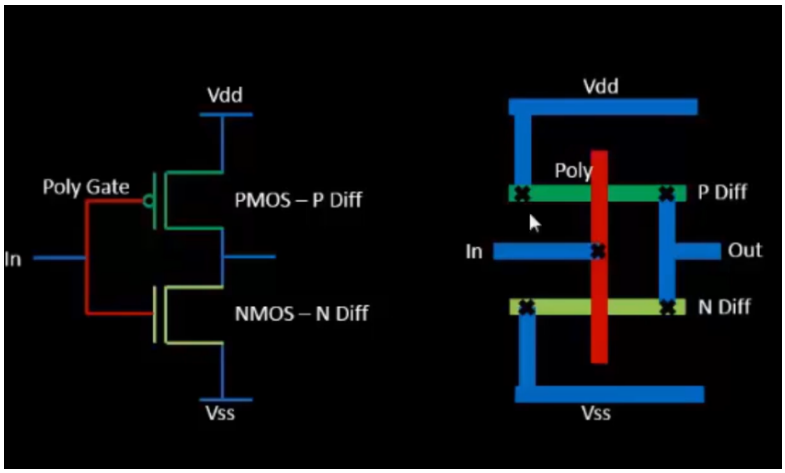

Figure 32: Layout Of Inverter

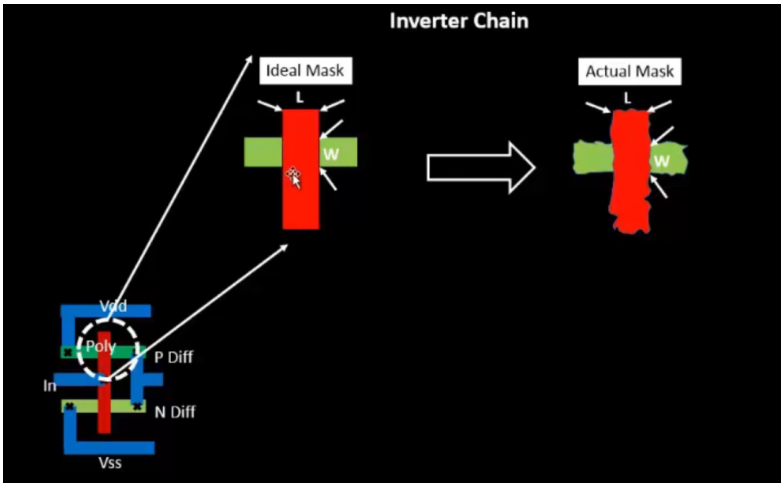

Figure 33: Ideal vs Real Masking

If we zoom into the P-Diffusion and Poly Gate intersection. We can see the masking.
Ideal masking is where the Area, L and W are well defined.
Real Masking contains distorted edges. The Area, L, W are not well defined.

It effects the drain current.

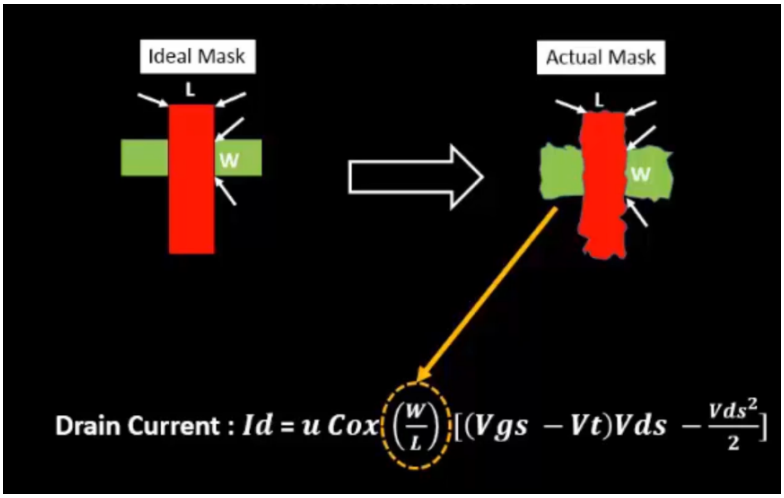

Figure 34: (W/L) variation due to etching process varies the drain current.

Source of Variation - Oxide Thickness

Taking the cross sectional view of a nmos transistor

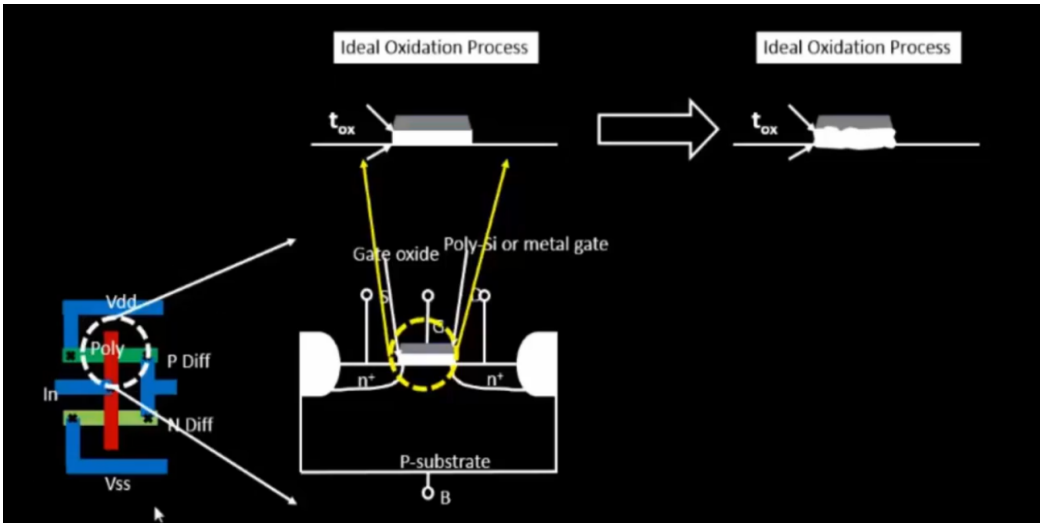

Figure 35: Ideal oxide(t_{ox} is well defined) vs real oxide(t_{ox} is not well defined)

Its effect on drain current is shown below:

$$\text{Drain Current : } Id = u\frac{\varepsilon ox}{tox}\left(\frac{W}{L}\right)\left[(Vgs - Vt)Vds - \frac{Vds^2}{2}\right]$$

Figure 36: Variation in t_{ox} varies I_D

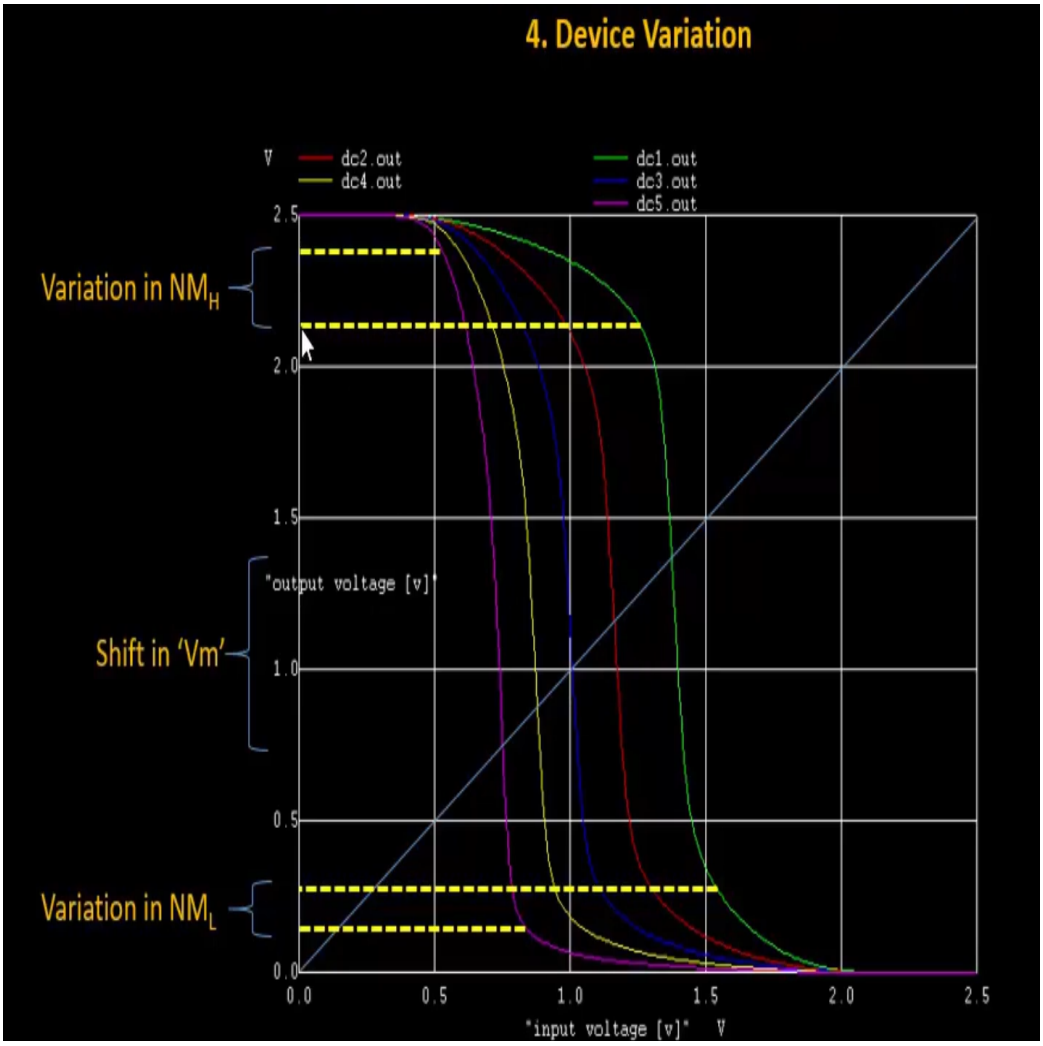

Figure 37: I/O Characteristics for different (W/L) of PMOS and NMOS

VTC Characteristics as function of Device Variation

Key Observations:

- There is a shift in Switching Threshold V_m, but even so, the operation of inverter is still in intact.
- Variation in Noise Margins We notice that there is a variation in noise margins(both low and high margins). This variation is not that significant to disrupt the inverter operator.

5.2 Conclusion

The CMOS inverter is a highly robust and reliable circuit element. It continues to operate effectively as an inverter under a wide range of operating conditions, demonstrating excellent tolerance to process variations and noise. This robustness makes the CMOS inverter an essential building block for designing complex digital integrated circuits.