Jake Humphrey

Objective

I am currently looking for a position in the field of hardware design using FPGAs, preferably in VHDL and/or with the Altera Quartus toolchain. Opportunities for travel would be beneficial.

Work Experience

Period	**September 2013 – December 2013**	
Employer	**EEE Department**	Imperial College London
Job Title	**Teaching Assistant**	
	Worked under the first-year Software Engineering lecturer to assist students in lab sessions. Responded to student queries and gave them advice and guidance.	
Period	**July 2013 – September 2013**	
Employer	**Altera**	Imperial College London
Job Title	**Intern**	
	Worked in the High-Performance Embedded and Distributed Systems laboratory at Imperial College. Ported a C program to a Java-like hardware description language to run on an Altera FPGA.	

Education

Period	**October 2011 – July 2015**	
Qualification	**MEng Electronic and Information Engineering**	
Rank	**First Class Honours**	
Institute	**Imperial College London** (Years 1–3)	London, UK
	Telecom ParisTech (Year 4)	Paris, France
	Final year abroad as part of the Erasmus scheme.	
Period	**September 2009 – July 2011**	
Qualification	**A-Levels**	
Institute	**Hymers College**	Kingston-upon-Hull, UK
	Mathematics A*, Physics A*, Further Maths A, Electronics A	

Projects

Period	**May 2012**	
Setting	**First-Year Project**	Imperial College London
Project Title	**Spacewar!**	

Task: With a partner, create a program in Handel-C using the DK Design Suite to run on an Altera FPGA which demonstrates Image Processing capabilities. Other details are left to the students.

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We decided to remake "Spacewar!", a very early video game developed for the PDP-1 in 1962. The image processing came from the fact that we stored certain game images as sprites, and the sprites representing the players' ships were rotated on-the-fly before being drawn to the screen.

We ran into some problems, such as not being able to reach the fixed framerate target, which we solved using our Computer Architecture knowledge to create a very rudimentary graphics pipeline.

For this project we received a departmental award for best in the year.

Period	**July 2013 – September 2013**	
Setting	**Altera Internship**	Imperial College London
Project Title	**Air Traffic Management Optimisation**	

For this project we were given a C program which used Sequential Monte Carlo simulations to provide travel vectors for aircraft. Our task was to analyse the code and see how it could be optimised by running on an FPGA. The FPGA was provided by Altera, and we were to use Maxeler's Maxcompiler Suite for hardware design.

The MaxCompiler suite facilitates writing programs for CPUs with FPGA coprocessors, and incorporates a C compiler along with a Java-like language for hardware (kernel) design.

Although documentation and support for MaxCompiler were sparse, we were able to succeed in designing a kernel to accelerate the most CPU-intensive parts of the code.

Period	**March 2014**	
Setting	**VHDL and Logic Synthesis course**	Imperial College London
Project Title	**VHDL Graphics Driver**	

Task: To design, implement, and test a logic circuit capable of interpreting a predefined list of commands and colouring appropriate locations in a pixel buffer. The commands allowed the user to draw lines and boxes with a black, white, or inverting brush. The pixel buffer was simply a contiguous area of RAM with a 0 representing a white pixel and 1 representing black.

The design was split into two parts: the Draw Block which interpreted commands and simplified them into a stream of "x, y, colour" commands to the RAM Control Block, which took these commands and made the appropriate changes in memory.

We also designed a suite of tests to validate the design, exploring exhaustive, random, targeted, and constrained random testing methodologies.

Period	**May 2014 – July 2014**	
Setting	**3rd Year Industry Group Project**	Imperial College London
Project Title	**VHDL Floating-Point Unit**	

As a group of six, design, implement, and test a VHDL Floating-Point Unit (FPU). This project was proposed by a team of engineers from the PowerVR Group at Imagination Technologies, and was carried out under the scope of the 3rd Year Project in the Electrical and Electronic Engineering department at Imperial College.

The six members split into four groups to handle four different tasks. While the Design Engineers wrote the VHDL code, the Architect wrote bit-equivalent C++ code. This was intended to mimic Imagination's own workflow, as they often ship C++ code for clients to test.

In addition, the Verification Engineers created testbenches to robustly identify flaws in the design, while the Application Engineer ensured that the design's projected area, frequency,

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and energy usages fell within expected parameters.

Period	**December 2014 – June 2015**	
Setting	**Master's Thesis**	Telecom Paristech
Project Title	**Hardware-based Buffer Overflow Protection**	

My Master's Thesis explored a hardware-based approach to preventing buffer overflow attacks. Using an OpenRISC processor (written in Verilog HDL) as a base, I added several hardware registers to the Memory Management Unit (MMU) to enable invalidation of sections of memory. Inspired by canary values, the CPU was wired to raise an exception when invalid memory was accessed, allowing OS intervention.

Proficiencies

Windows and Unix-based systems, Office software, Shell scripting, C, C++, Python, Lua, Java, Verilog, VHDL, Quartus, ModelSim, Synplify, Matlab, LaTeX, Git.

Interests

Graphics, Artificial Intelligence, FPGA Design, Network Security, Kendo, Japanese Culture, Video Games

References

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