Soft Processors

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Contents

1 Abstract

This document seeks to provide an impartial comparison of the various Soft Processors on the market.

2 Comparison of Soft Processors

The following metrics will be taken into account:

- Bus Used
- Architecture (MIPS/ ARM)
- Cache
- MMU (Memory Management Unit)
- Protection/User Levels
- License
- Documentation

- Toolchain/Debugger/Monitor/JTAG
- Maturity
- Resources, Speed on target FPGA

2.1 OpenRISC

Developer OpenCores

Bus Used OpenRISC uses Wishbone, an open source specification by OpenCores.

Architecture 32/64-bit Mips-like.

Cache 1–64kB for Instructions and Data each.

MMU Virtual Memory support. TLB with page size 8kB and 16–256 entries.

User Levels User/Supervisor Mode.

License There are two main open source implementations available. A Verilog implementation, OpenRISC 1200, is released under LGPL. Another Verilog implementation, mor1kx, is available under a weak copy-left licence created specifically for it, the OHDL.

Documentation The specification can be found here. Documentation for both implementations are also available at their respective Github pages: Mor1kx, OR1200.

Toolchain A Compiler (based on gcc) and Debugger (based on gdb) are available. See here.

Maturity The OpenRISC 1000 specification has been under development since 2001. Version 1.0 was released in 2012, and Version 1.1 in 2014. The OpenRISC 1200 implementation is stable but not in active development, and is the widely used version according to the OpenRISC project overview. Mor1kx is still in active development, but is stated to be more sophisticated.

2.2 LEON2/3/4

Developer Aeroflex Gaisler

Bus Used AMBA2

Architecture 32-bit. ISA based on SPARC-V8

Cache LEON2: Instruction and Data caches. Set-associative with 1–4 sets and 1–64kB/set. LRR or LRU replacement. LEON3/4: 1–4 sets, 1–256 kB/set. Random, LRR or LRU replacement. LEON4 includes an optional L2 cache. 256-bit internal, 1-4 sets, 16kB–8MB.

MMU SPARC Reference MMU (SRMMU) with configurable TLB

User Levels The User and Supervisor modes of SPARC.

License Gaisler state on their website that LEON2 is available from Atmel (AT697 and AT7913), but I found what appears to be the VHDL source code on Github. LEON3 is available under GPL as part of the GRLIB library. LEON4 is only available under a commercial license from Gaisler.

Documentation LEON3 and LEON4 have documentation.

Toolchain Being SPARC V8 conformant, compilers and kernels for SPARC V8 can be used with LEON processors. Cross compiler BCC. gdb can be used for debugging.

Maturity

2.3 Lm32

Developer Lattice

Bus Used Wishbone

Architecture 32-bit. ISA here.

Cache Configurable between no cache, 8kB I-cache, and 8kB I-cache and 8kB D-cache.

MMU None.

User Levels No separate modes.

License LatticeMico32 is licensed under a free (IP) core license.

Documentation Documentation is available here, but registration is required.

Toolchain GCC supports the LM32 since version 4.5.0, and Binutils since 2.19. gdb and Newlib are also supported.

Maturity Introduced in 2006.

2.4 Microblaze

Developer Xilinx

Bus Used Customisable between CoreConnect PLB, OPB, FSL, LMB, AXI4.

Architecture In terms of its instruction set architecture, MicroBlaze is very similar to the RISC-based DLX architecture, which in turn is based upon the MIPS architecture.

Cache 2kB–64kB Direct mapped write-through or write-back.

MMU

User Levels

License

Documentation

Toolchain

Maturity

2.5 Nios

Developer

Bus Used

Architecture

Cache

MMU

User Levels

License

Documentation

Toolchain

Maturity

2.6 Nios II

Developer

Bus Used

Architecture

Cache

MMU

User Levels

License

Documentation

Toolchain

Maturity

2.7 Cortex-M1

Developer

Bus Used

Architecture

Cache

MMU

User Levels

License

Documentation

Toolchain

Maturity