1. Architectural Overview

Introducing the CY8C58LP family of ultra low power, flash Programmable System-on-Chip (PSoC) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5LP platform. The CY8C58LP family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

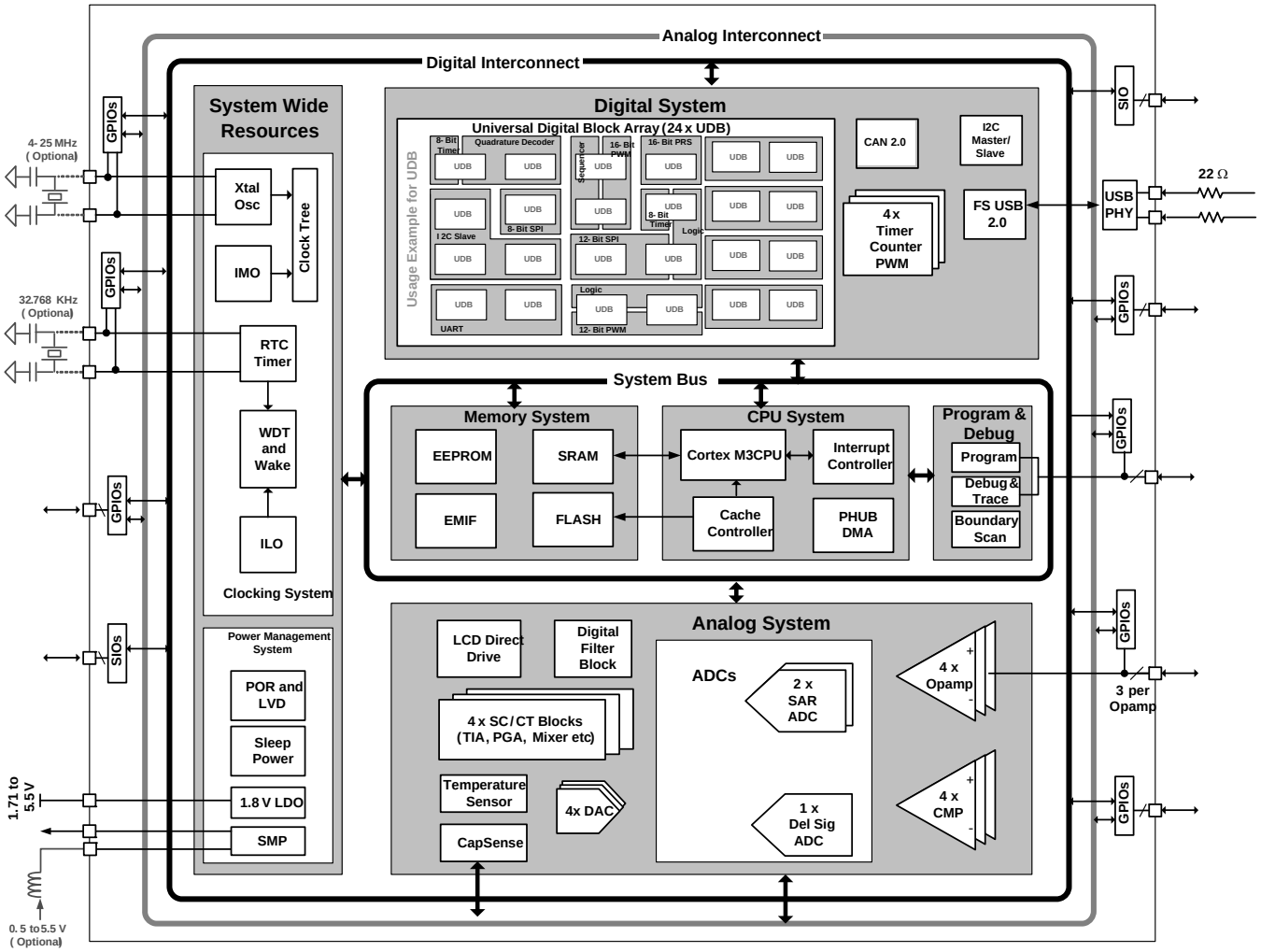


Figure 1-1 illustrates the major components of the CY8C58LP family. They are:

- ARM Cortex-M3 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low power UDBs. PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

Figure 2-4. 100-pin TQFP Part Pinout

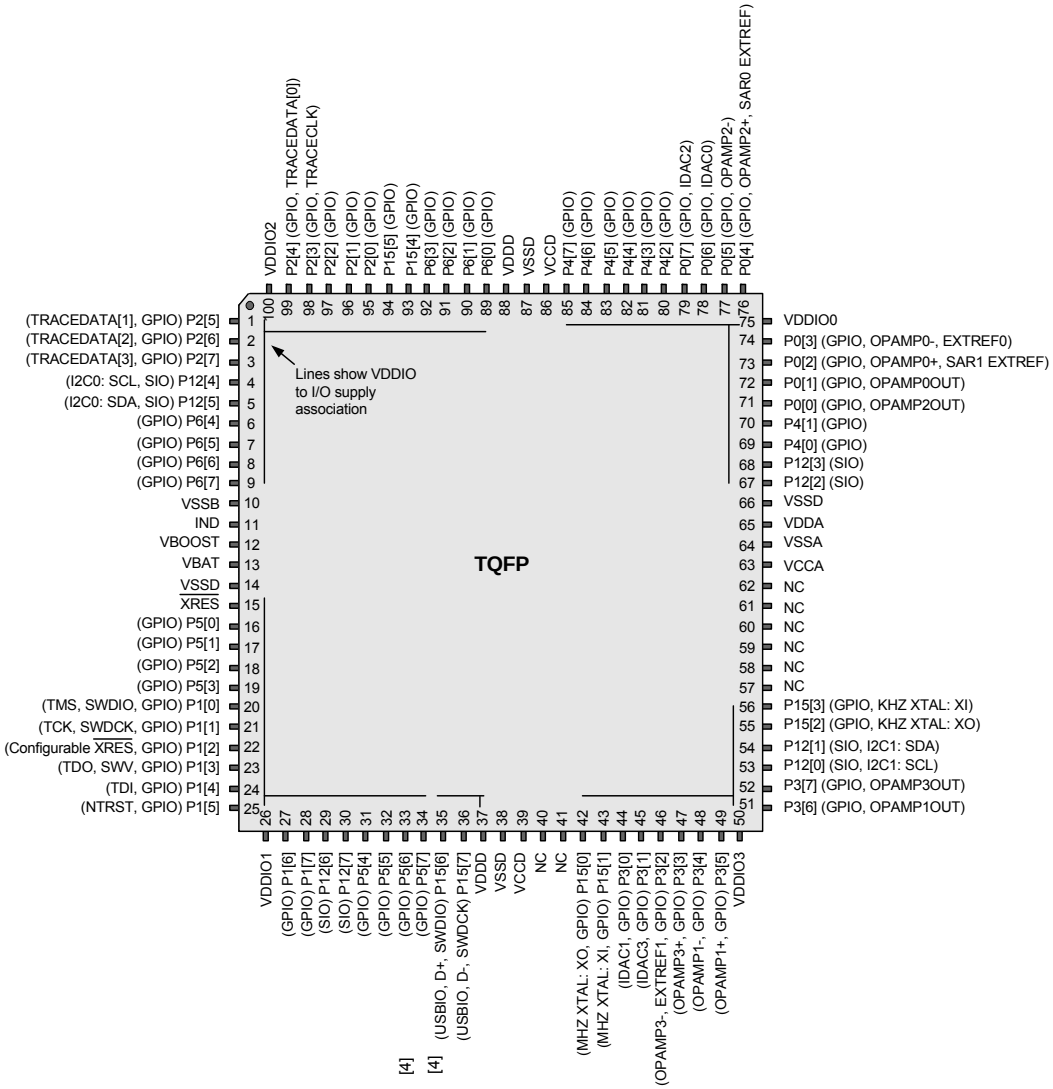


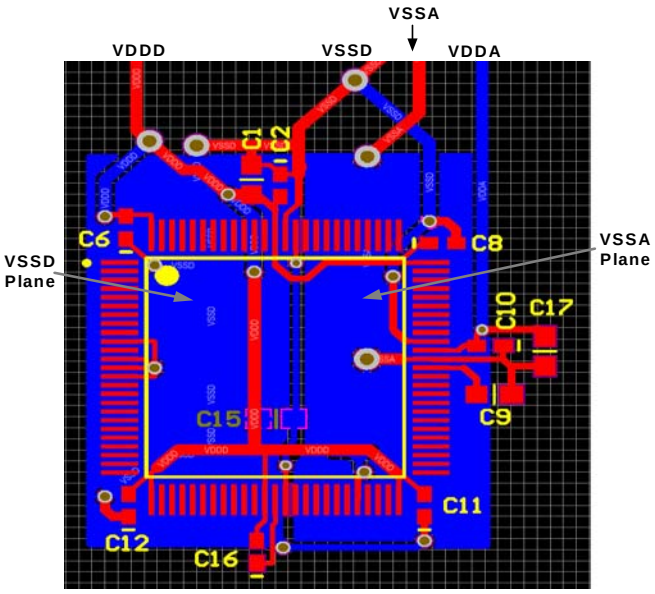
Figure 2-5 on page 9 and Figure 2-6 on page 10 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-5 and "Power System" section on page 25. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled VSSD must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note, AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

Note
4. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3. Low-resistance output pin for high-current DACs (IDAC).

Opamp0out, Opamp1out, Opamp2out, Opamp3out. High current output of uncommitted opamp.[5]

Extref0, Extref1. External reference input to the analog system.

SAR0 EXTREF, SAR1 EXTREF. External references for SAR ADCs

Opamp0-, Opamp1-, Opamp2-, Opamp3-. Inverting input to uncommitted opamp.

Opamp0+, Opamp1+, Opamp2+, Opamp3+. Noninverting input to uncommitted opamp.

GPIO. Provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense.[5]

I2C0: SCL, I2C1: SCL. I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA. I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

Ind. Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi. 32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi. 4 to 25-MHz crystal oscillator pin.

nTRST. Optional JTAG Test Reset programming and debug port connection to reset the JTAG connection.

SIO. Provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK. SWD Clock programming and debug port connection.

SWDIO. SWD Input and Output programming and debug port connection.

TCK. JTAG Test Clock programming and debug port connection.

TDI. JTAG Test Data In programming and debug port connection.

TDO. JTAG Test Data Out programming and debug port connection.

TMS. JTAG Test Mode Select programming and debug port connection.

TRACECLK. Cortex-M3 TRACEPORT connection, clocks TRACEDATA pins.

TRACEDATA[3:0]. Cortex-M3 TRACEPORT connections, output data.

SWV. SWV output.

USBIO, D+. Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D-. Provides D- connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are Do Not Use (DNU) on devices without USB.

VBOOST. Power sense connection to boost pump.

Note
5. GPIOs with opamp outputs are not recommended for use with CapSense.

VBAT. Battery supply to boost pump.

VCCA. Output of the analog core regulator or the input to the analog core. Requires a 1uF capacitor to VSSA. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator, (internally regulated mode, the default), do not tie any power to this pin. For details see "Power System" section on page 25.

VCCD. Output of the digital core regulator or the input to the digital core. The two VCCD pins must be shorted together, with the trace between them as short as possible, and a 1uF capacitor to VSSD. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator (internally regulated mode, the default), do not tie any power to this pin. For details see "Power System" section on page 25.

VDDA. Supply for all analog peripherals and analog core regulator. **VDDA must be the highest voltage present on the device. All other supply pins must be less than or equal to VDDA.**

VDDD. Supply for all digital peripherals and digital core regulator. VDDD must be less than or equal to VDDA.

VSSA. Ground for all analog peripherals.

VSSB. Ground connection for boost pump.

VSSD. Ground for all digital logic and I/O pins.

VDDIO0, VDDIO1, VDDIO2, VDDIO3. Supply for I/O pins. Each VDDIO must be tied to a valid operating voltage (1.71 V to 5.5 V), and must be less than or equal to VDDA.

$\overline{\text{XRES}}$ (and configurable $\overline{\text{XRES}}$). External reset pin. Active low with internal pull-up. Pin P1[2] may be configured to be a XRES pin; see "Nonvolatile Latches (NVLs)" on page 19.