1A.

!S	!R	Q_{curr}	Q_{new}
0	0	0	undefined
0	0	1	Undefined
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

latch operation		
S'	**R'**	**Action**
0	0	not allowed
0	1	Q = 1
1	0	Q = 0
1	1	No Change

1B.

This is an alternate model of the simple SR latch which is built with NAND logic gates. Set and reset now become active low signals, denoted S' and R' respectively. Otherwise, operation is identical to that of the SR latch.

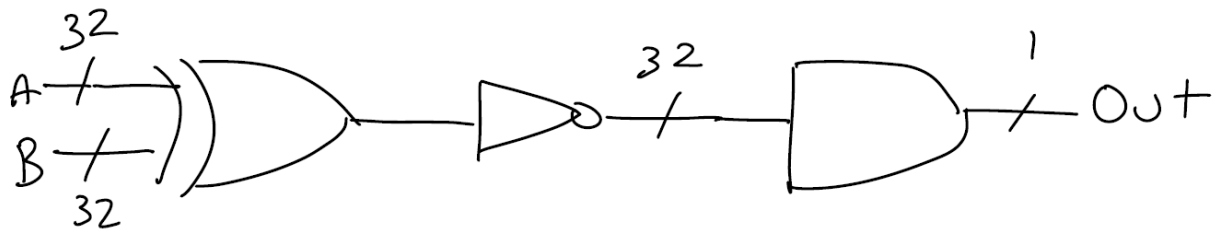
2.

Solution:

Current State		*Input*	*Next State*	
A	*B*	*X*	*A*	*B*
0	0	0	1	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	0	1

3.

Solution:



4. A. 256 MB = 2^8 * 2^20 Bytes = 2^28 Bytes. Hence 28 bits needed for addressing.

B. 34 bits can address 2^34 Bytes. 2^34 = 2^30 * 2^4 = 16 GB.

C. 34 bits can address 2^34 words. As each word is 64 bits (8 Bytes), 34 bits can address 2^34*8 Bytes = 2^30 * 2^4 * 2^3 B = 128 GB

D. 256 MB = 2^28 Bytes. Number of bytes per word = 8 (2^3). Therefore, number of words in 256 MB = 2^28/2^3 = 2^25. 25 bits are needed to address 2^25 words.

5.

Solution: