Datasheet for Chipsemi CHSC6540

DS-CHSC6540

Ver 1.0.0

CHIPSEMI SEMICONDUCTOR

Keyword:

Features; Benefits; Operation modes; CDSP; MCU; Clock; Timer; Watchdog; Interface; Interrupt; Memory; ADC; Electrical specifications; Applications.

Brief:

This datasheet is dedicated for the self-capacitive touch panel controller IC CHSC6540 developed by Chipsemi.

In this datasheet, key features, operation mode, main modules and reference design of the CHSC6540 are introduced.

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1 Introduction

1.1 General description

CHSC6540, latest generation single-chip self-capacitive touch panel controller SoC developed by Chipsemi, is designed to work with self-capacitance type sensor, and supports user-friendly gesture control and up to two-point touch with a capacitive touch panel. Single-chip CHSC6540 supports up to 7'' touch panel.

With built-in 32-bit RISC processor and CDSP module, the CHSC6540 is featured with outstanding noise immunity, fast response, low power consumption, excellent accuracy and linearity, as well as perfect waterproof performance.

CHSC6540, which operates in the -40℃~+125℃ industrial temperature range, can be applied to a diverse group of portable devices, such as cellular phones, tablets, and GPS navigator.

CHSC6540 offers high-volume-assembly and high integration level. Few external components are needed to satisfy customers' ultra-low cost requirement. It's completely RoHS-compliant and 100% lead (Pb)-free.

The GPIO pins (SDA,SCL,INT) of CHSC6540 are special designed for ESD capability improvement.

1.2 Key features

Table 1- 1 Key features of CHSC6540

Features	CHSC6540
Package	UQFN-48, 5X5X0.55mm
Touch sensor	G/G, G/F, P/F, OGS, Ultra-thin G/F **(Support ITO traces; support direct bonding; support frameless TP)**
ITO pattern	single layer self-capacitance
Touch panel size	4.3''~7''

Features	CHSC6540
Response time	Power-on time: <75ms; Latency time for first touch: <12ms. Scanning speed: up to 200Hz
Operating voltage	2.6V~3.6V
Operating temperature	-40℃~+125℃
Supported channel number	40
Supported channel driving resistance	<100kΩ
Supported single channel capacitance	Up to 400pF
Power consumption	Current-active: 8mA (Typ), Current-sleep: 7uA (Typ), I/O Latch-up current: 200mA (min)
ESD	HBM 7000V (min.), CDM 2000V (min.), Air Discharge +/-12 kV
Multi-point touch	Up to 2 points
Glove mode	Support
Anti-interference performance	Immune to noise from RF, LCD and power supply

1.3 Key benefits

(1) Anti-Interference and excellent noise-cancellation performance:

Immune to RF interferences, robust operation in noisy RF environment;

Insensitive to capacitance and environmental variety via auto calibration function;

Chipsemi's innovative adaptive-noise-cancellation technology and specially designed data processing unit can detect and silence the two noise sources which capacitive touch screen usually suffers from: display noise and charger noise. With the powerful 32bit MCU and specific built-in hardware, both the periodic and broadband

noise can be eliminated to obtain unmatched noise immunity.

(2) Fast response time:

The power-on time for the CHSC6540 is less than 75ms;

When it is powered up, the latency time for first touch is less than 12ms;

Scanning rate up to 200Hz makes fast response available, which is especially useful for the highly demanding applications for the responding speed, such as handwriting and game.

(3) Low power consumption:

The average current in typical case is 8mA at active state, and 7uA in suspend mode.

(4) Excellent waterproof performance:

Water mist even droplets on the surface will not influence normal operation of touch panel based on the CHSC6540.

When water mist or droplets are wiped off, the touch screen can also be operated normally without extra delays.

No malfunction or dummy points will be reported during water spurting and wiping process.

1.4 Typical application

The CHSC6540 is dedicated for self-capacitive touch panel; its typical applications are listed as follows:

- ✧ Smart phone
- ✧ Tablets
- ✧ Digital camera
- ✧ GPS navigator
- ✧ Portable media player
- ✧ Game consoles.

1.5 Ordering information

Table 1- 2

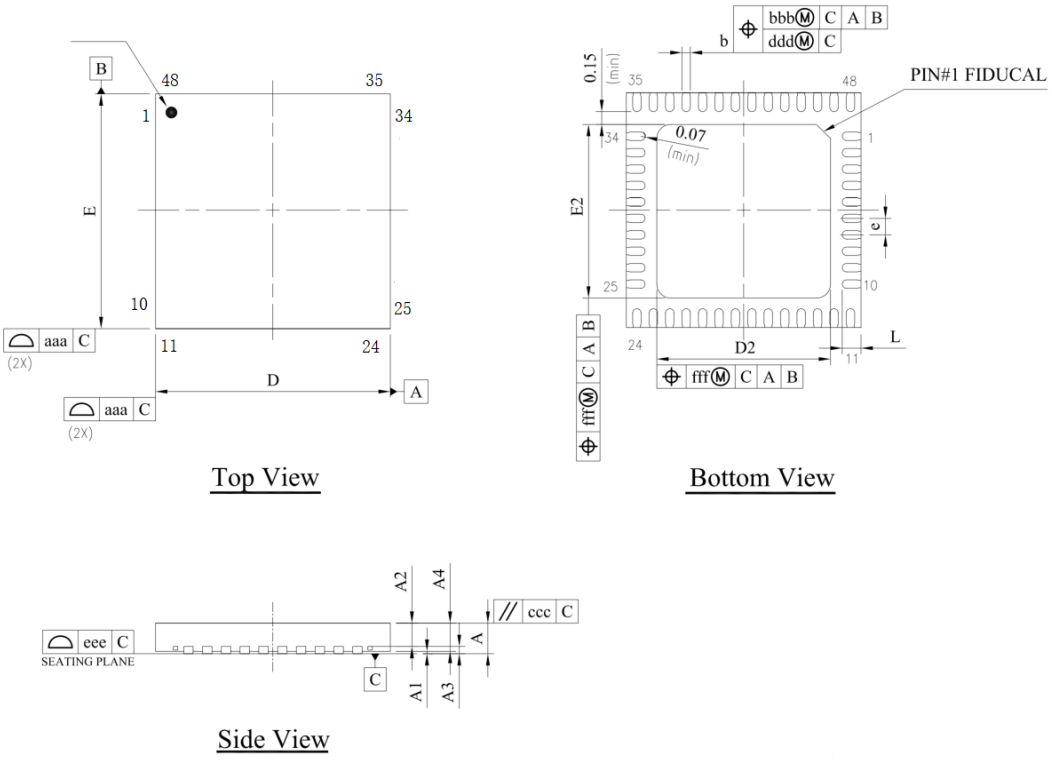
Ordering information of the CHSC6540

Product Series	Package Type	Temperature Range	Product Part No.	Packing Method	Ordering Number	Minimum Order Quantity
CHSC6540	48-pin 5x5x0.55mm UQFN	-40℃~+125℃	CHSC6540EU48	TR	CHSC6540EU48R	3000

*Note: Packing method “TR” means tape and reel.

1.6 Package

Package dimension for the CHSC6540EU48 is shown as Figure 1-1.



ITEM		Symbol	DIMENSION(mm)		
			MIN.	NOM.	MAX.
Total height		A	0.50	0.55	0.60
Stand off		A1	0	0.02	0.05
Mold thickness		A2	0.38	0.40	0.41
Leadframe thickness		A3	---	0.15REF	---
Mold+Leadframe thickness+Mold gap		A4	0.50	0.53	0.60
Lead width		b	0.13	0.18	0.23
Package size	X	D	4.90	5.00	5.10
	Y	E	4.90	5.00	5.10
E-PAD Size	X	D2	3.60	3.70	3.80
	Y	E2	3.60	3.70	3.80
Lead length		L	0.35	0.40	0.45
Lead pitch		e	0.25	0.35	0.45
Package profile of a surface		aaa	0.10		
Lead position		bbb	0.07		
Paralleliam		ccc	0.10		
Lead position		ddd	0.05		
Package profile of a surface		eee	0.08		
Epad position		fff	0.10		

NOTE:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. REFER TO JEDEC STD.MO-220 WJJE-1.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25mm FROM TERMINAL TIP.
4. LEADFRAME MATERIAL IS 194FH AND THICKNESS IS 0.203MM (8 MIL).
5. DIMENSION"D"&"E" WILL INCLUDE ALL SIDE BURR INDUCED DURING ASSEMBLY.

Figure 1- 1 Package dimension for the CHSC6540EU48

1.7 Pin layout

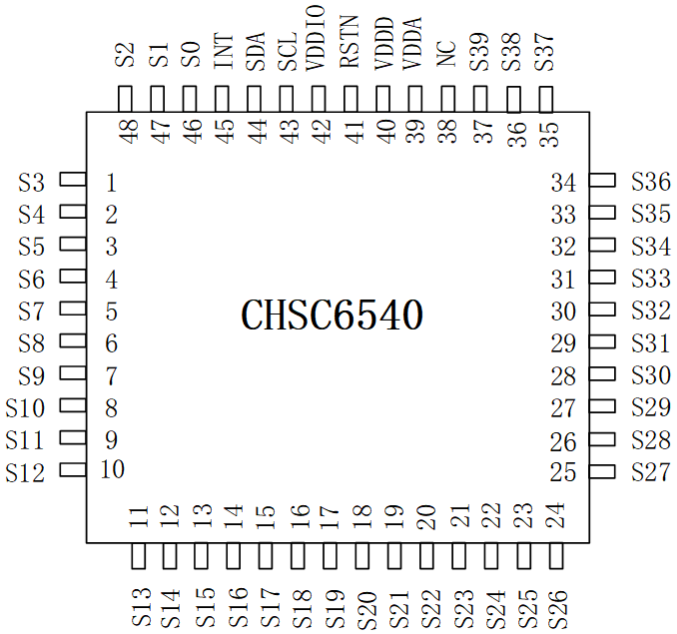


Figure 1- 2 Pin assignment for the CHSC6540

Functions of 48 pins for the CHSC6540 (CHSC6540EU48) are described in Table 1-3

Table 1- 3 Pin functions for the CHSC6540

Pin Name	Pin No.	Type	Description
S3	1	I	sense input
S4	2	I	sense input
S5	3	I	sense input
S6	4	I	sense input
S7	5	I	sense input
S8	6	I	sense input
S9	7	I	sense input
S10	8	I	sense input
S11	9	I	sense input
S12	10	I	sense input
S13	11	I	sense input
S14	12	I	sense input
S15	13	I	sense input
S16	14	I	sense input
S17	15	I	sense input
S18	16	I	sense input
S19	17	I	sense input
S20	18	I	sense input

Pin Name	Pin No.	Type	Description
S21	19	I	sense input
S22	20	I	sense input
S23	21	I	sense input
S24	22	I	sense input
S25	23	I	sense input
S26	24	I	sense input
S27	25	I	sense input
S28	26	I	sense input
S29	27	I	sense input
S30	28	I	sense input
S31	29	I	sense input
S32	30	I	sense input
S33	31	I	sense input
S34	32	I	sense input
S35	33	I	sense input
S36	34	I	sense input
S37	35	I	sense input
S38	36	I	sense input
S39	37	I	sense input
NC	38	NC	no connection
VDDA	39	PWR	Analog power supply, A 1μF ceramic capacitor to ground is required.
VDDD	40	PWR	Digital power supply, 1uF capacitor to ground is required.
RSTN	41	I	Capacitor to ground is required.
VDDIO	42	PWR	I/O power supply
SCL	43	I/O	I2C clock input
SDA	44	I/O	I2C data input and output
INT	45	I/O	External interrupt to the host
S0	46	I	sense input
S1	47	I	sense input
S2	48	I	sense input

*Note: Pins with bold typeface can be used as GPIOs.

2 Function Overview

2.1 Block diagram

The overall system block diagram of the CHSC6540 is shown as Figure 2-1.

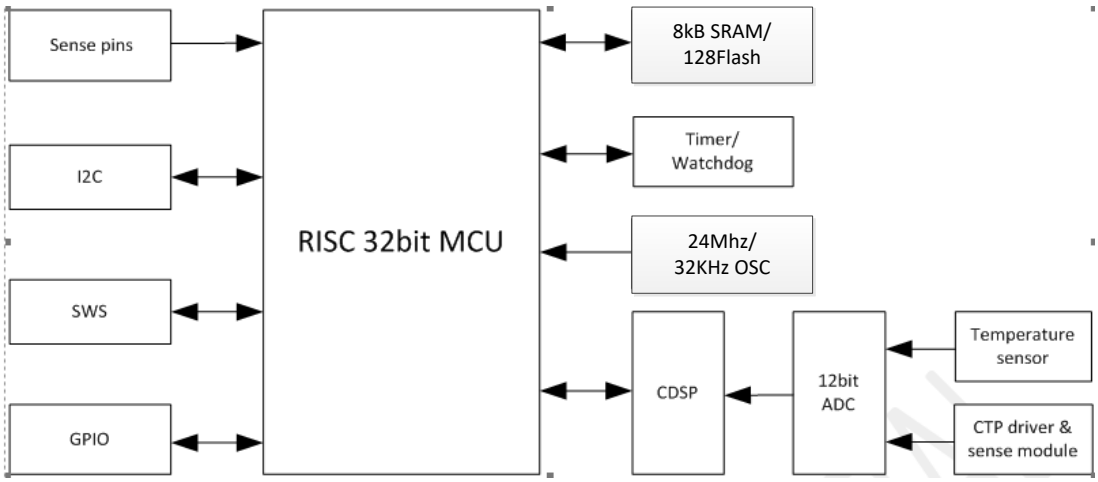


Figure 2- 1 Block diagram

2.1.1 Memory

- ✧ 128KB Flash;
  - ✧ SRAM: 8KB SRAM for system use; 2KB SRAM for CDSP use;

2.1.2 Interface

- ✧ CHSC6540: 40 CTP sense pins; GPIO/I2C/SWS.

2.1.3 Digital part

- ✧ A 32-bit RISC processor with a 32×32 multiplier and a 32/32 divider;
- ✧ Embeds CDSP module to obtain accurate coordinate of touch points via firmware; the CDSP supports totally up to 40 sensing lines for the CHSC6540;
- ✧ Timer: Integrates 3 timers and there are four modes available for each timer; Timer2 can be configured as a watchdog so as to reset chip from unexpected hang up or malfunction.

2.1.4 Analog part

- ✧ CTP driver & sense module: The sensing circuit adopts the patented charger fast detection technology for efficiency.
- ✧ Embeds a temperature sensor which serves to measure ambient environment

temperature so as to implement temperature compensation via firmware.

- ✧ ADC: The 12-bit ADC serves to take samples of temperature sensor/integrator output, conduct analog-to-digital signal conversion, and send digital signal after conversion to the CDSP module.
- ✧ Clock: Embeds a 24MHz RC oscillator with low temperature drift.
- ✧ Regulator: Embeds a LDO (Low Dropout) regulator to provide power for internal clock. Also embeds a DIG_LDO and a LC_LDO to provide power for digital parts in normal working mode and low current mode, respectively.
- ✧ Bandgap: Provides voltage reference value.
- ✧ Embeds a 32KHz RC oscillator which serves to generate a clock for suspend mode wakeup.

2.2 CTP operation modes

For the CHSC6540, there are three operation modes available as follows: normal mode, low-power mode and suspend mode.

2.2.1 Normal mode

In normal mode, the CHSC6540 scans the touch screen panel with certain scanning rate, such as the default scanning rate: 60 frames per second.

Users can also speed up or slow down the scanning rate via configuration.

2.2.2 Low-power mode

In low-power mode, the CHSC6540 scans the touch screen panel with a relatively lower rate. The default scanning rate for this mode is 10 frames per second.

Users can also speed up or slow down the scanning rate via configuration.

When in this mode, touch detection is feasible for the CHSC6540, and the chip will enter the normal mode if a touch is detected.

2.2.3 Suspend mode

In suspend mode, the CHSC6540 is in standby state and will only respond to external “WAKEUP” signal. Very little current is consumed in this mode, so that the standby time for portable devices can be prolonged.

3 CDSP

The CHSC6540 embeds CDSP and supports up to 40 sensing lines which are configurable. Calculation for accurate touch point coordinate information is implemented via firmware.

The CDSP configures analog front-end parameters, control analog-to-digital conversion and channel switch for flexible scanning time and sensor usage. The collected sampling data from ADC will be stored into internal SRAM and will be translated into accurate touch position information using advanced algorithms.

4 MCU

4.1 Description

The CHSC6540 integrates a powerful 32-bit MCU developed by Chipsemi. The digital core is based on 32-bit RISC, and the length of instructions is 16 bits; four hardware breakpoints are supported.

4.2 Clock

4.2.1 System clock

System clock can be configured through registers.

4.2.2 ADC clock

ADC clock can be configured through registers.

4.3 Reset, Wakeup and Power down enabling

Except for power on reset, it is also feasible to carry out software reset for some modules via registers: if some bit is set to logic “1”, corresponding module is reset.

5 Timers

The CHSC6540 supports three timers: Timer0 ~ Timer2. The three timers all support four modes: Mode 0 (System Clock Mode), Mode 1 (GPIO Trigger Mode), Mode 2 (GPIO Pulse Width Mode) and Mode 3 (Tick Mode).

Timer 2 can also be configured as “watchdog” to monitor firmware running.

5.1 Mode0 (System Clock Mode)

In Mode 0, system clock is employed as clock source.

After Timer is enabled, Timer Tick (i.e. counting value) is increased by 1 on each positive edge of system clock from preset initial Tick value. Generally the initial Tick value is set to 0.

Once current Timer Tick value matches the preset Timer Capture (i.e. timing value), an interrupt is generated, Tick value is cleared to 0 automatically and Timer status is updated.

5.2 Mode1 (GPIO Trigger Mode)

In Mode 1, GPIO is employed as clock source.

After Timer is enabled, Timer Tick (i.e. counting value) is increased by 1 on each positive edge of GPIO from preset initial Tick value. Generally the initial Tick value is set to 0.

Once current Timer Tick value matches the preset Timer Capture (i.e. timing value), an interrupt is generated and Tick value is cleared to 0 automatically.

5.3 Mode2 (GPIO Pulse Width Mode)

In Mode 2, system clock is employed as the unit to measure the width of GPIO pulse.

After Timer is enabled, Timer Tick is triggered by a positive edge of GPIO pulse. Then Timer Tick (i.e. counting value) is increased by 1 on each positive edge of system clock from preset initial Tick value. Generally the initial Tick value is set to 0.

While a negative edge of GPIO pulse is detected, an interrupt is generated. The GPIO pulse width could be calculated in terms of tick count and period of system clock.

5.4 Mode3 (Tick Mode)

In Mode 3, system clock is employed.

After Timer is enabled, Timer Tick starts counting upward, and Timer Tick value is increased by 1 on each positive edge of system clock.

This mode could be used as time indicator. There will be no interrupt generated. Timer Tick keeps rolling loop from 0 to 0xffffffff. When Timer tick overflows, it returns to 0 and starts counting upward again.

5.5 No-wrap mode

When in Mode0 or Mode1, Timer works normally with auto reload feature as described in **section 5.2** or **section 5.3**. In this mode, when Timer tick value reaches preset capture value, an interrupt is generated, and Timer tick value is cleared to 0 automatically. Timer tick value starts rolling from 0 to the capture value again.

5.6 Watchdog

Programmable watchdog could reset chip from unexpected hang up or malfunction.

Only Timer2 supports Watchdog.

6 Interface

The CHSC6540 integrates interfaces as follows:

- 40 CTP sense pins: S1~S40;
- Configurable pins with multiplexing functions:
  - Up to 4 GPIOs: refer to Table 1-3 of section 1.7
  - I2C: Pin43 SCL –> I2C_SCL, Pin44 SDA –> I2C_SDA;

As shown in Figure 6-1, the interface between a host processor and the CHSC6540 consists of I2C interface and an interrupt signal interface. Host gets data and sends “SUSPEND” command to the CHSC6540; while the CHSC6540 reminds Host of reading data.

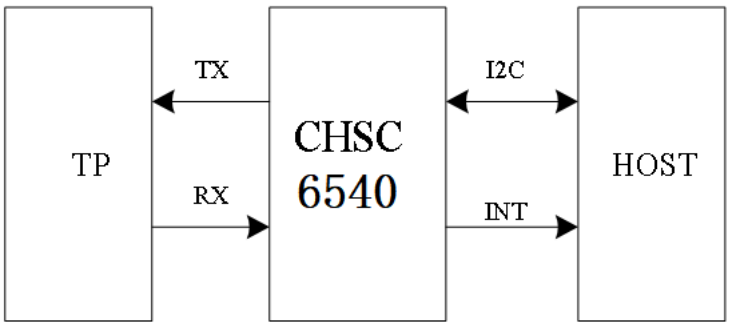


Figure 6- 1 Schematic diagram for interface

6.1 I2C

I2C module of the CHSC6540 acts as slave. Its related registers are as follows:

Be default, I2C Master can read any internal register and RAM space of the CHSC6540 via I2C.

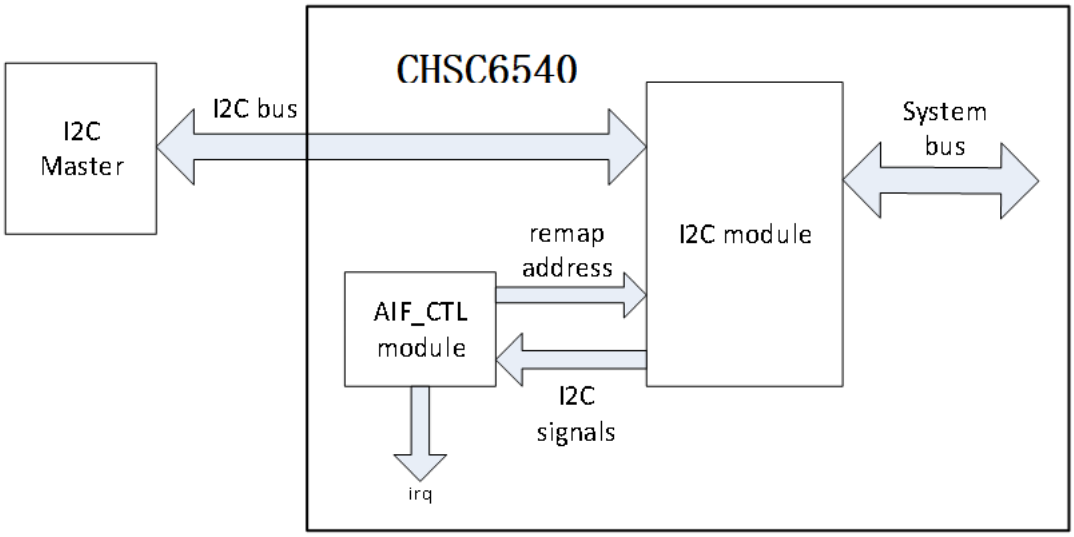


Figure 6- 2 Connection schematic between I2C and AIF_CTL module

The AIF_CTL module embedded in the CHSC6540 serves to implement I2C address mapping, and provide cmd register to generate interrupt signal for I2C communication.

6.2 GPIO

The CHSC6540 supports up to 4 GPIOs.

After GPIO function is enabled for some pin, if the pin is used as output, both “OEN” and “Input Enable” should be cleared, then set “Output” value; if the pin is used as input, both “OEN” and “Input Enable” should be set to logic “1”, then set “Input” value.

Drive strength is set as the strongest drive level by default. In actual applications, drive strength can be decreased to lower level if necessary.

7 Interrupt system

The interrupting function is applied to manage dynamic program sequencing based on real-time events triggered by timers, pins and etc.

The CHSC6540 supports 24 interrupt sources and two priority levels.

When CPU receives an interrupt request (IRQ) from some interrupt source, it will decide whether to respond to the IRQ. If CPU decides to respond, it pauses current routine and starts to execute interrupt service subroutine. Program will jump to certain code address and execute IRQ commands. After finishing interrupt service subroutine, CPU returns to the breakpoint and continues to execute main function.

7.1 Enable interrupt sources and priority

Various interrupt sources can be enabled and set as Low Priority via registers.

Any interrupt source could be enabled and set as High priority via registers.

When more than one interrupt sources assert interrupt requests meanwhile, CPU will respond depending on respective interrupt priority level. If there's interrupt source enabled with high priority, CPU should respond to it first.

7.2 Interrupt source indication

Three bytes in register table serve to indicate interrupt sources that have asserted IRQ (Interrupt Request). Once IRQ occurs from certain source, corresponding flag bit will be raised to "High".

7.3 Clear IRQ source

When handling edge-triggered type interrupt, the corresponding IRQ source flag needs to be cleared registers.

As for level-type interrupt, IRQ interrupt source status needs to be cleared via setting corresponding module status register.

8 Power on reset sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn’t be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after ini- tializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

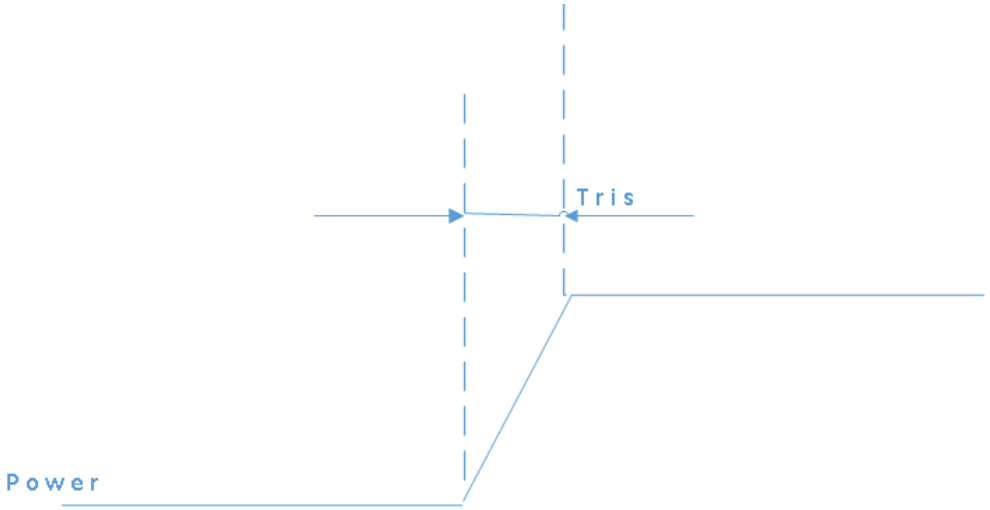


Figure 8.1 power on time

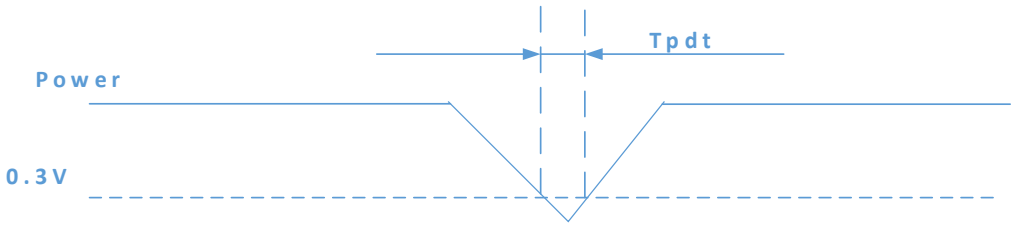


Figure 8-2 Power Cycle requirement

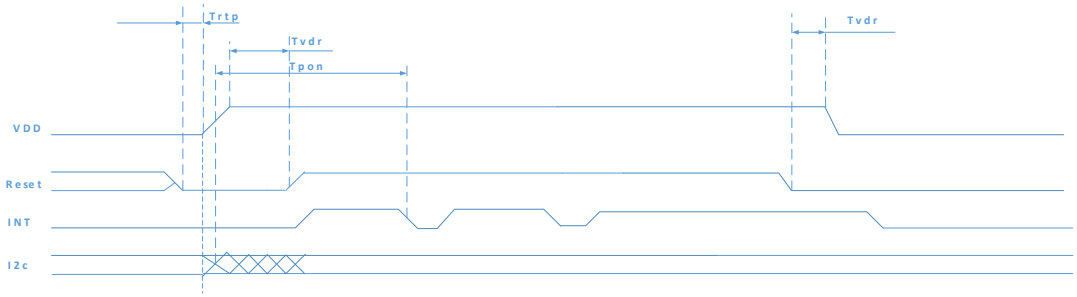


Figure 8-3 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

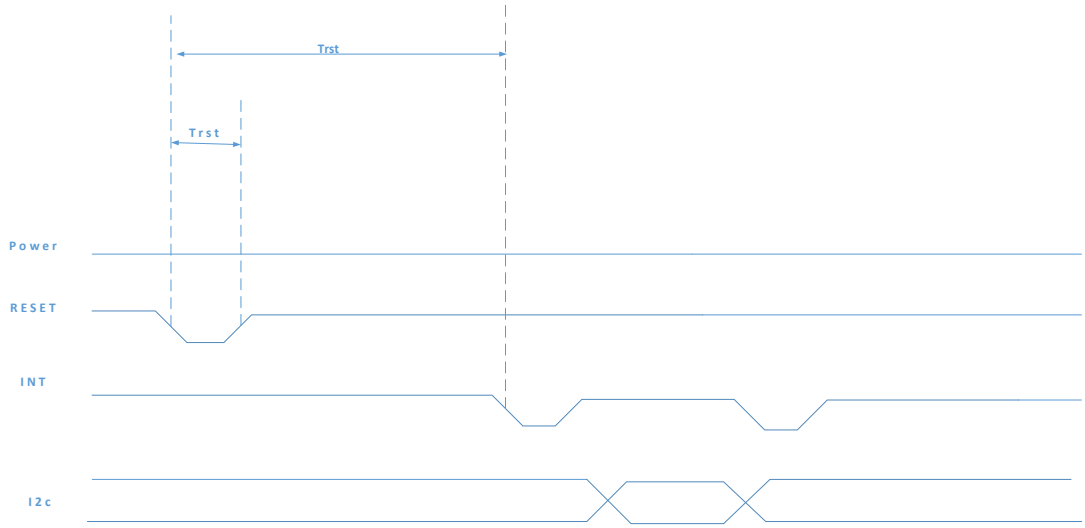


Figure 8.4 Reset Sequence

Table 8-1 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	2	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tpon	Time of starting to report point after powering on	--	200	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	500	--	us

9 Memory configuration

The CHSC6540 embeds 128KB program memory (Flash), 8KB data memory (SRAM) for system use, as well as 2KB SRAM for CDSP use.

10 SAR ADC

The CHSC6540 integrates one SAR ADC module, which can be used to sample CTP module output and internal test point.

10.1 Clock

As for SAR ADC clock configuration, please refer to **Section 4.2.2** ADC clock.

10.2 Resolution

The resolution is selectable via registers.

ADC data format is always 12bits no matter the conversion bit is set. For example, 7 bits conversion will have higher 7 bits as valid bits and the rest bits are to be “1”.

10.3 Reference voltage and sampling period

The reference voltage (V_{REF}) is selectable via registers: VDDA.

The sampling frequency can be up to 1MHz with operating frequency of 24M for VDD;

Beware of the ADC clock selection and set correct ADC clock divider value. Sampling period is determined by SAR ADC clock period * (sampling clock cycle + conversion bit + 1).

10.4 Input mode and channel selection

The SAR ADC for the CHSC6540 supports single-end or differential input mode which is selectable via registers.

10.5 Reset and power down

ADC_DATA, ADC_DATA1 and all SAR ADC configuration registers can be cleared to default value after reset.

11 Key Electrical Specifications

11.1 Absolute maximum ratings

Table 10- 1 Absolute Maximum Ratings

Characteristics	Sym.	Min.	Max	Unit	Test Condition
Supply Voltage	VDD	-0.3	3.6	V	
Voltage on Input Pin	V_{In}	-0.3	VDD+0.3 Max 3.6	V	
Output Voltage	V_{Out}	-0.3	VDD+0.3 Max 3.6	V	
Storage temperature Range	T_{Str}	-65	150	°C	
Soldering Temperature	T_{Sld}		260	°C	

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

11.2 Recommended operating condition

Table 10- 2 Recommended operation condition

Item	Sym.	Min	Typ.	Max	Unit	Condition
Power-supply voltage	VDD	2.6	2.8	3.6	V	
Operating Temperature Range	T_{Opr}	-40		125	°C	

11.3 DC characteristics

Table 10- 3 DC characteristics

Item	Sym.	Min	Typ.	Max	Unit	Condition
Power Consumption	Idd		7		mA	
Suspend Current	I_{Susp}		7		uA	

*Note: All tests above are done at room temperature (T=25℃).

11.4 AC characteristics

Table 10- 4 AC Characteristics

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
Digital inputs/outputs						
Input high voltage	VIH	0.7VDD		VDD	V	
Input low voltage	VIL	VSS		0.3VDD	V	
Output high voltage	VOH	VDD-0.3		VDD	V	
Output low voltage	VOL	VSS		0.3	V	
ADC						
Differential nonlinearity	DNL		0.6		LSB	
Integral nonlinearity	INL		2		LSB	
Effective number of bits	ENOB		10.5		bit	
Signal-to-noise and distortion ratio (f_{in}=1kHz, f_S=16kHz)	SINAD		65		dB	
Spurious free dynamic range (f_{in}=1kHz, f_S=16kHz)	SFDR		84		dB	

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
Sampling frequency	F_S			2	MHz	VDD reference
				1	MHz	Vbg reference
48MHz RC oscillator						
Nominal frequency	f_{NOM}		48		MHz	
Frequency tolerance	f_{TOL}		1		%	On chip calibration
32kHz RC oscillator						
Nominal frequency	f_{NOM}		32		kHz	
Frequency tolerance	f_{TOL}		0.5		%	On chip calibration