MOSFETS

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The **MOSFET (metal oxide semiconductor field-effect transistor) is another category** of field-effect transistor.

The MOSFET, different from the JFET, has no *pn junction* structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer.

The two basic types of MOSFETs are enhancement (E) and depletion (D).
Of the two types, the enhancement MOSFET is more widely used.

Because polycrystalline silicon is now used for the gate material instead of metal, these devices are sometimes called IGFETs (insulated-gate FETs).

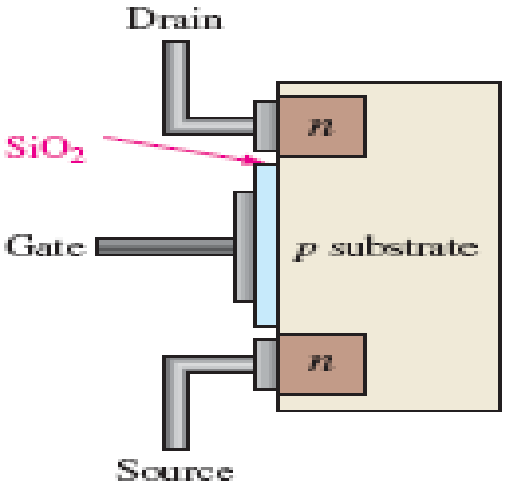
Enhancement MOSFET (E-MOSFET)

The E-MOSFET operates only in the enhancement mode and has no depletion mode.

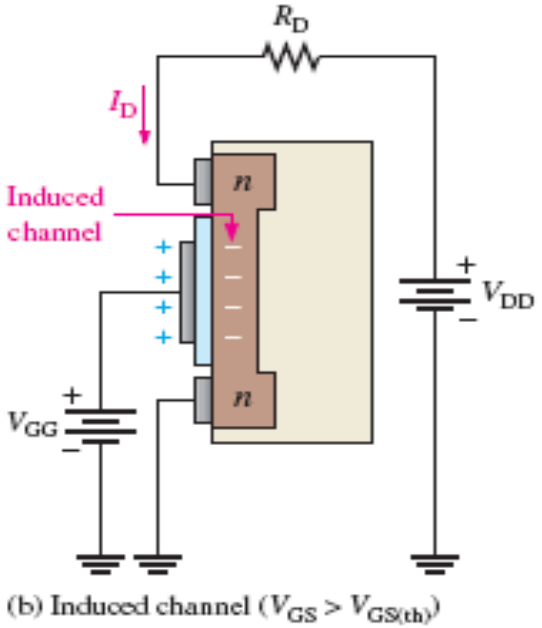
Notice in Figure (a) that the substrate extends completely to the SiO_2 layer.

For an n-channel device, a positive gate voltage above a threshold value induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in Figure (b).

The conductivity of the channel is enhanced by increasing the gate-to-source voltage and thus pulling more electrons into the channel area. For any gate voltage below the threshold value, there is no channel.

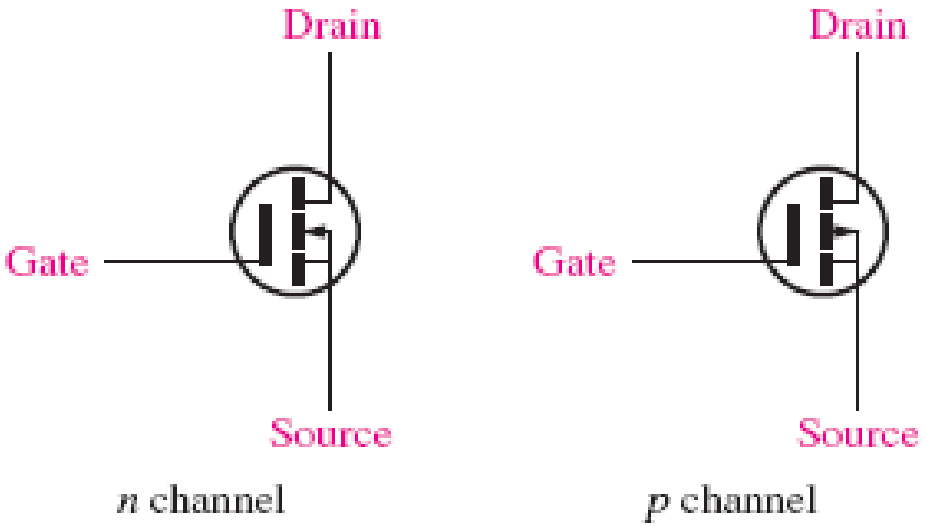


(a) Basic construction



(b) Induced channel ($V_{GS} > V_{GS(th)}$)

E-MOSFET Symbols

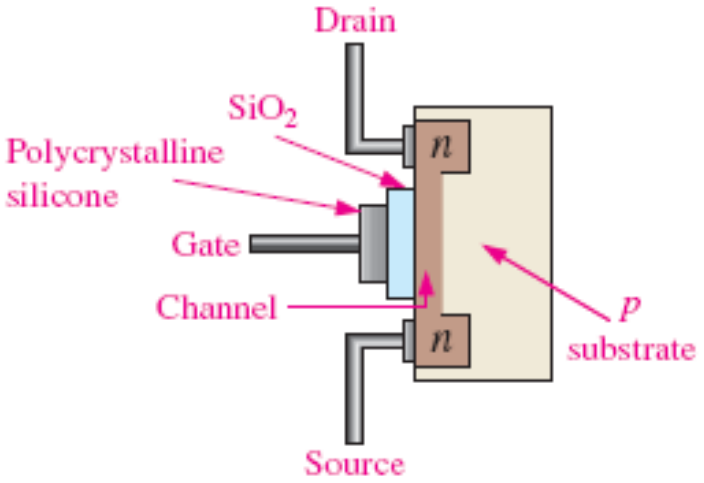


Depletion MOSFET (D-MOSFET)

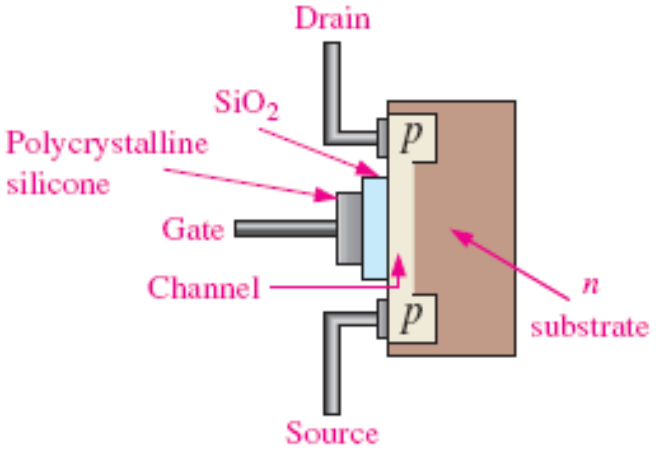
The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate.
Both n-channel and p-channel devices are shown in the figure.

The D-MOSFET can be operated in either of two modes, the depletion mode or the enhancement mode, and is sometimes called a depletion/enhancement MOSFET.

The n-channel MOSFET operates in the **depletion mode when a negative** gate-to-source voltage is applied and in the **enhancement mode when a positive** gate-to-source voltage is applied. These devices are generally operated in the depletion mode.



(a) *n* channel



(b) *p* channel

Depletion Mode

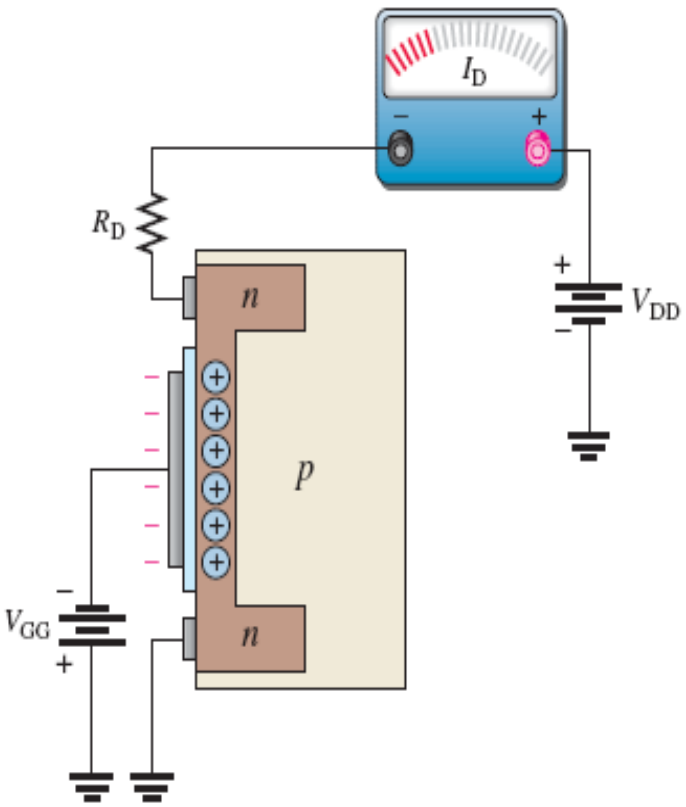
Visualize the gate as one plate of a parallel-plate capacitor and the channel as the other plate. The silicon dioxide insulating layer is the dielectric.

With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place.

Thereby, the n channel is depleted of some of its electrons, thus decreasing the channel conductivity.

The greater the negative voltage on the gate, the greater the depletion of n-channel electrons.

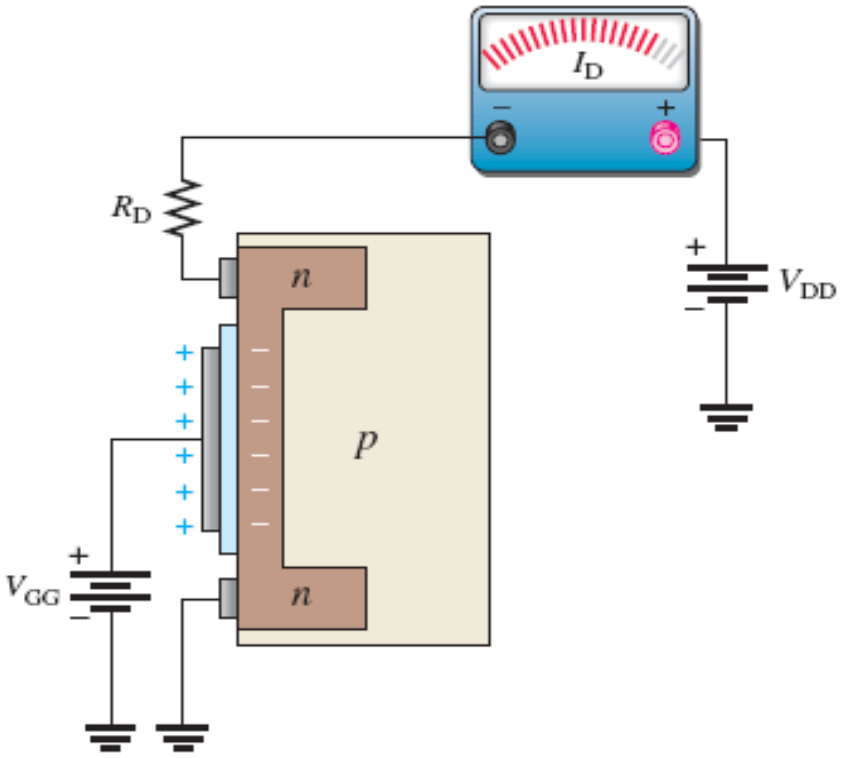
At a sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero. This depletion mode is illustrated in Figure. Like the n-channel JFET, the n-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$ and zero. In addition, the D-MOSFET conducts for values of V_{GS} above zero.



(a) Depletion mode: V_{GS} negative and less than $V_{GS(off)}$

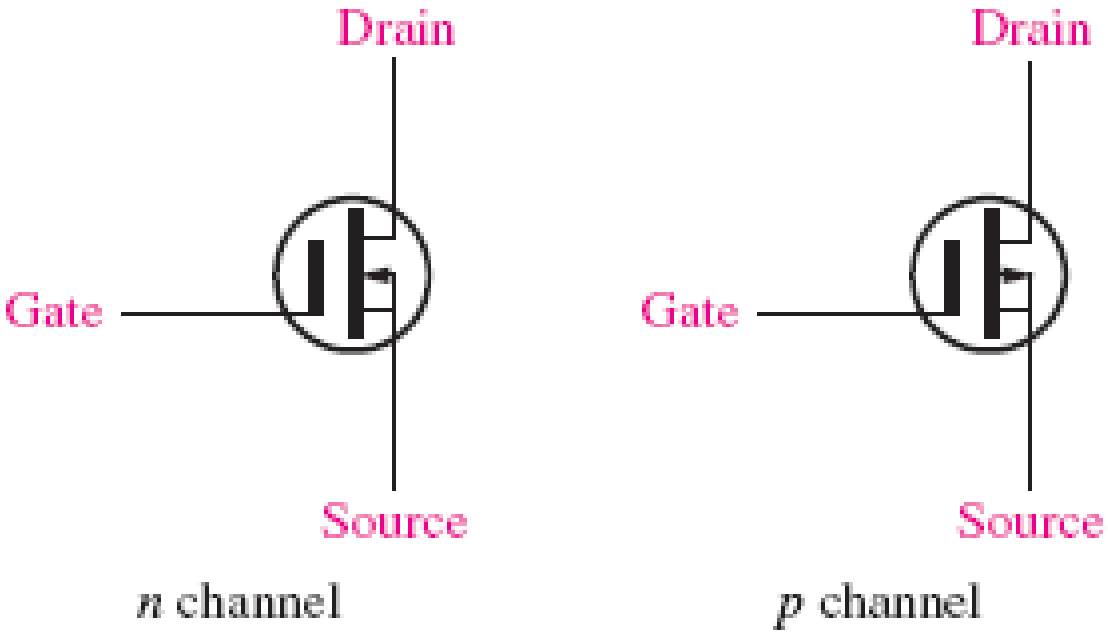
Enhancement Mode

With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure.



(b) Enhancement mode: V_{GS} positive

D-MOSFET Symbols

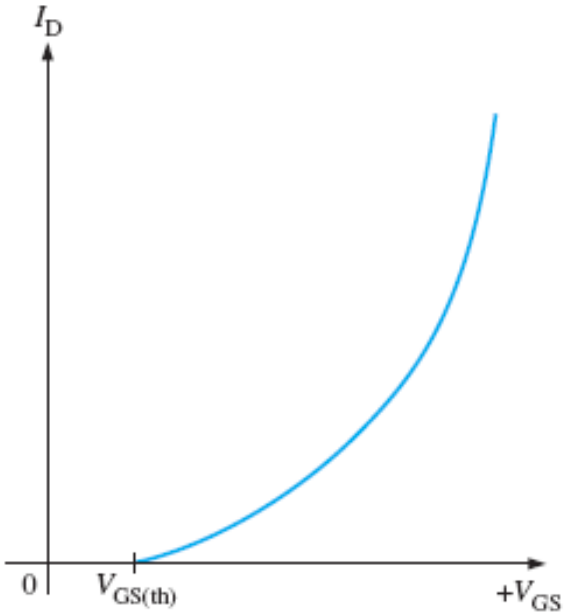


MOSFET CHARACTERISTICS AND PARAMETERS

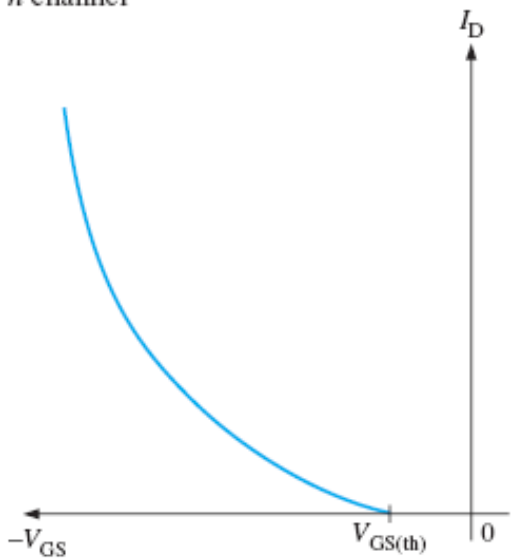
The E-MOSFET uses only channel enhancement. Therefore, an n-channel device requires a positive gate-to-source voltage, and a p-channel device requires a negative gate-to-source voltage.

As you can see, there is no drain current when $V_{GS} = 0$. Therefore, the
E-MOSFET does not have a significant I_{DSS} parameter, as do the JFET and the D-MOSFET.

Notice also that there is ideally no drain current until V_{GS} reaches a certain nonzero value called the threshold voltage, $V_{GS(th)}$.



(a) *n* channel



(b) *p* channel

The equation for the parabolic transfer characteristic curve of the E-MOSFET differs from that of the JFET and the D-MOSFET because the curve starts at $V_{GS(th)}$ rather than $V_{GS(off)}$ on the horizontal axis and never intersects the vertical axis.

The equation for the E-MOSFET transfer characteristic curve is

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

The constant K depends on the particular MOSFET and can be determined from the datasheet by taking the specified value of I_D, called $I_{D(on)}$, at the given value of V_{GS}

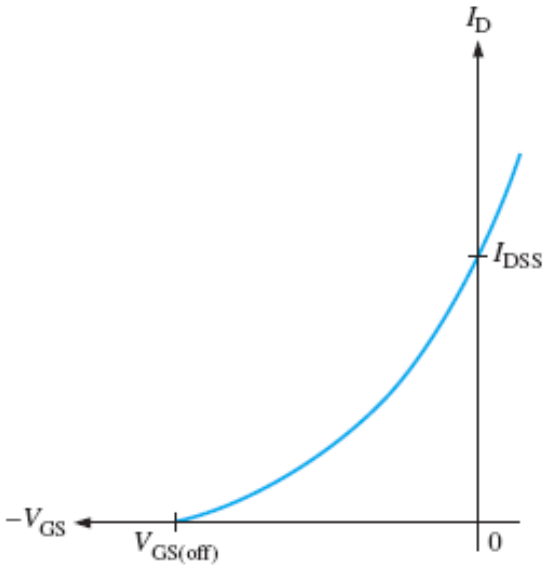
D-MOSFET Transfer Characteristic

Since the D-MOSFET can operate with either positive or negative gate voltages.

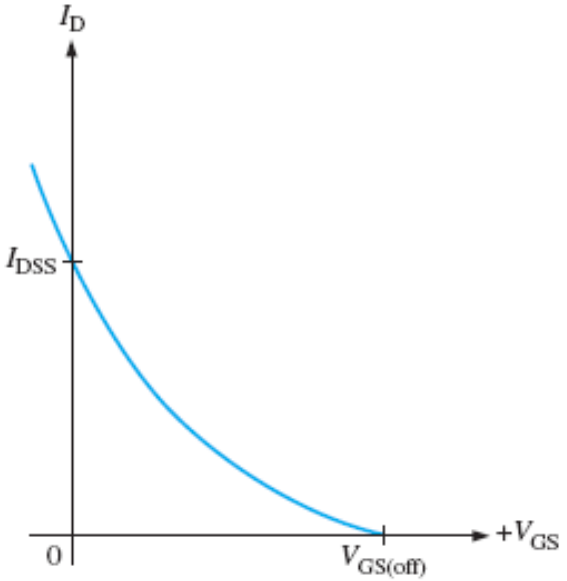
The point on the curves where $V_{GS} = 0$ corresponds to I_{DSS}. The point where $I_D = 0$ corresponds to $V_{GS(off)}$.

As with the JFET, The square-law expression in Equation for the JFET curve also applies to the D-MOSFET curve.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$



(a) *n* channel



(b) *p* channel

MOSFET BIASING

Three ways to bias a MOSFET are zero-bias, voltage-divider bias, and drain-feedback bias.

E-MOSFET Bias

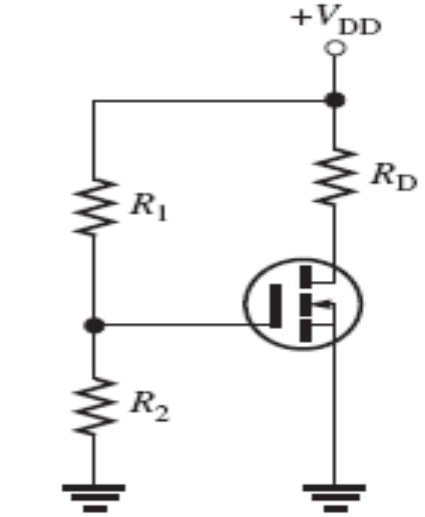
Because E-MOSFETs must have a VGS greater than the threshold value, $V_{GS(th)}$, zero bias cannot be used.
In either the voltage-divider or drain- feedback bias arrangement, the purpose is to make the gate voltage more positive than the source by an amount exceeding $V_{GS(th)}$.

In the drain-feedback bias, there is negligible gate current, therefore, no voltage drop across R_G. This makes $V_{GS} = V_{DS}$.

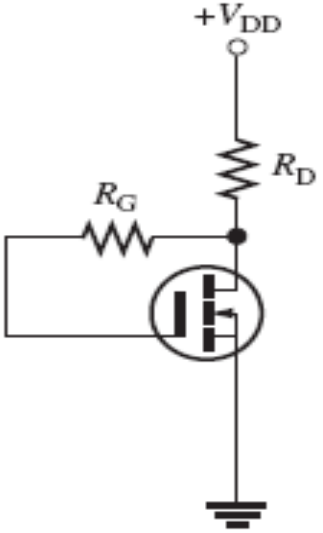
$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$V_{DS} = V_{DD} - I_D R_D$$

where $I_D = K(V_{GS} - V_{GS(th)})^2$



(a) Voltage-divider bias



(b) Drain-feedback bias

D-MOSFET Bias

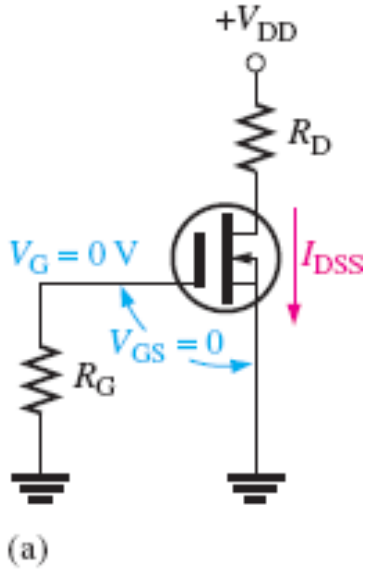
Recall that D-MOSFETs can be operated with either positive or negative values of V_{GS}.

A simple bias method is to set $V_{GS} = 0$ so that an ac signal at the gate varies the gate-to-source voltage above and below this 0 V bias point.

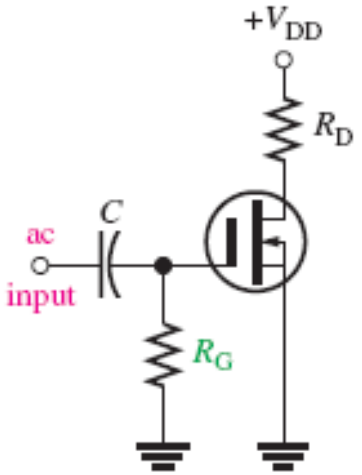
Since $V_{GS} = 0$, $I_D = I_{DSS}$ as indicated.
The drain-to-source voltage is expressed as follows:

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

The purpose of R_G is to accommodate an ac signal input by isolating it from ground, as shown in Figure (b).
Since there is no dc gate current, R_G does not affect the zero gate-to-source bias.



(a)



(b)