Transistor Bias Circuits

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DC Bias

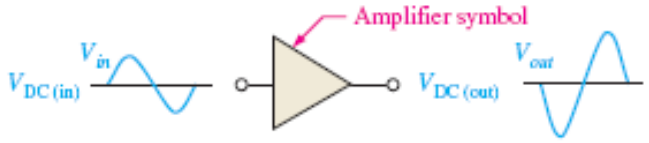
Bias establishes the dc operating point (**Q-point) for proper linear operation of an amplifier.**

If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied.

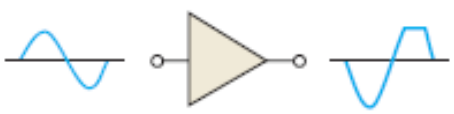
Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c).

Part (b) illustrates limiting of the positive portion of the output voltage as a result of a Q-point (dc operating point) being too close to cutoff.

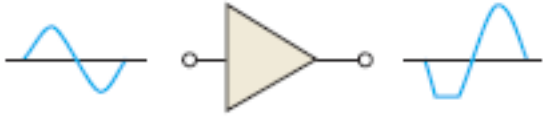
Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation.



(a) Linear operation: larger output has same shape as input except that it is inverted



(b) Nonlinear operation: output voltage limited (clipped) by cutoff

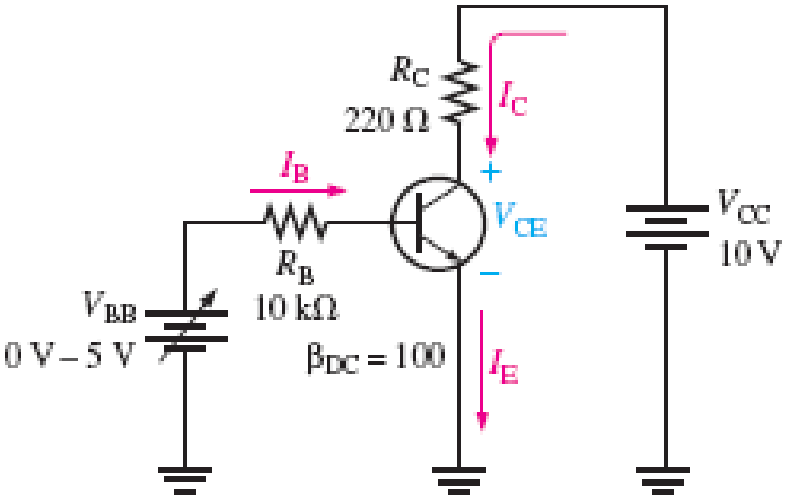


(c) Nonlinear operation: output voltage limited (clipped) by saturation

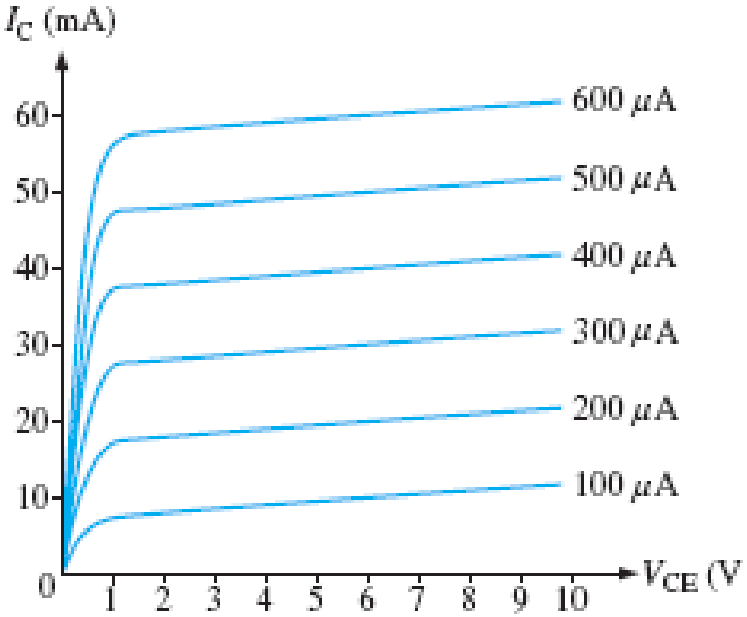
Graphical Analysis

The transistor in Figure (a) is biased with VCC and VBB to obtain certain values of I_B, I_C, I_E, and V_{CE}.

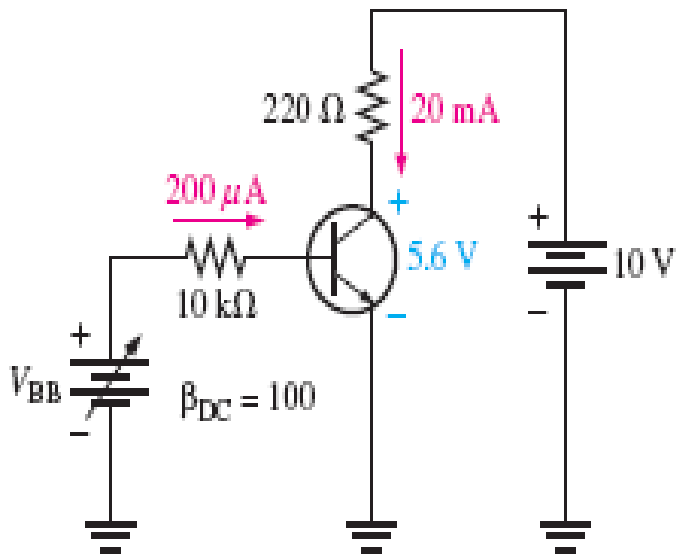
The collector characteristic curves for this particular transistor are shown in Figure (b); we will use these curves to graphically illustrate the effects of dc bias.



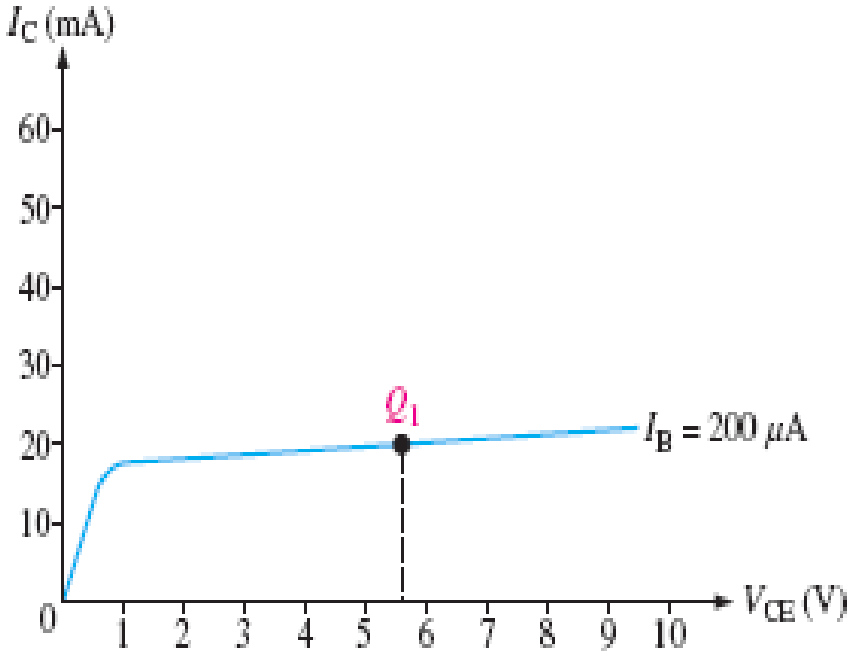
(a) DC biased circuit



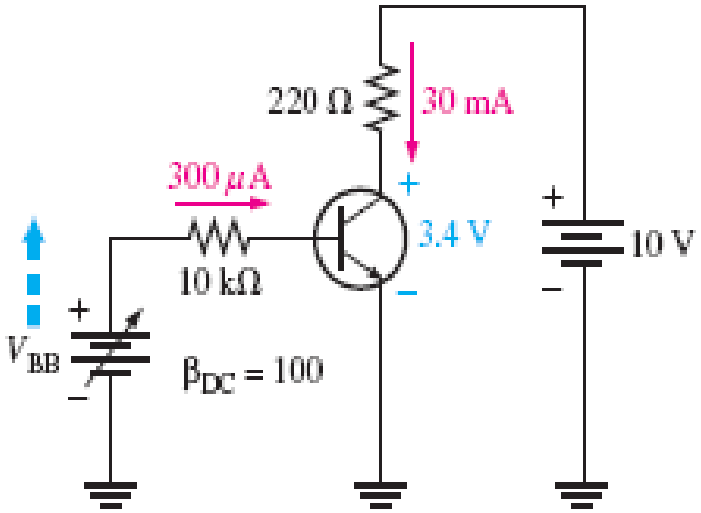
(b) Collector characteristic curves



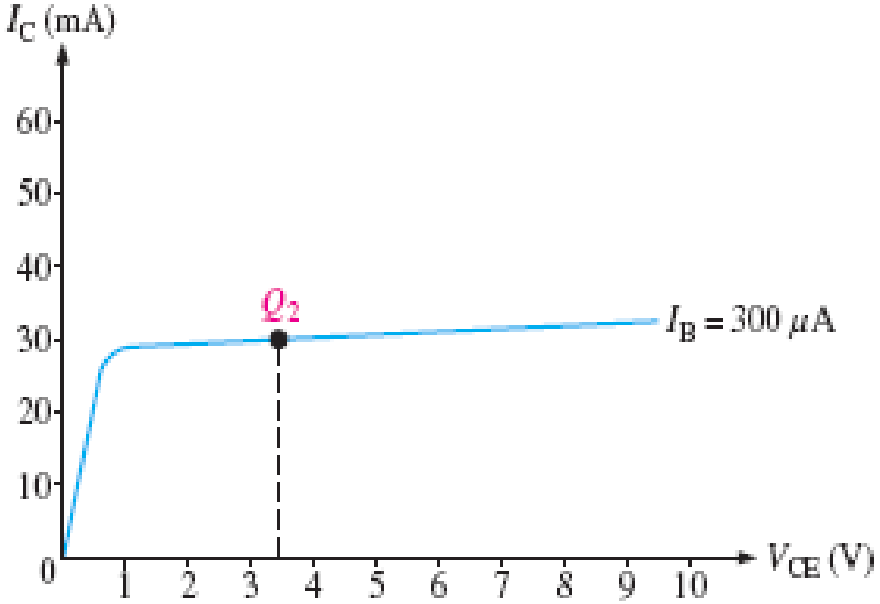
(a) $I_B = 200\ \mu A$



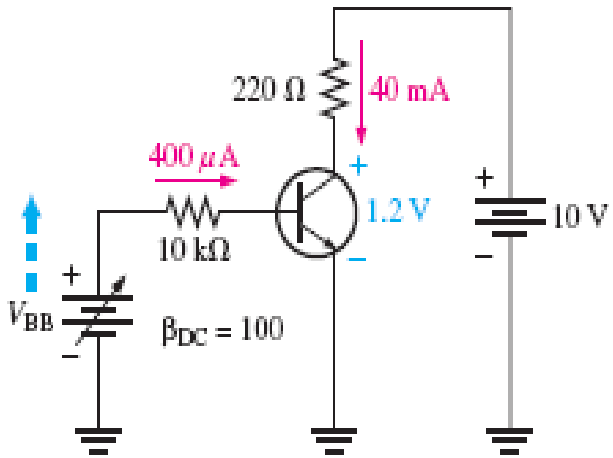
$$V_{CE} = V_{CC} - I_C R_C = 10\,\text{V} - (20\,\text{mA})(220\,\Omega) = 10\,\text{V} - 4.4\,\text{V} = 5.6\,\text{V}$$



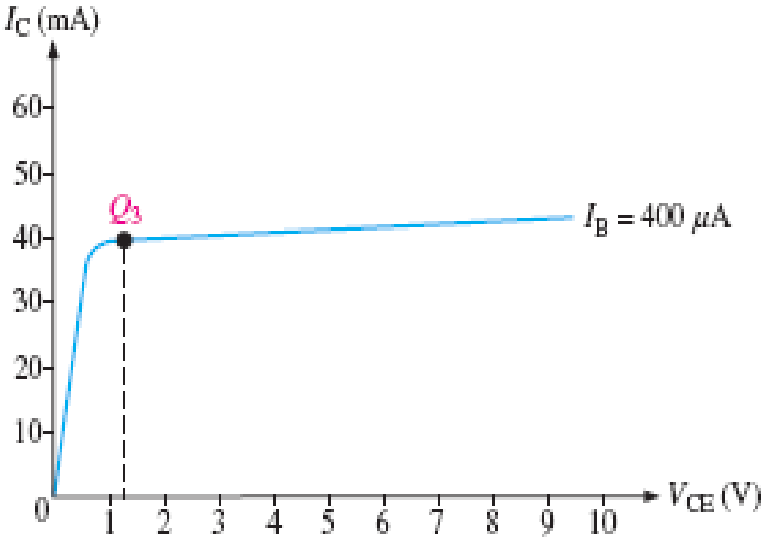
(b) Increase I_B to 300 μ A by increasing V_{BB}



$$V_{CE} = 10\,V - (30\,mA)(220\,\Omega) = 10\,V - 6.6\,V = 3.4\,V$$



(c) Increase I_B to 400 μA by increasing V_{BB}



$$V_{CE} = 10\,V - (40\,mA)(220\,\Omega) = 10\,V - 8.8\,V = 1.2\,V$$

DC Load Line

The dc operation of a transistor circuit can be described graphically using a dc load line. This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the y-axis to the cutoff value where V_{CE} V_{CC} on the x-axis,

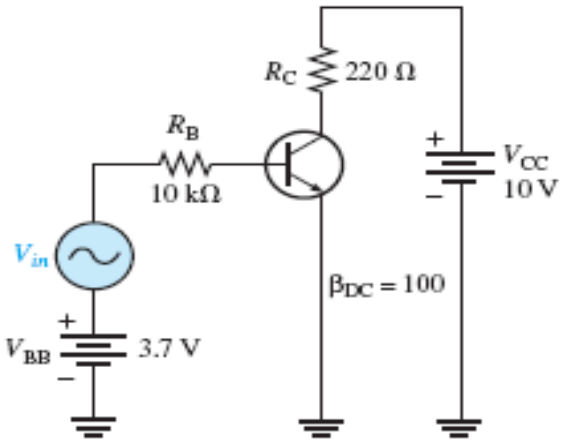
$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C} = -\left(\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C}$$

This is the equation of a straight line with a slope of $-1/R_C$, an x intercept of $V_{CE} = V_{CC}$, and a y intercept of V_{CC}/R_C, which is $I_{C(sat)}$.

Linear Operation

The region along the load line including all points between saturation and cutoff is generally known as the linear region of the transistor's operation.

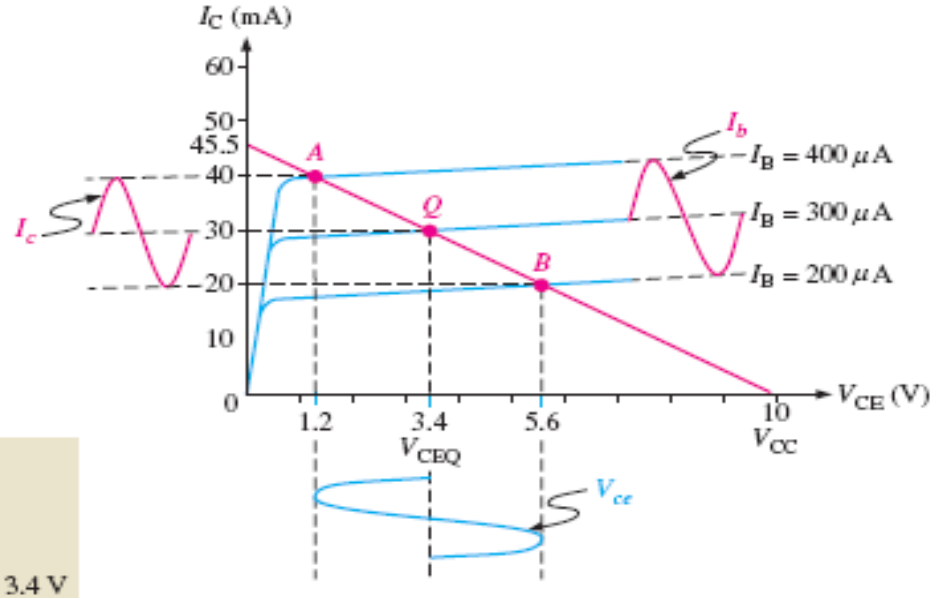
As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.



$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\,\mu\text{A}$$

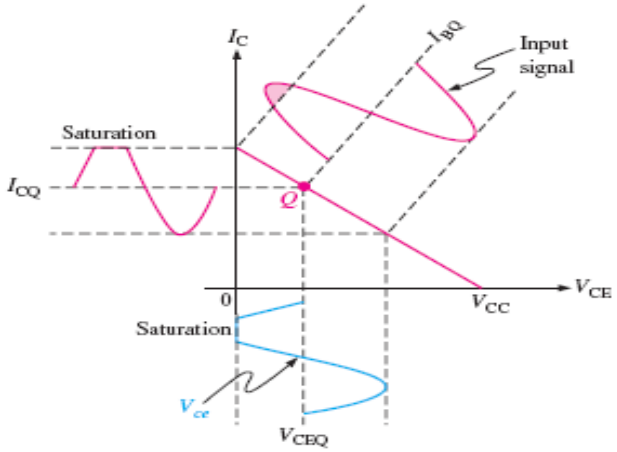
$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\,\mu\text{A}) = 30\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\text{ V} - (30\text{ mA})(220\,\Omega) = 3.4\text{ V}$$

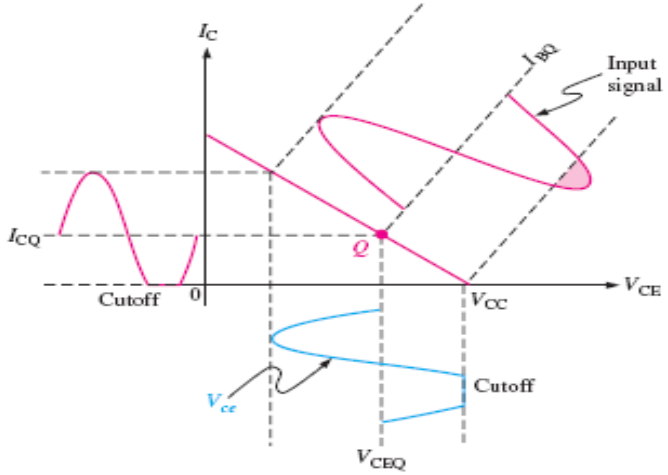


Waveform Distortion

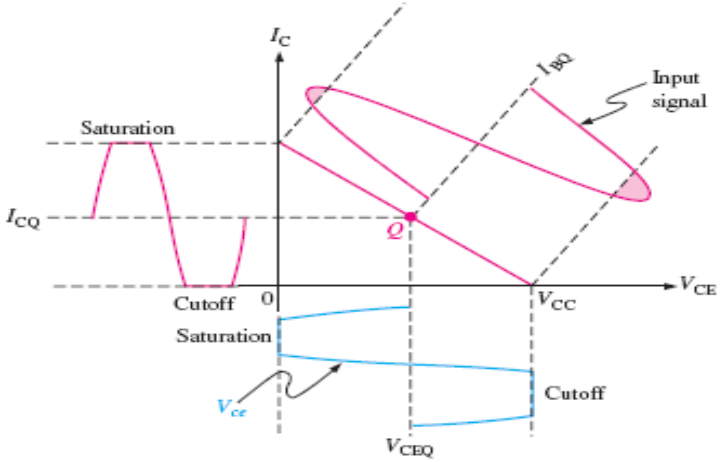
As previously mentioned, under certain input signal conditions the location of the Q-point on the load line can cause one peak of the Vce waveform to be limited or clipped,



(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



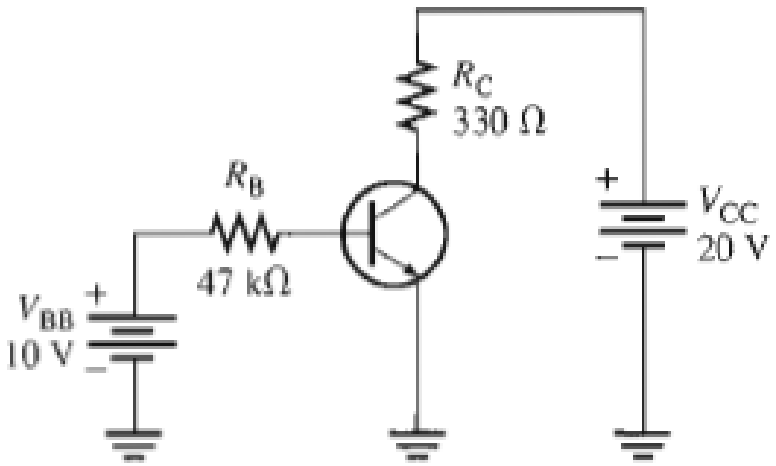
(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.



(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

Example

Determine the Q-point for the circuit in Figure 5–7. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 200$.



The Q-point is defined by the values of I_C and V_{CE}. Find these values by using formulas you learned in Chapter 4.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 198\ \mu\text{A}$$

$$I_C = \beta_{DC} I_B = (200)(198\ \mu\text{A}) = \mathbf{39.6\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - 13.07\text{ V} = \mathbf{6.93\ V}$$

The Q-point is at $I_C = 39.6$ mA and at $V_{CE} = 6.93$ V.

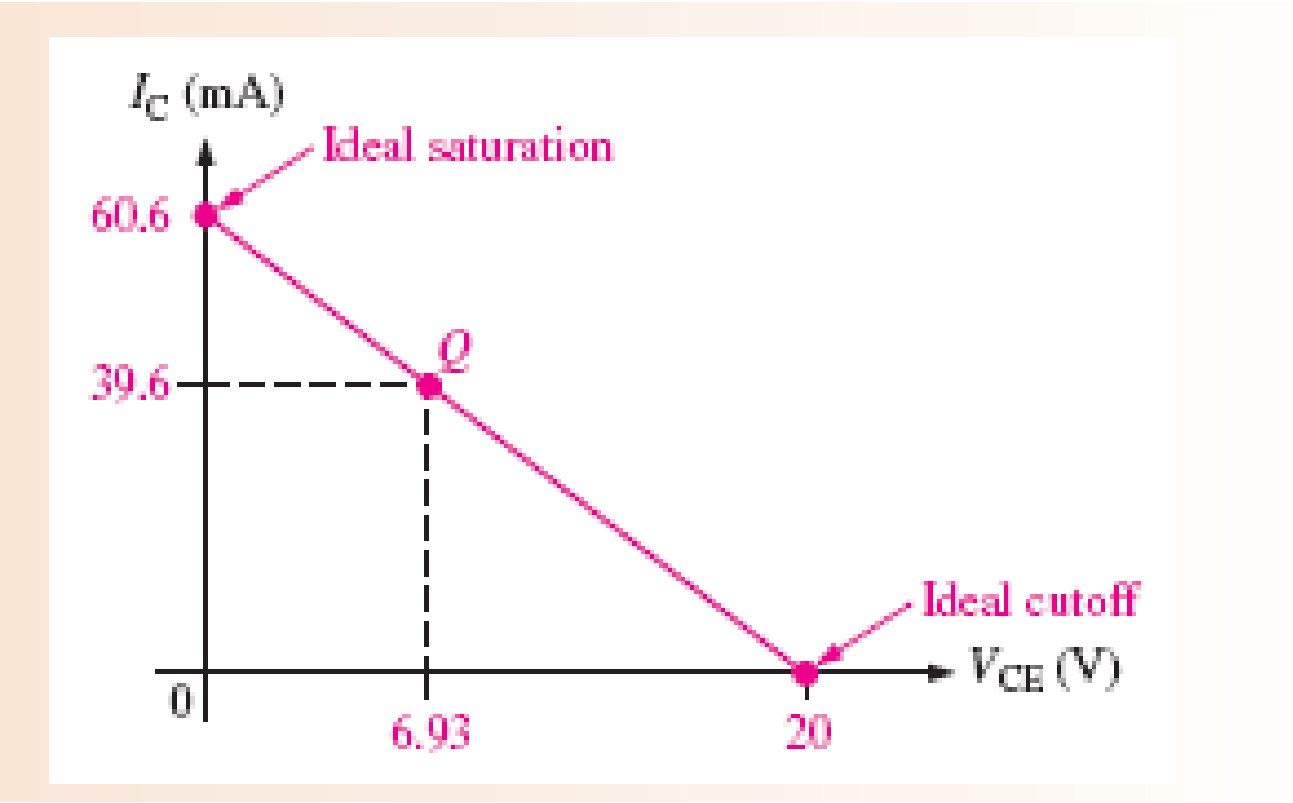
Since $I_{C(cutoff)} = 0$, you need to know $I_{C(sat)}$ to determine how much variation in collector current can occur and still maintain linear operation of the transistor.

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{330\ \Omega} = 60.6\text{ mA}$$

The dc load line is graphically illustrated in Figure 5–8, showing that before saturation is reached, I_C can increase an amount ideally equal to

$$I_{C(sat)} - I_{CQ} = 60.6\text{ mA} - 39.6\text{ mA} = 21\text{ mA}$$

However, I_C can decrease by 39.6 mA before cutoff ($I_C = 0$) is reached. Therefore, the limiting excursion is 21 mA because the *Q-point is closer to saturation than to cutoff.* The 21 mA is the maximum peak variation of the collector current. Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero.



Determine the maximum peak variation of the base current as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21\text{ mA}}{200} = \mathbf{105\ \mu A}$$