MOSFETS LOGIC GATES

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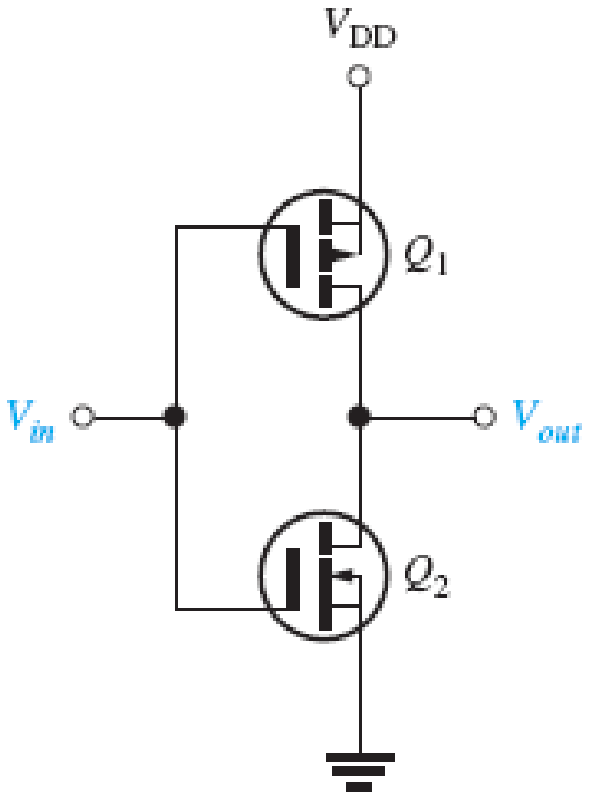
CMOS (Complementary MOS)

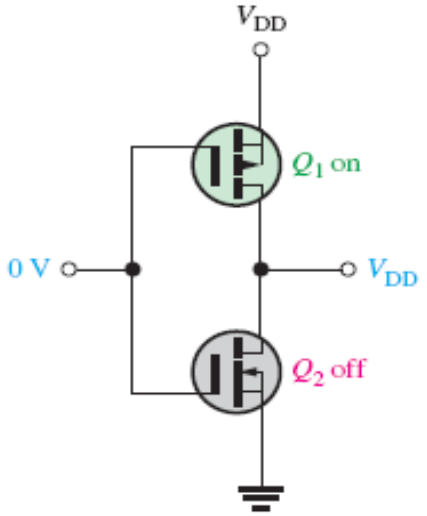
CMOS combines n-channel and p- channel E-MOSFETs in a series arrangement The input voltage at the gates is either 0 V or V_{DD}. Notice that V_{DD} and ground are both connected to source terminals of the transistors.

The term V_{DD} is used for the positive voltage, which is on the p-channel device's source terminal.



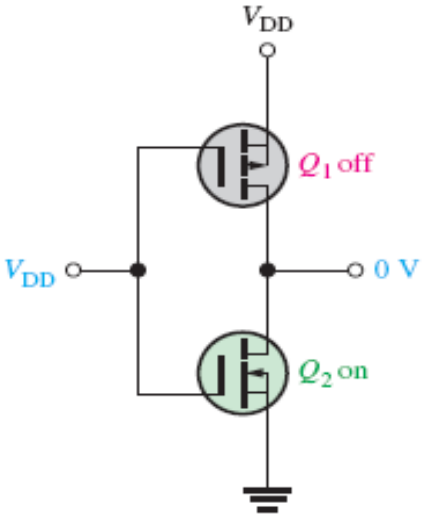
When V_{in} = 0 V, Q1 is on and Q_2 is off.

Because Q_1 is acting as a closed switch, the output is approximately V_{DD}.



When V_{in} = V_{DD}, Q_2 is on and Q_1 is off,

Because Q_2 is acting as a closed switch, the output is essentially connected to ground (0 V).

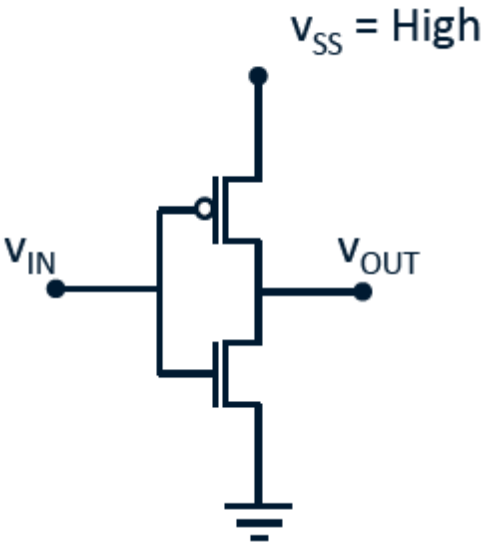


Inverter

V_{IN}	V_{OUT}
High	Low
Low	High

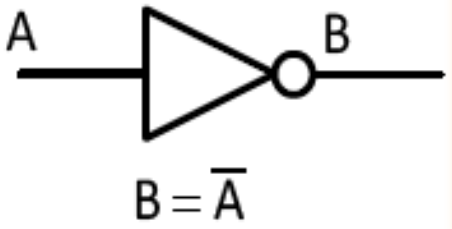
Truth Table

A	B
0	1
1	0



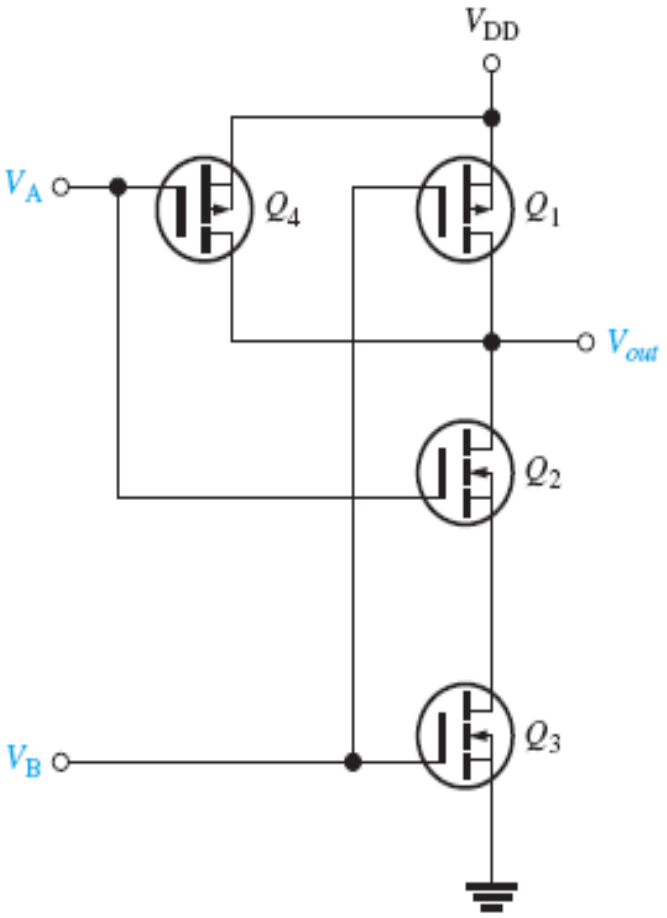
NOT

A	B
0	1
1	0



NAND

V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	off	off	on	V_{DD}
0	V_{DD}	off	off	on	on	V_{DD}
V_{DD}	0	on	on	off	off	V_{DD}
V_{DD}	V_{DD}	off	on	on	off	0

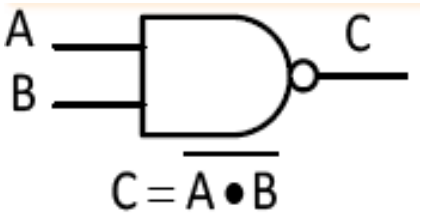


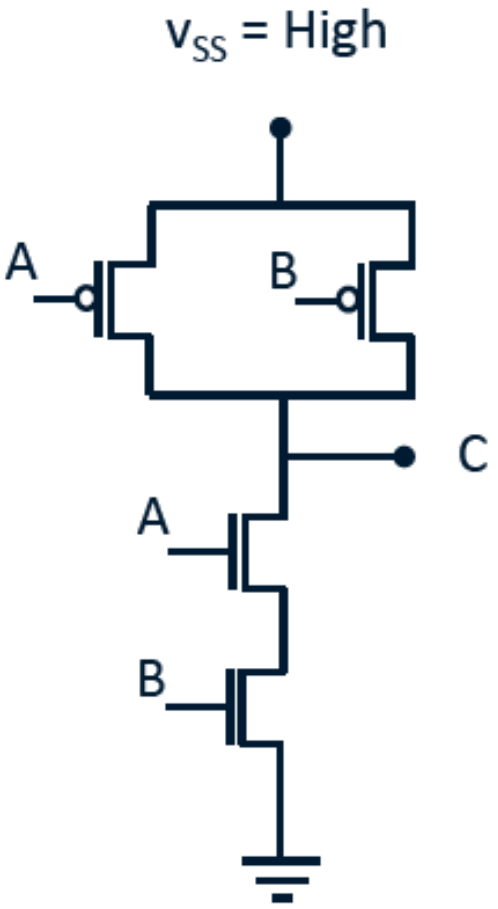
When V_A and V_B are high, the output is low; otherwise, the output is high.

NAND

NAND

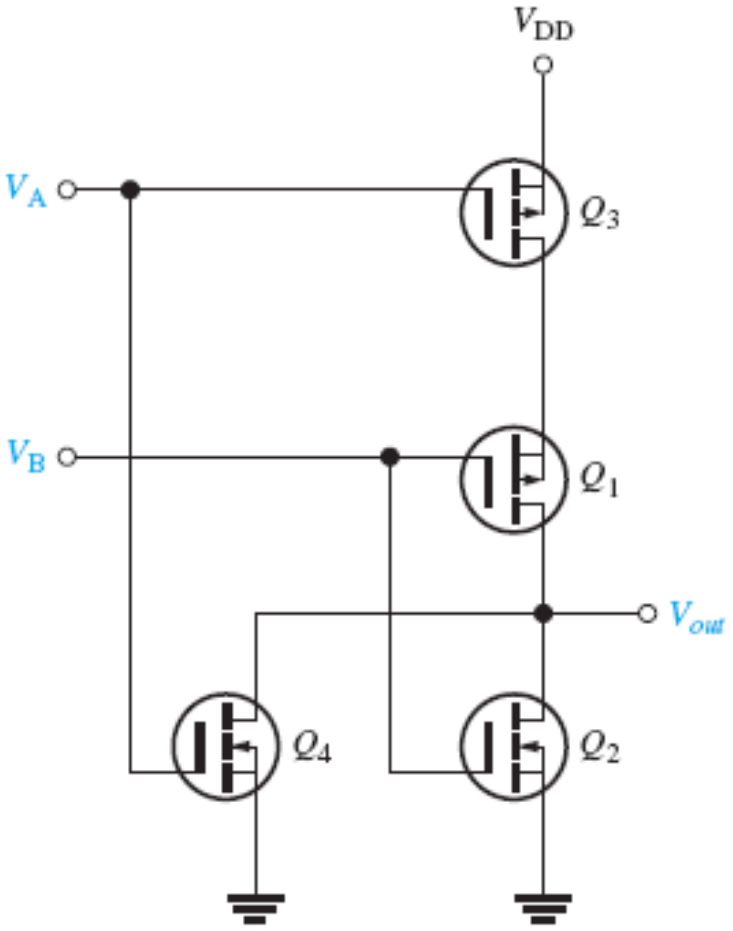
A B	C
0 0	1
0 1	1
1 0	1
1 1	0





NOR

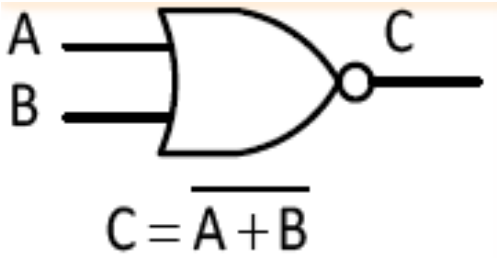
V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	off	on	off	V_{DD}
0	V_{DD}	off	on	on	off	0
V_{DD}	0	on	off	on	off	0
V_{DD}	V_{DD}	off	on	off	on	0

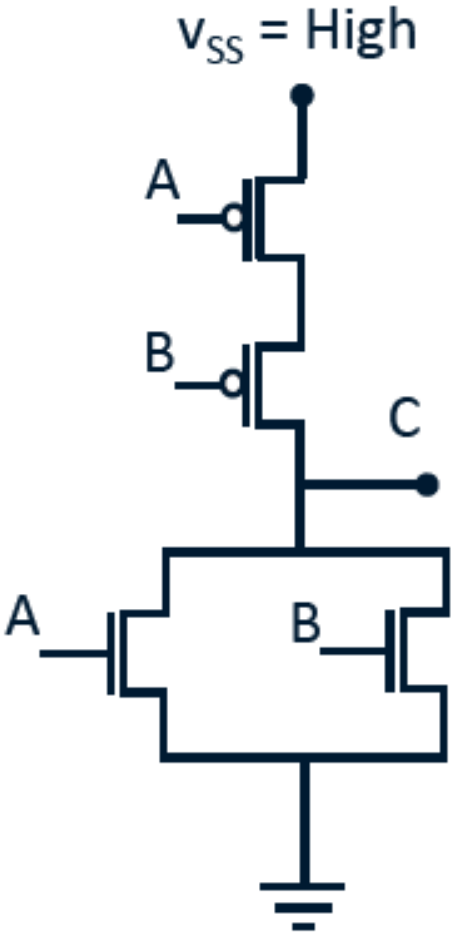


NOR

NOR

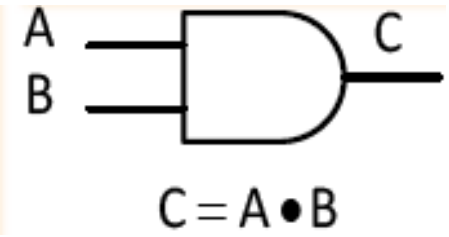
A B	C
0 0	1
0 1	0
1 0	0
1 1	0



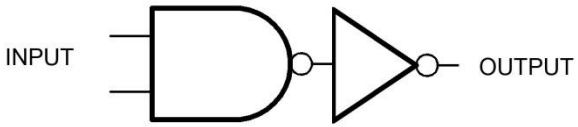


AND

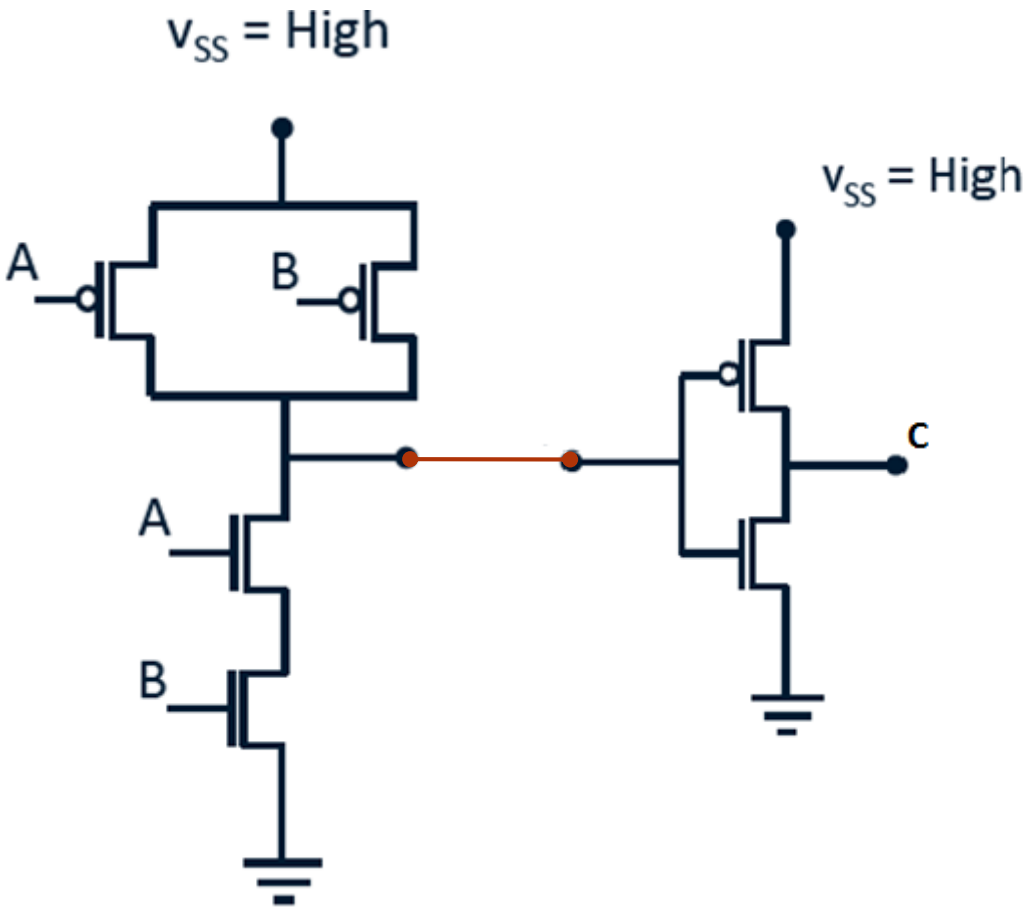
AND	
A B	C
0 0	0
0 1	0
1 0	0
1 1	1



May you draw the circuit now….?

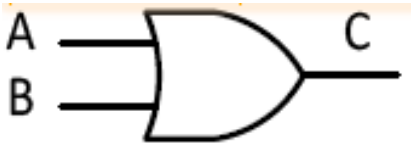


AND



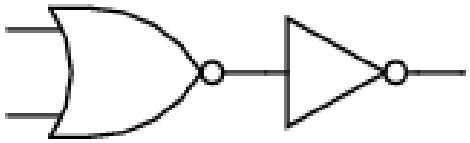
OR

A B	C
0 0	0
0 1	1
1 0	1
1 1	1



$C = A + B$

May you draw the circuit now….?



OR