FAST NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES
KARACHI CAMPUS.
FINAL EXAMINIATION, Spring 2018 Practice

Computer Logic Design (EE 227)

Total Points: 40 | 10 *May, 2018* | Time Allowed: 135 minutes

Section B

Roll No: _____ **Student's Signature:** _____

Note : 1. Attempt *all* questions.
2. **Sequence of questions and its respective parts is important, otherwise marks will be deducted.**

Table 4(a): Excitation Table for J-K Flip-Flop

Output Transitions		Flip-Flop Inputs	
Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table 5: Truth Table for S-R and J-K Flip-Flops

A	B	Q_N
0	0	NC
0	1	0
1	0	1
1	1	Invalid /Toggle

Table 4(a): Excitation Table for J-K Flip-Flop

Q	Q_N	D
0	0	0
0	1	1
1	0	0
1	1	1

Combinational Logic Circuits --- Design & Implementations

Q. No. 2 (a) Simplify and then implement the following Boolean function F using two-level forms of logic by using OR-NAND gates. [02 Credits]

$F(A, B, C, D) = \Pi(1, 3, 7, 9, 11, 12, 14) = \sum(0, 2, 4, 5, 6, 8, 10, 13, 15)$

(b) Design a 4-to-2 line priority (MSB) encoder. Also write its VHDL code using the if-then else statements. [02 Credits]

Q. No. 3 Implement the logic expression derived in Q. No. 2 using: [04 Credits]

(i) a 16-to-1 Multiplexer
(ii) 4-to-16 Decoder and OR gates

Q. No. 4 (a) Design a Gray Code to BCD converter. [02 Credits]

(b) Implement a full adder circuit by using: [04 Credits]

(i) 3 – to - 8 line Decoder

(ii) 4 X 1 Multiplexers

Q. No. 5 A BCD-to-seven segment decoder, is a combinational logic circuit that converts a coded decimal number to a suitable code for the input of a seven segment display. The decoder has four inputs (A, B, C, D) and seven outputs (a, b, c, d, e, f, g). The seven segment display consists of seven LEDs (Light Emitting Diode), each of which is called a segment, to display the decimal numbers. When an output of the decoder becomes logical 1, the corresponding LED lights.

For the output *a*, obtain the simplified Boolean function by means of the Karnaugh map. [02 Credits]

Waveforms Formation

Q. No. 6 (a) The input waveforms in Figure 02 are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram. [02 Credits]

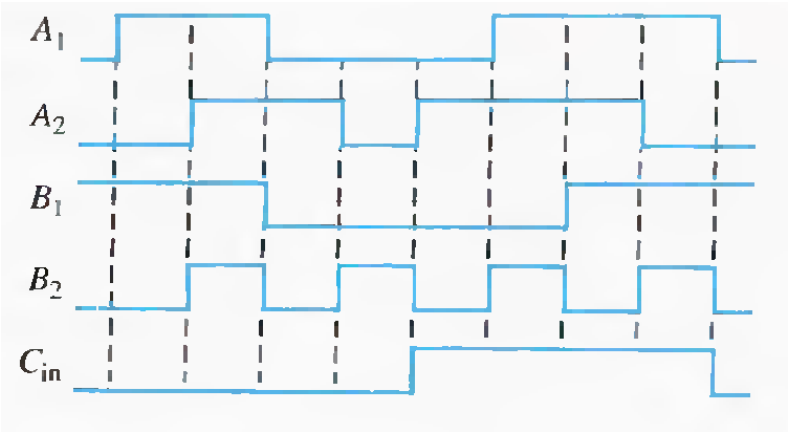

Figure 02

(b) The serial data-input waveform (Data in) and data-select inputs (S_0 and S_1) are shown in Figure 3(b). Determine the data-output waveforms of D_0 through D_3 for the demultiplexer in Figure 3(a).

[02 Credits]

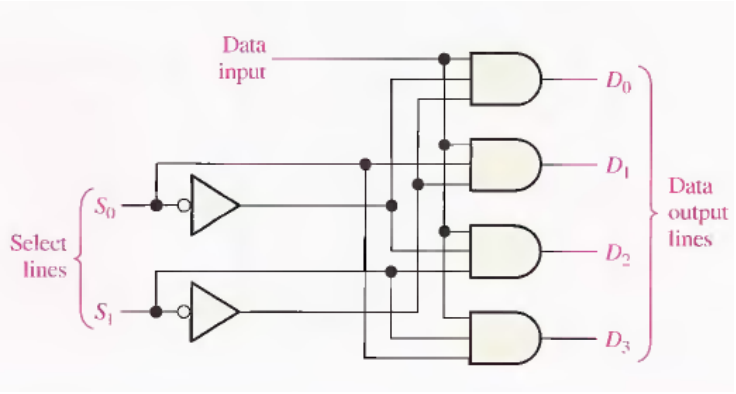

Figure 03 (a)

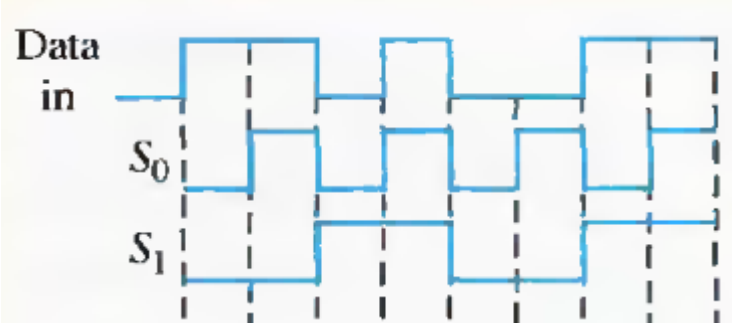

Figure 03 (b)

Sequential Logic Circuits --- Design & Implementations

Q. No. 7 (a) Determine the sequence of the counter in Figure 4. Also, implement the decoding of binary states 2 and 4 in the following 3-bit counter. [02 Credits]

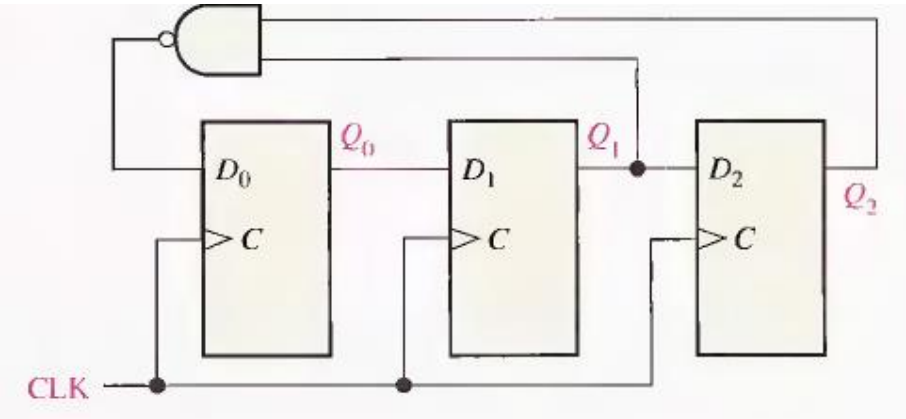

Figure 04

(b) The direct current required by a particular flip-flop that operates on a +5 V dc source is found to be 12 mA. A certain digital device uses 100 of these flip-flops. Determine the current capacity required for the + 5 V dc supply and the total power dissipation of the system. [02 Credits]

Q. No. 8 Design a counter that counts down, with the repeated sequence: 2, 1, 0, when the input to the counter circuit is 1. The counter does not count (stays at the same state) when the input is 0. The circuit is to be designed by treating the unused states as don't care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states. [04 Credits]

Waveforms Formation

Q. No. 9 (a) The Q output of an edge-triggered S-R flip-flop is shown in relation to the clock signal in Figure 5. Determine the input waveforms on the S and R inputs that are required to produce this output if the flip-flop is a positive edge-triggered type. [02 Credits]

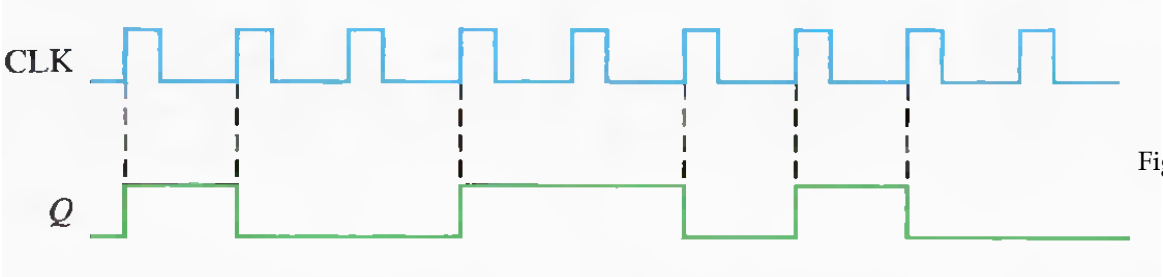

Figure 5

(b) Determine the Q waveform relative to the clock if the signals shown in Figure 6 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW. [02 Credits]

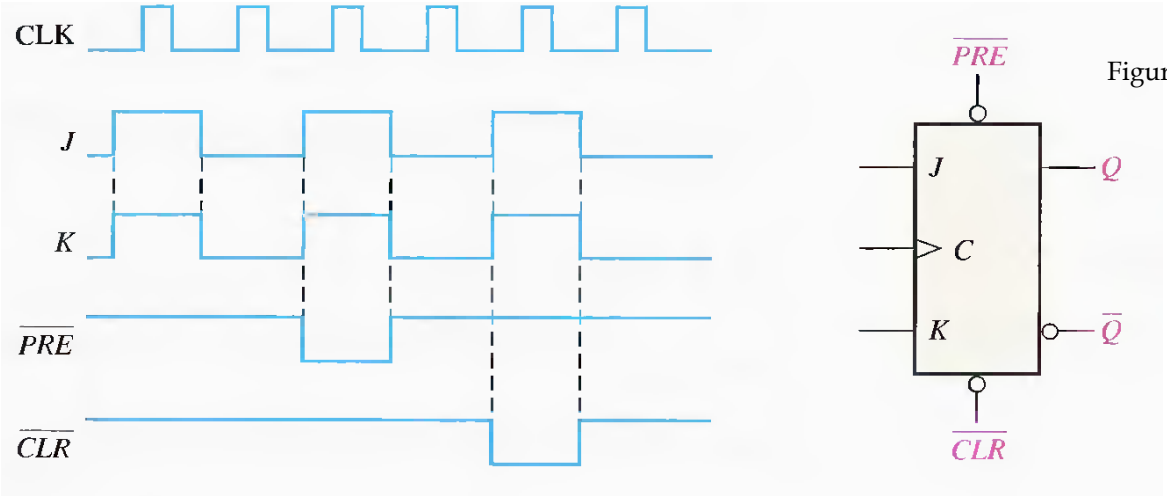

Figure 6

(c) A master-slave *D* flip-flop constructed with two *D* latches and an inverter is shown in Figure 7(a). The clock pulses and the logical level changes at the input of the master flip-flop are given in Figure 7(b). Assuming that the outputs *Y* and *Q* are both initially at logical level 0, draw the logical levels at the *Y* and *Q* outputs of the *D* flip-flops on the same timing diagram. [02 Credits]

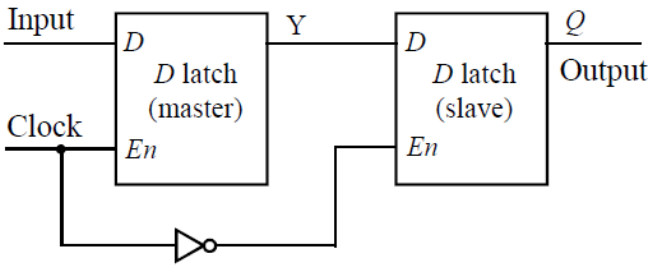

Figure 07(a)

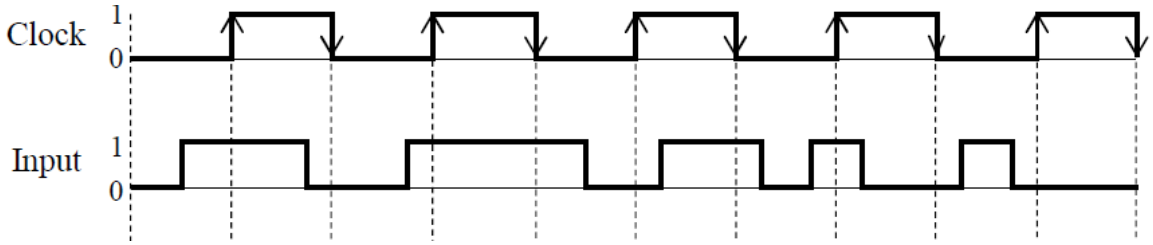

Figure 07(b)

(d) A master-slave flip-flop constructed with two negative-edge triggered T flip-flops is shown in Figure 8(a). The characteristic table of the T flip-flop is given in Table 6.The clock pulses and the logical level changes at the input of the master flip-flop are shown in Figure 8(b). Assuming that the outputs Y and Q are both initially at logical level 0, draw the logical levels at the Y and Q outputs of the T flip-flops on the same timing diagram. [02 Credits]

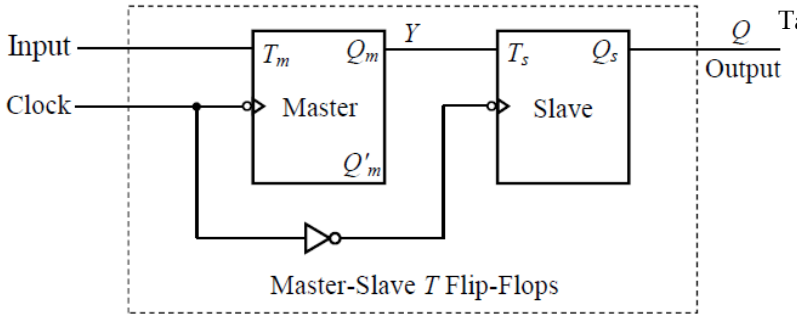

Figure 08(a)

Table 6: Characteristic table of the T flip-flop

Q	T	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0

At the triggering instant:

For $t = 0$: $Q(t+1) = Q(t)$

For $t = 1$: $Q(t+1) = Q'(t)$

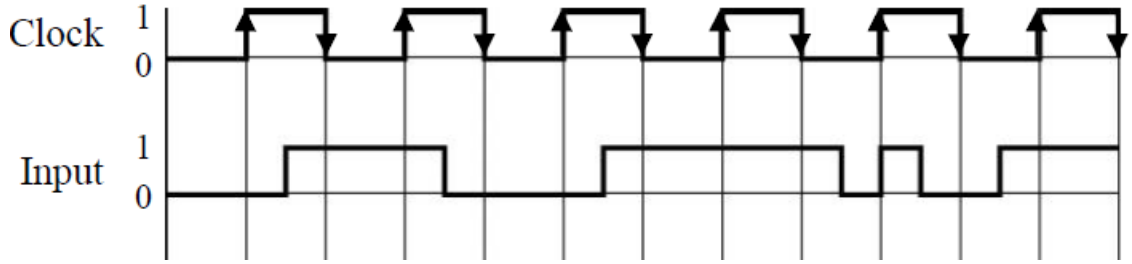

Figure 08(b)

Q. No. 10 (a) Design a 4-bit serial in/parallel out shift register. Also, show a complete timing diagram showing the parallel outputs for the designed serial in/parallel out shift register. Use the waveforms in Figure 9. Assume that the registers are initially cleared (all 0s). [02 Credits]

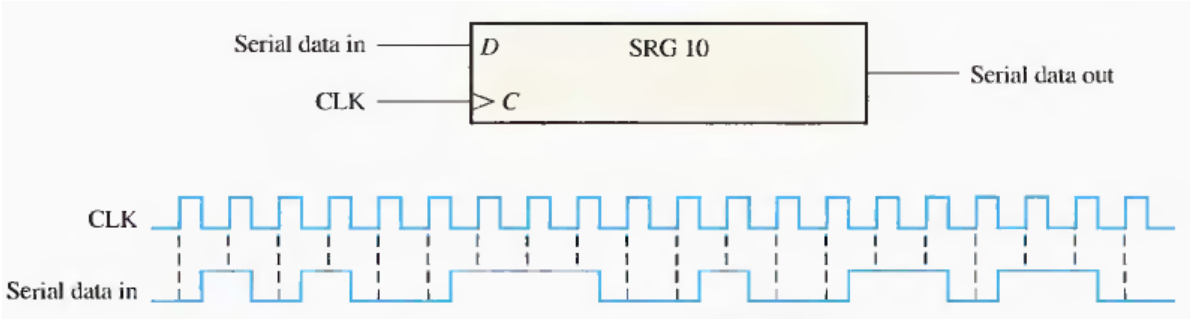

Figure 09

(b) Show the data-out put waveform for a 4-bit register with the parallel input data and the clock and SHIFT/LOAD waveforms given in Figure 10(b). Refer Figure 10(a) for the logic diagram.

[02 Credits]

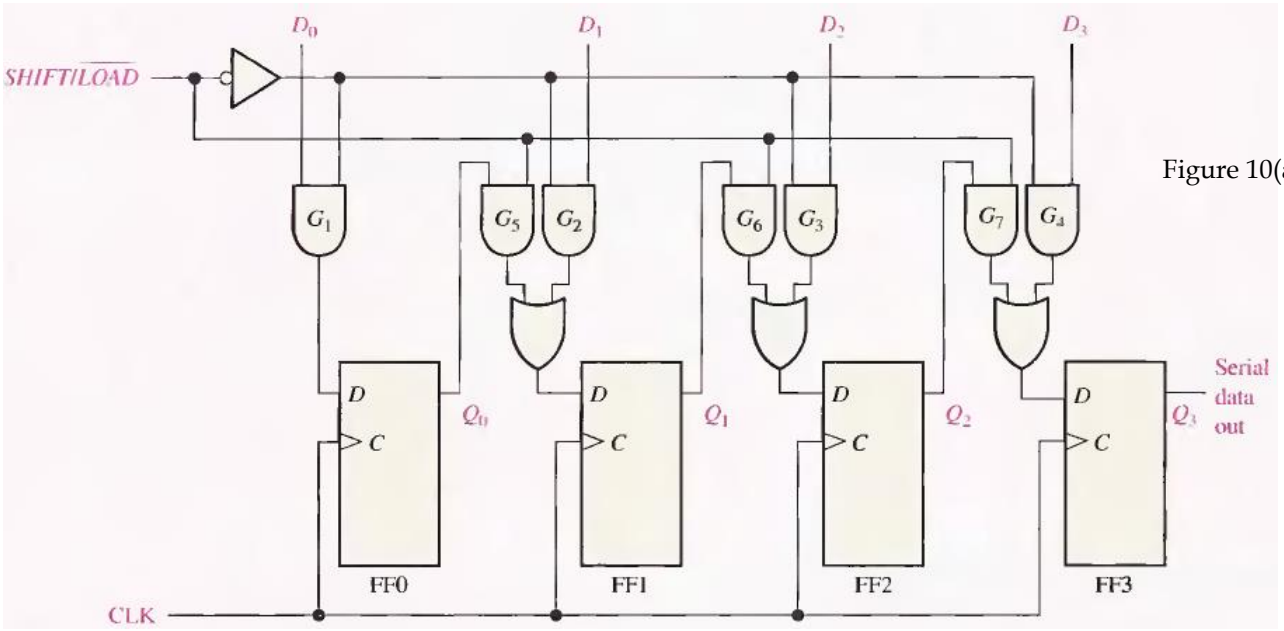

Figure 10(a)

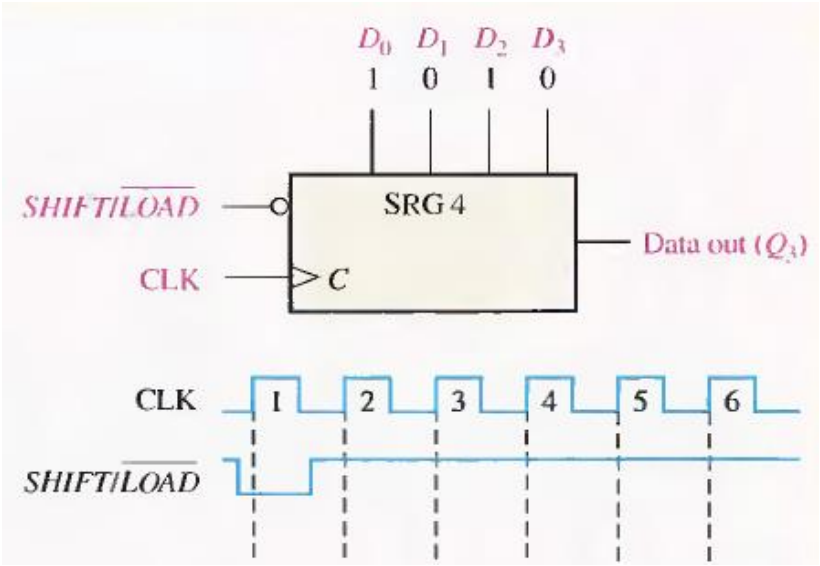

Figure 10(b)