Chapter-7 (Practice Questions)

1. If the waveforms in Figure 7–70 are applied to an active-HIGH S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q starts LOW.

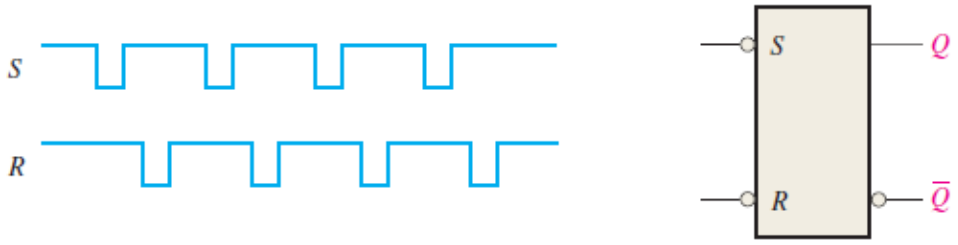

FIGURE 7–70

2. Solve Problem 1 for the input waveforms in Figure 7–71 applied to an active-LOW $\overline{S} - \overline{R}$ latch.

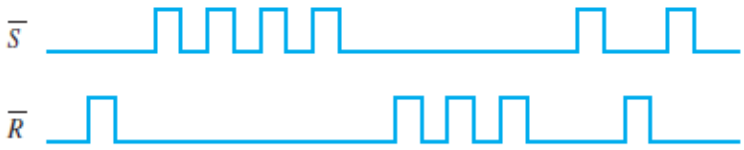

FIGURE 7–71

3. Solve Problem 1 for the input waveform in Figure 7–72.

FIGURE 7–72

4. For a gated S-R latch, determine the Q and $\overline{Q}$ outputs for the inputs in Figure 7–73. Show them in proper relation to the enable input. Assume that Q starts LOW.

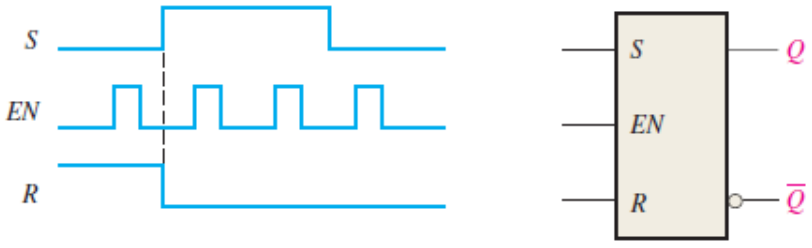

FIGURE 7–73

5. Determine the output of a gated D latch for the inputs in Figure 7–74.

FIGURE 7–74

6. Determine the output of a gated D latch for the inputs in Figure 7–75.

FIGURE 7–75

7. For a gated D latch, the waveforms shown in Figure 7–76 are observed on its inputs. Draw the timing diagram showing the output waveform you would expect to see at Q if the latch is initially RESET.

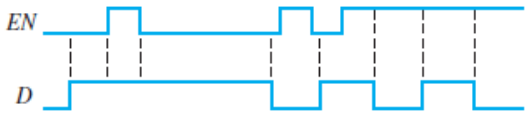

FIGURE 7–76

Section 7–2 Flip-Flops

8. Two edge-triggered J-K flip-flops are shown in Figure 7–77. If the inputs are as shown, draw the Q output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.

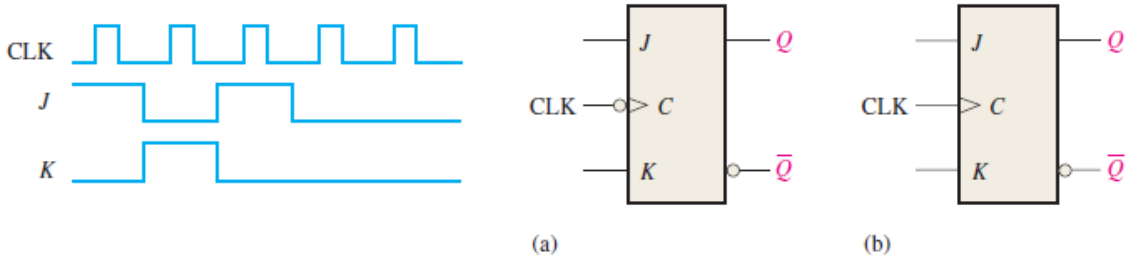

FIGURE 7–77

9. The Q output of an edge-triggered D flip-flop is shown in relation to the clock signal in Figure 7–78. Determine the input waveform on the D input that is required to produce this output if the flip-flop is a positive edge-triggered type.

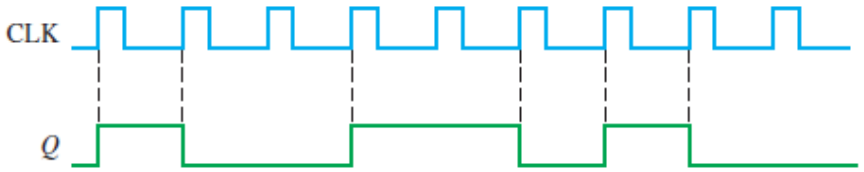

FIGURE 7–78

10. Draw the Q output relative to the clock for a D flip-flop with the inputs as shown in Figure 7–79. Assume positive edge-triggering and Q initially LOW.

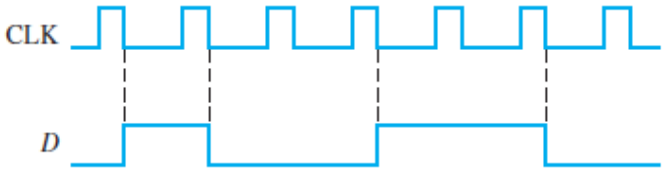

FIGURE 7–79

11. Solve Problem 10 for the inputs in Figure 7–80.

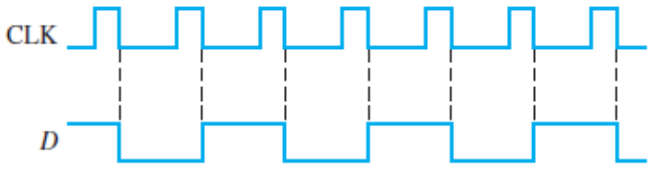

FIGURE 7–80

12. For a positive edge-triggered D flip-flop with the input as shown in Figure 7–81, determine the *Q* output relative to the clock. Assume that *Q* starts LOW.

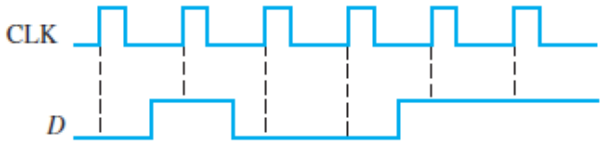

FIGURE 7–81

13. Solve Problem 12 for the input in Figure 7–82.

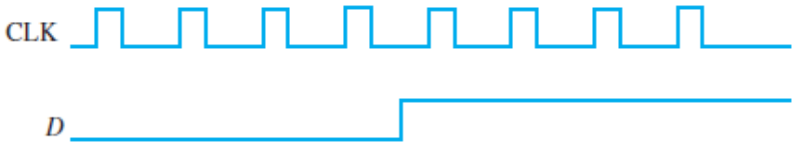

FIGURE 7–82

14. Determine the Q waveform relative to the clock if the signals shown in Figure 7–83 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.

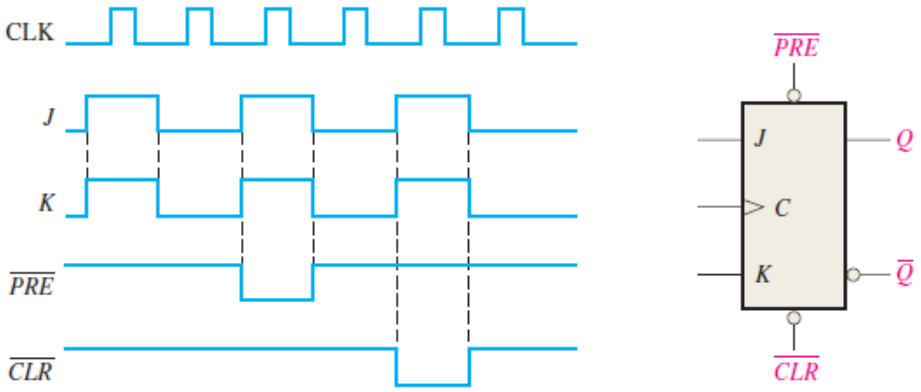

FIGURE 7–83

15. For a negative edge-triggered J-K flip-flop with the inputs in Figure 7–84, develop the Q output waveform relative to the clock. Assume that Q is initially LOW.

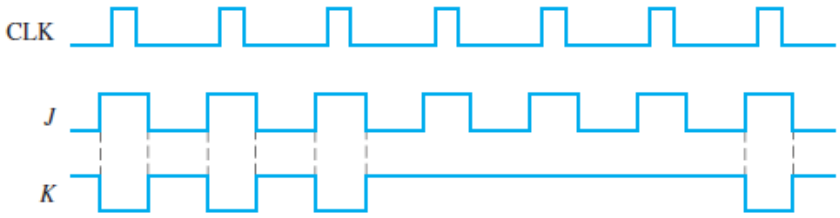

FIGURE 7–84