FAST NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES

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FINAL EXAMINIATIONS Spring 2018

Digital Logic Design (EE-227)

Total Points: 30 *10 May, 2018* Time Allowed: 45 Minutes

"I certify that I have neither received nor given unpermitted aid on this examination and that I have reported all such incidents observed by me in which unpermitted aid is given."

Student Roll No: _____ Section: **A / B / C / D / E / F**

Signature: _____ *Invigilator's Signature*: _____

Instructions:

1. Please verify that your paper contains 05 pages including this cover.
2. Write down your Student-Id on the top of each page.
3. This exam is closed book. No notes or other materials are permitted.
4. *Section A* consists of 30 Multiple Choice Questions (30 x 1 =30 Points). Section B consists of 08 Questions.
5. To receive points you must show your work clearly.
6. **As shown, mark the best choice(s) with a clear *dark down diagonals.***

Section A

	A	B	C	D	E		A	B	C	D	E
1	A	B	C	D	E	**06**	A	B	C	D	E
2	A	B	C	D	E	**07**	A	B	C	D	E
3	A	B	C	D	E	**08**	A	B	C	D	E
4	A	B	C	D	E	**09**	A	B	C	D	E
5	A	B	C	D	E	**10**	A	B	C	D	E
11	A	B	C	D	E	**16**	A	B	C	D	E
12	A	B	C	D	E	**17**	A	B	C	D	E
13	A	B	C	D	E	**18**	A	B	C	D	E
14	A	B	C	D	E	**19**	A	B	C	D	E
15	A	B	C	D	E	**20**	A	B	C	D	E
21	A	B	C	D	E	**26**	A	B	C	D	E
22	A	B	C	D	E	**27**	A	B	C	D	E
23	A	B	C	D	E	**28**	A	B	C	D	E
24	A	B	C	D	E	**29**	A	B	C	D	E
25	A	B	C	D	E	**30**	A	B	C	D	E

Choose the one alternative that best completes the statement or answers the question.

1) Assuming that only X and Y logic inputs are available and their complements X' and Y' are not available, what is the minimum number two input NAND gates require to implement X $\oplus$ Y ?
(A) 2 (B) 3 (C) 4 (D) 5

2) Which of the following represents the correct counting sequence from $9FE_{16}$?
A) 9FF, 1AF0, 1AF1, 1AF2, 1AF3, 1AF4
B) AFF, 1AF0, 1AF1, 1AF2, 1AF3, 1AF4
C) 9FF, A00, A01, A02, A03, A04
D) 9FF, 1A00, 1A01, 1A02, 1A03, 1A04

3) Two signals (A and B) are ORed. Then they are ANDed with the product of signals C and D. Which of the following expressions describes this series of operations?
A) A + BCD B) (A + B)CD C) A + (B + CD) D) A + B(CD)

4) If you apply DeMorgan's theorem to the expression $\overline{\overline{(\overline{A}\,\overline{B})}\,\overline{(C+D)}}$, you get:
A) $\overline{AB}$ + C + D B) $(\overline{A}\,\overline{B})$ + C + D C) $(\overline{A} + \overline{B})$ + C + D D) $\overline{A} + \overline{B}$ + C + D

5) You need to build a circuit to perform parallel data transfers from one set of registers to another. The interconnections between the registers must be held to a minimum. The best choice for the register FFs is the _____ type.
A) "D" B) latch C) "J-K" D) "S-C"

6) The symbol for a flip flop has a small triangle - and no bubble - on its clock (CLK) input. The triangle indicates:
A) The FF is edge-triggered and can only change states when the clock goes from 1 to 0.
B) The FF is an active LOW device and can only change states when the CLOCK = 0.
C) The FF is edge-triggered and can only change states when the clock goes 0 to 1.
D) The FF is level active and can only change states when the CLOCK = 1.

7) The process of designing a synchronous counter that will count in a nonbinary sequence is primarily based on:
A) modifying asynchronous counters to change states on every second input clock pulse.
B) modifying BCD counters to change states on every second input clock pulse.
C) elimination of the counter stages and the addition of combinatorial logic circuits to produce the desired counts.
D) external logic circuits that decode the various states of the counter to apply the correct logic levels to the J-K inputs.

8) A primary advantage of using J-K flip-flops in asynchronous counter circuits is their ability to:
A) Toggle on the clock if the PRESET and CLEAR inputs are held HIGH.
B) Toggle on the clock if the J-K inputs are held HIGH.
C) Toggle on the clock if the PRESET and CLEAR inputs are held LOW.
D) Toggle on the clock if the J-K inputs are held LOW.

9) A production plant needs a counter that will count 4,000 items before resetting and recycling. How many flip-flop stages would this counter require?
A) 13 B) 12 C) 10 D) 11

 Roll No:

10) A parallel in/parallel out register normally has data inputs loaded _____ and data outputs transferred _____.

A) Asynchronously, asynchronously
B) Synchronously, asynchronously
C) Asynchronously, synchronously
D) Synchronously, synchronously

11) The primary difference between a 3-bit up-counter and a 3-bit down-counter is:

A) An up counter's output decreases by one with each input clock pulse whereas a down counter's output increases by one with each input clock pulse.
B) In a normal count sequence, a 000 is followed by 001 (in an up-counter) and by 111 (in a down-counter).
C) An up counter's output increases by one with each input clock pulse whereas a down counter's output decreases by one with each input clock pulse.
D) Both B and C
E) Both A and C

12) The best way to eliminate decoding glitches in asynchronous counters is to:

A) Use a strobe signal to disable the decoding AND gates until the flip-flops reach a stable state in response to a clock pulse.
B) Use a strobe signal to disable the counter flip-flops until a time greater than N(t_{pd}) has elapsed.
C) Use a strobe signal to enable the decoding AND gates until the flip-flops reach a stable state in response to a clock pulse.
D) Use a strobe signal to enable the counter flip-flops until a time greater than N (t_{pd}) had elapsed.

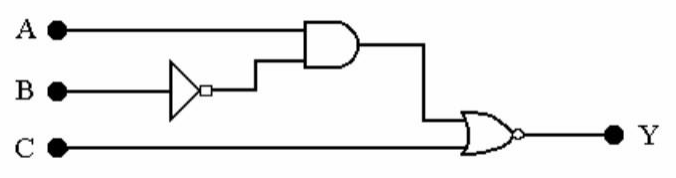

Figure 01

13) Refer to Figure 01. If A = 1, B = 1, and C = 0, the output (Y) will be:

A) HIGH.
B) invalid.
C) LOW.
D) floating.

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Table 1

L	M	N	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

14) The truth table in Table 1 indicates that:

A) The output (Z) is HIGH only when the binary input count is an odd number.

B) The output (Z) is HIGH only when the binary input count is an even number greater than zero.

C) The output (Z) is HIGH only when a single input is HIGH.

D) The output (Z) is HIGH only when the majority of the inputs are HIGH.

15) Which of the following methods would be used to disable the PRESET ($\overline{PRE}$) and CLEAR ($\overline{CLR}$) inputs to a clocked flip-flop in a circuit application where they are not used?

A) Connect the $\overline{PRE}$ and $\overline{CLR}$ inputs to a LOW logic level.

B) Connect the $\overline{PRE}$ input to a LOW logic level and the $\overline{CLR}$ input to a HIGH logic level.

C) Connect the $\overline{PRE}$ and $\overline{CLR}$ inputs to a HIGH logic level.

D) Connect the $\overline{PRE}$ input to a HIGH logic level and the $\overline{CLR}$ to a LOW logic level.

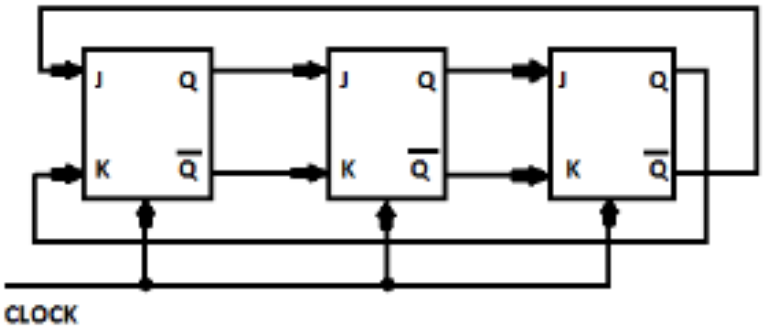
16) How many shift pulses would be required to serially shift the contents of one six-stage register to another?

A) 7 B) 5 C) 6 D) 8

17) For the initial state of 000, the function performed at the arrangement of the J-K flip-flop in the given figure is:

A) shift register B) mod-3 counter C) mod-6 counter D) mod-2 counter

Figure 02



18) The output of an 8-bit serial in - serial out shift register is connected back to its input. Assume the initial content of the shift register is 11000011. After 4 clock pulses, the content becomes:

A) 11000011 B) 00001100 C) 00111100 D) 00001111 E) 11110000

Roll No:

19) How many clock pulses are needed to shift a byte of data into and out of an eight-bit serial in - serial out shift register?

A) 4 B) 8 C) 12 D) 16 E) none of the above

20) How many clock pulses are needed to shift a byte of data into and out of an eight-bit serial in - parallel out shift register?

(A) 4 B) 8 C) 12 D) 16 E) none of the above.

21) When an 8-bit serial in/serial out shift register is used for a 24 ns time delay, the clock frequency must be:

A) 41.67 kHz B) 333 kHz C) 125 kHz D) 8 MHz

22) In the timing diagram shown in Figure 03, A and B are the flip-flop's inputs, Qs are the outputs, and C is the clock input. It could be a timing diagram of:

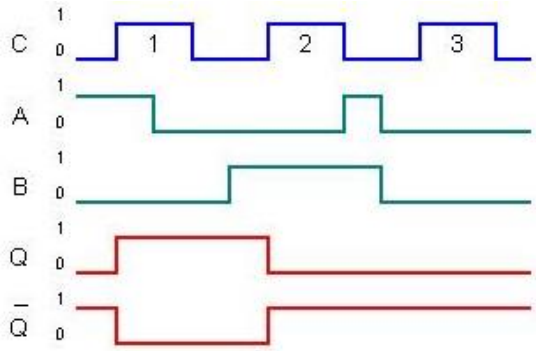


Figure 03

A) a positive edge-triggered S-R flip-flop B) a negative edge-triggered J-K flip-flop

C) a negative edge-triggered S-R flip-flop D) None of the above.

23) Assume the circuit above has initially been reset. X is high and Y is low. After one clock pulse, Q becomes:

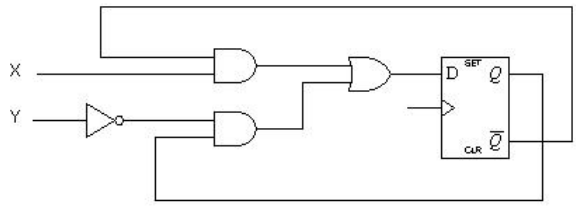


Figure 04

A) high B) low C) Can't be determined

24) A combinational logic circuit which generates a particular binary word or number is

A) Decoder (B) Multiplexer C) Encoder (D) Demultiplexer

25) Which one of the following set of gates are best suited for 'parity' checking and 'parity' generation.

A) AND, OR, NOT gates B) EX-NOR or EX-OR gates
C) NAND gates D) NOR gates

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26) In the circuit above, X is high. After one clock pulse, Y would become:

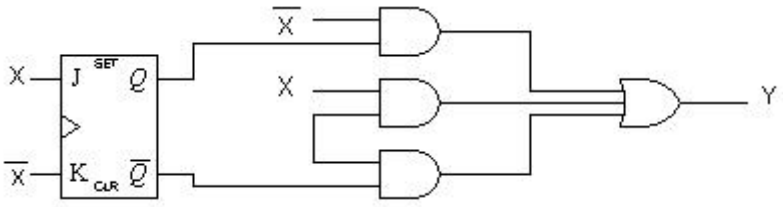

Figure 05

A) high B) low C) Can't be determined

27) To make the following circuit a tautology?

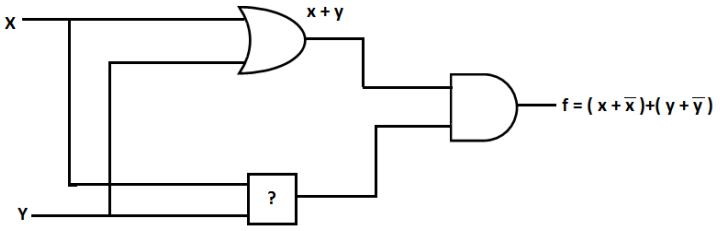

Figure 06

A) OR gate B) AND gate C) NAND gate D) EX-OR GATE

28) In the following gate network which gate is redundant gate network

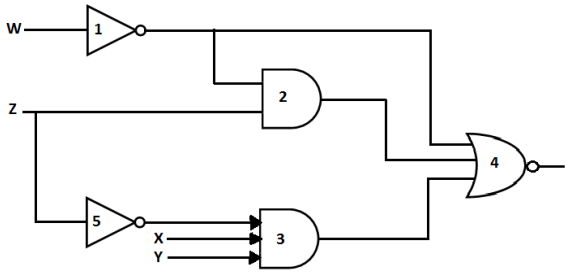

Figure 07

A) Gate no. 1 B) Gate no. 2 C) Gate no. 3 D) Gate no. 4

29) If a clock with time period 'T' (in sec) is used with n stage shift register, then output of final stage will be delayed by

A) nT sec B) (n-1)T sec C) n/T sec D) (2n+1)T sec

30) The MOD number of a counter:

A) Indicates the value of the highest state.
B) Indicates the value of the lowest state.
C) Indicates the number of possible counter output states.
D) Indicates sum of inputs.

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