FAST NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES
KARACHI CAMPUS

Final EXAMINIATIONS 2018
Digital Logic Design (EE 227)

Total Credits: 110 *10 May, 2018* Time Allowed: 180 Minutes

"I certify that I have neither received nor given unpermitted aid on this examination and that I have reported all such incidents observed by me in which unpermitted aid is given."

Student Roll No: _____ Section: **A / B / C / D / F /**

Signature: _____ *Invigilator's Signature*: _____

Instructions:

1. Please verify that your paper contains 14 pages including this cover.
2. Write down your Student-Id on the top of each page of this final.
3. This exam is closed book. No notes or other materials are permitted.
4. *Section A* consists of 25 Multiple Choice Questions (25 *x* 1 =25 Credits) and *Section B* consists of *8* questions (*25* Credits).
5. To receive credit you must show your work clearly.
6. As shown, mark the best choice(s) with a clear *dark down diagonals*.

Section A

	A	B	C	D	E		A	B	C	D	E
1	A	B	C	D	E	**06**	A	B	C	D	E
2	A	B	C	D	E	**07**	A	B	C	D	E
3	A	B	C	D	E	**08**	A	B	C	D	E
4	A	B	C	D	E	**09**	A	B	C	D	E
5	A	B	C	D	E	**10**	A	B	C	D	E
11	A	B	C	D	E	**16**	A	B	C	D	E
12	A	B	C	D	E	**17**	A	B	C	D	E
13	A	B	C	D	E	**18**	A	B	C	D	E
14	A	B	C	D	E	**19**	A	B	C	D	E
15	A	B	C	D	E	**20**	A	B	C	D	E
21	A	B	C	D	E	**24**	A	B	C	D	E
22	A	B	C	D	E	**25**	A	B	C	D	E
23	A	B	C	D	E						

FAST NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES
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Final EXAMINIATIONS Spring 2018
Digital Logic Design (EE 227)

Total Credits: 115 | *10 May, 2018* | Time Allowed: 180 Minutes

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Student Roll No: _____

Credits= 25 **Section A** Time allowed: 30 Minutes

Question No. 1 Choose the best choice(s) in the following Multiple Choice Questions (MCQs):

1. Select the canonical sum-of-products representation of the following function:

   f(x,y,z) = xy′ + y(x+z)

   (A) f(x,y,z) = xy′ + xy + yz
   (B) f(x,y,z) = x + yz
   (C) f(x,y,z) = xy′z + xy′z′ + xyz + x′yz + xyz′
   (D) f(x,y,z) = (x + y + z).(x + y + z′).(x + y′ + z)
   (E) f(x,y,z) = x′y′z′ + x′y′z + x′yz′

2. Select the derivation with minimum number of literals for the function represented in the following K-map:

X_1X_0 \ Y_1Y_0	00	01	11	10
00				
01	1			
11	1	1		1
10	1	1		

   (A) X1Y1′+ X0Y1′Y0′+ X1X0Y0′
   (B) X1Y1 + X0Y1Y0 + X1X0Y0
   (C) X1′Y1 + X0′Y1Y0 + X1′X0′Y0
   (D) X1Y1′ + X0Y1Y0 + X1X0Y0′
   (E) X1′X0Y1′Y0′ + X1X0Y1′Y0′ + X1X0Y1Y0′ + X1X0′Y1′Y0′ + X1X0′Y1′Y0 + X1X0Y1Y0′

3. For the positive-edge triggered D flip-flop shown below, the clock input is logic low (0) from t = 0ns to t = 10ns, makes a transition from logic low to logic high (1) at t = 10ns, and stays high until t = 20ns. However, for the input at D to be propagated to Q correctly at this clock transition, the flip-flop designer specifies that the input has to be available before t = 9ns and has to remain unchanged until t = 12ns. The setup and hold times for this D flip-flop are:

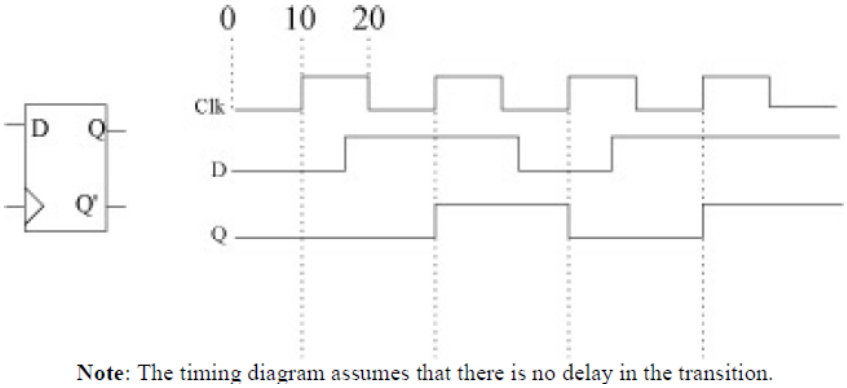


Figure 01

Note: The timing diagram assumes that there is no delay in the transition.

(A) Tsetup = 9ns, Thold = 12ns
(B) Tsetup = 1ns, Thold = 2ns
(C) Tsetup = 2ns, Thold = 1ns
(D) Tsetup = 9ns, Thold = 8ns
(E) Tsetup = 8ns, Thold = 9ns

4. The circuit below is the NAND-gates implementation of:

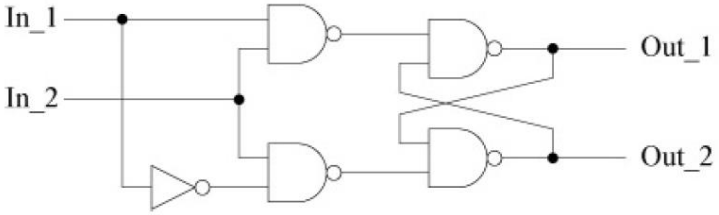


Figure 02

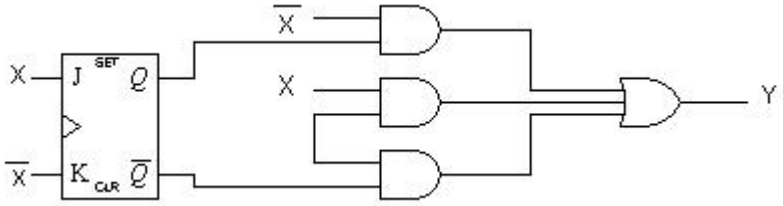
(A) S-R latch.
(B) D latch.
(C) D flip-flop.
(D) Gated S-R latch.
(E) Gated D latch

5. Which of the following has an invalid state:

(A) S-R flip-flop
(B) J-K flip-flop
(C) D flip-flop
(D) None of the above

6. In the circuit above, X is high. After one clock pulse, Y would become:

Figure 03



(A) high
(B) low
(C) Can't be determined

7. Assume the circuit above has initially been reset. X is high and Y is low. After one clock pulse, Q becomes:

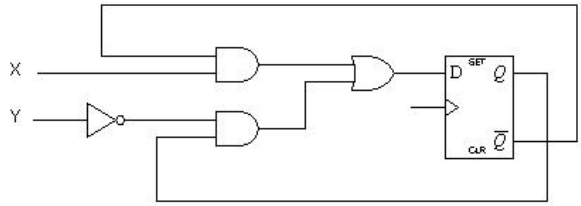


Figure 04

(A) high (B) low (C) Can't be determined

8. Assume the circuit above has initially been reset. X is low and Y is high. After 3 clock pulses, Q becomes:

(A) high (B) low (C) Can't be determined

9. Assume the circuit above has initially been reset. X and Y are both high. After 3 clock pulses, Q becomes:

(A) high (B) low (C) Can't be determined

10. The above circuit is a construction of:

(A) S-R flip-flop (B) J-K flip-flop (C) D flip-flop

(D) None of the above.

11. In the timing diagram shown in Figure 05, A and B are the flip-flop's inputs, Qs are the outputs, and C is the clock input. It could be a timing diagram of:

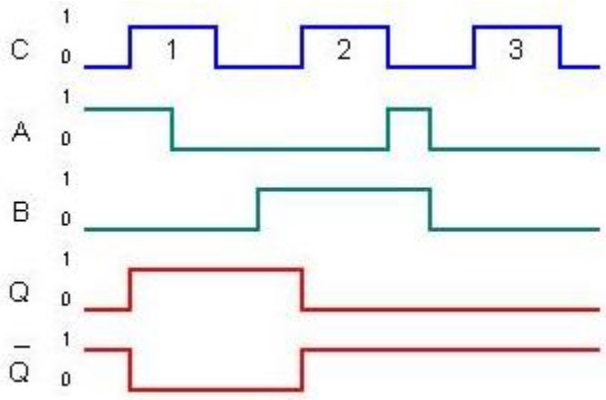


Figure 05

(A) a positive edge-triggered S-R flip-flop (B) a negative edge-triggered J-K flip-flop.

(C) a negative edge-triggered S-R flip-flop (D) None of the above.

12. How many states does a modulus-12 counter have?

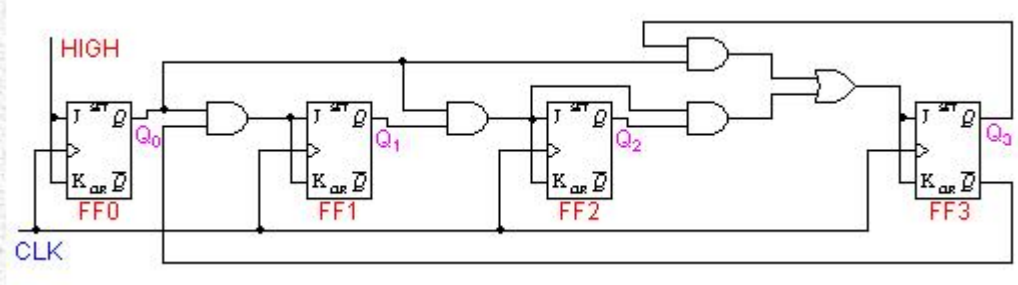
(A) 24 (B) 12 (C) 8 (D) 6 (E) 4

13. The current state of a decade counter is 1000. After 3 clock pulses, the state becomes:

(A) 1000 (B) 1001 (C) 1010 (D) 0001

14. The above is a construction of:

Figure 06



(A) a 4-bit synchronous up-down counter. (B) a 4-bit asynchronous up-down counter.

(C) a synchronous decade counter. (D) an asynchronous decade counter.

(E) none of the above.

15. The output of an 8-bit serial in - serial out shift register is connected back to its input. Assume the initial content of the shift register is 11000011. After 4 clock pulses, the content becomes:

(A) 11000011 (B) 00001100 (C) 00111100 (D) 00001111 (E) 11110000

16. How many clock pulses are needed to shift a byte of data into and out of an eight-bit serial in - serial out shift register?

(A) 4 (B) 8 (C) 12 (D) 16 (E) none of the above

17. How many clock pulses are needed to shift a byte of data into and out of an eight-bit serial in - parallel out shift register?

(A) 4 (B) 8 (C) 12 (D) 16 (E) none of the above.

18. When an 8-bit serial in/serial out shift register is used for a 24 ns time delay, the clock frequency must be:

(A) 41.67 kHz (B) 333 kHz (C) 125 kHz (D) 8 MHz

19. An asynchronous counter differs from a synchronous counter in

(A) the number of states in its sequence (B) the method of clocking

(C) the type of flip- flops used (D) the value of the modulus

20. Like the latch, the flip-flop belongs to a category of logic circuits known as

(A) monostable multivibrators (B) bistable multivibrators

(C) astable multivibrators (D) one-shots

21. Assuming that only X and Y logic inputs are available and their complements X′ and Y′ are not available, what is the minimum number two input NAND gates require to implement $X \oplus Y$?

(A) 2 (B) 3 (C) 4 (D) 5

22. Output of the following circuit is

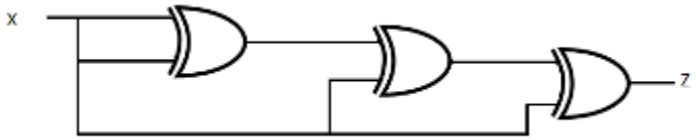


Figure 07

(A) 0 (B) 1 (C) x (D) x'

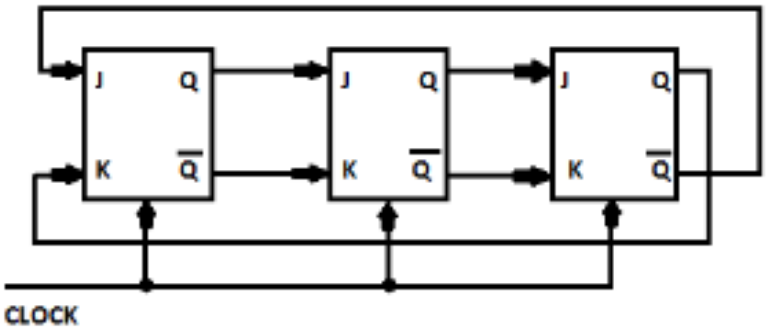
23. How many bits are required to encode all twenty-six letters, ten symbols, and ten numerals?

(A) 5 (B) 6 (C) 10 (D) 48

24. For the initial state of 000, the function performed at the arrangement of the J-K flip-flop in the given figure is:

(A) shift register (B) mod-3 counter (C) mod-6 counter (D) mod-2 counter

Figure 08



25. The inputs of the J-K flip-flop are PRESET ' = 0, CLEAR '= 1 , and J = K = 1. If a single clock pulse is applied, then device will

(A) Toggle (B) Set (C) Reset (D) No change

Total Credits= 90 **Section B** **Time Allowed= 150 Minutes**

Table 1 (a): Excitation Table for J-K Flip-Flop

OUTPUT TRANSITIONS Q_N		Q_{N+1}	FLIP-FLOP INPUTS J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Table 1 (b):Truth Table for S-R and J-K Flip-Flops

A	B	Q	Q_N
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1 / Invalid
1	1	1	0 / Invalid

Combinational Logic Circuits

NAND and NOR Implementation

Q. No. 2 Simplify and then implement the following Boolean function F using two-level forms of logic by using: [06 Credits]

(i) OR-NAND
(ii) AND-NOR.

$F(A, B, C, D) = \Pi(1,3,6,9,11,12,14) = \sum(0,2,4,5,7,8,10,13,15)$

Adders

(iii) The input waveforms in Figure 09 are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram. [02 Credits]

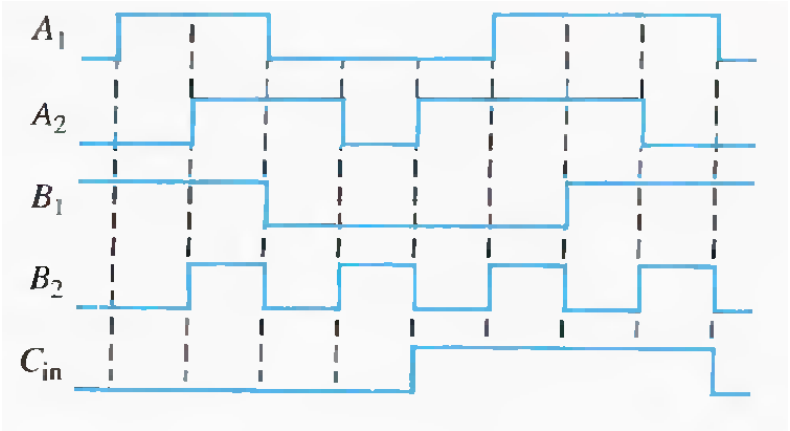


Figure 09

Comparators

(iv) Derive an expression for 2-bit magnitude comparator using Table 2. [03 Credits]

A2	A1	B2	B1	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0	1	0	0
1	1	1	1			

Multiplexer and Decoders

Q. No. 3 (i) Implement a full adder circuit by using: [06 Credits]

(a) 3 – to - 8 line Decoder

(b) 4 X 1 Multiplexers

(ii) Design a 8-to-1 multiplexer using 4-to-1 and 2-to-1 multiplexers. [02 Credits]

(iii) If the data-select inputs to the multiplexer in Figure 10 (a) are sequenced as shown by the waveforms in Figure 10(b). Determine the output waveform with the data inputs.[02 Credits]
Do = 0. D1 = 1. D2 = 1. D3 = 0.

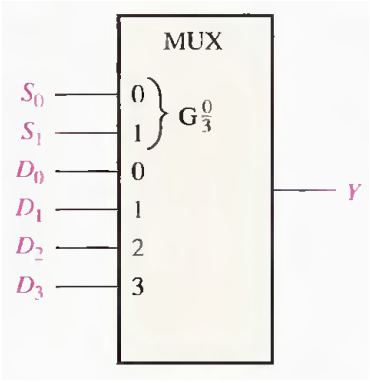
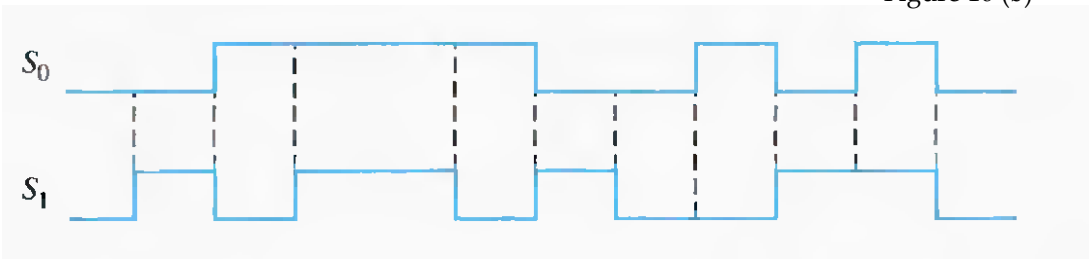


Figure 10 (a)

Figure 10 (b)



(iv) Implement the logic function in table by using a 74S151 8 input data selector/multiplexer. [03 Credits]

$X(A_3, A_2, A_1, A_0) = \sum(2,3,4,8,9,10,11,15)$

Latches

Q. No. 4 (i) If the waveforms in Figure 11 are applied to an active-LOW input S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q starts LOW. [02 Credits]

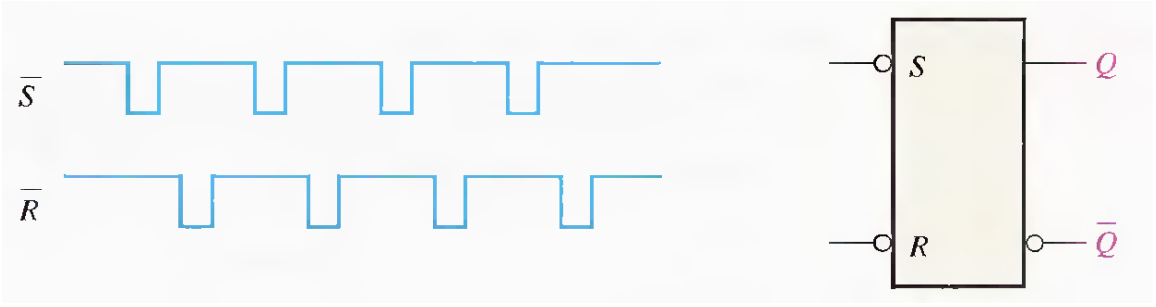


Figure 11

(ii) For a gated S-R latch. determine the Q and Q outputs for the inputs in Figure 12. Show them in proper relation to the enable input. Assume that Q starts LOW. [02 Credits]

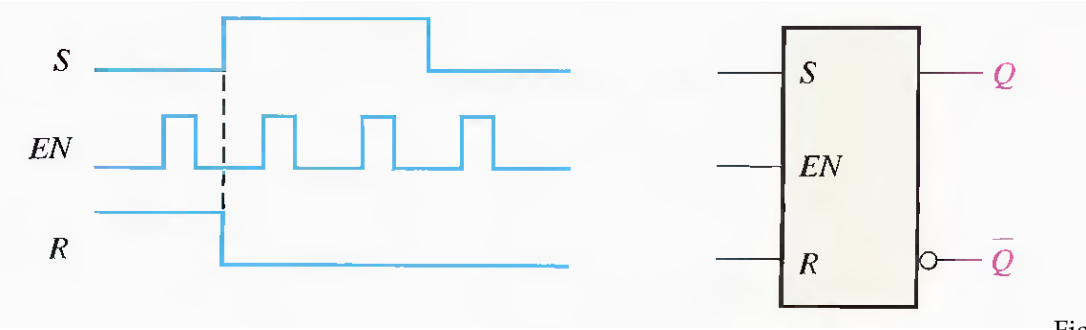


Figure 12

(iii) For a gated D latch. the waveforms shown in Figure 13 are observed on its inputs. Draw the timing diagram showing the output waveform you would expect to see at Q if the latch is initially RESET.

[02 Credits]

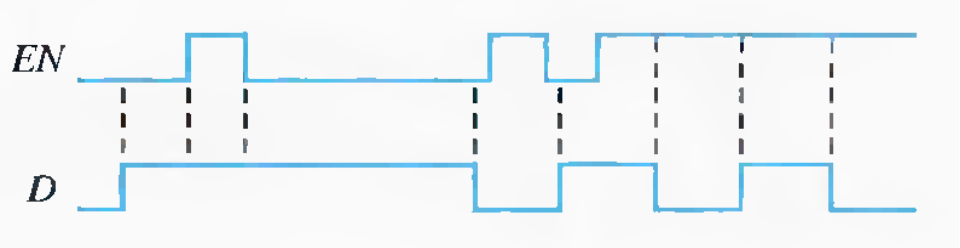


Figure 13

Flip Flops

Q. No. 5 (i) Two edge-triggered S-R flip-flops are shown in Figure 14. If the inputs are as shown. draw the Q output of each flip-flop relative to the clock. and explain the difference between the two. The flip-flops are initially RESET. [04 Credits]

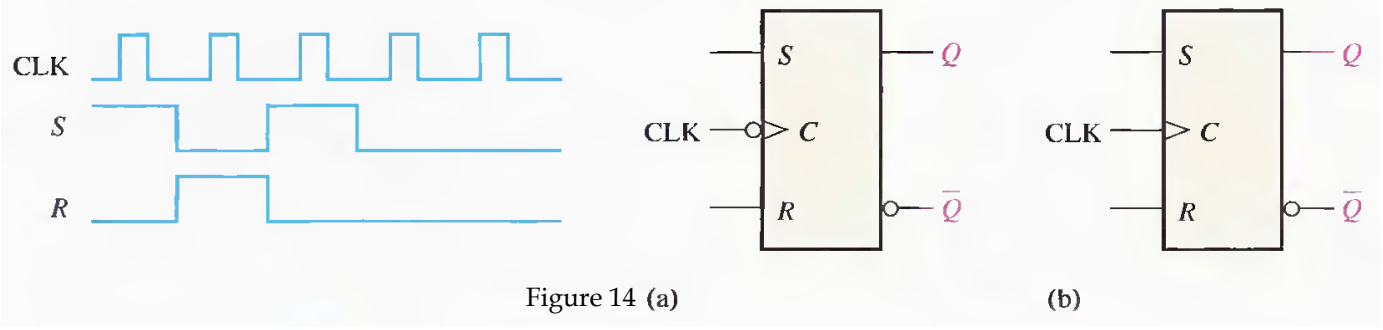


Figure 14 (a) (b)

(ii) The Q output of an edge-triggered S-R flip-flop is shown in relation to the clock signal in Figure 15. Determine the input waveforms on the Sand R inputs that are required to produce this output if the flip-flop is a positive edge-triggered type. [04 Credits]

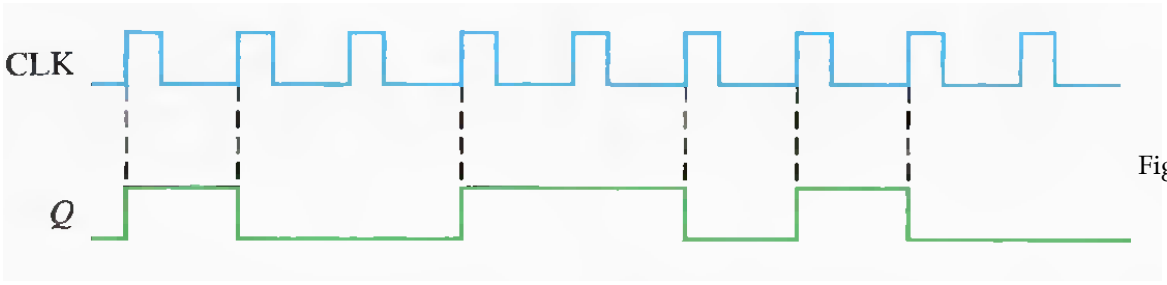


Figure 15

(iii) For a positive edge-triggered J-K flip-flop with inputs as shown in Figure 16, determine the Q output relative to the clock. Assume that Q stm1s LOW. [02 Credits]

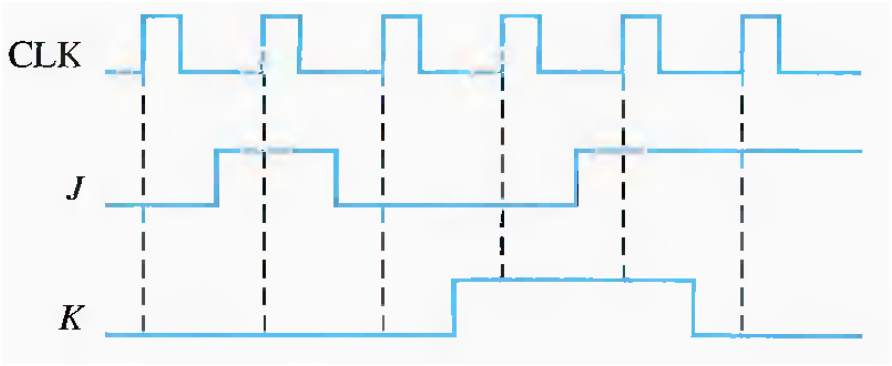


Figure 16

(iv) Determine the Q waveform relative to the clock if the signals shown in Figure 17 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW. [02 Credits]

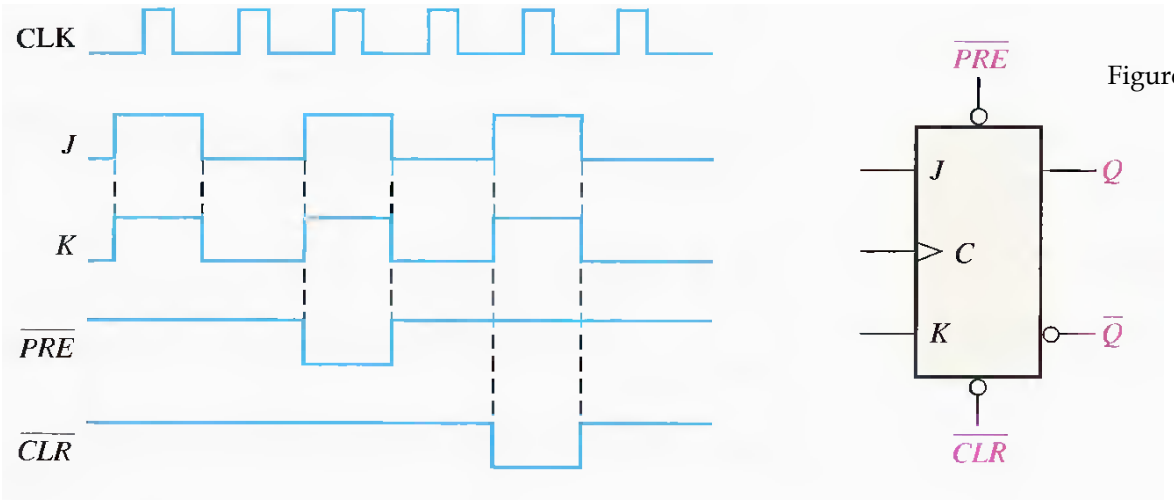


Figure 17

(v) A D flip-flop is connected as shown in Figure 18. Determine the Q output in relation to the clock. What specific function does this device perform? [02 Credits]

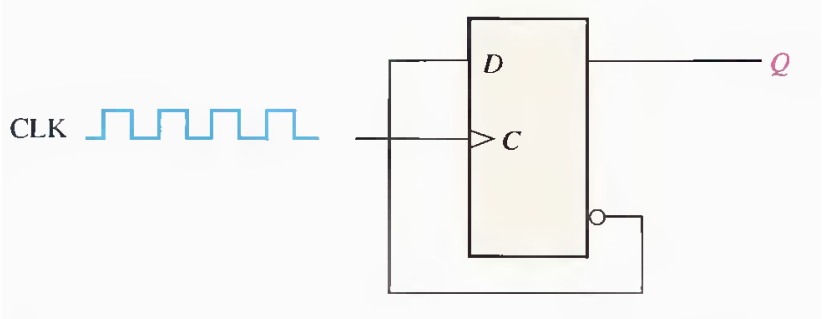


Figure 18

Operating Characteristics of Flip Flops

Q. No. 6 (i) Typically, a manufacturer's data sheet specifies four different propagation delay times associated with a flip-flop. Name and describe each one. [02 Credits]

(ii) The direct current required by a particular flip-flop that operates on a +5 V dc source is found to be 12 mA. A certain digital device uses 20 of these flip-flops. Determine the current capacity required for the + 5 V dc supply and the total power dissipation of the system. [01 Credits]

(iii) The data sheet of a certain flip-flop specifies that the minimum HIGH time for the clock pulse is 30 ns and the minimum LOW time is 37 ns. What is the maximum operating frequency? [01 Credits]

Counters Design

Q. No. 7 (i) Determine the sequence of the counter in Figure 19. [03 Credits]

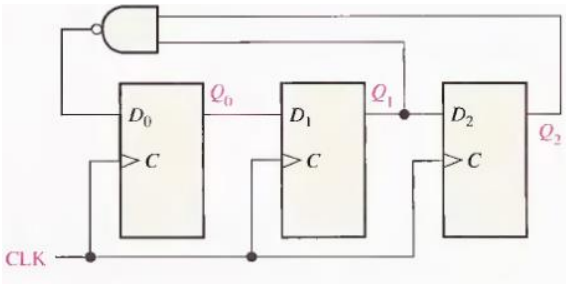


Figure 19

(ii) Implement the decoding of binary state 2 and binary state 7 of a 4-bit synchronous counter. Show the entire counter timing diagram and the output waveforms of the decoding gates. (Binary 3 = $Q_3'Q_2'Q_1Q_0$ and binary 9 = $Q_3Q_2'Q_1'Q_0$) [04 Credits]

(iii) Design a binary counter with the sequence shown in the state diagram of Figure 20 by using JK or D flip flop. [05 Credits]

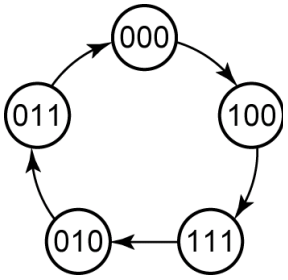


Figure 20

Registers

Q. No. 8 (i) Show the states of the 5-bit register in Figure 21 for the specified data input and clock waveforms. Assume that the register is initially cleared (all 0s). [05 Credits]

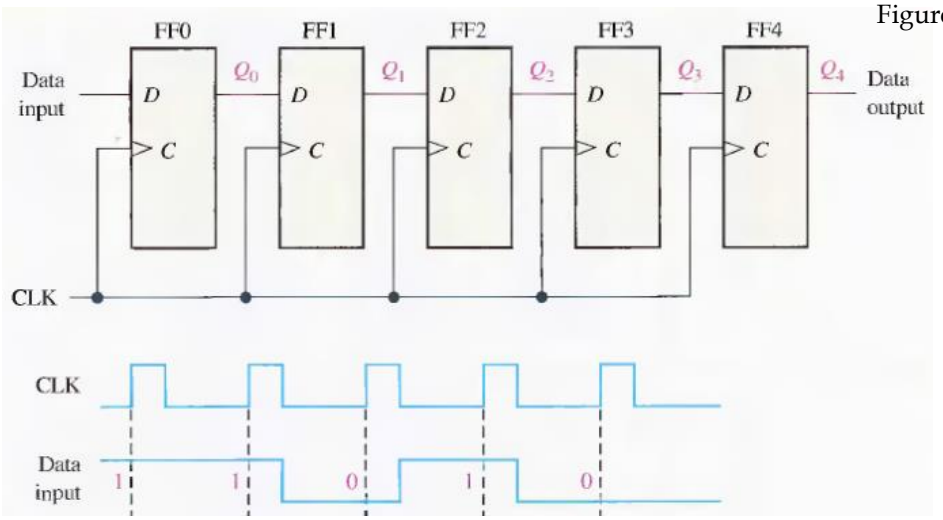
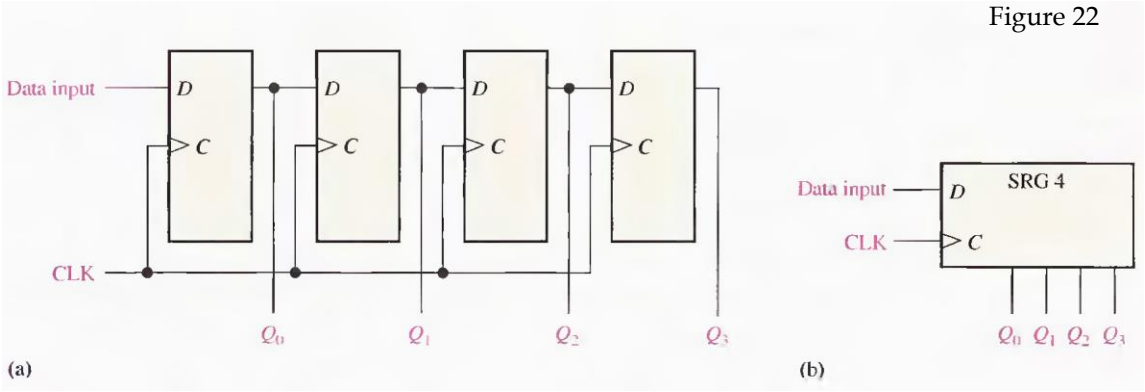


Figure 21

(ii) Show a complete timing diagram showing the parallel outputs for the shift register in Figure 22. Use the waveforms in Figure 23with the register initially clear. [04 Credits]

Figure 22



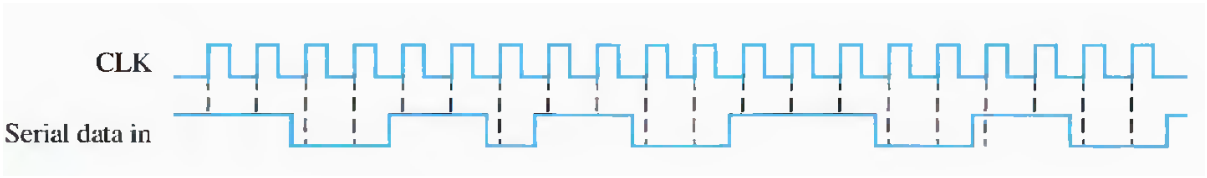


Figure 23

Design of Sequential Circuits and State Diagrams

Q. No. 9 (i) Assume that the following state diagram is provided: [10 Credits]

a) Starting from state 00 determine state transitions and output sequence that will be generated when an input sequence of 01011011011110 is applied.

b) Design a sequential circuit using D/JK flip fops.

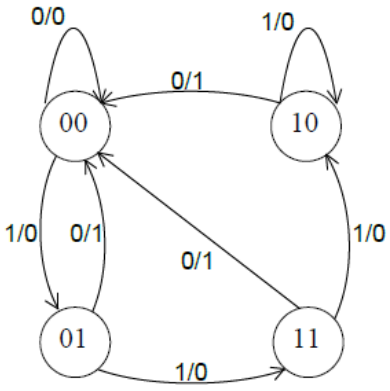


Figure 24

(ii) Design a counter that counts down, with the repeated sequence: 2, 1, 0, when the input to the counter circuit is 1. The counter does not count (stays at the same state) when the input is 0. The circuit is to be designed by treating the unused states as don't care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states. Use JK or D flip-flops in your design.

OR

Design a binary counter with the sequence shown in the state diagram of Figure 25 by using J-K or D flip flop. [10 Credits]

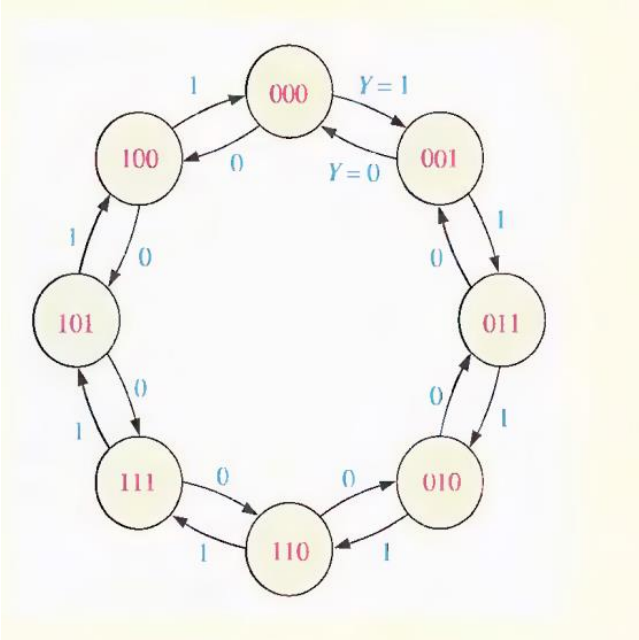


Figure 25