FAST NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES
KARACHI CAMPUS.
FINAL EXAMINIATIONS, SPRING 2018
Digital Logic Design (EE 227)

Total Points: 80 *10 May, 2018* Time Allowed: 135 Minutes

Name: _____ Roll No: _____

Signature: _____ Section: A / B / C / D /E/ F

Serial No: _____ *Invigilator's signature*: _____

Section B

Instructions:

- Attempt all Questions
- Pencil is only allowed to draw diagrams and waveforms

Question No.	Obtained Points	Points	Question No.	Obtained Points	Points
01		30	06		12
02		10	07		12
03		08	08		10
04		08	09		10
05		10			

Total Obtained Points	
Total Points	110
Signature	

Basic Combinational Logic

Q No. 02 (a) In how many different ways the *inversion* operation could be implemented? [02 Points]

(b) Simplify the output expression of Figure 08. Also draw the circuit diagram for the simplified expression. [03 Points]

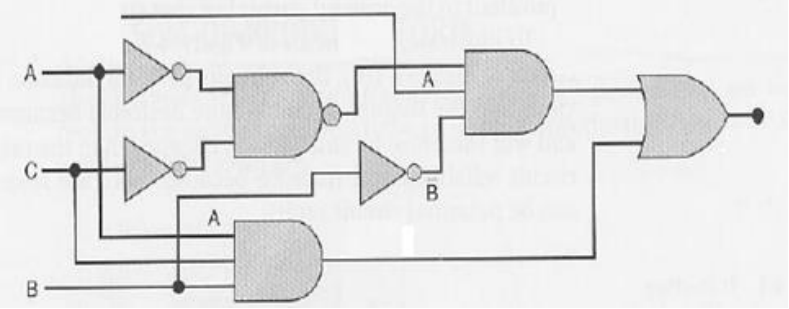


Figure 08

(c) Develop a truth table for the standard SOP expression ABC+ BCD'+ A'BC. Also, simplify the expression using *Karnaugh Map* and implement each expression with NAND logic using appropriate dual symbols: [05 Points]

Q. No.03 (a) Implement the following *Boolean function f*, using the two-level forms.
(a) *AND-OR-Inverter* logic diagram (b) *OR-AND-Inverter* logic diagram
$f(a,b,c,d)=\sum(m(1,4,5,9,12) + d(0,2,3,6,14))$ [05 Points]

(b) A four-bit binary number is represented as A_3, A_2, A_1, A_0, where A_3, A_2, A_1 and A_0 represent the individual bits and A_0 is equal to the LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than1000.

[03 Points]

Q. No. 04 (a) The following sequence of bits (right –most bit LSB) appear on the input of a *4-bit parallel adder*. Determine the resulting sequence of bits on each sum output. [02 Point]

Table 2

A1	1001
A2	1110
A3	0000
A4	1011
B1	1111
B2	1100
B3	1010
B4	0010

(b) Implement a full adder circuit by using:
(i) *3 – to - 8 line Decoder* (ii) *4 X 1 Multiplexers* [06 Points]

Q No. 05 (a) Use a *4-to-16 Decoder* and basic logic gates to implement the function F.

OR

Use an *8-to-1 Multiplexor* to implement the function F. Simply draw the *decoder* as a block, no need to show the internal logic. [05 Points]

$$F(A,B,C,D) = \pi M(0, 2, 3, 7) + \pi d(4, 8, 9, 10, 11, 13, 15)$$

(b) Design a *7-segment display* (2 Inputs: A1 and A0, 7 Outputs: a to g). You only need to display 0, 1, 2, 3, therefore, only a *2-to-4 decoder* is needed on the input side. You don't need to draw the details of the decoder, simply draw it as a block. Also, if the waveforms shown in Figure 09 are applied as indicated, determine the sequence of digits that appears on the display. [05 Points]

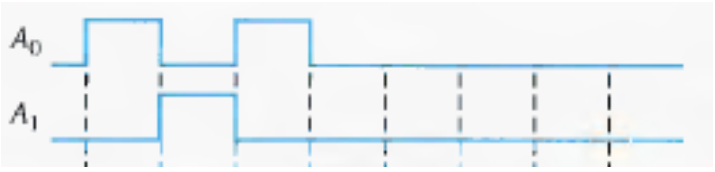
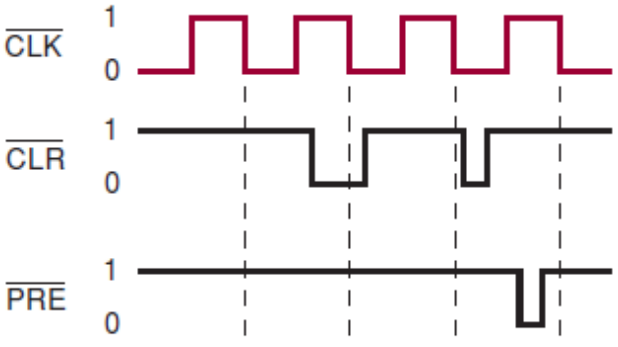


Figure 09

Roll No:

Q. No. 06 (a) Implement the decoding of binary state 5 and 9 of a *4-bit decade counter*. Draw its timing diagram and the output waveforms of the decoding gates. (Binary 3 = $Q_3'Q_2'Q_1Q_0$ and binary 9 = $Q_3Q_2'Q_1'Q_0$) [06 Points]

(b) Determine the *Q* waveform for the FF in Figure 10. Assume that Q=0 initially. [02 Points]



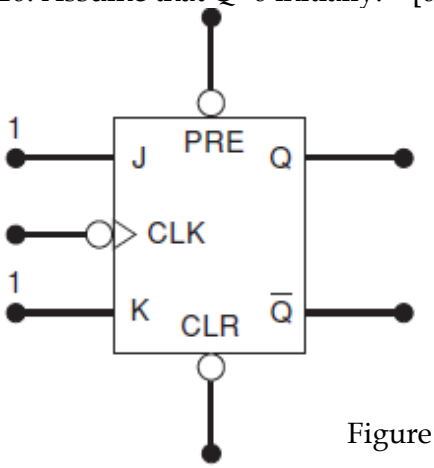
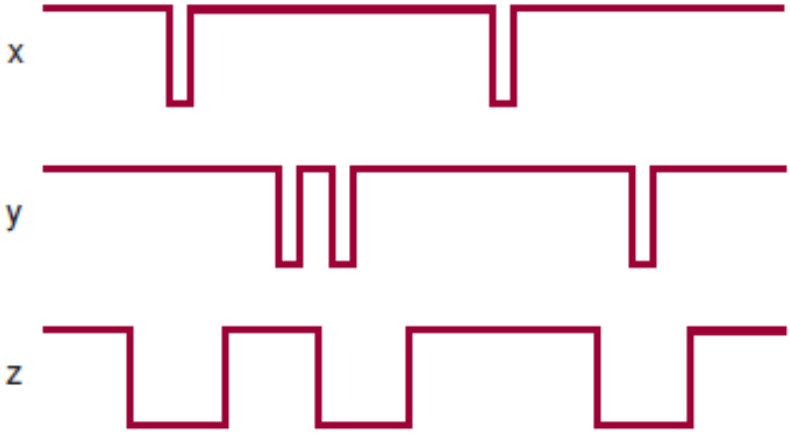
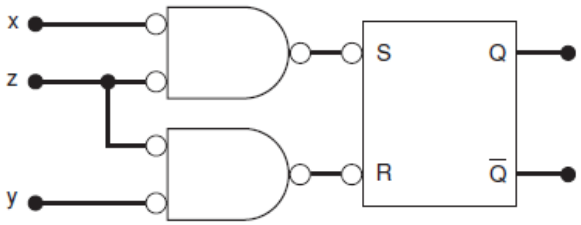


Figure 10

(c) The waveforms of Figure 11 a. are connected to the circuit of Figure 11 b. Assume that $Q = 0$ initially, determine the Q waveform. [04 Points]



a.



b.

Figure 11

 Roll No:

Sequential Logic – Counter

Q. No. 07 (a) Design a *synchronous counter* to produce the following binary sequence. Show all the design steps properly. [10 Points]

1, 4,3,5,7,6,2,1**...**

 Roll No:

(b) *Decoding glitches* sometimes appear when a synchronous device is sending data to *decoder* which may cause wrong decoded outputs. What should you do to overcome or remove this problem? Explain your answer by giving suitable example of a counter and decoder.
[02 Points]

Q. No. 08 (a) Determine the sequence of the counter shown in Figure 12. Initially Q_0=0, Q_1=0 and Q_2=0.
[04 Points]

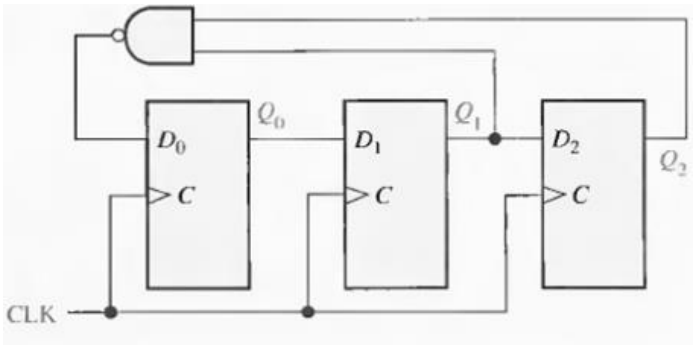


Figure 12

Roll No:

(b) Analyze the *synchronous counter* in Figure 13. Draw its timing diagram and determine the counter's modulus. [06 Points]

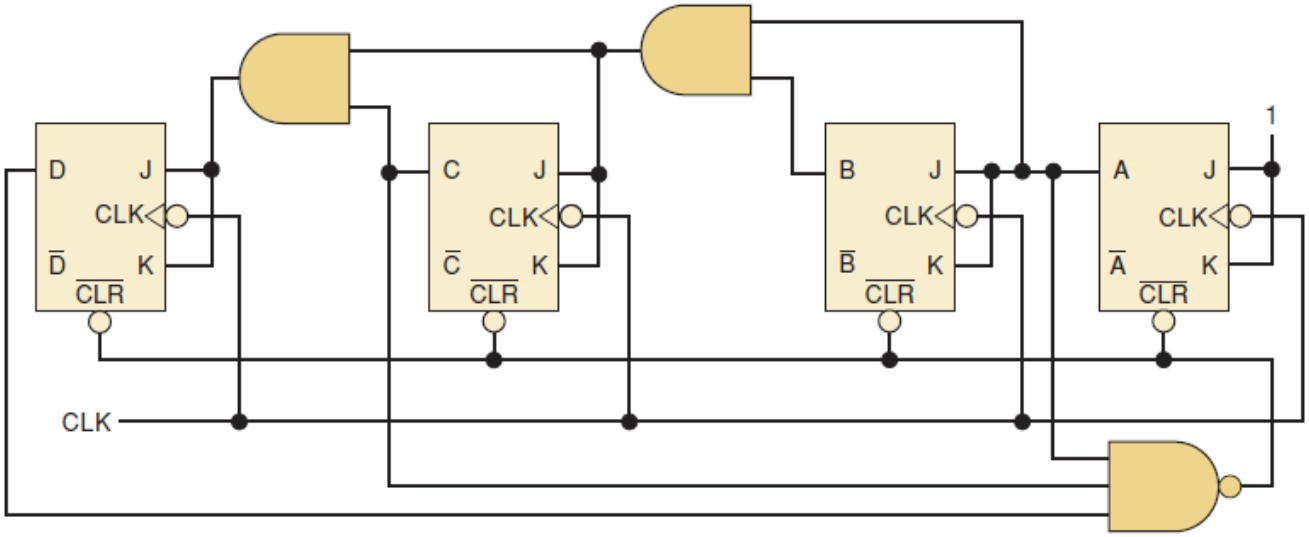


Figure 13

 Roll No:

Q No. 09 (a) Given below is the package of a *shift register*.

(i) What is the function of pin (9)?

(ii) What is the response of the package when pin (1) is low and when pin (1) is high?

(iii) A clock pulse is applied on pin (10), when the states of the package will change on rising edge or on falling edge of pulse?

(iv) If the following package is used to perform *parallel in/serial out* operation. Which pin is used to collect data out serially?

[04 Points]

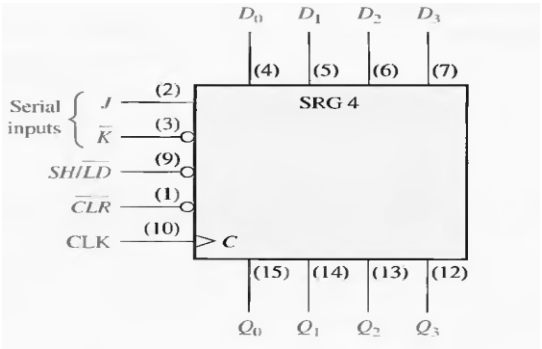


Figure 14

 Roll No:

b. Design a *4-bit serial in/parallel out shift register*. Also, for the data input and clock in Figure 15, determine the states of each flip-flop and show the Q waveforms. Assume that the register contains all 1s initially. [06 Points]

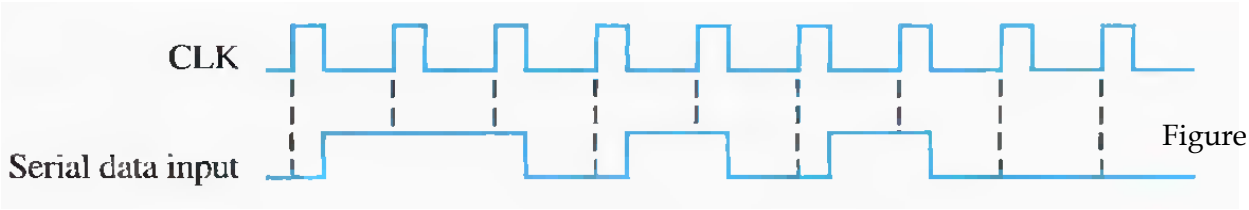


Figure 15

Roll No: