Computer Architecture (EE204)

Instructor: Dr. Hassan Jamil Syed
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Year and Semester: Fall 2019
Course code: EE 204
Course Title: Computer Architecture
Credits:3 hrs

Course Objectives:

- Get a working knowledge of architecture of subsystems and the general principles that affect their performance
- Get knowledge about advanced architectural features that boost the performance of computers with pipelining and superscalar architecture
- Analyze the performance of systems and quantify the performance measurements
- Study the major trends towards parallelism with respect to a single processor and multicore architecture

Course Status:

Core course for BS (CS)

Pre-requisites:

Digital Logic Design, Computer Organization & Assembly Language

Text book

Computer Architecture : A Quantitative Approach

John L. Hennessy & David A. Patterson 6th Edition

Reference Books

1. *Computer Organization & Design* : *The Hardware/ Software Interface*
   By Patterson & Hennessy
2. *Computer Organization and Architecture, Designing for Performance by* William Stallings, 9th Edition
3. *Computer Architecture and Organization By*

4. *Computer Architecture* By Morris Mano

Grading Scheme

Term exams (1 and 2)	30%
Quizzes	8%
Assignments	7%
Project	5%
Final	50%

Course Outline(Tentative):

Week	Lecture Topics	Chapter
1	Introduction to Computer Architecture Computer Classes	**Ch1**
2	Performance Metrics of a System Measuring and Reporting Performance	**Ch1**
3	Amdahl Law, CPU Performance Equation Chapter related fallacies and pitfalls	**Ch1**
4	Principles of ISA, internal storage, Memory addressing, Addressing Modes, Control Flow instructions, role of Compilers, instruction set encoding, register allocation	**Appendix A**
5	MIPS architecture, Instruction usage, Chapter related fallacies and pitfalls	**Appendix A**
6	**Midterm 1** Pipelining Overview, basic concepts, limitations, Major hazards of pipelining, Internal forwarding	**Appendix C**
7	Control hazards, branch prediction schemes, static and dynamic branch prediction, implementation of simple MIPS pipeline	**Appendix C**
8	Exception in pipeline, precise exceptions, Floating-point pipeline	**Appendix C**
9	MIPS R4000 pipeline, superscalar and VLIW architecture, Chapter related fallacies and pitfalls	**Appendix C**
10	Instruction level parallelism, data and name dependence, loop unrolling,	**Ch3**
11	Dynamic Scheduling - Scoreboarding technique and Tomasulo's approach	**Ch3 & App. C**
12	**Midterm II** Basics of Caches, Caches miss, hits & Organizations	**Appendix B**
13	Four memory hierarchy questions, Six basic cache optimizations, chapter related fallacies and pitfalls	**Appendix B**
14	Advanced cache optimizations, details of some advanced optimizations, Virtual memory, DRAM optimizations	**Ch2**
15	Simultaneous Multithreading (SMT), Multiprocessors Thread-level parallelism	**Ch 5**
16	Symmetric multiprocessors, UMA and NUMA architecture	**Ch 5**

Office Timings
Monday, Tuesday, Thursday 2:00 - 3:30 P.M

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