Algorithm Design of Mode S Downlink Signal Processing Based on 20MHZ Sampling Rate

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Abstract

Preamble detection, bit and confidence declaration are the most important part in signal processing of Mode S radar. If preamble detection or bit and confidence declaration algorithm do not perform well, it will affect error detection and correction. An effective algorithm to preamble detection, bit and confidence declaration based on 20MHZ sampling rate is proposed in this paper. Simulation results show that this algorithm is excellent in preamble detection, bit and confidence declaration.

Keywords: Mode S; preamble detection; bit and confidence declaration

1. Introduction

Continuing growth in air traffic is creating increasing demands upon the radar surveillance systems that are fundamental to the control of that traffic. It is recognized that, in certain areas, the limits of current systems are already being reached [1]. Mode S is the next generation SSR (Secondary Surveillance Radar) system. Mode S provides enhanced surveillance and complete air-ground data link capability, as well as A/C mode function of traditional SSR. Both features are required to support the planned automation of air traffic control [2, 3]. With GPS/DGPS as the source of the navigation data, ADS-Mode S can support many types of surveillance needs including: en route surveillance; terminal area surveillance; precision runway monitoring; surface surveillance; TCAS; and CDTI [4].

Currently the Mode S Extended Squitter is widely used. The signal waveform of Extended Squitter includes a preamble and a data block [5]. As shown in Fig.1, the whole signal encodes data using pulse position modulation (PPM) at a 1M/S data rate [4]. Reception of the signal begins with the detection of the four-pulse preamble. After one four-pulse preamble is detected, the bits in the data block will be decoded. The preamble is the unique character of Mode S signal, and how to detect the preamble is the key point for Mode S ground receiver. An algorithm that based on 10M sampling is proposed in [6]. In their algorihm, they detect leading edge only to ensure data existence, but we can not guarantee every bit in DF has a leading edge.

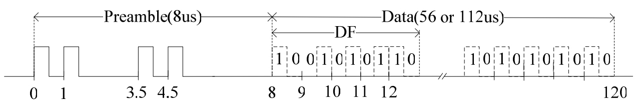

Fig.1 Mode S waveform

2. Preamble Detection

Preamble detection identifies the beginning of ADS-B signal reception. Two outputs of this process are the start time and the received power level of this signal.

2.1. Threshold

The preamble detection process includes a threshold power level used to discard very weak receptions. Typical value = -88dBm (referred to the antenna) for A3 receiver (Class A is interactive aircraft/vehicle participant systems. Class A3 systerm has more sensitive receiver than Class A0 and can interface with avionics source required for aircraft trajectory intent data).

2.2 Leading Edge

A leading edge is declared for a particular sample if the following conditions are met: 1) The sample is above the threshold and also is followed consecutive by 7 or more sample above the threshold; 2) It has substantial slope with sample before this one and less than substantial slope with sample next this one (The slope threshold is 2.4dB).

2.3. Falling Edge

A falling edge is declared for a particular sample if the following conditions are met: 1) The sample is above the threshold and there are 7 or more consecutive sample above the threshold before this sample; 2) It has substantial slope with sample next this one and less than substantial slope with sample before this one (The slope threshold is also 2.4dB).

2.4. Four-Pulse Preamble

Four pulses have been detected if one sample has characteristics as follows: 1) the sample is above the threshold, the 1~6th, 20~26th, 70~76th, 90~96th samples behind it are all above the threshold; 2) at least two leading edges has been detected at this sample or 20th sample or 70th or 90th sample behind it.

2.5 Reference Power Level

One reference Power level should be generated when a Four-Pulse Preamble is detected which will be used in re-triggering and during demodulation of data block: 1) Select the 1~6th, 21~26th, 71~76th, 91 ~ 96th samples behind the 4-Pulse Preamble; 2) For each sample, compute the number of other sample which amplitude is in +/-1db of it; 3) Find the

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maximum of these numbers, if the maximum number is unique, the sample which generate the maximum number is taken to be the reference power level. Or else the mean amplitude of these samples which generate these maximum numbers is taken to be the reference power level.

2.6 Consistent Power Test

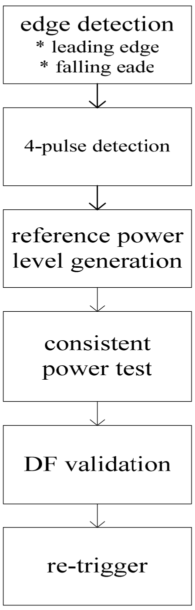
One test to validate the preamble is whether at least two or more pulses in the four preamble pulses agree in power level: 1) Select the 1~6th, 21~26th, 71~76th, 91 ~ 96th samples behind the 4-Pulse Preamble; 2) For each six samples, calculate the mean amplitudes; 3) If two or more of these mean amplitudes are with in +/-3db of the Reference Power Level, the preamble is past the test ,or else the preamble is rejected.

2.7 DF Validation

Another validation test is whether the first five bits (DF is the first five bits of data block) in the data block are available: 1) Select +/-1 samples of the 170th, 190th, 210th, 230th, 250th sample after the 4-Pulse preamble; 2) For each +/-1 samples, one leading edge or falling edge should be detected at these samples; select 7 samples after the leading edge or before the falling edge; the mean amplitude of the 7 samples should be in +/-3db of the Reference Power Level, otherwise the preamble is rejected.

2.8. Re-Triggering

If one 4-Pulse passes all tests above, a preamble is detected, but the preamble detection process continues to be applied searching for later preamble. If a particular preamble has passed all tests, its Reference Power Level and 5 mean amplitudes in DF Validation are compare with the earlier one preamble being processed. If the new signal is 3db stronger than the earlier one, the earlier preamble will be rejected, so that the new signal will be processed. Otherwise the new preamble will be rejected. Fig.2 summarizes the preamble detection process.



3. Bit and Confidence Declaration

After a preamble is detected, the bits in the data block will be decoded. In this step, all samples are used, rather than the middle sample in every chip [7].The first step is to categorize the samples in one bit block [6].

A：Samples which amplitude with in Reference Level +/-3db

B：Samples which amplitude below Reference Level 6db

The second step is to count the number of sample that are of each category. Every bit contains two chips (Chip1, Chip0) and each chip has 10 samples. Considering the wider high chip signal, we set weight in Chip 1 and Chip 0 as follows:

Weight of 10 samples in Chip 1 = {1，1，2，2，2，2，2，2，1，1}

Weight of 10 samples in Chip 0 = {1，1，2，2，2，2，2，2，1，1}

The four counts are summarized as follows:

1ChipTypeA = Sum of weight of samples of Type A in Chip

1ChipTypeB = Sum of weight of samples of Type B in Chip 1

0ChipTypeA = Sum of weight of samples of Type A in Chip 0

0ChipTypeB = Sum of weight of samples of Type B in Chip 0

Finally, two equations will produce two score using counts above.

1Score = 1ChipTypeA– 0ChipTypeA+ 0ChipTypeB – 1ChipTypeB

0Score = 0ChipTypeA– 1ChipTypeA+ 1ChipTypeB – 0ChipTypeB

The higher score determines the bit value is 1 or 0, and the difference of the two scores determines the confidence. If 1Socre is higher than 0Score 8 or more, the bit value is 1 with high confidence; if 1Score is higher than 0Score no less than 8, the bit value is 1 with low confidence; if 0Score is higher than 1Score no less than 8, the bit value is 0 with low confidence; if 0Score is higher than 1Score 8 or more, the bit value is 0 with high confidence.

4. Simulation Result Analyze

We simulated the algorithm using Matlab. The signal used was produced by Matlab Simulation.

1) Digital signal was modulated by Sina Wave signal to be analog signal which passed through AWAG Channel. Fig.3 shows this process.

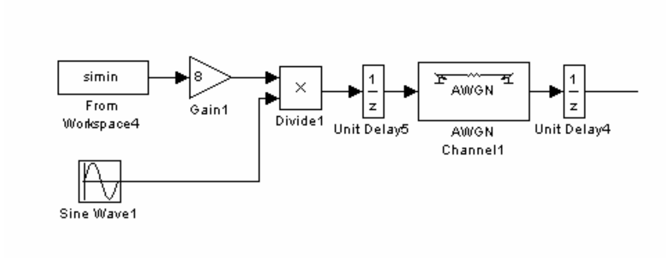


Fig.3 Analog Signal Producing Block

2) After the analog signal was received it was demodulated by the same Sine Wave signal and was filter by an low pass analog filter. This process is shown in Fig.4.

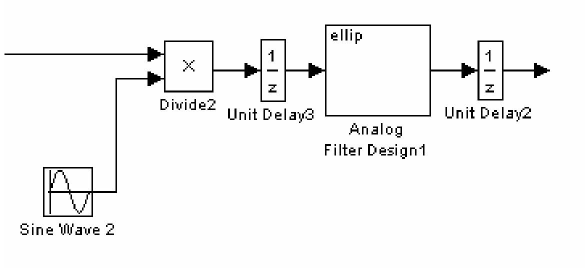


Fig.4 Demodulation and Filter Block

3) The signal was processed and amplified by block shown in Fig.5.

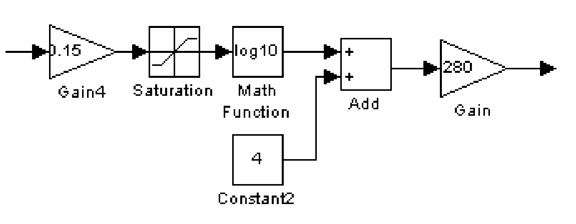


Fig.5 Signal Processing and Amplifying Block

After the signal passed through all block above, the signal was used for the algorithm simulation. Fig.6 shows the signal used for simulation.

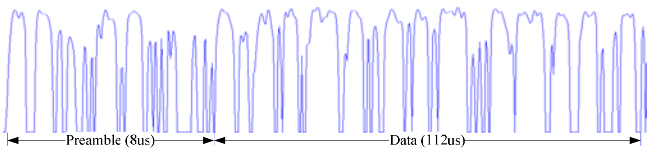


Fig.6 Signal Used for Simulation

Simulation results show that this algorithm is excellent in preamble detection, bit and confidence declaration. 50 frames signal is used for simulation, all preambles are detected when the SNR of AWAG Channel is higher than 0db. 47 preambles are detected when the SNR is -1db. All preambles detected can be decoded with low confidence bits no more than 5. All bits of detected signals which are decoded wrong can be corrected by brute force error correction technique [6,8].

5. Conclusions

An algorithm used for preamble detection, bit and confidence declaration based on 20MHZ sampling rate is proposed in this paper. The simulation result shows that this algorithm is rational and can detect the preamble pulse of Mode S signal rapidly and accurately. However, this algorithm has not considered the condition that one signal overlaps on another, and future study will focus on this point.

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