7.3 A 224Gb/s 3pJ/b 40dB Insertion Loss Transceiver in 3nm FinFET CMOS

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With datacenters introducing 800G/1.6T switches and emerging artificial intelligence accelerator ASICs demanding higher aggregate I/O bandwidth, 224Gb/s PAM-4 transceivers are expected to supersede today's dominant 112Gb/s SERDES. Such transceivers must double analog I/O bandwidth to 56GHz while maintaining or exceeding the previous generation's energy efficiency. This requires substantial improvements in the data and clock paths. With the baud rate doubled, channel losses exceeding 35dB must be addressed by higher order digital equalizers and optional maximum likelihood sequence detection (MLSD). The growing digital signal processing (DSP) complexity is compensated by the logic gate density offered by advanced FinFET nodes. This paper presents solutions for a 224Gb/s receiver frontend and transmitter backend and their associated clock paths.

The SERDES macro comprises a central clock multiplier unit (CMU) and 4 transceiver lanes. Multiple clock phases are generated locally by the receiver and transmitter clock conditioner units (RX CCU, TX CCU). The clocking system shown in Fig. 7.3.1 utilizes 1/8th-rate clocks throughout the entire path, which enables the use of an all-CMOS implementation. The two digital, bang-bang phase-locked loops (PLL) with individual 20% tuning range cover a full octave (7GHz to 14GHz) in combination with an optional 1.5 output prescaler. Low clock jitter is achieved in part by the fine resolution (0.5MHz/LSB), inversion-mode varactor-tuned, digitally controlled oscillator (DCO) that is paired with a digital loop filter operating at a quarter of the DCO frequency [1]. A 650MHz hold range ensures that the PLL remains locked over the -40°C to +125°C temperature range. With the PLL output frequency limited to 14GHz, the differential rail-to-rail clock is distributed passively and inductor-free to the TX and RX CCUs. Here, a multi-path, high frequency jitter rejecting, injection locked ring oscillator (ILO) generates the 8 clock phases required by the transmitter's 112GS/s DAC. Clock phases must be accurate within 100fs to lessen data converter distortion, which is 1 to 2 orders of magnitude below the ILO's inherent accuracy. A digital feedback loop eliminates phase errors by a combination of phase shifting buffers inserted at the ILO output and a set of 24b time-to-digital converters (TDC), capable of evaluating the time elapsed between either polarity edges of a clock pair. The phase shifting buffers, controlled by two 11b MASH-2 DACs setting the DC voltages at the buffer's AC-coupled NMOS and PMOS gates, move the position of the positive and negative clock edges independently with sub-25fs accuracy. Additional TDCs and a DAC are used to control the ILO supply voltage, eliminating errors caused by the injection locking process. With the receiver and transmitter clock paths sharing the same PLL, the RX CCU generates the recovered clock by a 10b phase rotator. The latter interpolates between the clock phases of a second ILO instance and a phase selector. To ensure the best possible linearity, phase errors are minimized by dedicated phase shifting buffers after detection by TDCs present at the phase interpolator input.

Shown in Fig. 7.3.2, the received signal is passed from the analog frontend (AFE) to a 7b 112GS/s ADC. The choice of an 8-way interleaved converter allows the RX CCU to directly clock the ADC track and hold (T&H) circuits. This greatly reduces clock skew and thus ADC distortion, at the expense of a higher signal bandwidth to the rank of 10 successive approximation registers (SAR), compared to a 16-way interleaved ADC. This is addressed by the choice of a low T&H output impedance and a small SAR input capacitance. With a total of 80 SAR units, the latter's conversion rate is reduced to 1.4GS/s which allows for a low 750mV supply and minimum power consumption. To ensure that the PAM-4 signal reaches the data converter with minimum degradation, the RX bump to converter signal chain must provide adequate bandwidth, translating into a per-stage 3dB bandwidth from 75GHz to 80GHz. To meet this stringent requirement and preserve sufficient return loss, the receiver bumps are terminated by two cascaded T-coils, thereby isolating the ESD capacitance from the AFE input capacitance. The active section of the AFE, consisting of two continuous time linear equalizer (CTLE) stages, a variable-gain amplifier (VGA) and 4 T&H buffers, are built from inverter-based g_m/g_{md} gain stages and reactive passives built from low resistivity top metal layers. Up to 20dB (10dB per stage) signal boost is realized by the CTLE shown in Fig. 7.3.2. Series peaking, formed by a transformer and the input capacitance of the following stage, creates a conjugate complex pole pair sized to emphasize the signal close to the Nyquist frequency. With the peaking gain determined by the resonator loaded quality factor, high frequency signal boost is set in 1dB steps by programmable resistor R_Q, implemented as a compact transmission gate. Signal emphasis in the low GHz range is provided by an additional zero/pole pair formed by g_{m1}/g_{md1} and AC-coupled g_{m2}/g_{md2} gain stages. Finally, the CTLE DC gain is set by programmable transmission gate resistor R_C. The VGA utilizes a programmable gain stage with shunt-series coupling to 4 T&H buffers. The latter are implemented with unity gain stages with moderate active peaking applied.

The transmitter aggressively minimizes power consumption by use of a direct 8:1 multiplexer and driver combination, eliminating the power hungry 8:4 multiplexer and 28GHz quarter rate-clock generator proposed in previous 224Gb/s transmitter architectures [4,5]. The 8:1 multiplexer is formed by 8-transistor, dynamic logic complex gate (NAND/NOR, INV, shown in Fig. 7.3.3) instances, generating 1 unit interval (UI) data pulses at nodes P[7:0]. The data pulses turn on and turn off are defined by the positive and negative CK8[7:0] clock edges respectively. Highly accurate 1UI pulse separation is enabled by the TX CCU calibrated clock phases. The 4-transistor, dynamic logic latch-based retiming of the data bus D8[7:0] provides 5UI setup and 2UI hold times at the pulse generator data input, reliably avoiding timing violations, which could result in a corrupted transmitter output signal. The output stage relies on an NMOS current source driver to avoid the complexity of a voltage mode driver with the added benefit of variable output swing set by programmable gate bias voltage VB. Directly controlled by the pulse generator, current source switching is performed at the NMOS source node. With each switch conducting only 1/8 of the total multiplexer DC current, the switch size can be reduced, which, unlike previous architectures [4,5], allows for rail-to-rail signaling at the full rate P[7:0] nodes. Two pulse generators share the same current source to limit the driver output capacitance to 110fF, which allows for an 80GHz output bandwidth helped by two T-coils optimized for -12dB return loss and 1ps group delay variation up to the Nyquist frequency. The transmitter contains two identical 7b single-ended DACs built from 10 slices with the 12× highest slice strength dictated by bandwidth considerations. The transmitter is completed by standard cell logic based 2:1 multiplexers in addition to shared decoder logic and 4:1 multiplexers. Timing violations between CMOS and dynamic logic are avoided by the introduction of a phase rotator (PR).

A 4-transceiver test chip has been fabricated and packaged in a flip-chip organic package substrate. The die micrograph in Fig. 7.3.7 shows the transceiver lanes measuring 0.5mm², which includes the embedded DSP. Phase noise is measured from a TX configured to generate a 14GHz, 1/8th-rate clock. The rms jitter, integrated from 1kHz to 100MHz, is 90fs as shown in Fig. 7.3.4. The same figure shows the eye diagram of a 55GHz half-rate clock. The rms jitter is lowered to 55fs when filtered by the oscilloscope's 4MHz-bandwidth CDR and deterministic jitter is limited to 170fs after TDC-based calibration. Figure 7.3.4 shows 224Gb/s and 106.25Gb/s QPRBS13 TX eye diagrams without de-emphasis applied, but with 5.5dB test fixture loss removed by the sampling oscilloscope, which is configured to have 4MHz CDR bandwidth. Transmitter parameters swing, ratio level mismatch (RLM), differential and integrated nonlinearity are measured as 960mV$_{ppd}$, 0.992, ±0.2LSB and ±0.5LSB respectively. The phase shifting buffers shift the 1/8th-rate clock up to 14ps with an average step size of 14fs, as shown in Fig. 7.3.5. Measurements rely on on-die TDCs to overcome the accuracy limitation of external test equipment. The same figure shows the AFE frequency response, confirming the expected 50GHz peaking frequency and maximum peaking gain of 20dB. The ADC effective number of bits (ENOB) was measured as 5.5b and 4.0b with a 1GHz and 50GHz sine wave applied at the RX input. The receiver achieves a pre-FEC bit-error-rate (BER) of 1e-6 with a 40dB bump-to-bump insertion loss channel, using AFE and embedded DSP engine equalization. The latter utilizes a 44-tap feed-forward equalizer (FFE) assisted by MLSD. The signal level histogram and the receiver eye diagram constructed from 80×4096 samples are shown in Fig. 7.3.5. Here, MLSD was replaced by a single-tap decision feedback equalizer (DFE). Energy efficiency is 1.0pJ/b and 2.0pJ/b for TX and RX respectively, with on-die linear voltage regulation overhead included, but excluding power consumed by the DSP engine. Figure 7.3.6 compares this work with previous state-of-the-art 112Gb/s SERDES [2,3] and 200Gb/s class stand-alone TX [4,5] and RX solutions [6]. This work presents a complete 224Gb/s transceiver, effectively doubling the bitrate of previous PAM-4 SERDES generations while simultaneously reducing the power efficiency from 3.5-4.0pJ/b [2,3] to 3.0pJ/b.

References:

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[2] M. LaCroix et al., "A 116Gb/s DSP-Based Wireline Transceiver in 7nm CMOS achieving 6pJ/b at 45dB Loss in PAM-4/Duo-PAM-4 and 52dB in PAM-2", *ISSCC*, pp.132-133, Feb. 2021.

[3] H. Park et al., "A 4.63pJ/b 112Gb/s DSP-Based PAM-4 Transceiver for a Large-scale Switch in 5nm FinFET", *ISSCC*, pp. 110-111, Feb. 2023.

[4] J. Kim et al., "A 224Gb/s DAC-Based PAM-4 Transmitter with 8-Tap FFE in 10nm CMOS", *ISSCC*, pp. 126-128, Feb. 2021.

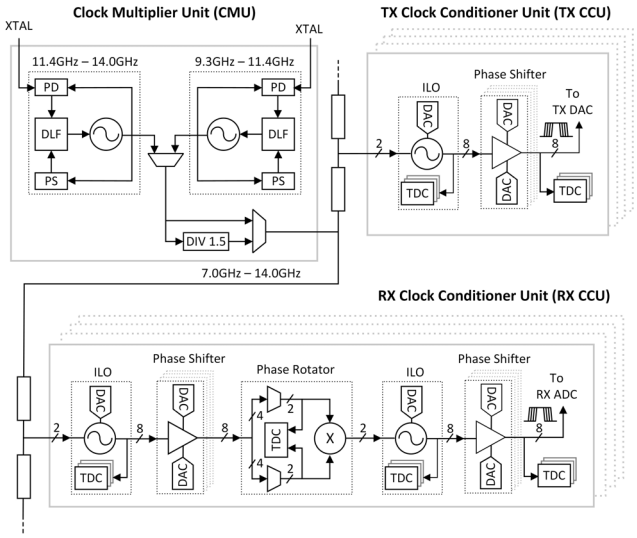

Figure 7.3.1: Clock path block diagram with central clock multiplier unit (CMU), transmitter clock conditioner unit (TX CCU) and receiver clock conditioner unit (RX CCU).

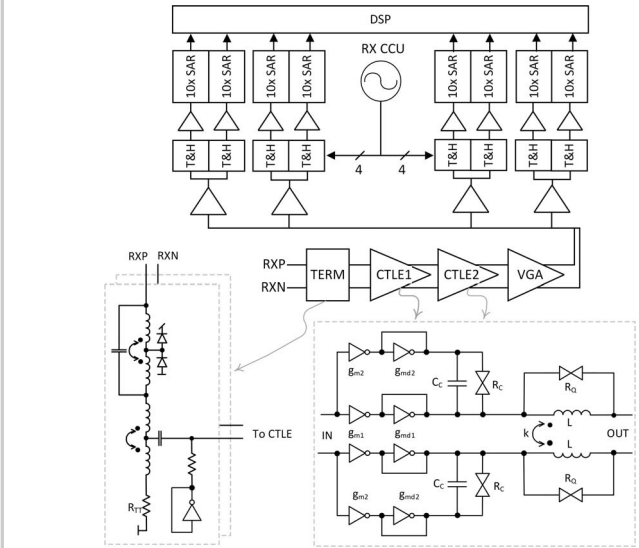

Figure 7.3.2: Receiver signal path block diagram with analog frontend (termination TERM, CTLE1, CTLE2, VGA, 4 T&H buffers) and 8-way time-interleaved ADC. The termination and CTLE implementation are shown bottom, left, and right, respectively.

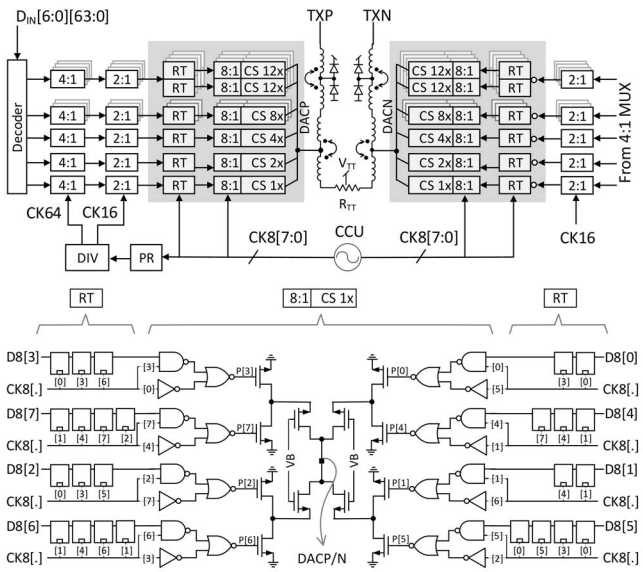

Figure 7.3.3: Transmit data path block diagram and implementation details of re-timer (RT) circuit, 8:1 MUX and current (CS) source driver.

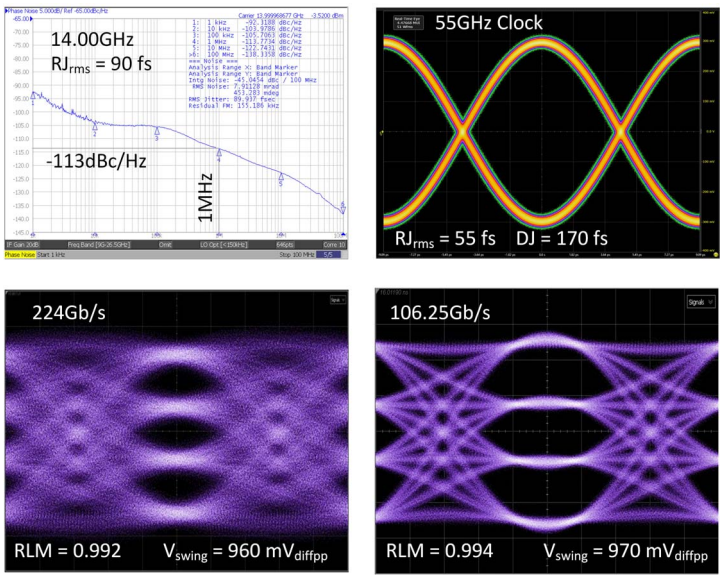

Figure 7.3.4: Measured clock phase noise and jitter, measured transmitter eye diagrams.

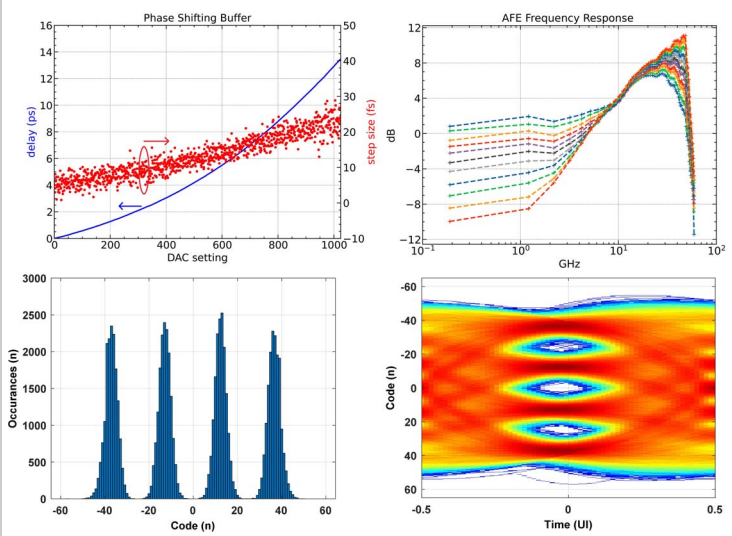

Figure 7.3.5: Measured delay realized by phase shifting buffer, measured AFE frequency response, measured receiver level histogram and receiver eye diagram.

	[2]	[3]	[4]	[5]	[6]	This Work
Process	7nm	5nm	10nm	28nm	5nm	3nm
Data Rate	112Gb/s	112Gb/s	224Gb/s	200Gb/s	224Gb/s	224Gb/s
BER @ Loss	1e-5 @45dB	7e-6@48dB	N/A	N/A	6e-7 @38dB	1e-6 @40dB
Efficiency: Analog Lane Analog TX Analog RX	 4.0pJ/bit --- ---	 3.5pJ/bit --- ---	 --- 1.88pJ/bit ---	 --- 4.63pJ/bit ---	 --- --- 1.41pJ/bit	 3.0pJ/bit 1.0pJ/bit 2.0pJ/bit
Supply	0.675V 0.8V 1.2V		0.85V 1.0V 1.5V	1.5V	0.9V 1.5V	0.75V 1.1V 1.5V
Lane Area: TX Area RX Area	0.531mm^2 --- ---	0.461mm^2 --- ---	--- 0.088mm^2 ---	--- 0.432mm^2 ---	--- --- 0.34mm^2	0.5mm^2 0.1mm^2 0.22mm^2
TX Architecture: DAC Driver FIR taps	 7-bit CML+SST ---	 7-bit SST 6	 7-bit CML 8	 7-bit CML 5	N/A	 7-bit CML 5
RX Architecture: ADC AFE FFE taps DFE taps	 7-bit CTLE/VGA 25 2	 7-bit VGA/CTLE 32 1	N/A	N/A	 6-bit CTLE/VGA(2) 30 ---	 7-bit CTLE(2)/VGA 44 1

Figure 7.3.6: Comparison table.

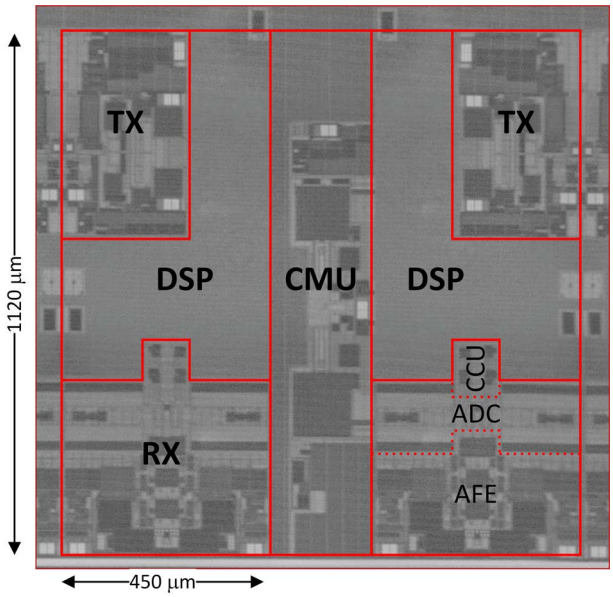

Figure 7.3.7: Die micrograph.

Additional References:

[5] M. Choi et al., "An output-bandwidth-optimized 200 Gb/s PAM-4 100 Gb/s NRZ transmitter with 5-tap FFE in 28 nm CMOS", *ISSCC*, pp. 128-129, Feb 2021.
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