A Novel Design Optimization Framework for Regulated Cascode Transimpedance Amplifiers

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***Abstract*—This work exploits the well-known g_m over I_D methodology to develop a novel approach to optimize the design of regulated cascode amplifiers (RGC). The proposed design framework starts extracting a set of lookup tables describing the circuit's figures of merit as a function of the g_m over I_D ratio. Due to the feedback topology of the circuit, the performances, in terms of bandwidth, gain, and DC power consumption, exhibit a behavior that is counter-intuitive with respect to the typical tradeoffs suggested by the g_m/I_D theory. The proposed method is validated designing a RGC with the 0.13 µm IHP SiGe process. The performance of the proposed solution are obtained through post-layout simulations**.

Keywords—g_m over I_D; regulated cascode amplifier; non-dominant poles optimization; TIA;

I. INTRODUCTION

The design of the front-end transimpedance (TIA) amplifier present in any optical receiver is extremely critical. Its performances directly affect the characteristics of the entire system. Its main role is to make it possible to interface the large photodetector present at the front-end of the fiber optic receiver. Over the years several circuit solutions have been proposed for the design of high bandwidth CMOS TIAs [1]-[5]. Among these, the regulated cascode (RGC) (Fig. 1) improves the effective TIA's bandwidth exploiting negative feedback to reduce the input resistance appearing in parallel to the large photodetector's capacitance present at input of the system.

This work relies on the g_m over I_D design technique to introduce a novel design methodology that allows to achieve the best tradeoff between the RGC performance metrics [6]. Using this methodology, the transistor parameters (e.g. transit frequency, f_T, intrinsic gain, g_m/g_{DS}, and current density, I_D/W) are expressed as lookup tables that are function of the inversion level of the transistor (i.e. g_m/I_D) and are then thoroughly explored to extract the best biasing point. The transistor exhibits higher speed in strong inversion. This is due to the smaller value of the associated gate capacitance. However, in this operating region the transistor dissipates more power because it needs higher bias voltages. On the opposite side, in weak inversion the intrinsic gain becomes higher, but the speed (i.e., f_T) gets lower. This is because in weak inversion for the transistor to generate the same amount of current I_D the width of the transistor, and so its total intrinsic capacitances, need to be increased.

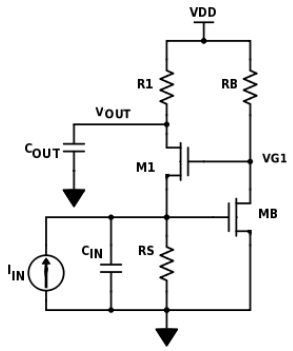

Fig. 1. RGC input stage

The proposed framework uses a set of technology lookup tables to extract the design parameters of the MOSFET at different levels of inversion. The lookup tables generated are specific to the technology process used for designing the circuit. In our case, the RGC has been designed utilizing an IHP SiGe process with minimum channel length of 130 nm and 1.5V supply voltage. Once the technology-based tables are extracted, they are used for generating a new set of lookup tables providing the circuit performance index of interest (e.g., gain, bandwidth, and DC power consumption) as a function of the g_m over I_D ratio. Contrary to common intuition, due to the strong role that the feedback plays in determining the behavior of the RCG topology, the circuit exhibits its best performance in terms of DC power consumption in strong inversion and its best performance in terms of bandwidth in weak inversion. Indeed, the optimal performances are not in line with the expectations that the g_m/I_D theory applied to the single transistor would suggest.

The work is organized as follows: section II describes the optimization framework implemented for designing the RGC; section III shows the simulation results of the circuit with emphasis on the counter-intuitive behavior of the amplifier performances. Section IV provides conclusions.

II. DESIGN FRAMEWORK

The schematic of the designed RGC amplifier is provided in Fig. 1. Here the photodetector has been substituted with a simple model composed by an ideal current source generator

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(I_{IN}) and an input capacitance C_{IN}. The RGC schematic is composed by a common gate (CG) input circuit (M_1, R_1 and R_S) with a feedback loop, consisting of a common source (CS) amplifier (R_B and M_B). The aim of the feedback is to reduce the input impedance by a factor approximately equal to the gain of the CS stage:

$$A_{VB} \approx g_{mB} R_B \tag{1}$$

Fig. 2 shows the small signal model of the amplifier. The small signal circuit has been symbolically analyzed, and the closed loop transfer function extracted has been used as the underlying equation to implement the design framework. The RGC transfer function is composed by two zeros, one simple pole and one complex conjugate pole pair. Usually the zeros are at a significantly higher frequency than the poles, so they can be neglected [7] and the general form of the RGC transfer function can be approximated as follows:

$$A(s) \cong \frac{A_0}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_0 Q}+\frac{s^2}{{\omega_0}^2}\right)} \tag{2}$$

The poles can be expressed as:

$$\begin{aligned} p_1 &= -\omega_{p1} \\ p_{2,3} &= -\frac{\omega_0}{2Q}\left(1 \mp \sqrt{1-4Q^2}\right) \end{aligned} \tag{3}$$

Assuming the poles are spaced according to the relationship $0.5\omega_0/Q >> \omega_{p1}$, the circuit behaves like a first order system with a dominant pole. In this case, the RGC bandwidth can be determined essentially by the input and output time constants expressed below [7]:

$$\tau_x = C_X R_X \; and \; \tau_Y = C_Y R_Y \tag{4}$$

where C_X is the sum of the photodetector's capacitance and the intrinsic capacitances of M_1 and M_B:

$$C_X = C_{IN} + C_{GSB} + C_{SB1} \tag{5}$$

while C_Y is the sum of the load capacitance (C_{OUT}) and the drain-bulk capacitance of M_1:

$$C_Y = C_{OUT} + C_{DB1} \tag{6}$$

Neglecting the transistors body effect and channel length modulation, the resistances R_X and R_Y can be obtained as follows:

$$R_X \cong R_S || \frac{1}{g_{m1}(1+g_{mB}R_B)} \; and \; R_Y = R_1 \tag{7}$$

and if we can also assume that $g_{m1}R_S(1+g_{mB}R_B) >> 1$ the DC gain of the TIA can be approximated as follows:

$$A_0 \cong R_1 \frac{g_{m1}R_S(1+g_{mB}R_B)}{g_{m1}R_S(1+g_{mB}R_B)+1} \cong R_1 \tag{8}$$

The max value of R1 is constrained by the bias condition ($V_{DS1} > V_{GS1} - V_{TH}$) required to maintain M_1 in saturation. The time constants, τ_X and τ_Y, usually dominate the response of the system and the other time constants, associated with the parasitic capacitances C_Z, C_{ZY} and C_{ZX} can be neglected.

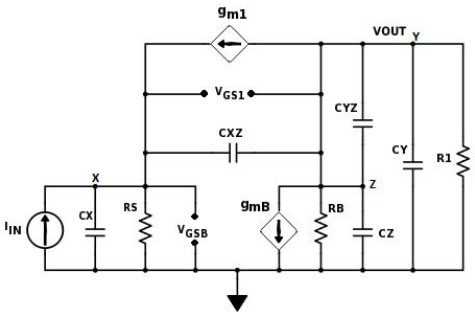

Fig. 2. RGC Small Signal Model

Unfortunately, these assumptions are accurate only when the simple pole occurs at a much lower frequency than the complex conjugates poles [7]. In practice, the RGC bandwidth can be further increased by positioning the complex conjugate poles at a lower frequency than the simple pole. However, in this case, the designer must take care of flattening the potential peaking in the frequency response of the circuit [8].

The aim of this work is to develop a novel design methodology that starting from (4), (7), and (8) finds the optimal circuit solution that maximizes gain and bandwidth, and minimizes power consumption. The optimization process is based on varying the g_m/I_D ratio for both transistor M_1 and M_B. Using the proposed methodology is possible to achieve an optimization strategy able to meet the circuit's specifications without the use complex ad-hoc solutions.

From (8), we see that the target gain of the TIA sets the value of the resistance R_1. Once R_1 is fixed, imposing the condition $R_S = R_1$ and setting the desired bias current I_{D1}, it is possible to compute the source voltage of M_1 (V_{S1}) and the gate-source voltage of M_B (V_{GSB}). To prevent M_B from turning off, the V_{GSB} must be greater than the threshold voltage of M_B. From the DC analysis of the system we see that the gate-source voltage of M_1 is defined by the difference between the drain voltage of M_B (V_{G1}) and the gate voltage of M_B (V_{S1}). Since $V_{G1} = V_{DD} - I_{DB} \times R_B$ the value of V_{G1} can be computed by setting the value of R_B and constraining the value of I_{DB} based on the power budget allowed by the specifications. For guaranteeing the correct bias point operation of the circuit, I_{DB} was set to one half of I_{D1}. The value of R_B was then varied according to the g_m/I_D ratio and the target gain of the feedback loop stage (A_{VB}). For convenience, we re-write the expression of A_{VB} given in (1) as follows:

$$\frac{g_{mB}}{I_{DB}} \cong \frac{A_{VB}}{R_B I_{DB}} \tag{9}$$

Solving (9) for R_B and considering that the minimum g_m/I_D in strong inversion is equal to 5 S/A, and the maximum value of g_m/I_D in weak inversion is equal to 25 S/A, the range of

$$\frac{A_{VB}}{25 I_{DB}} \leq R_B \leq \frac{A_{VB}}{5 I_{DB}} \tag{10}$$

allowed values for R_B at different inversion levels is given by:

Sweeping the value of the g_m/I_D ratio for M_B changes the required value of R_B accordingly. R_B exhibits its maximum value in strong inversion while it presents its minimum value in weak inversion. Consequently, the voltage V_{G1} increases its

value as we move from strong to weak inversion. The case for which the MOSFET exhibits the highest bias voltage leads to the maximum DC power consumptions for the circuit, that is power consumption increases as the g_m/I_D ratio increases. This behavior is due to the feedback topology of the circuit and it is in apparent contrast with the common g_m/I_D theory's insight that for obtaining the minimum DC power consumptions the transistor must be biased in weak inversion. As illustrated by the blue plot in Fig. 3, if we consider a fixed value of g_m, when we are moving from weak to strong inversion, since the current I_D increases, the value of the g_m/I_D ratio decreases.

Once the design specifications have been set, the proposed framework varies automatically the g_m/I_D ratio for both M_1 and M_B according to (10), and finds a viable interval of DC operating points based on the design constraint that both transistors must be on and operate in saturation. For each acceptable solution, the framework computes the performance of the circuit in term of gain, bandwidth and DC power consumption and it records both performances and associated parameters (W_1, R_B, W_B). At this point, the framework explores the solutions' space and extracts the operating DC points that maximize the performance of the RGC.

III. Simulations and Results

The framework was entirely designed in Matlab and the solutions' space was computed through SPECTRE simulations. In our design the target specification for the gain was 60 dBΩ, so we set R_1=1kΩ=R_S. Next, since selecting the minimum channel length for both transistors allow to obtain the maximum transit frequency f_T [9]-[12], we decided to set L_1=L_B=130nm. In addition, given that for our technology the threshold voltage V_{TH} is approximately 0.4V, and we derived in the previous section that V_{GSB} must be greater the V_{TH}, to achieve V_{R1} = V_S = V_{GSB} = 500 mV we chose a drain current I_{D1} of 500 µA. The output voltage is equal to 1 V, and the drain to source voltage of M_1 is 0.5 V. In the proposed framework, the voltage V_{G1} varies according to (10). The gain of the feedback stage (A_{VB}) was set to 7 as a design specification. The photodetector capacitance (C_{IN}) was specified at 200fF and the load capacitance (C_{OUT}) at 20 fF.

The performances obtained by using the methodology developed are summarized in Fig. 4. The blue zone represents infeasible solutions, that is, the solutions found do not meet the design specification. These are mostly concentrated in the strong inversion region. In fact, as previously described, in strong inversion region, due to the value of the resistor R_B the

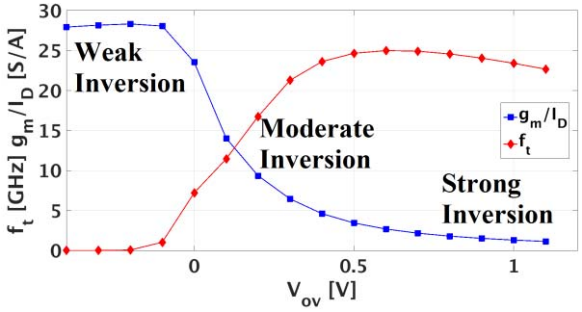

Fig. 3. Plot of g_m/I_D and f_t (normalized) at different levels of inversion V_{ov} (voltage overdrive V_{GS}-V_{TH}) for 130nm nMOS transistor.

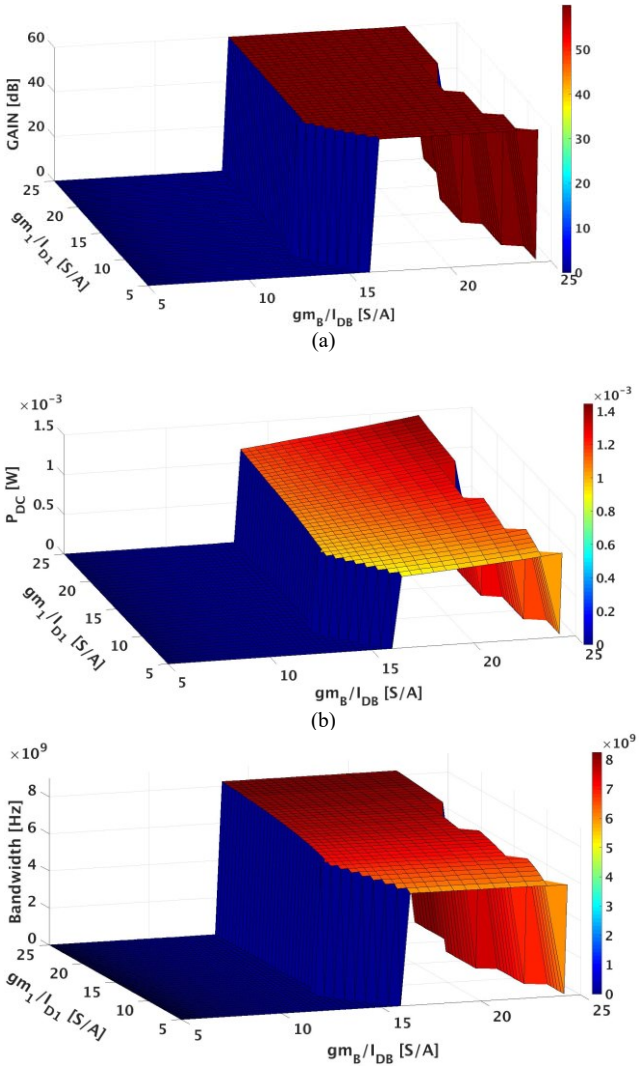

Fig. 4. (a) RGC gain vs. g_m/I_D, (b) DC power consumption vs. g_m/I_D (c) RGC bandwdth vs. g_m/I_D.

transistors tend to operate at extremely low voltages. In the space where the solutions are feasible, it is worth to notice that the gain if very flat, as expected from the fact that the value of the gain is essentially determined by the value of R_1 (fig. 4(a)). From fig. 4(b), we see that the behavior of the DC power consumption is the opposite of what we would have expected from the g_m/I_D theory's insights that can be inferred when considering the single transistors M_1 and M_B in isolation. Contrary to expectations, when both transistors are biased in weak inversion, they exhibit the highest value of the bias voltage V_{G1} and therefore the circuit dissipates the highest value of DC power.

For high values of g_{m1}/I_{D1}, the trend of the bandwidth is also counter-intuitive with respect to the general g_m/I_D theory (fig. 4(c)). From (5), we see that C_X depends on a fix term (C_{IN}) and on two variable terms (C_{GSB} and C_{SB1}). From (7), we see that R_X depends on two fix values (R_S and A_{VB}=g_{mB}×R_B) and on the reciprocal of g_{m1}. Hence, when the transistor M_1 passes from strong to weak inversion the value of g_{m1} increases at a much faster rate than the value of C_X, consequently, since the bandwidth depends on the inverse of the time constants of the

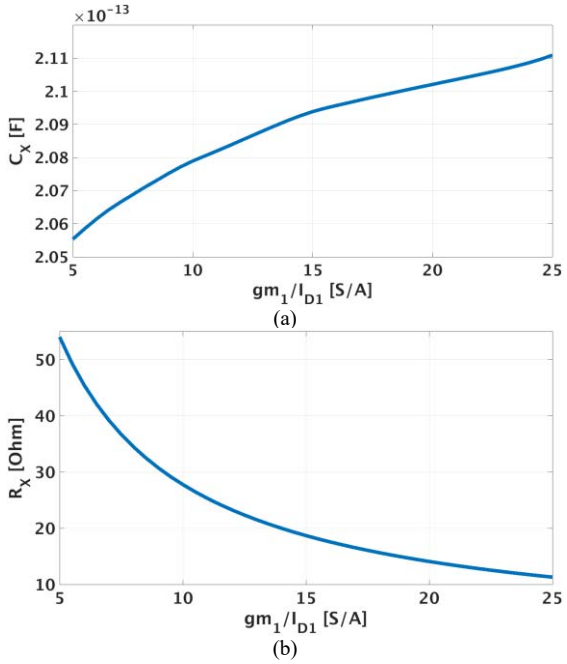

Fig. 5 (a) C_X vs. g_{m1}/I_{D1}, and g_{mB}/I_{DB} = 20 S/A (b) R_X vs. g_{m1}/I_{D1}, and g_{mB}/I_{DB} = 20 S/A

circuit, the bandwidth it is larger in strong inversion. Fig. 5 sketches the plots of C_X and R_X versus g_{m1}/I_{D1} with a fix value of 20 S/A for g_{mB}/I_{DB}. When we are passing from strong to weak inversion, R_X exponentially decreases from a value of 55 Ω to a value of 10 Ω, with a decrement of about 80%. On the contrary, for the same value of g_{mB}/I_{DB}, C_X increases only of about 3% passing from 206fF in strong inversion to 212fF in weak inversion.

From the point of view of g_{mB}/I_{DB}, the trend of the bandwidth agrees with the general g_m/I_D theory: its value slowly decreases as we move from strong to weak inversion. In fact, if we consider the expression of C_Y reported in (6), we see that the time constant, τ_Y, is expected to increase. This is because the intrinsic capacitance C_{DB1} grows with the width of the transistor, but the value of R_Y is fixed and equal to R_1. However, due to the technology process used in this work the values of the intrinsic capacitances are not decreasing significantly and hence the resulting plots are extremely flat.

Finally, Tab 1 reports the performances obtained for the optimal circuit extracted by exploiting the proposed method. The RGC achieves a gain of 60 dBΩ with a bandwidth of 7.27 GHz and it dissipates only 1 mW from a 1.5V power supply.

IV. CONCLUSION

The work introduces a novel systematic design methodology to design a nanoscale regulated cascode amplifier in absence of closed-form MOSFET equations. The proposed method shows the benefits of combining symbolic analysis and the g_m/I_D approach. Matlab and SPECTRE simulation were performed to validate the design of a RGC amplifier utilizing a 130 nm CMOS process with 1.5V supply. Due to the feedback topology of the circuit and to the process used, the bandwidth and the DC power consumption trends are not in agreement with some of the common insights suggested by the g_m/I_D theory. The lowest DC power consumption is achieved in strong inversion while the highest value of bandwidth is achieved in weak inversion. Hence, designers must be extremely careful when using the g_m over I_D based methodology to design circuits presenting feedback loops. Finally, given the importance of low noise in the design of any TIA topology, it is worth to mention, that although we did not explicitly consider noise as one of our primary targets, the final design achieved an input referred noise of about 12.2 pA/√Hz.

TABLE I. RGC PARAMETERS

Parameter	Value
g_{m1}/I_{D1}	10 S/A
g_{mB}/I_{DB}	13.7 S/A
W_1	15.6 µm
W_B	19.4 µm
L	130 nm
BW	7.28 GHz
P_{DC}	1 mW
Gain	60 dBΩ

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