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# The Design of an Equalizer—Part One

Equalizers are widely used in broadband wireline systems. At high data rates, the imperfections of the medium through which the signal travels (the "channel") become more critical, making equalization an essential function in receivers (Rxs).

In this two-part article, we study the transistor-level design of a high-speed equalizer in 28-nm CMOS technology. The first part describes channel modeling and linear equalizer design. The second part deals with decision-feedback equalizers (DFEs). We target the following performance:

- Data format: nonreturn to zero
- Data rate = 56 Gb/s
- Channel loss at 28 GHz = 20 dB
- Input differential swing = 800 $mV_{pp}$
- Bit error rate (BER) $<10^{-12}$
- Power consumption = 10 mW
- $V_{DD}$ = 1 V.

It is customary to specify the channel loss at the "Nyquist frequency," $f_{Nyq}$, i.e., the frequency equal to half of the data rate. The reader is referred to several background articles [1]–[3] and the vast literature on the subject [4]–[17]. The simulations are carried out with $V_{DD} = 1\,V - 5\%$ in the slow-slow corner of the process and at $T = 75\,^{\circ}C$.

## General Considerations

The purpose of equalization in an Rx is to compensate for channel nonidealities and reproduce the transmitted data with a low error rate. The design must therefore assume certain characteristics for the channel. We employ a "scalable" model that reflects the physical loss mechanisms in copper media [1]. Shown in Figure 1(a) is one section of the model, with its horizontal and vertical branches representing frequency-dependent copper and dielectric losses, respectively [1]. The component values are obtained by fitting the circuit's magnitude and phase responses to those computed by electromagnetic field simulations of a 50-Ω channel. Cascading 12 such sections yields the loss profile depicted in Figure 1(b) and a value of 21 dB at 28 GHz. Note that the line is driven by a 50-Ω source and is terminated with a 50-Ω load.

In addition to loss, copper media can also suffer from impedance discontinuities. For example, a connector attaching a cable to a line card

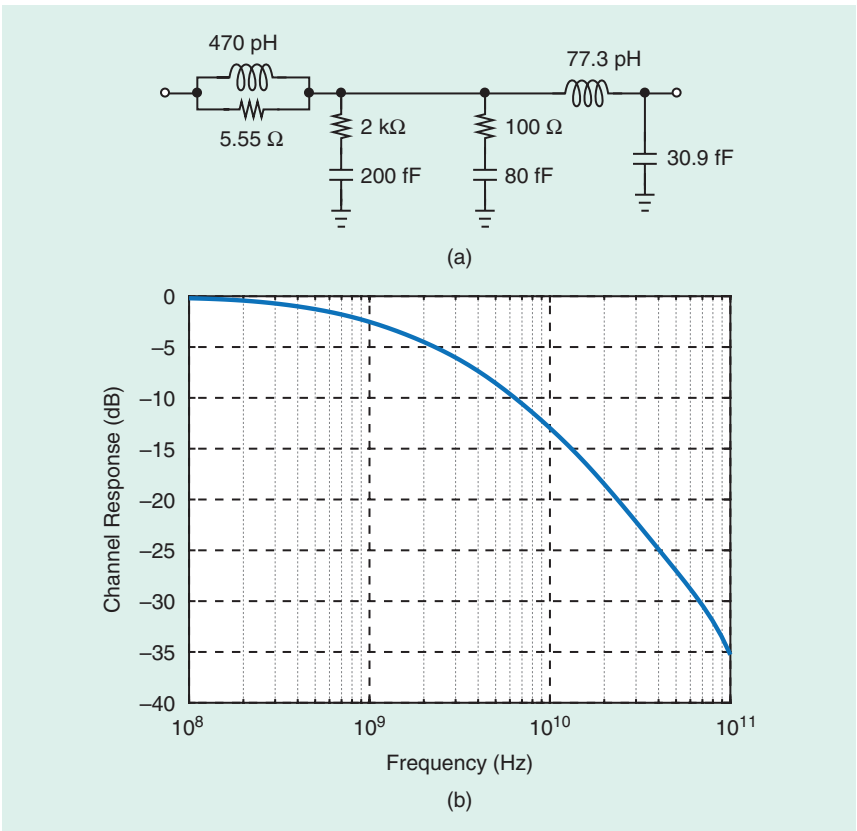


**FIGURE 1:** (a) One section of a scalable channel model and (b) the loss profile for 12 cascaded sections.

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may exhibit an impedance that has a real component different from 50 Ω as well as a finite imaginary value. As a result, the frequency response experiences a deep notch, an effect that can be compensated by a DFE but not by a linear equalizer.

Analog equalization in Rxs is realized by a continuous-time linear equalizer (CTLE) and a DFE [Figure 2(a)]. The CTLE ideally "inverts" the channel, i.e., it provides the inverse of the channel's frequency response so that the product of their transfer functions has a relatively flat magnitude up to the Nyquist frequency [Figure 2(b)]. We say that the CTLE "boosts" the high-frequency components of the received data. In practice, however, various tradeoffs in CTLE design allow only partial flattening of the response, thereby requiring that the DFE perform further equalization.

The significance of the Nyquist frequency, $f_{Nyq}$, is better appreciated by examining the channel response in the time domain. Consider a random sequence of ones and zeros arriving at a rate of $r_b$ bits per second, i.e., with a bit period of $1/r_b = T_b$. As depicted in Figure 3(a), such a sequence can follow a 0–1–0–1 pattern for some time, e.g., from 5.3 to 5.4 ns, which we consider a periodic signal having a fundamental frequency of $(1/r_b)/2 = f_{Nyq}$. This periodic segment experiences the greatest degradation in the channel, as illustrated by the differential waveforms in Figure 3(b) for a loss of 12 dB at $f_{Nyq}$. But we also recognize that the worst case occurs for the first transition, which arrives after 5.25 ns, i.e., after the channel has "relaxed." As the periodic segment proceeds, the output reaches the steady state and a greater swing.

## Basic CTLE Stage

The most common approach to creating a boost at high frequencies incorporates resistive and capacitive degeneration in a differential

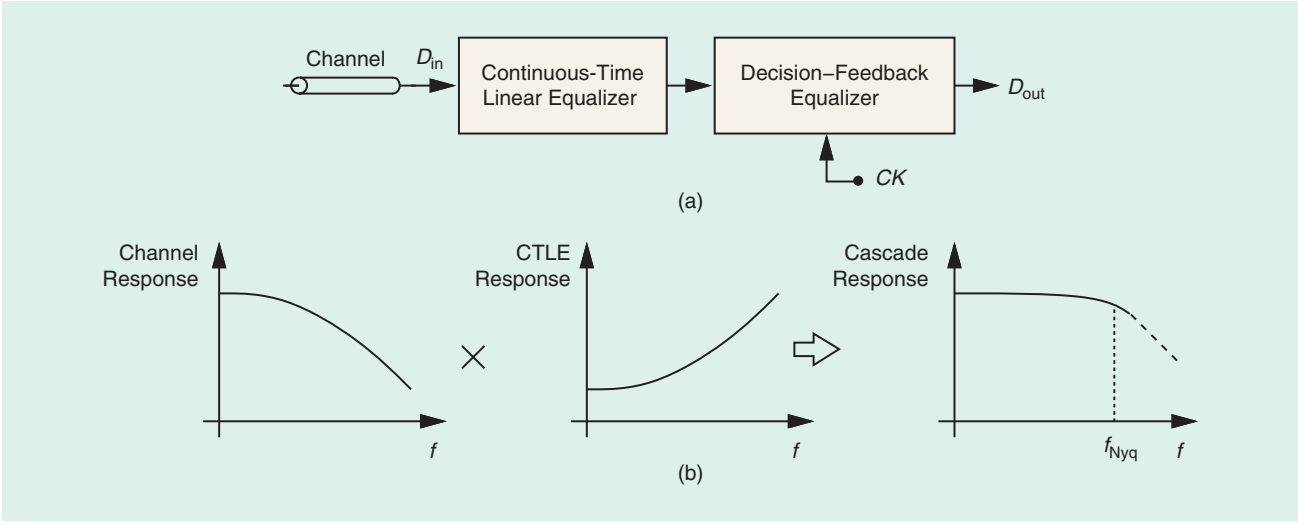



**FIGURE 2:** (a) A typical equalizer architecture and (b) an illustration of its overall frequency response.

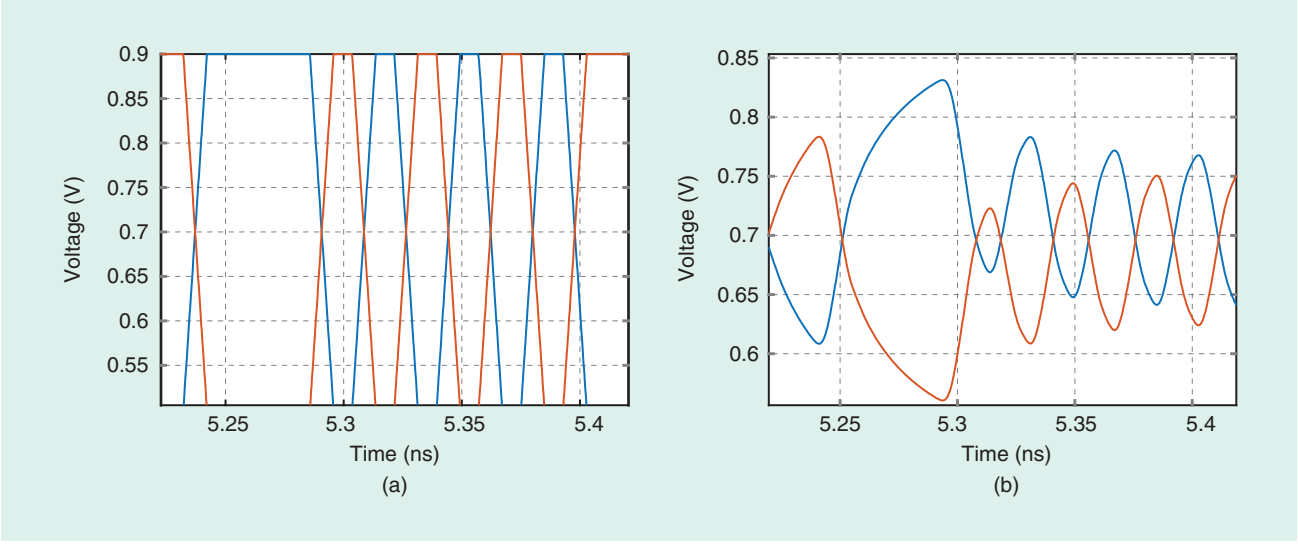



**FIGURE 3:** (a) The input and (b) output waveforms of a lossy channel.

pair, as shown in Figure 4(a). It can be readily proved that the circuit's transfer function, $H(s) = V_{out}/V_{in}$, is given by

$$H(s) = \frac{-g_m R_D (R_S C_S s + 1)}{R_S C_S s + 1 + g_m R_S/2}, \quad (1)$$

where $g_m$ denotes the transconductance of $M_1$ and $M_2$ and channel-length modulation is neglected. The stage exhibits a zero and a pole, respectively:

$$|\omega_z| = \frac{1}{R_S C_S} \quad (2)$$

$$|\omega_p| = \frac{1 + g_m R_S/2}{R_S C_S}, \quad (3)$$

and the magnitude of its response varies from $g_m R_D/(1 + g_m R_S/2)$ at low frequencies to $g_m R_D$ at high frequencies [Figure 4(b)]. The circuit thus provides a boost factor of $1 + g_m R_S/2$. Note that the zero and pole frequencies are separated by the same factor.

The CTLE stage of Figure 4(a) merits two remarks. First, the boost factor trades with the low-frequency gain (also called the *dc gain*), $g_m R_D/(1 + g_m R_S/2)$. We wish to maintain this gain around unity so that the received data swings are not attenuated. With low supply voltages and channel-length modulation, the boost factor typically does not exceed 6 dB. Second, we surmise that $\omega_p$ should be placed roughly around the Nyquist frequency, but as indicated by the red plot in Figure 4(b), the limited bandwidth at the output makes it difficult to do so. For this reason, high-speed CTLEs often employ inductive peaking.

The output pole, $\omega_0$, in Figure 4(a) results from the load resistance and capacitance, presenting significant challenges in high-speed CTLE design. The relative magnitudes of this pole and that due to source degeneration lead to different responses and dependencies upon $C_S$. As shown in Figure 5(a), if $\omega_0 > \omega_p$, then increasing $C_S$ simply shifts the high-pass response to the left. On the other hand, if $\omega_0 < \omega_p$ [Figure 5(b)], then two effects emerge. First, $|H|$ fails to reach its maximum value of $g_m R_D$. Second, a greater $C_1$ and hence a lower $\omega_p$ reduce the frequency at which the peak occurs. These points encourage us to apply inductive peaking so as to approach the first case.

To raise the boost factor, we can cascade multiple CTLE stages, but at the cost of reduced small-signal bandwidth and greater power consumption. If each stage's bandwidth limitation is approximated by a single pole at $2\pi f_0$, then $n$ identical stages yield a total bandwidth of

$$BW_{tot} = \sqrt{2^{1/n} - 1}\, f_0. \quad (4)$$

For example, two stages lower the bandwidth by 35%. These constraints imply that it is difficult to use more than two CTLE stages, and that the DFE in Figure 2(a) must shoulder the remainder of the equalization.

## Pole-Placement Considerations

In the CTLE stage studied previously, we may naturally conclude that the degeneration pole, $\omega_p$, should be placed around the Nyquist frequency. In reality, however, the situation is more complex. With the low available boost factor per stage, the Bode plot of $|H(j\omega)|$ in Figure 4(b) proves inaccurate because $\omega_z$ and $\omega_p$ are separated by a factor of only 2 to 3. The actual behavior is depicted in Figure 6 and can be quantified as follows. We express $|H(j\omega)|^2$ from (1) as

$$|H(j\omega)|^2 = K^2 \frac{\omega^2 + \omega_z^2}{\omega^2 + \omega_p^2}, \quad (5)$$

where $K = g_m R_D$, and evaluate it at $\omega = \omega_p = (1 + g_m R_S/2)\omega_z$:

$$|H(j\omega_p)|^2 = \frac{K^2}{2}\left[1 + \frac{1}{\left(1 + \frac{g_m R_S}{2}\right)^2}\right]. \quad (6)$$

That is,

$$|H(j\omega_p)| = \frac{K}{\sqrt{2}} \sqrt{1 + \frac{1}{\left(1 + \frac{g_m R_S}{2}\right)^2}}. \quad (7)$$

If the boost factor, $1 + g_m R_S/2$, ranges from 2 to 3, then $|H(j\omega_p)|$ falls between $0.79K$ and $0.74K$, i.e., roughly 2 to 2.5 dB below the maximum value. The key

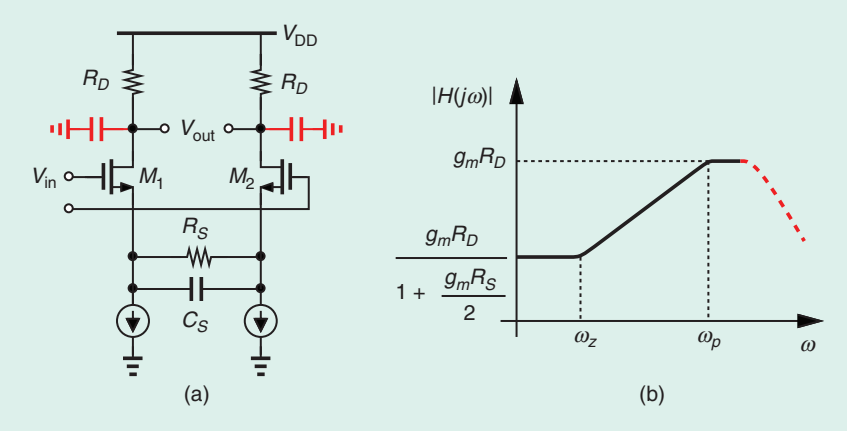



**FIGURE 4:** (a) A basic CTLE stage and (b) its approximate response.

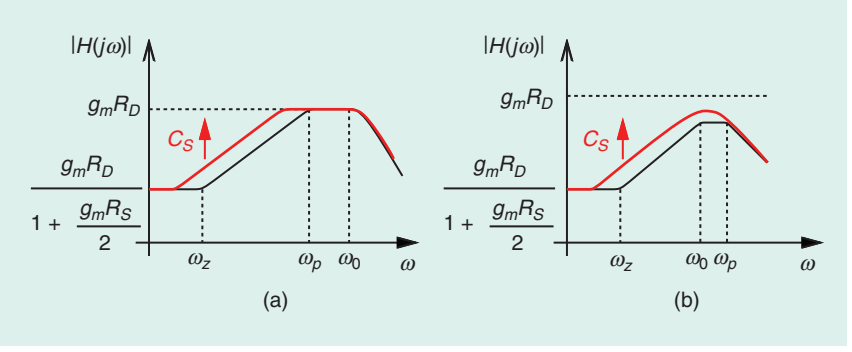



**FIGURE 5:** The CTLE response for (a) $\omega_0 > \omega_p$ and (b) $\omega_0 < \omega_p$.

point here is that, to create maximum boost at $f_{Nyq}$, the pole frequency should be chosen well below this frequency. For example, to obtain $|H(j2\pi f_{Nyq})| = 0.95K$, (7) indicates that $\omega_p$ must be chosen according to

$$\omega_p = \frac{0.312(2\pi f_{Nyq})}{\sqrt{0.95^2 - \dfrac{1}{\left(1+\dfrac{g_m R_S}{2}\right)^2}}}. \quad (8)$$

For a boost factor of 2 to 3, $\omega_p$ ranges from $0.39(2\pi f_{Nyq})$ to $0.35(2\pi f_{Nyq})$, i.e., the pole frequency should be roughly 2.5 to 3 times less than $f_{Nyq}$.

## CTLE Design

CTLE design proceeds in four steps. 1) We place the degeneration pole around one-third of $f_{Nyq}$ and implement the CTLE. 2) We precede the CTLE with the channel and examine the flatness of the cascade response. 3) We study and optimize the eye diagram at the CTLE output. 4) We realize a programmable boost factor. We can then design the DFE and study the performance of the overall equalizer.

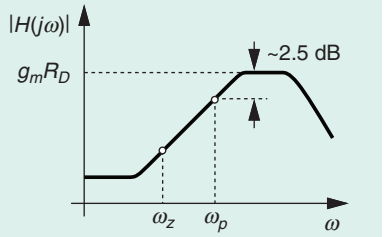



**FIGURE 6:** An illustration of an actual CTLE response.

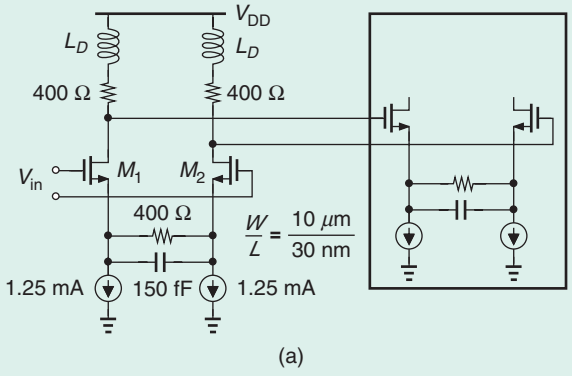
We begin the design of our two-stage CTLE with a power budget of 5 mW, leaving the other 5 mW for the DFE. Biased at 2.5 mW, each stage then allows a current of 1.25 mA per transistor. We then select the aspect ratio, $W/L$, of $M_1$ and $M_2$ in Figure 4(a) according to two requirements, namely, the desired transconductance and an acceptable gate-source overdrive voltage. The former plays a role in the boost factor while the latter determines the voltage headroom for the tail current sources and across the drain resistors. According to simulations, a $W/L$ of 10 $\mu$m/30 nm gives a $g_m$ of 10 mS and an overdrive of 170 mV, both reasonable values. We then target a boost factor of $1 + g_m R_S/2 = 3$, obtaining $R_S = 400\,\Omega$. We also place $\omega_p$ at $2\pi(28\,\text{GHz})/3$ and arrive at a value of 150 fF for $C_S$. The drain resistors are constrained by the voltage headroom; we select $R_D = 400\,\Omega$ for a voltage drop of 500 mV.

Figure 7(a) depicts the design of the first stage. We load the circuit by an identical stage for now. Figure 7(b) plots the response with $L_D$ = 0 and $L_D$ = 600 pH, suggesting that inductive peaking raises the boost from 5.4 to 6.2 dB and its corresponding frequency from 15 GHz to approximately 20 GHz. The dc gain is about unity. The bandwidth falls short of $f_{Nyq} = 28$ GHz and can be increased by lowering $R_D$ but at the cost of dc gain. This tradeoff must eventually be studied when the CTLE-DFE chain is formed.

We now cascade two such stages so as to raise the boost factor [see Figure 8(a)]. As an approximation of the input capacitance of the next stage, two NMOS devices with $W/L = 10\,\mu$m/30 nm are attached to the output nodes. Plotted in Figure 8(b), the overall response exhibits a boost of 14 dB at 25 GHz. Preceding the CTLE with the channel yields the behavior in Figure 8(c) and hence, roughly 8 dB of loss at $f_{Nyq}$. Unlike the first stage, the second does not see Miller capacitance multiplication, thus achieving a wider bandwidth.

The next step is to study the eye diagrams. Depicted in Figure 9(a) and (b) are the channel and CTLE outputs, respectively. We observe a vertical opening of 250 mV and a horizontal opening of 13 ps.

As mentioned previously, the tradeoff between the dc gain and the boost factor should be examined in a given design. Specifically, does the vertical eye opening in Figure 9(b) increase if the dc gain is raised and the boost is, inevitably, reduced? For example, we can choose $R_S = 300\,\Omega$ and $C_S = 200$ fF. But simulations



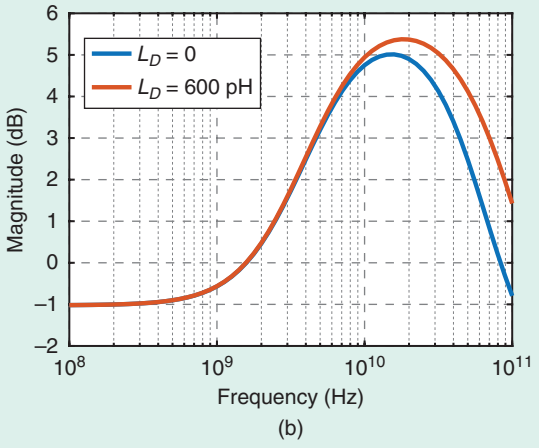




**FIGURE 7:** (a) The design of the first CTLE stage and (b) its frequency response.

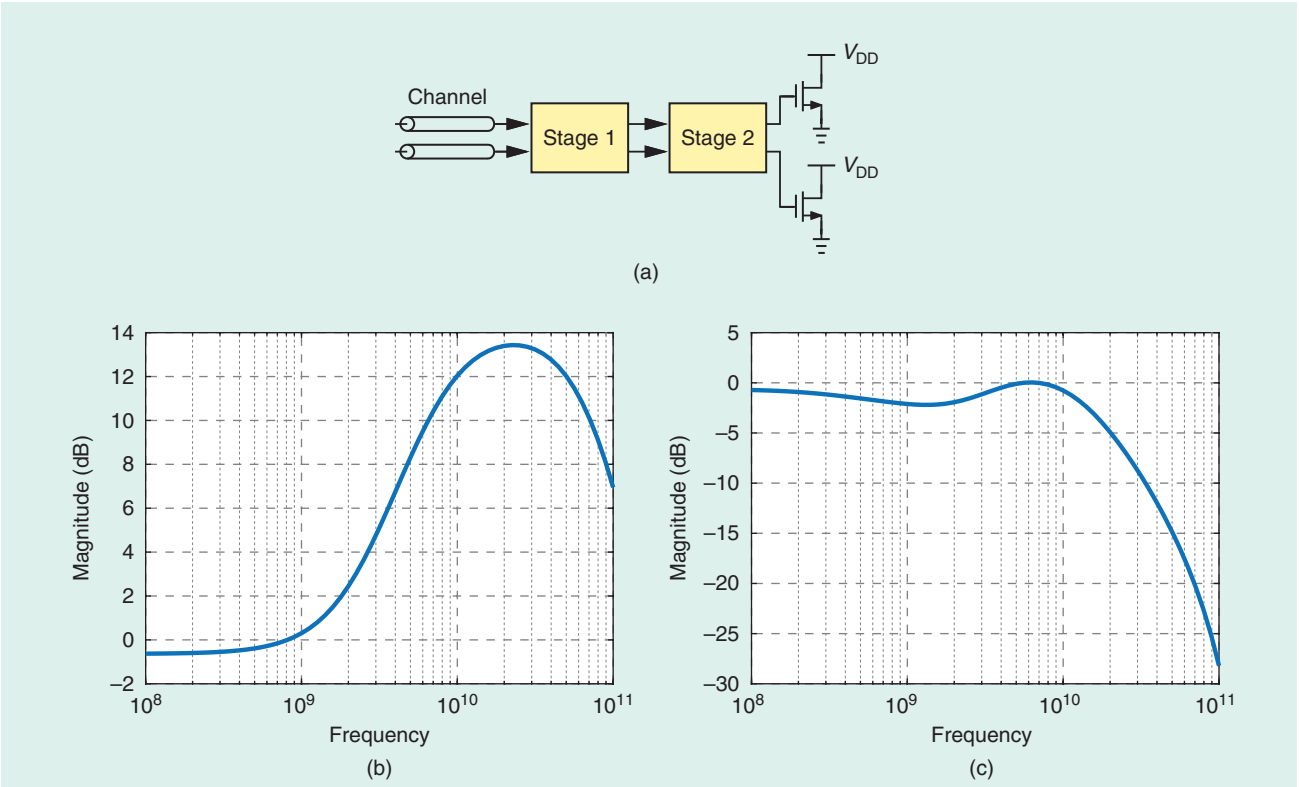



**FIGURE 8:** (a) The two-stage CTLE, (b) its frequency response, and (c) the channel-CTLE cascade response.

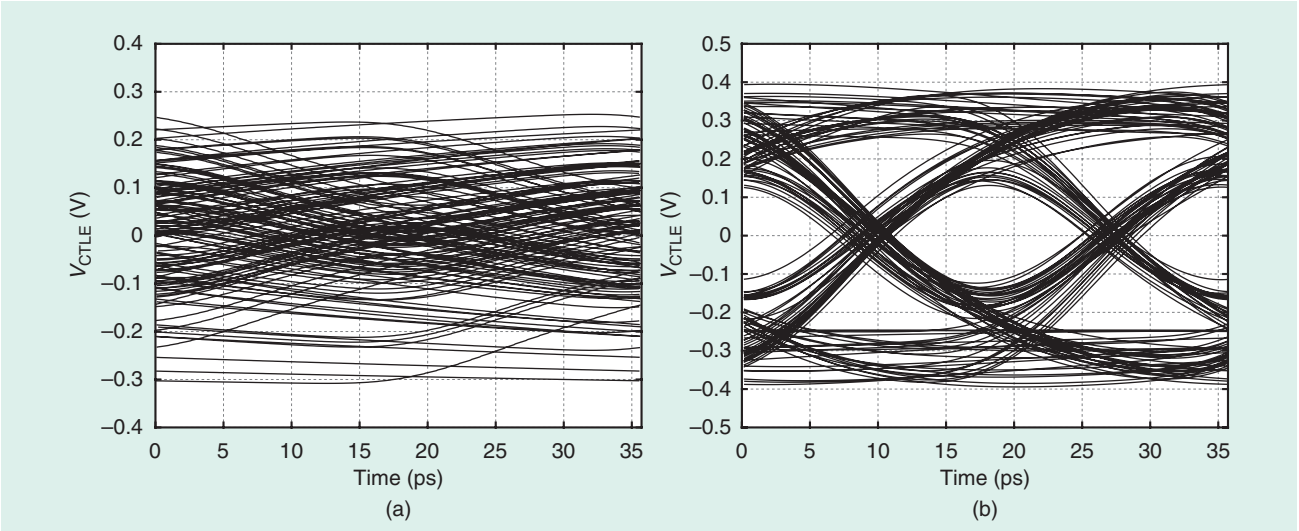



**FIGURE 9:** The output eyes of (a) the channel and (b) the CTLE.

reveal that the eye suffers further closure in this case. Conversely, $R_S = 600\,\Omega$ and $C_S = 100$ fF increase the boost factor but do not improve the output eye.

Whether the eye opening depicted in Figure 9(b) is adequate for a BER $< 10^{-12}$ or not is ultimately determined by the DFE design. Our assumption at this point is that the DFE will further improve the eye.

## The Need for Programmable Boost

Broadband Rxs must operate properly with different channel responses. The CTLE developed thus far is optimized for a loss of approximately 20 dB at $f_{Nyq}$, and "overequalizes" the data if the loss is lower. As a result, significant intersymbol interference appears at the CTLE output. For this reason, the boost must be variable. This is typically accomplished by implementing the degeneration capacitors as programmable units. A lower

*(continued on p. 160)*


**FIGURE 9:** The Best Demo Paper Award was given to two papers at the VLSI 2021: "Energy-Efficient Reliable HZO FeFET Computation-in-Memory with Local Multiply and Global Accumulate Array for Source-Follower and Charge-Sharing Voltage Sensing" by the University of Tokyo, and "A Sub-mW Dual-Engine ML Inference System-on-Chip for Complete End-to-End Face-Analysis at the Edge" by CSEM and ETH Zürich.

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## THE ANALOG MIND *(continued from p. 11)*

value pushes the pole to higher frequencies, thereby providing less equalization at $f_{Nyq}$.

In the second part of this article, we design a DFE and cascade it with the CTLE.

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