

See discussions, stats, and author profiles for this publication at: <https://www.researchgate.net/publication/347292175>

An Analysis of an Input Impedance of a Regulated Cascode Cross Couple Power Amplifier

Conference Paper · October 2020

DOI: 10.23919/ICCAS50221.2020.9268319

CITATIONS

2

READS

152

1 author:



Kittipong Tripetch

Rajamangala University of Technology Suvarnabhumi

39 PUBLICATIONS 17 CITATIONS

SEE PROFILE

An Analysis of an Input Impedance of a Regulated Cascode Cross Couple Power Amplifier

Kittipong Tripetch
Division of Electronic and
Telecommunication engineering
Faculty of Engineering and
Architecture
Rajamangala University of
Technology Suvarnabhumi
Kittipong.tripetch.mr@ieee.org

Abstract—The input impedance of a regulated cascode cross couple amplifier is derived. The frequency response of the input impedance polynomial form can be plotted with MATLAB. From the polynomial form of the input impedance of the proposed circuit, it can be transformed by substitute complex frequency s with $j\omega$ into the polynomial form equation. After that, this function can be grouped into a symbolic real and a symbolic imaginary form. The next step in derivation is to multiply this function with a complex conjugate function of the symbolic complex form of the input impedance. The last step is to plot a real and an imaginary part as a function of the input frequency so that the power amplifier can be matching with the various matching circuit according to the condition of the maximum power transfer.

Keywords— a regulated cascode amplifier, input impedance, oscillator, power amplifier, a regulated cascode cross couple amplifier

I. INTRODUCTION

The Regulated Cascode amplifier was proposed by Sackinger since 1990 [1]. This topology of amplifier is famous because it has a higher output impedance compared with cascode amplifier counterpart. Thus, its output voltage is higher than other types of an amplifier such as a common source, a common gate and a cascode amplifier. The concept of the regulated transistor can be replaced by an amplifier block diagram which is used to regulated drain-source voltage drop of the first stage transistor but it used more transistor which was proposed since 1990 [2]. The advantage of this idea is a more voltage gain but the disadvantage is, it has more parasitic capacitances which degrade the bandwidth of the amplifier. The circuit technique called a regulated cascode also have many types of application like a switched current integrator which can be replaced in the signal flow graph of the high order switched current filter which was published since 1993 [3]. It can be used as the core circuit of current mirror. Its advantageous compared to other circuit technique is a fast settling time for a low value of current mirror between 10 microampere to 600 microampere. It is much slower than a simple current mirror if it is designed to operate for 530

microampere to 800 microampere. It is published since 1994 [4]. Other applications of the regulated cascode amplifier can be modified as a transconductance amplifier and transimpedance amplifier which are published during 1997-2015 [5]-[12]. The tuning range of the regulated cascode cross couple oscillator can be approximated since 2013 [13]. Recent specifications which are related with a transimpedance amplifier based on RGC circuit diagram and its modification are published in [14]-[16]

In section II, a straightforward definition of input impedance and circuit diagram definition is described. A high frequency equivalent circuit is shown and described in Section III. In section IV, a luculent and rigorous contribution for a detail circuit analysis procedure example of the regulated cascode cross coupled amplifier input impedance polynomial form is proposed for the first time. Without this equation, it is very iterative for impedance matching of the proposed circuit. In section V, the graphs of input impedance as a function of input frequency and current consumption are plotted by programming with level1 transistor model. In section VI, A dc operating point of the Regulated Cascode cross coupled (RGC) power amplifier is described. In section VII, an experimental result of the RGC cross coupled power amplifier is performed after the connection of silver wires on the breadboard are finished.

II. INPUT IMPEDANCE OF THE REGULATED CASCODE CROSS COUPLED AMPLIFIER DESCRIPTION

The input impedance is a ratio of input voltage and input current. It can be derived by using Kirchhoff's current law and Ohm's law. The Circuit diagram of the regulated cascode cross couple amplifier is drawn in figure1. The high frequency equivalent circuit of MOSFET is used to substitute for circuit analysis purpose. It is shown in figure 2. The regulated cascode amplifier can be described as a cascade of a first stage common-source amplifier which used transistor M_1 and a common gate amplifier. A regulated transistor can be seen as a cascade of a second stage common source amplifier which used transistor M_3 with a first stage common source amplifier. The output of

the second stage of a common source amplifier can be cascaded with the cascode transistor M_2 .

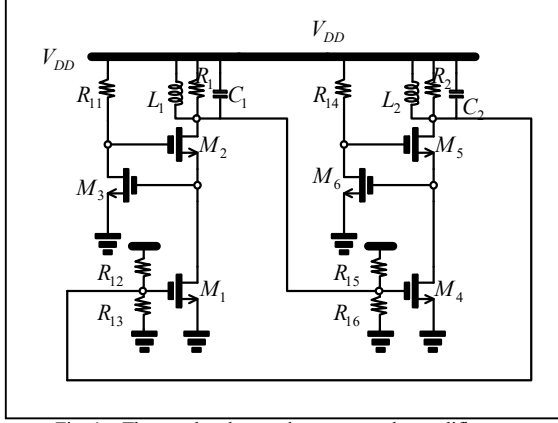


Fig. 1. The regulated cascode cross couple amplifier

The regulated cascode cross coupled amplifier is shown in figure1. It composed of 6 NMOS transistors. The circuit has 4 bias resistors which are used to controlled drain current of the MOSFET. There are two resonance circuits which used two parallel inductor, capacitor and resistors. The output of the first regulated cascode amplifier is connected with the input of the second regulated cascode amplifier. The output of the second regulated cascode amplifier is feedback to the input of the first regulated cascode amplifier. That's why it is called the regulated cascode cross coupled amplifier. The high frequency equivalent circuit of the proposed circuit is shown in figure2. The two bulk source voltage controlled current source are included for the cascode transistors.

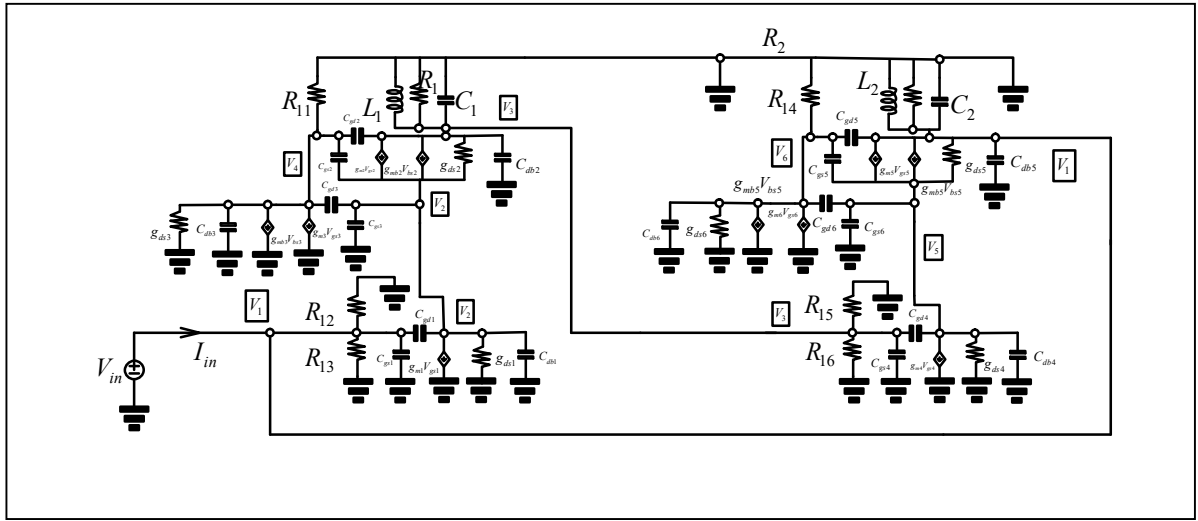


Fig. 2. The regulated cascode cross couple amplifier topology after substituted with a high frequency MOSFET equivalent circuit

III. A HIGH FREQUENCY EQUIVALENT CIRCUIT OF A REGULATED CASCODE CROSS COUPLE AMPLIFIER DESCRIPTION

The high frequency equivalent circuit of a regulated cascode cross couple amplifier is a crucial building block for circuit analysis and design purpose. It can be substituted with the circuit diagram in figure1. Some transistors used equivalent circuit elements only 5 elements. Some transistors used equivalent circuit elements for 6 elements. It is difference as a result of a fabrication process which has a bulk source voltage effect for a drain current can be modeled with voltage controlled current sourced which is labeled with g_{mb} which can be pronounced as a transconductance of the bulk source voltage for a cascode transistor. There are six bias resistors in the circuit which can be labeled as R_{11} , R_{12} , R_{13} , R_{14} , R_{15} and R_{16} . The total elements in the circuit can be counted to have 46 elements.

IV. A DETAIL PROCEDURE EXAMPLE FOR INPUT IMPEDANCE POLYNOMIAL FORM DETERMINATION

There are six nodes in this circuit. It could be labeled as V_1 , V_2 , V_3 , V_4 , V_5 and V_6 . After using Kirchhoff's current

law and grouping the small signal parameters and its passive elements. It can be written as following.

$$\begin{bmatrix} -b_2 & 0 & 0 & 0 & b_3 & b_4 \\ b_5 & -b_6 & 0 & b_7 & 0 & 0 \\ 0 & a_{14} & -b_8 & b_9 & b_{10} & 0 \\ 0 & b_{11} & b_{12} & -b_{13} & 0 & 0 \\ a_{25} & 0 & b_{14} & 0 & -b_{15} & b_{16} \\ b_{17} & 0 & 0 & 0 & b_{18} & b_{19} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} -I_{in}b_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (1)$$

a_i and b_i are novel coefficients which are a function of the small signal parameters and passive elements parameters in the regulated cascode cross couple amplifier. All of the novel coefficients could not be defined if it is duplicated the label of the coefficients.

$$\begin{aligned}
a_1 &= L_2 R_{12} R_{13} \\
a_2 &= L_2 R_{12} R_{13} C_2 + L_2 R_{12} R_{13} C_{gd5} + L_2 R_{12} R_{13} C_{db5} \\
a_3 &= \frac{L_2 R_{12} R_{13}}{R_2} + L_2 R_{13} + L_2 R_{12} + L_2 R_{12} R_{13} g_{gds5} \\
a_4 &= R_{12} R_{13} \\
a_5 &= L_2 R_{12} R_{13} (g_{m5} + g_{mb5} + g_{ds5}) \\
a_6 &= C_{gd5} L_2 R_{12} R_{13} \\
a_7 &= g_{m5} L_2 R_{12} R_{13}
\end{aligned} \tag{2}$$

$$\begin{aligned}
b_1 &= sa_1 \\
b_2 &= s^2(a_2) + s(a_3) + (a_4) \\
b_3 &= sa_5 \\
b_4 &= s^2(a_6) - s(a_7)
\end{aligned} \tag{3}$$

$$\begin{aligned}
a_8 &= C_{gd1} \\
a_9 &= g_{m1} \\
a_{10} &= C_{gd3} + C_{gs2} + C_{gs3} + C_{gd1} + C_{db1} \\
a_{11} &= +g_{m2} + g_{mb2} + g_{ds2} + g_{ds1} \\
a_{12} &= sC_{gd3} + sC_{gs2} + g_{m2} \\
a_{13} &= g_{m2}
\end{aligned} \tag{4}$$

$$\begin{aligned}
b_5 &= sa_8 - a_9 \\
b_6 &= sa_{10} + a_{11} \\
b_7 &= sa_{12} + a_{13}
\end{aligned} \tag{5}$$

$$\begin{aligned}
a_{14} &= sL_1 (g_{m2} + g_{mb2} + g_{ds2}) \\
a_{15} &= L_1 \left(\frac{1}{R_1} + \frac{1}{R_{15}} + g_{ds2} + \frac{1}{R_{16}} \right) \\
a_{16} &= L_1 (C_1 + C_{gd4} + C_{gd2} + C_{db2} + C_{gs4}) \\
a_{17} &= (L_1 C_{gd2}), a_{18} = (L_1 g_{m2}), a_{19} = (L_1 C_{gd4})
\end{aligned} \tag{6}$$

$$\begin{aligned}
b_8 &= 1 + sa_{15} + s^2(a_{16}) \\
b_9 &= s^2 a_{17} - sa_{18} \\
b_{10} &= s^2 a_{19}
\end{aligned} \tag{7}$$

$$\begin{aligned}
a_{20} &= (C_{gd3} + C_{gs2}) \\
a_{21} &= g_{m3} \\
a_{22} &= C_{gd2} \\
a_{23} &= [C_{gd2} + C_{db3} + (C_{gd3} + C_{gs2})] \\
a_{24} &= \left[\frac{1}{R_{11}} + g_{ds3} \right]
\end{aligned} \tag{8}$$

$$\begin{aligned}
b_{11} &= [sa_{20} - a_{21}] \\
b_{12} &= (sa_{22}) \\
b_{13} &= (sa_{23} + a_{24})
\end{aligned} \tag{9}$$

$$\begin{aligned}
a_{25} &= g_{ds5}, a_{26} = C_{gd4}, a_{27} = g_{m4} \\
a_{28} &= (C_{gd6} + C_{gs5} + C_{gs6} + C_{gd4} + C_{db4}) \\
a_{29} &= (g_{m5} + g_{mb5} + g_{ds5} + g_{ds4}) \\
a_{30} &= (C_{gd6} + C_{gs5}), a_{31} = g_{m5}
\end{aligned} \tag{10}$$

$$\begin{aligned}
b_{14} &= [sa_{26} - a_{27}] \\
b_{15} &= [sa_{28} + a_{29}] \\
b_{16} &= [sa_{30} + a_{31}]
\end{aligned} \tag{11}$$

$$\begin{aligned}
a_{32} &= (C_{gd6} + C_{gs5}) \\
a_{33} &= g_{m6} \\
a_{34} &= C_{gd5} \\
a_{35} &= [C_{gd5} + C_{db6} + (C_{gd6} + C_{gs5})] \\
a_{36} &= \left[\frac{1}{R_{14}} + g_{ds6} \right]
\end{aligned} \tag{12}$$

$$\begin{aligned}
b_{17} &= sa_{32} \\
b_{18} &= sa_{33} - a_{34} \\
b_{19} &= sa_{35} + a_{36}
\end{aligned} \tag{13}$$

All of the first stage intermediate coefficients which are written in the matrix of KCL are shown. From the matrix, it is a good time to describe how to eliminate column variables by writing $V_1 = f(V_5, V_6, I_{in})$. There are four equations which are related with the first column. The starting equation is the first row. There are 3 equations which needs to eliminate the first variable which is called V_1 . After substitute variable V_1 , the function can be grouped as following

$$d_1 = \left(\frac{b_3 b_5}{b_2} \right), d_2 = \left(\frac{b_4 b_5}{b_2} \right), d_3 = \left(\frac{b_1 b_5}{b_2} \right) \tag{14}$$

$$d_4 = \left(\frac{b_3 a_{25}}{b_2} - b_{15} \right), d_5 = \left(\frac{b_4 a_{25}}{b_2} + b_{16} \right), d_6 = \left(\frac{b_1 a_{25}}{b_2} \right) \tag{15}$$

$$d_7 = \left(\frac{b_3 b_{17}}{b_2} + b_{18} \right), d_8 = \left(\frac{b_4 b_{17}}{b_2} - b_{19} \right), d_9 = \left(\frac{b_1 b_{17}}{b_2} \right) \tag{16}$$

The process of grouping after eliminate the first column variable is finished here. The second column is started as following. The function can be written as $V_2 = f(V_4, V_5, V_6, I_{in})$. The system of equation can be update here so that the matrix in the single column can be seen as a single row left. It can be seen that the third and fourth row can be eliminate in the second column by substitute the function $V_2 = f(V_4, V_5, V_6, I_{in})$

$$\begin{bmatrix} -b_2 & 0 & 0 & 0 & b_3 & b_4 \\ 0 & -b_6 & 0 & b_7 & d_1 & d_2 \\ 0 & a_{14} & -b_8 & b_9 & b_{10} & 0 \\ 0 & b_{11} & b_{12} & -b_{13} & 0 & 0 \\ 0 & 0 & b_{14} & 0 & d_4 & d_5 \\ 0 & 0 & 0 & 0 & d_7 & d_8 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} -I_{in} b_1 \\ -I_{in} d_3 \\ 0 \\ 0 \\ -I_{in} d_6 \\ -I_{in} d_9 \end{bmatrix} \tag{17}$$

$$\begin{aligned}
d_{10} &= \left[b_9 + \frac{b_7 a_{14}}{b_6} \right], d_{11} = \left(b_{10} + \frac{d_1 a_{14}}{b_6} \right) \\
d_{12} &= \left(\frac{d_2 a_{14}}{b_6} \right), d_{13} = \left(\frac{d_3 a_{14}}{b_6} \right)
\end{aligned} \tag{18}$$

$$\begin{aligned}
d_{14} &= \left(\frac{b_7 b_{11}}{b_6} - b_{13} \right), d_{15} = \left(\frac{d_1 b_{11}}{b_6} \right) \\
d_{16} &= \left(\frac{d_2 b_{11}}{b_6} \right), d_{17} = \left(\frac{d_3 b_{11}}{b_6} \right)
\end{aligned} \tag{19}$$

The process of grouping after eliminate the second column variable is finished here. The third column variable can be eliminated by writing the function. It can be written as $V_3 = f(V_4, V_5, V_6, I_{in})$

$$\begin{bmatrix} -b_2 & 0 & 0 & 0 & b_3 & b_4 \\ 0 & -b_6 & 0 & b_7 & d_1 & d_2 \\ 0 & 0 & -b_8 & d_{10} & d_{11} & d_{12} \\ 0 & 0 & b_{12} & d_{14} & d_{15} & d_{16} \\ 0 & 0 & b_{14} & 0 & d_4 & d_5 \\ 0 & 0 & 0 & 0 & d_7 & d_8 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} -I_{in} b_1 \\ -I_{in} d_3 \\ -I_{in} d_{13} \\ -I_{in} d_{17} \\ -I_{in} d_6 \\ -I_{in} d_9 \end{bmatrix} \tag{20}$$

$$\begin{aligned}
d_{18} &= \left[\frac{d_{10} b_{12}}{b_8} + d_{14} \right], d_{19} = \left[\frac{d_{11} b_{12}}{b_8} + d_{15} \right] \\
d_{20} &= \left[\frac{d_{12} b_{12}}{b_8} + d_{16} \right], d_{21} = \left(\frac{d_{13} b_{12}}{b_8} + d_{17} \right)
\end{aligned} \tag{21}$$

$$\begin{aligned}
d_{22} &= \left[\frac{d_{10} b_{14}}{b_8} \right], d_{23} = \left[\frac{d_{11} b_{14}}{b_8} + d_4 \right] \\
d_{24} &= \left[\frac{d_{12} b_{14}}{b_8} + d_5 \right], d_{25} = \left[\frac{d_{13} b_{14}}{b_8} + d_6 \right]
\end{aligned} \tag{22}$$

The process of grouping after eliminate the third column variable is finished here. The fourth column variable can be eliminated by writing the function. It can be written as $V_4 = f(V_5, V_6, I_{in})$

$$\begin{bmatrix} -b_2 & 0 & 0 & 0 & b_3 & b_4 \\ 0 & -b_6 & 0 & b_7 & d_1 & d_2 \\ 0 & 0 & -b_8 & d_{10} & d_{11} & d_{12} \\ 0 & 0 & 0 & d_{18} & d_{19} & d_{20} \\ 0 & 0 & 0 & d_{22} & d_{23} & d_{24} \\ 0 & 0 & 0 & 0 & d_7 & d_8 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} -I_{in} b_1 \\ -I_{in} d_3 \\ -I_{in} d_{13} \\ -I_{in} d_{21} \\ -I_{in} d_{25} \\ -I_{in} d_9 \end{bmatrix} \quad (23)$$

$$d_{26} = \left[d_1 - \frac{d_{19} b_7}{d_{18}} \right], d_{27} = \left[d_2 - \frac{d_{20} b_7}{d_{18}} \right], d_{28} = \left[\frac{d_{21} b_7}{d_{18}} - d_3 \right] \quad (24)$$

$$\begin{aligned} d_{29} &= \left[d_{11} - \frac{d_{19}d_{10}}{d_{18}} \right], d_{30} = \left[d_{12} - \frac{d_{20}d_{10}}{d_{18}} \right] \\ d_{31} &= \left[\frac{d_{21}d_{10}}{d_{18}} - d_{13} \right] \end{aligned} \quad (25)$$

$$\begin{aligned} d_{32} &= \left[d_{23} - \frac{d_{19}d_{22}}{d_{18}} \right], d_{33} = \left[d_{24} - \frac{d_{20}d_{22}}{d_{18}} \right] \\ d_{34} &= \left[\frac{d_{21}d_{22}}{d_{18}} - d_{25} \right] \end{aligned} \quad (26)$$

The process of grouping after eliminate the fourth column variable is finished here. The fifth column variable can be eliminated by writing the function. It can be written as $V_5 = f(V_6, I_{in})$

$$\begin{bmatrix} -b_2 & 0 & 0 & 0 & b_3 & b_4 \\ 0 & -b_6 & 0 & 0 & d_{26} & d_{27} \\ 0 & 0 & -b_8 & 0 & d_{29} & d_{30} \\ 0 & 0 & 0 & d_{18} & d_{19} & d_{20} \\ 0 & 0 & 0 & 0 & d_{32} & d_{33} \\ 0 & 0 & 0 & 0 & d_7 & d_8 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} -I_{in} b_1 \\ I_{in} d_{28} \\ I_{in} d_{31} \\ -I_{in} d_{21} \\ I_{in} d_{34} \\ -I_{in} d_9 \end{bmatrix} \quad (27)$$

$$d_{35} = \left[b_4 - \frac{d_{33}b_3}{d_{32}} \right], d_{36} = \left[\frac{d_{34}b_3}{d_{32}} + b_1 \right] \quad (28)$$

$$d_{37} = \left[d_8 - \frac{d_{33}d_7}{d_{32}} \right], d_{38} = \left[\frac{d_{34}d_7}{d_{32}} + d_9 \right] \quad (29)$$

The variable V_5 of the first row and the sixth row can be eliminated from the fifth column. Thus, the last function to be written is $V_6 = f(I_{in}) = -I_{in} \left(\frac{d_{38}}{d_{37}} \right)$. This function

can be used to eliminate the V_6 variable so that the ratio of input impedance from the first row equation can be determined as

$$\begin{bmatrix} -b_2 & 0 & 0 & 0 & 0 & d_{35} \\ 0 & -b_6 & 0 & 0 & d_{26} & d_{27} \\ 0 & 0 & -b_8 & 0 & d_{29} & d_{30} \\ 0 & 0 & 0 & d_{18} & d_{19} & d_{20} \\ 0 & 0 & 0 & 0 & d_{32} & d_{33} \\ 0 & 0 & 0 & 0 & 0 & d_{37} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} -I_{in}d_{36} \\ I_{in}d_{28} \\ I_{in}d_{31} \\ -I_{in}d_{21} \\ I_{in}d_{34} \\ -I_{in}d_{38} \end{bmatrix} \quad (30)$$

The closed form equation of the input impedance can be derived as following

$$Z_{in} = \frac{V_1}{I_{in}} = \left[d_{36} - \frac{d_{38}d_{35}}{d_{37}} \right] \quad (31)$$

After closed form equation is finished. The polynomial form can be derived by considering the intermediate coefficients which have only 38 variables.. The last equation can be written in a polynomial which is suitable to define in MATLAB. It is shown below.

[illegible]

[illegible]

This equation is very high order polynomial form with order very close to 200. It is very difficult for the reader to understand or recognize the definition of this equation without the detail report for the process of derivation of this equation which has very laborious detail definition of the principle of the symbolic ratio determination and all of the novel coefficients (approximately 350 pages).

Table1 DC Operating Point Experimental Results
Of the Regulated Cascode amplifier

R_{11}	V_{R11}	V_{OUT}	V_{GS,M_2}	V_{D,M_3}	V_{DS,M_1}
46 $k\Omega$	308 mV	6.23 V	93 mV	5.85 V	
100 $k\Omega$	1.89 V	6.08 V	84 mVac	2.23 V	78 mVac
220 $k\Omega$	1.00V	6.08 V	0.20Vac	4.87 V	196mVac
430 $k\Omega$	1.36V	6.08 V	0.15Vac	4.58 V	68 mVac
510 $k\Omega$	1.67 V	6.08 V	0.16 Vac	4.48 V	58mVac
681 $k\Omega$	2.05 V	6.08 V	87 mVac	4.14 V	61 mVac
910 $k\Omega$	1.961 V	6.08 V	0.18 Vac	3.89 V	77mVac

V The Input Impedance graph of the Regulated Cascode Cross Coupled Power Amplifier

The input impedance graph of the Regulated cascode cross coupled power amplifier can be simulated and plotted from MATLAB and SciLab as a result of substitution of the numerical value of the MOSFET transistor level1 0.5 micron , 0.18 micron, respectively. There are the figures which can be explained as follows. The first figure is the graph which is simulated by assuming that a resonance circuit has four values of capacitor and inductor which can be listed as 1 nanohenry and 1 nanofarad, 100 picohenry and 100 picofarad, 10 picohenry and 10 picofarad, 1 picohenry and 1 picofarad. The current consumption of the transistor are designed to have a constant value at a one microampere in the program. After that, the dc bias which are a serie resistors are designed from the value of the resistor and gate source voltage drop of the transistors. The graph of the first figure can be seen as a ramp function which means its input impedance is risen as a function of the input frequency approximately 1000 dB per decade.

The second figure is the graph which is simulated by assuming four values of the drain current at 1 microampere, 100 microampere, 1 milliampere and 10 milliampere. The aspect ratio of all of the transistors in the circuit diagram are designed from the level1 drain current equation. The gated source voltage drop of the transistor are designed to have a value very close to the supply voltage which is 3 volt because there are approximately no voltage drop across the resonance circuit from experiment as a result of the short circuit of the dc current supply according to the traditional

property which can be written as $V_L = L \frac{dI_L}{dt}$.

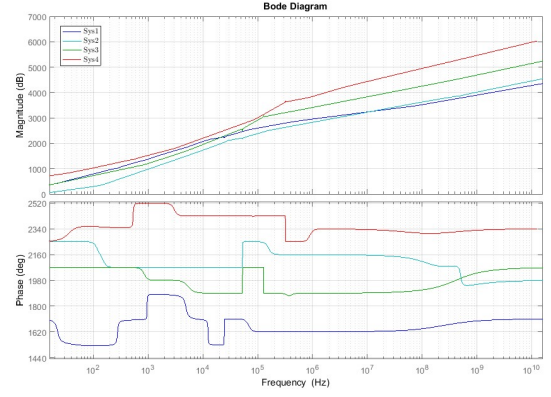


Fig. 3 Simulation results of the input impedance of the Regulated Cascode Cross Coupled Power Amplifier

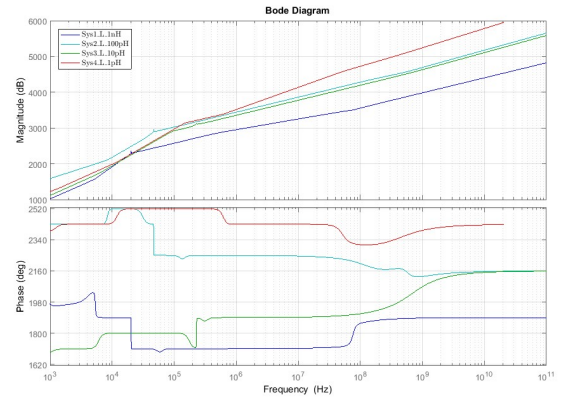


Fig. 4 Simulation results of the input impedance of the Regulated Cascode Cross Coupled Power Amplifier

VI A Design of a dc operating point of the Regulated Cascode Amplifier

The DC operating point design is usually an iterative design process because there are more variables than the equations. These design equation are written from KCL and KVL of a large signal drain current. Typical dc operating points are shown in the Table1. DC operating points are changed as a function of the resistor R_{11} . From measurement, the resonance circuit do not have voltage drop as a result of derivative of current of the supply voltage which should be zero if the battery has no ripple voltage. Thus, the input voltage bias of the second stage regulated cascode amplifier is not half of the supply voltage but it has approximately equal to the supply voltage of the battery.

VII Experimental Results of the time domain waveform of the RGC cross coupled power amplifier

The oscilloscope is used to measure 1MHz of input frequency and output of the RGC cross coupled power amplifier. It can be seen from figure (5a) that it is a self-modulated waveform as a results of two active inductors which is a connection of the output of the cascade of common source amplifier (M_3 and M_6) which is the input of

the additional common source amplifier of the transistor (M_2 and M_5). It can be seen from the figure (5c) that , the output signal can be seen

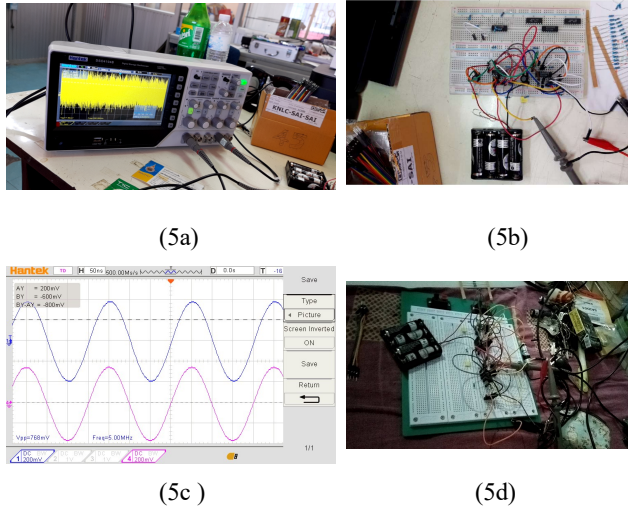


Fig. 5 Experimental Results of the RGC cross coupled power amplifier

(a) Input frequency 1MHz , input amplitude 100mV

(b) The breadboard of the RGC cross coupled power amplifier with wire connection with ALD transistor array

(c) Input frequency 5MHz, input amplitude 1.0V

(d) The breadboard of the RGC cross coupled power amplifier with wire connection with ALD transistor array

VIII Conclusion

The principles of eliminate column variable is clearly described. It is used to derive the ratio of input impedance of the regulated cascode cross couple power amplifier. The matrix coefficient update are used to show what is happened after the coefficients are grouped and defined many times so that it is easy to see which are the coefficient that can be eliminated in the next column. The column variable in the column matrix is left only one variable per column. The experimental result of a transistor array from ALD (ALD210802) is used to illustrate the difficulty to make a regulated transistor operating in the saturation region because of a drain to source voltage of the input transistor is too low. The input transistor is operating in the triode region. MATLAB is used to execute the polynomial form of the input impedance after all of the coefficients are typed into the text file with the level1 drain current model. From the experimental results, the results are shown at the different dc operating points. The high frequency modulated wave is shown in figure 5(a). The output of the RGC cross coupled circuit is shown to have lower amplitude than the input voltage as a result of a higher input frequency.

REFERENCES

- [1] E. Sackinger, W. Guggenbuhl, "A High-Swing, High-Impedance MOS Cascode Circuit", IEEE Journal of Solid-State Circuits, Vol.25, No.1, February 1990, pp. 289-298
- [2] K. Bult, G. J. G. M. Geelen, "A Fast-settling CMOS Op Amp for SC Circuits with 90-dB DC Gain", IEEE Journal of Solid-State Circuits, No.25, No.6, December 1990, pp. 1379-1384
- [3] N. C Battersby and C. Toumazou, "A 5th order Bilinear Elliptic Switched-Current Filter", IEEE 1993 CICC, pp. 6.3.1- 6.3.4
- [4] T. Serrano, B. Linares-Barranco, "The Active-Input Regulated-Cascode Current Mirror", IEEE Transactions on Circuits and System I: Fundamental Theory and Applications, Vol.41, No.6, June 1994, pp. 464-467
- [5] A. H. Bratt, T. Olbrich and A.P. Dorey, "Class AB regulated cascode current memory cell", Electronics Letters, 27th October 1994, Vol.30, No.22, pp. 1821-1822
- [6] M. Goldenberg, R. Croman, T. S. Fiez, "Accurate SI Filters using RGC Integrators", IEEE Journal of Solid-State Circuits, Vol.11, November 1994, pp. 1388-1395
- [7] D. Flandre, A. Viviani, J-P Eggermont, B. Gentinne, P. G. A. Jespers, "Improved Synthesis of Gain-Boosted Regulated-Cascode CMOS Stages using Symbolic Analysis and gm/ID Methodology", IEEE Journal of Solid-State Circuits, Vol.32, No.7, July 1997, pp. 1006-1012
- [8] M. Das, "Improved Design Criteria of Gain-Boosted CMOS OTA with High-Speed Optimizations", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol.49, No.3, March 2002, pp. 204-207
- [9] S. M. Park, Hoi-Jun Yoo, "1.25 Gb/s Regulated Cascode CMOS Transimpedance Amplifier for Gigabit Ethernet Applications", IEEE Journal of Solid-State Circuits, Vol.39, No.1, January 2004, pp. 112-121
- [10] J. Nissinen, J. Kostamovaara, "Fully Differential, Regulated Cascode Amplifier", IEEE MELECON 2006, pp. 51-54
- [11] Y. Zheng, C. E. Saavedra, "Feedforward-Regulated Cascode OTA for Gigahertz Applications", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol.55, No.11, December 2008, pp. 3373-3382
- [12] P. Vajpayee, A. Shrivastava, S.S. Rajput, G.K. Sharma, "Wide Output Swing Inverter fed Modified Regulated Cascode Amplifier for Analog and Mixed Signal Applications", TENCON 2009, pp.1-4
- [13] S. Bashiri Amid, C. Plett, P. Schvan, "Fully Differential, 40 Gb/s Regulated Cascode Transimpedance Amplifier in 0.13 micron SiGe BiCMOS Technology", 2010, pp. 33-36
- [14] C. Li, S. Palermo, "A Low-Power 26 GHz Transformer Based Regulated Cascode SiGe BiCMOS Transimpedance Amplifier", IEEE Journal of Solid-State Circuits, Vol. 48, No.5, May 2013, pp. 1264-1275
- [15] K. Tripetch, "Comparative Analysis of Tuning Range of Regulated Cascode Cross Coupled CMOS Oscillator", Proceedings of the World Congress on Engineering 2013, Vol. II, WCE2013, July 3-5, 2013, London, U. K.
- [16] M H. Taghavi, L. Belostotski, James W. Haslett, P. Ahmadi, "10 Gb/s 0.13 micron CMOS Inductorless Modified-RGC Transimpedance Amplifier", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 62, No.8, August 2015, pp. 1971-1980
- [17] Oscar T.C. Chen, C-T Chan, Robin R-B Sheen, "Transimpedance Limit Exploration and Inductor-Less Bandwidth Extension for Designing Wideband Amplifiers", IEEE Transactions on Very Large Integration (VLSI) Systems, Vol.24, No.1, January 2016, pp. 348-352
- [18] G. Piccinni, G. Avitabile, G. Coviello, "A Novel Design Optimization Framework for Regulated Cascode Transimpedance Amplifiers", 2017
- [19] R. Costanzo, Steven M. Bowers, "A Current Reuse Regulated Cascode CMOS Transimpedance Amplifier with 11 GHz Bandwidth", IEEE Microwave and Wireless Components Letters, Vol. 28, No.9, September 2018, pp. 816-818
- [20] S. B. Song Lee, Hang Liu, X. Yu, Jer-Ming Chen, Kiat Seng Yeo, "An Inductorless 5 GHz Differential Dual Regulated Cross Cascode Transimpedance Amplifier using 40 nm CMOS", 2019
- [21] A. Kassem, I. Darwazeh, "A High Bandwidth Modified Regulated Cascode TIA for High Capacitance Photodiode in VLC", 2019