8.7 A 112Gb/s ADC-DSP-Based PAM-4 Transceiver for Long-Reach Applications with >40dB Channel Loss in 7nm FinFET

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Driven by the proliferation of rich media services and a drastic increase of data availability, the demand for high-speed data transfer in the data center continues to grow at greater than 26 percent year-over-year [1]. This urges the imminent solution of top-of-rack switches in hyperscale networks with faster I/O interfaces to simultaneously support both low power and high throughput. Supporting the substantial bandwidth increase has driven the development of new electrical and optical interconnect standards which enable 100Gb/s per channel including IEEE 802.3ck and CEI-112G with PAM-4 modulation in conjunction with forward error correction (FEC) [2]. For long-reach applications, a transceiver architecture with >40dB channel equalization is critical due to the extra 8-10dB package insertion loss. To resolve those bottlenecks, this work presents an ADC-DSP based PAM-4 transceiver capable of equalizing >41.5dB lossy channels and achieving 112Gb/s per channel and 896Gb/s overall retimer throughput in 7nm FinFET.

Figure 8.7.1 shows the 896Gb/s retimer architecture consisting of 16 transceiver lanes (8 TX+RX on the line-side interface and 8 TX+RX on the host-side interface). In the receiver (RX), the analog front end (AFE) includes the on-die termination (ODT), continuous time linear equalizer (CTLE), variable gain amplifier (VGA) and 8b 56GS/s self-calibrated analog-to-digital converter (ADC). The DSP engine consists of a Mueller-Muller timing recovery circuit driving the ADC to track data at the baud rate. To get the full advantage of the technology scaling, different digital equalization schemes are implemented to allow optimization under various channels. The chip supports three detection schemes, namely memoryless adaptive PAM slicer, decision-feedback equalizer and an innovative very low power maximum likelihood sequence estimation detector (MLSD) for long-reach performance without any noise penalty. The RX topology is depicted in Fig. 8.7.2. The input signal is first passed through the ODT followed by a 2-stage CTLE with 0-12.5dB adjustable peaking. Then the rate of the input signal is decimated by 64× through a two-step process. At the first step, the signal is interleaved via 16 track-and-hold (TAH) samplers with 4UI-pulse-width 16-phase clocks. Afterwards, a VGA with 0-6dB tunable gain adjusts the signal amplitude to an appropriate level for the subsequent 4-way 8b asynchronous SAR ADCs to form the second-step decimation. To relax capacitive DAC settling requirements, redundancy with radix 1.6 on the 3 MSBs is used in the capacitive DAC while the 5 LSBs are scaled with conventional binary weighting. Note that TAH timing and VGA gain mismatches among channels could potentially limit the overall link performance. Background calibration in the DSP engine compensates those mismatches over process, voltage and temperature (PVT) variation in real time.

Figure 8.7.3 shows the simplified single-ended ODT and CTLE. To support 112Gb/s PAM-4 signal, circuits with ~30GHz bandwidth are required. In addition, an integrated AC-coupling cap is often needed in wireline applications to minimize off-chip components and to increase port-density. The employed ODT topology consists of a bridged bandwidth-extension T-Coil with integrated AC-coupling C combo. A tunable termination resistor to achieve optimal 50Ω impedance matching. To retain critical low-frequency signal energy (down to ~200kHz), a large RC time constant relating to the AC-coupling structure is required. To optimize bandwidth & noise, a small C, large shunt-R in this bridged T-coil configuration is used. An additional series inductor isolates the input capacitance of the CTLE/VGA gain block. The DSP-controlled gain range of this block is from -10dB to 16dB. To compensate >40dB channel and package loss, the AFE needs to meet the stringent analog peaking specification of 12.5dB while maintaining ~30GHz bandwidth and low noise. As shown in Fig. 8.7.3, the CTLE is designed with a common-source amplifier with resistive and capacitive degeneration. Two CTLEs are separated by AC capacitors to ease common mode requirements. The corner frequency of the AC coupling structure between two stages of the CTLE is ~100KHz. A shunt-peaking inductor is leveraged to resonate out the parasitic & transistor gate capacitances. A flipped voltage follower buffer is used to isolate the CTLE from the 16 TAHs. The DC-gain normalized frequency response at the output of the AFE for various CTLE settings is shown in the Fig. 8.7.3.

Figure 8.7.4 shows the block diagram of the half-rate transmitter. With 4-tap FIR and 7-tap predistortion embedded, the DSP engine generates the pre-emphasized 64 parallel-streams of data into the 64:2 serializer, which is partitioned into multiple stages in order to achieve minimum power. Duty-cycle correction circuitry corrects the differential half-rate clocks driving the 2:1 serializer. A sub-UI bit-equalization technique is used inside the pre-driver and in the clock paths to minimize ISI and jitter-amplification. Within a chain of four inverters, the output of the final inverter is fed back to the output of the first inverter via a CMOS transmission gate. After the pre-driver, the output driver is a pseudo-differential 7b DAC that outputs $1.0V_{pp}$ swing from a 1.15V supply. The pseudo differential DAC architecture provides high output swing with good linearity and bandwidth. On-chip T-coils are used at the output to extend the bandwidth and reduce return loss. A bleeder is used to bias the output common mode, further improving the linearity of the DAC.

A common TX PLL is shared between two TXs, while each RX utilizes independent RX-PLL and CDR loop. The PLL is implemented with a phase/frequency detector followed by an offset charge pump, a loop filter, an LC-VCO and a delta-sigma dithered multi-modulus divider for fractional-N operation. In fractional-N mode, delta-sigma noise folding is avoided by operating the charge pump to force an offset between the reference and feedback clock. A complementary-Gm class-B LC-VCO, with dual-tail 2nd-harmonic resonance filters to reject up-conversion of flicker noise, operates at 26.5GHz with >12% tuning range over PVT.

With 42dB loss tolerance, the measured power per lane including digital DSP is 730mW. The return loss of the receiver is shown on Fig. 8.7.6. The front end of the receiver achieves >35dB SNDR (shown on Fig. 8.7.2) with the PLL contributing $<150fs_{rms}$ jitter. The performance of the digital MLSD is shown in Fig. 8.7.5. For this high-speed link, MLSD is key and provided >4dB channel equalization, or >2 orders of BER improvement with minimal power and no noise penalty. MLSD is a known detection technique that can provide better detection SNR for ISI channels [6]. The JTOL performance with additional 0.05UI RJ and 0.05UI BUJ meeting IEEE and CEI specifications is illustrated in Fig. 8.7.5. The TX eye diagram and SNDR performance over VT are shown in Fig. 8.7.5. With $>1.0V_{ppd}$ swing, the DAC achieves >40dB SNDR and >95% RLM. The overall link performance and comparison table is shown in Fig. 8.7.6. The transceiver meets IEEE 802.3ck and CEI-112G standards with 41.5dB loss at Nyquist (28G), over a temperature range from -40 to 85C. Figure 8.7.7 shows the chip micrograph for one lane.

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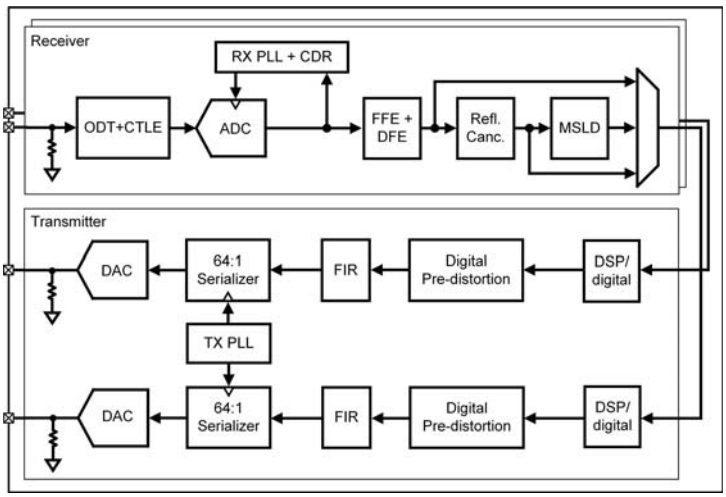

Figure 8.7.1: Block diagram of the 112Gb/s ADC-DSP-based PAM-4 transceiver.

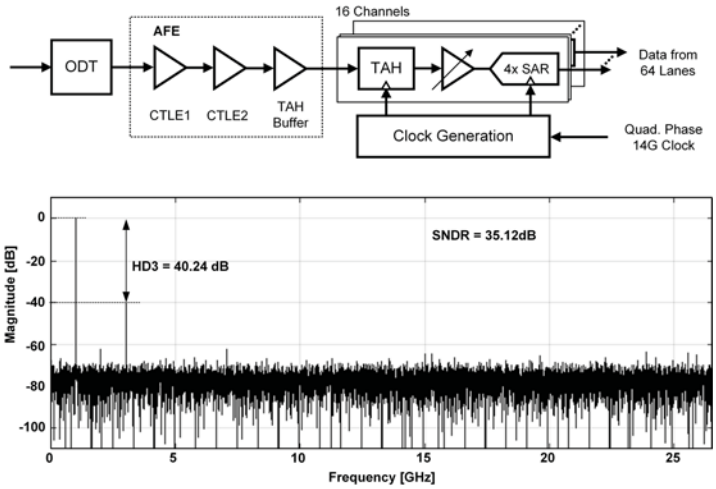

Figure 8.7.2: Block diagram of the RX architecture and AFE SNDR performance for a low speed sine signal.

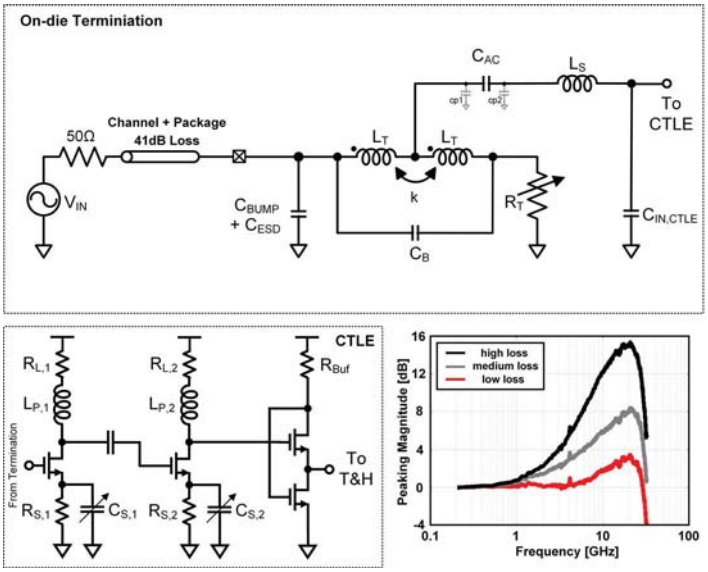

Figure 8.7.3: Simplified single-ended on-die termination and CTLE architecture with various CTLE peaking responses.

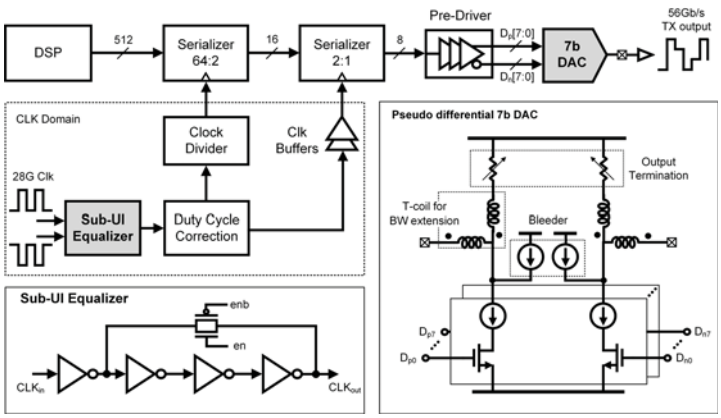

Figure 8.7.4: TX architecture with the implementation of pseudo-differential 7b DAC and sub-UI equalization technique.

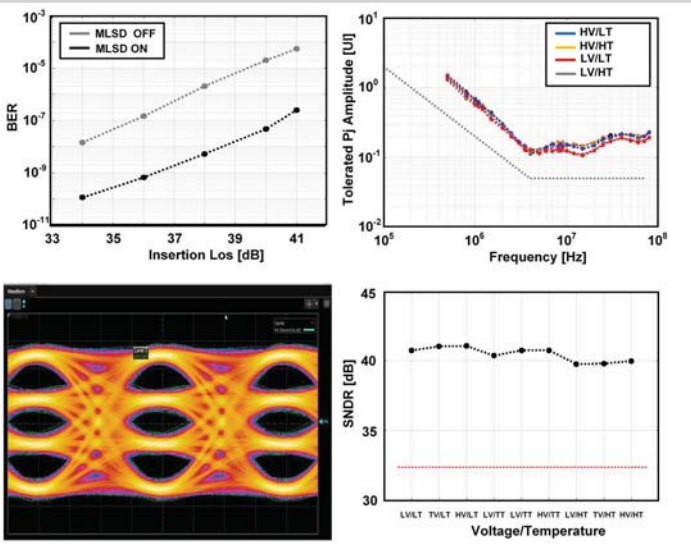

Figure 8.7.5: Measured MLSD performance, stressed receiver jitter tolerance, transmitter full-rate eye diagram with PRBS31 pattern, and TX SNDR measurements over voltage and temperature.

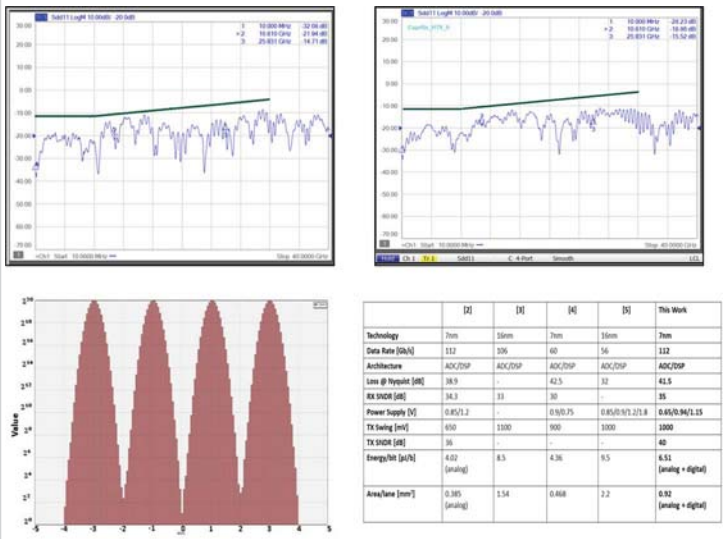

Figure 8.7.6: Measured receiver input return loss, transmitter output return loss, receiver recovered signal histogram (pre-FEC) and the comparison table.

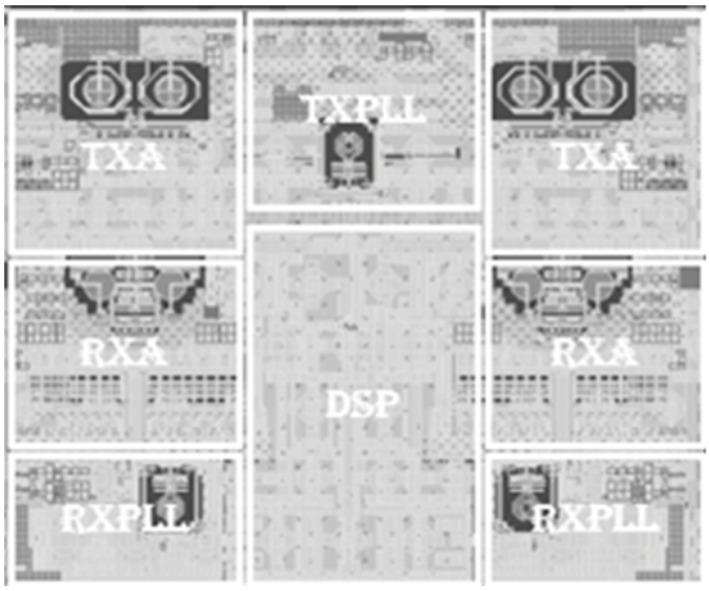

Figure 8.7.7: Chip micrograph.

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