6.1 A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation

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The emergence of cloud computing, machine learning, and artificial intelligence is gradually saturating network workloads, necessitating rapid growth in datacenter bandwidth, which approximately doubles every 3-4 years. New electrical interfaces that demand dramatic increases in SerDes transceiver speed are being developed to support this. This paper presents a power-efficient 224Gb/s-PAM-4 ADC-based receiver in a 5nm CMOS process that targets next generation Ethernet for chip-to-module applications, envisioned to be the first use-case scenario at this data-rate. Doubling the data-rate from the current IEEE 802.3ck and OIF standards at 112Gb/s, while keeping the same modulation – which is desirable for maintaining backward compatibility with 112/56Gb/s electrical and optical PAM-4 standards – requires doubling the bandwidth and lowering both the clock jitter and circuit noise by a factor of two. These new constraints are met by using 1) a hybrid continuous-time linear equalizer (CTLE) incorporating both inductive peaking and source-degeneration [1], 2) heavy bandwidth extension topologies employing several types of inductive peaking, 3) a low-power interleaved ADC and 4) an inductive clock distribution network with jitter filtering.

The receiver architecture shown in Fig. 6.1.1 consists of the analog front-end (AFE), ADC front-end (ADC-FE), a 64-way time-interleaved SAR ADC, LC-DCO-based CDR, and digital equalizer. The input matching network in the AFE feeds the received signal into the CTLE followed by two variable-gain-amplifier (VGA) stages. The VGA drives the ADC-FE that uses four wide-band pre-buffers to interleave the incoming data by 16× using a track-and-hold (T/H) clocked at 7GHz to generate the effective 112GS/s sampling rate. Each of these 16 interleaved channels is amplified by a post-amplifier feeding four SAR sub-ADCs with 6b resolution operating at 1.75GHz. The ADC output is then equalized by a 16-tap digital FFE. A CDR system based on an LC-DCO uses fully digital Mueller-Muller baud-rate phase detectors from the 16 T/H paths sampled from either the ADC or the digital FFE outputs. The 16 sampling clocks for the T/H are generated using phase interpolators (PIs) with inputs derived from the DCO.

The AFE (Fig. 6.1.2) is composed of a passive input network, CTLE (ST1) and two VGAs (ST2, ST3). The input network provides broadband impedance matching, ESD protection, and is AC-coupled to ST1 using an on-die capacitor for DC isolation. As shown in Fig. 6.1.2, ST1 uses a hybrid architecture for the CTLE, with inductive peaking and source degeneration to shape its frequency response. Unlike classic CTLE implementations, the role of the degeneration capacitance (Cd) is to control the mid-frequency slope of the transfer function, while the 53GHz high-frequency peaking is provided by the shunt inductor. As shown in the simulated results in Fig. 6.1.2, controlling Cd allows the CTLE response to better match the channel slope that it is equalizing, thereby reducing over- or under-equalization throughout the entire pass-band with a single stage. The AFE is targeted to support up to 25dB boost and 20dB gain at the Nyquist frequency. The VGA is a two-stage design with tapered gain scaling, with the load resistor calibrated to achieve a desired resistance value across process variations. To achieve a 3dB bandwidth in excess of 70GHz, series-shunt inductive peaking is used in the VGA to realize a bandwidth extension ratio of 2.5×. The inductor network was optimized to achieve minimal pass-band ripple in the frequency response. To ensure proper common-mode operation, a low-impedance buffer is connected to the central tap of each load resistor, which provides improved wide-band CMRR/PSRR.

The ADC-FE pre-buffer circuit is similar to AFE ST2 depicted in Fig. 6.1.2. The pre-buffer isolates first-rank T/H (TH1) switches from the input and from other TH1 switches that are in track mode. For this purpose, TH1 switches are divided into 4 groups of 4 switches, each driven by a single pre-buffer. TH1 clocking ensures that within any of the 4 groups of TH1 switches, only 1 switch will be tracking at a time. The clock system (clkgen), depicted as part of the overall ADC in Fig. 6.1.1, generates sixteen 7GHz clocks for TH1 and sixty-four 1.75GHz clocks for second-rank T/H (TH2). It consists of an LC-DCO, dividers, 16 PIs, combinational logic to generate 1UI-spaced 25% duty-cycle TH1 clocks, and a shift-register-based clock divider to generate TH2 clocks. The clock system is locked by a CDR that detects the digital phases at the ADC or digital FFE output and controls the DCO and the PIs to correct the required phase.

As depicted in Fig. 6.1.1, the 14GHz DCO output is fed into an I/Q divider to generate 4 quadrature phases with 50% duty-cycle, which drive a set of 16 CMOS PIs to generate the 16 1UI-separated clocks for TH1. The divider supports divide-by-2,4 and 8 ratios to enable operation at 112, 56 and 28Gb/s providing backward compatibility with existing OIF and Ethernet rates. By applying analog voltages to the enable controls of a single slice of the CMOS PI at a time, the required resolution of ~100fs for TH1 is achieved. Due to the high capacitive load of the PIs, achieving low jitter (Rj<100fs) with low power is a challenge. A series-shunt inductive peaking technique is used for the driver of the PIs to both provide higher swings at the PI inputs, and filter up to 40% of the DCO and divider jitter. Also depicted in Fig. 6.1.1 is the combinational logic used to create the 25% duty-cycle for TH1 clock and the 50% duty-cycle TH2 master clock from the 50% duty-cycle PI clock. The TH2 master clock is divided by 4 to generate each SAR TH2 clock. To meet timing margins across different clock frequencies, a clock mux with 4UI range is used to tune the delay between TH1 and TH2. Additional duty-cycle control is used to increase the pulse width of TH2 clock, giving TH2 more time to settle.

As shown in Fig. 6.1.3, the TH1 switch is implemented by a PMOS switch. To achieve 56GHz sampling BW, the time constant of the switch is compensated by the inductive peaking of the pre-buffer which drives it, and the rising slopes of the sampling clock (clkb) are maximized. The sampled TH1 output voltage is buffered and amplified by the post-amplifier that drives the group of 4 SARs through TH2 switch during track mode. The post-amplifier has two stages. The first gain stage has a programmable load to enable gain calibration and utilizes cascode devices for improved reverse isolation. The second stage is a semi-differential source follower capable of driving the SAR's input capacitance. The source follower is a combination of a flipped voltage follower (FVF) and a super source follower (SSF) to maximize speed while using less current.

A 1.75Gs/s sub-ADC is implemented for the 64-way time-interleaved ADC with an overall sampling rate of 112GS/s. To achieve this high sampling rate with low power and area, a loop-unrolled (LU) SAR ADC is used (Fig. 6.1.4) with a unique comparator for each bit. Each comparator triggers the next one once its decision is completed. Unlike commonly used LU ADCs, the presented topology does not assert a comparator reset during SAR conversion. As each comparator holds its decision, this topology eliminates the need for a memory unit between comparator and CDAC and therefore reduces power, delay, and complexity. However, the lack of comparator reset creates an input common-mode voltage drift due to comparator kickback. This common-mode voltage drift is minimized by using a single-ended CDAC. To ensure proper common-mode for comparators offset calibration, the CDAC must be updated during calibration similar to normal operation.

Figure 6.1.7 shows a die photo of the receiver that is manufactured in a 5nm process with an area of 0.3397mm^2 and 430µm width to minimize die edge usage. An arbitrary waveform generator (Keysight M8199A AWG) was used to generate the 224Gb/s PRBS-13 (due to memory limitation of the AWG) PAM-4 input signal with a 4-tap TX-FFE emulation. The signal was routed through a channel comprised of cables, connectors, ISI board, PCB and package with 31.6dB total attenuation at 56GHz (Fig. 6.1.5). The 64K PAM-4 symbols were captured to produce the sample plots and histograms shown in Fig. 6.1.5. The BER of 1.0E-6 was measured using back-to-back data captures. Additionally, the AFE and ADC frequency responses were extracted using a sine-wave generator, measuring a peak gain of 18dB at a frequency of 53GHz, as shown in Fig 6.1.5.

Total analog receiver power is 315.2mW, corresponding to 1.41pJ/b. The breakdown of analog receiver power, which excludes digital signal processing, is shown in Fig. 6.1.5. Note that the AFE, which significantly amplifies and equalizes the signal, consumes only 14% of the power. The results of the presented receiver are summarized in Fig. 6.1.6 and compared against recent 112Gb/s ADC-based receivers. The measured results meet the aggressive bandwidth, jitter and equalization requirements for 224Gb/s signaling. The energy efficiency is better than prior 112Gb/s PAM-4 references with similar receiver equalization boost and resolution, and the area is comparable to 112Gb/s references.

Acknowledgement:
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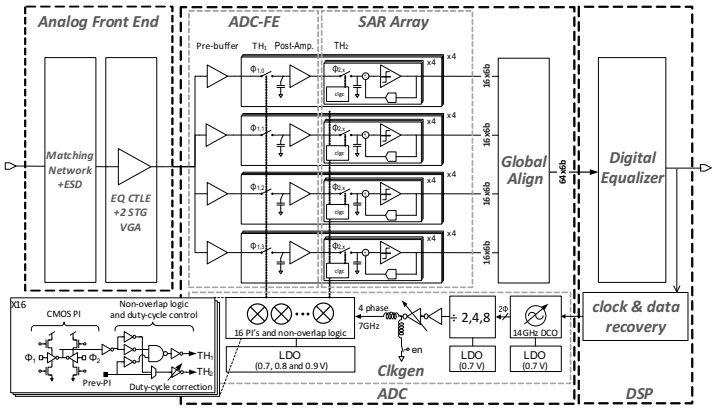

Figure 6.1.1: Receiver block diagram.

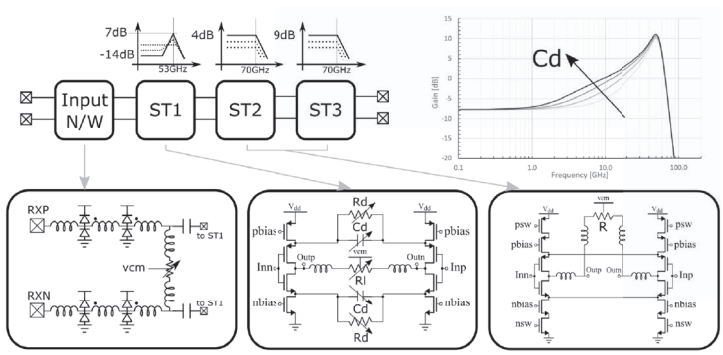

Figure 6.1.2: AFE block diagram including input network, CTLE ST1, VGA ST2,3 and simulated hybrid CTLE transfer function.

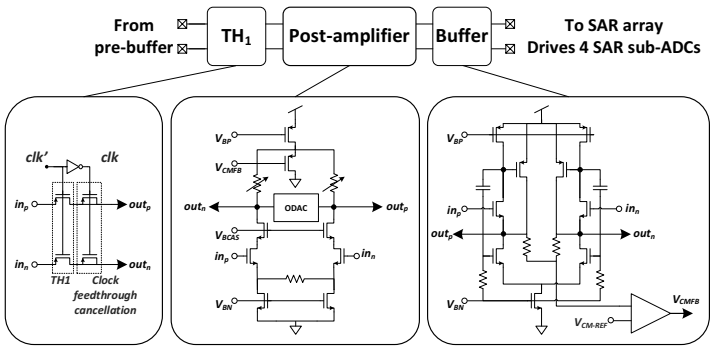

Figure 6.1.3: ADC-FE TH1 and its post-amplifier.

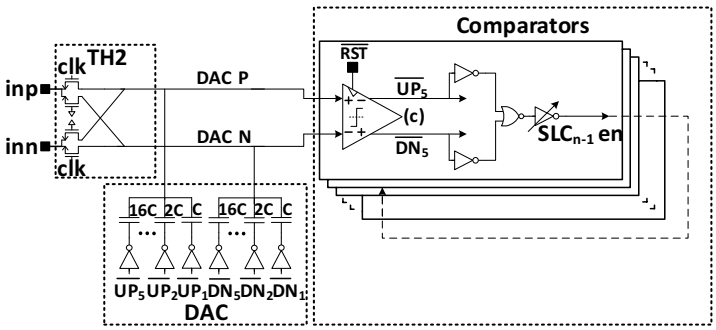

Figure 6.1.4: Loop-unrolled SAR ADC unit.

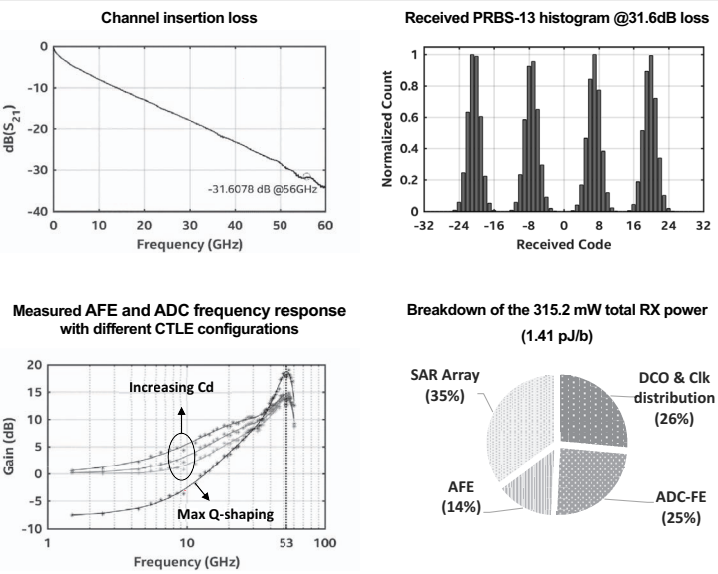

Figure 6.1.5: Receiver measured results: measured channel, AFE and ADC frequency response, receiver histogram and power break down.

	SSC-L'20 [3]	JSSC'21 [4]	ISSCC'20 [5]	JSSC'20 [6]	This work
Data rate	112Gb/s	112Gb/s	112Gb/s	112Gb/s	224Gb/s
Technology	CMOS 7nm	CMOS 7nm	CMOS 7nm	CMOS 10nm	CMOS 5nm
Power Supply	0.88,1.2,1.5 V	1.0, 1.2 V	0.88,1.2.1.5 V	0.9,1.5 V	0.9,1.5 V
Receiver Power Efficiency*	5.1pJ/b	3.18pJ/b	3.6pJ/b	4.2pJ/b	1.41pJ/b
Channel loss @ Nyquist	33dB	36dB	37.5dB	35dB	31.6dB
BER	1.00E-06	1.00E-06	1.00E-06	1.00E-06	1.00E-06
Area mm²*	0.383	0.293	0.265	0.281	0.34

*Excluding DSP

Figure 6.1.6: RX performance comparison.

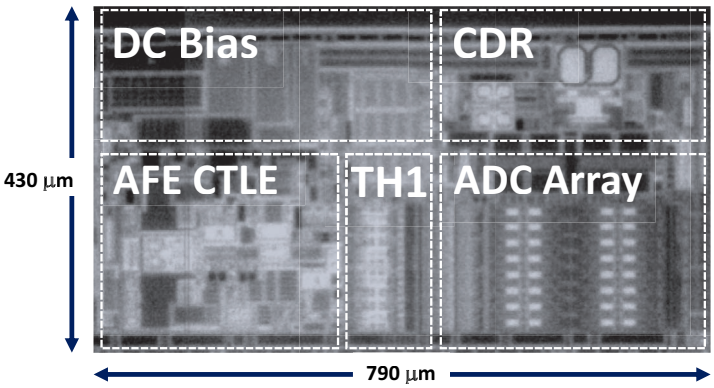

Figure 6.1.7: Die micrograph.

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