A 56-Gb/s PAM4 Receiver Analog Front-End With Fixed Peaking Frequency and Bandwidth in 40-nm CMOS

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***Abstract*—This paper discusses a 56-Gb/s PAM4 receiver analog-front end (AFE) implemented in TSMC 40-nm CMOS process. The system consists of a differential 100-Ω termination, a two-stage continuous-time linear equalizer (CTLE), a variable gain amplifier (VGA), and an output buffer. The source-degenerated transconductance stage and inverter-based transimpedance (TIA) with source follower structure are adopted for both CTLE and VGA. The utilization of source follower can solve the harsh DC operation problem in conventional inverter-based TIA and extend the bandwidth. By altering the source-degenerated resistors and capacitors in the two-stage CTLE, the proposed AFE can reach fixed peaking frequency with 9-dB compensation range at high frequency. Moreover, it can also achieve a fixed bandwidth at 14 GHz and 9.5-dB DC gain tuning range when altering the feedback resistors and negative capacitance compensation network (NCC) in VGA. Measurement results demonstrate that: it can compensate for 7.3-dB channel loss at 14-GHz Nyquist frequency and open the closed eye for 56-Gb/s PAM4 signal with BER $< 10^{-8}$ from $2^{15} - 1$ PRBS input. The core of the AFE occupies 0.32-mm^2 area and consumes 30-mW power from 1.1/1.2-V supply.**

***Index Terms*—Analog front-end, CTLE, PAM4, receiver, source follower, TIA, VGA.**

I. Introduction

With the rapid growth in the data center traffic, the demand for the SerDes with higher bandwidth shows the necessity to develop high-speed data communications [1]–[3]. To satisfy this demand and improve the utilization of bandwidth as much as possible, the latest standard IEEE802.3bs with 4-level pulse amplitude modulation (PAM4) signaling is proposed. By using PAM4 signaling to replace the non-return-to-zero (NRZ) signaling, the data rate can be doubled without expending the bandwidth.

Receivers with equalization capabilities are used to solve problems caused by channel loss, such as inter-symbol interference (ISI). More specifically, a high-performance PAM4 receiver has many challenges including low power consumption, small area, low bit error rate (BER), and enough equalization. In receiver analog front-end (AFE), equalizers like decision feedback equalizer (DFE) and continuous-time linear equalizer (CTLE) are used extensively [4]–[8]. Compared to CTLE, normally DFE consumes more power than CTLE in high-speed applications. Moreover, with the data rate increases, CTLE-based active copper cable (ACC) technology has been used in data centers [9]. In the ACC application, it is necessary to give different equalizations at the same frequency according to different cable lengths. However, the peaking frequency of the conventional AFE would be changed when altering the boosting range and the gain, resulting in a deterioration in signal quality. Therefore, the AFE with fixed peaking frequency and constant bandwidth is desirable for these applications.

The architecture presented in [1] is widely used in high-speed AFEs. However, there is a trade-off between the DC operating point and the circuit performance in this conventional gm-transimpedance (TIA) structure. To obtain a suitable DC operating point, the dimension of the PMOS needs to be increased. This will introduce a large parasitic capacitance at the output nodes of the gm-cell and reduce the bandwidth of the circuit. To solve this problem, source follower (SF) stages are used in the proposed AFE.

This paper is organized as follows. The system architecture of the proposed AFE is described in Section II. Section III presents and analyzes the measurement results. Section IV draws the conclusion.

II. AFE Architecture

The AFE architecture is illustrated in Fig. 1, incorporating a differential 100-Ω termination, a two-stage CTLE, a variable gain amplifier (VGA), and an output buffer. The 100-Ω resistor is adopted to match the circuit's differential input with the equipment. Both the CTLE and the VGA adopt the gm-TIA topology, compensating for the channel loss at 14-GHz Nyquist frequency and adjusting the output amplitude without bandwidth deterioration, respectively. The output buffer

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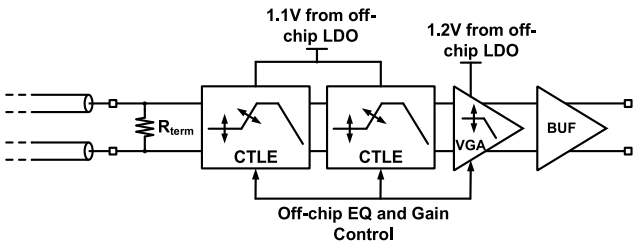


Fig. 1. AFE architecture.

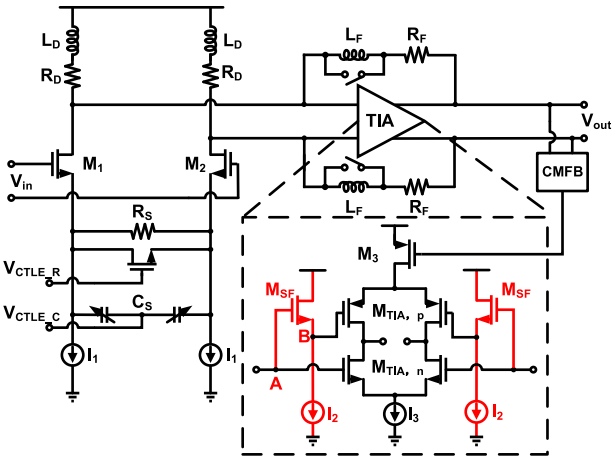


Fig. 2. Schematic of the proposed single stage CTLE.

with current mode logic (CML) topology is utilized to provide adequate output swings.

A. Continuous-Time Linear Equalizer

Fig. 2 depicts a single-stage CTLE, which consists of a gm stage and a TIA stage. The shunt peaking inductor in gm-cell and the series feedback inductor in TIA are adopted to extend the bandwidth. As the first block of AFE, the utilization of source-degenerated gm-cell can relax the input signal amplitude by manually/automatically tuning, achieving good linearity. As discussed in Section I, the SF M_{SF} in Fig. 2 is used to lower down the gate voltage of PMOS, reduce the size, enlarge the effective g_m, and broaden the bandwidth. By using the current source I_2 with a smaller W/L ratio, the gain $A_{v,SF}$ is closer to 0 dB. However, this topology consumes more power than the conventional inverter-based TIA, for the SF stage needs enough current to get higher bandwidth. Otherwise, the signal at node B will be mismatched with the signal at node A, which will deteriorate the performance.

In a conventional CTLE, when increasing its equalization value by changing R_S or C_S, its peaking frequency would also move left forward, deteriorating the bandwidth performance. Therefore, it is important to decouple the equalization capability and the peaking frequency, i.e., the circuit bandwidth. In our proposed AFE, R_S and C_S in the two-stage are adjusted delicately at the same time to achieve a fixed peaking frequency.

The source degenerated gm-cell is chosen that the gain is degenerated through R_S, resulting in good linearity to the system. A zero can also be introduced through the combination of C_S and R_S. The shunt inductive peaking is utilized together

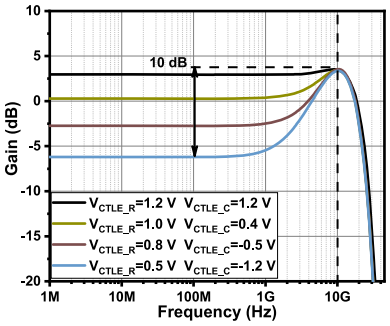


Fig. 3. Post-layout simulation results with CTLE enabled.

with the gm-cell to boost its output bandwidth by providing a simple zero and a quadratic pole. For the inverter-based TIA, an SF is utilized before the PMOS transistor in the inverter to shift down the PMOS gate voltage, increasing the $|V_{GS}|$ for larger PMOS transconductance.

The overall transconductance of the inverter-based TIA is equal to the parallel summation of the transconductances of NMOS and PMOS. As a result, this adoption of SF further boosts the transconductance and minimizes the RC constant at the output of gm-cell for larger bandwidth operation. Moreover, an inductor in series with the feedback resistor can also extend its peaking to higher frequencies. However, the inductance value needs to be taken into consideration to avoid the potential oscillation. The overall transfer function of one single stage is listed as follow:

$$A_{v,DC} = -\frac{g_m R_D\left(1 - g_{m,TIA}R_F\right)}{\left(1 + g_m R_s\right)\left(1 + g_{m,TIA}R_D\right)} \tag{1}$$

$$A_{v,AC} = A_{v,DC} \cdot \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\left(1+\frac{s}{\omega_{z3}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left[\left(\frac{s}{\omega_{n1}}\right)^2+\frac{2\zeta_1 s}{\omega_{n1}}+1\right]\left[\left(\frac{s}{\omega_{n2}}\right)^2+\frac{2\zeta_2 s}{\omega_{n2}}+1\right]} \tag{2}$$

where $\omega_{z1} = 1/(R_S C_S)$, $\omega_{z2} = 2\zeta_1\omega_{n1}$, $\omega_{z3} = (g_{m,TIA}R_F - 1)/(g_{m,TIA}L_F)$, $\omega_{p1} = (1 + g_m R_S/2)/(R_S C_S)$, $\omega_{n1} = \sqrt{(1 + g_{m,TIA}R_D)/(L_D C_{L1})}$, $\omega_{n2} = \sqrt{1/(L_F C_{L2})}$, $\zeta_1 = \frac{(R_D C_{L1} + g_{m,TIA}L_D)\sqrt{(1+g_{m,TIA}R_D)/L_D C_{L1}}}{2(1+g_{m,TIA}R_D)}$, $\zeta_2 = (R_F\sqrt{C_{L2}/L_F})/2$, C_{L1} and C_{L2} are the loading parasitic capacitors at the output nodes of gm-cell and TIA, respectively. When R_S is tuned to its minimum value to achieve the maximum DC gain and 0-dB equalization, C_S is tuned to its maximum value to compensate for the dominant pole and obtain a large bandwidth by providing a large $\omega_{z1} = 1/(R_S C_S)$. At this operation mode, the switch parallel with the L_F is off to avoid in-band sharp peaking caused by ω_{n2}. The DC gain, $A_{v,DC}$, decreases with larger R_S (according to eq. (1)), but the gain at high frequency determined by $A_{v,HF} = -\frac{g_m R_D(1-g_{m,TIA}R_F)}{(1+g_{m,TIA}R_D)}$ is nearly unchanged. This DC and high-frequency gain variation are used for channel loss compensation. However, the increasing R_S decreases ω_{p1} that causes the peaking frequency to move left forward. To achieve a fixed peaking frequency, C_S is minimized at the same time to maintain $\omega_{p1} = 1/(R_S C_S) + g_m/(2C_S)$ unchanged.

The proposed CTLE consists of two stages, and each stage is comprised of a source degenerated gm-cell with inductive peaking technique followed by an inverter-based TIA with switchable inductive feedback shown in Fig. 2. The first stage is responsible for low-frequency (LF) equalization. R_S

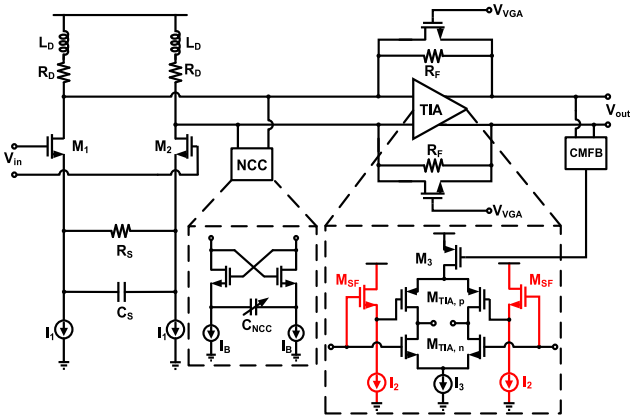
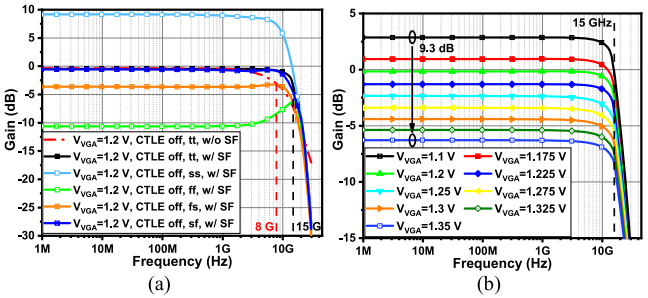


Fig. 4. Schematic of the proposed VGA.



(a) (b)

Fig. 5. (a) Post-layout simulated progressive AFE bandwidth enhancement and (b) gain-bandwidth decoupling with CTLE disabled.

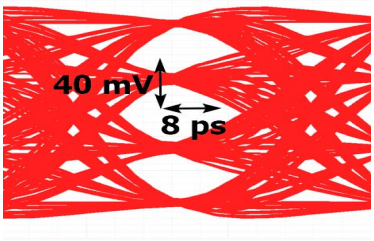


Fig. 6. Post-layout simulation eye diagram (differential).

in the first stage needs to be small, so that the difference between the DC gain $Gain_{DC} = \frac{g_m R_D}{1+(g_m R_S)/2}$ and the gain at LF $Gain_{LF} = g_m R_D$ is small, compensating for the small LF channel loss due to skin effect. Since R_S is small, the paralleled capacitor C_S needs to be large to generate zero at LF. R_S is parallel with a tunable CMOS resistor that can tune the source degenerated resistance. Furthermore, C_S is implemented by the CMOS varactor.

The second stage is adopted to compensate for the channel loss at Nyquist frequency, which is at high frequency (HF). Consequently, R_S in the gm-cell of the second stage needs to be a large value to distinguish the DC gain and HF gain. Moreover, its C_S needs to be smaller compared to C_S in the first stage. Besides CMOS varactors for C_S and parallel tunable CMOS resistors in gm-cell stages, the parallel switch is also implemented with the feedback inductor in both stages, to further enhance the peaking when it is on, or to ensure a flattened in-band performance when it is off. The fixed peaking frequency is realized by tuning the zeros and poles of the second-stage CTLE. While increasing R_S to degrade the DC gain and achieve a peak at high frequency, the first pole ω_{p1} would decrease, causing the peaking frequency to move left-forward. At the same time, L_F is switched on and C_S is minimized to enlarge ω_{n2} and increase ω_{p1} without changing the DC gain. By carefully controlling the positions of zeros and poles, the proposed CTLE can achieve a nearly fixed peaking frequency while altering the compensation range. In the future work, a fine DAC with the Look-up Table (LUT) will be used to achieve better tuning accuracy and system performance. Fig. 3 shows the post-layout simulation results of the proposed AFE by only tuning the two-stage CTLE, which successfully achieves an equalization range of 10 dB and a fixed peaking frequency of 10 GHz. The step size of DC gain is about 2.5 dB.

B. Variable Gain Amplifier

Fig. 4 depicts the core schematic of the proposed VGA. The source-degenerated gm-cell and the inverter-based TIA with SF are also adopted for both better linearity and higher bandwidth performance. For the transmission of PAM4 signals requires higher linearity, the source degeneration resistor R_S is used to increase the linearity of the circuit. The SF stages are introduced to increase the VGA bandwidth. By doing so, the bandwidth of overall AFE can be extended from 8 GHz to 15 GHz with CTLE disabled, shown in Fig. 5(a).

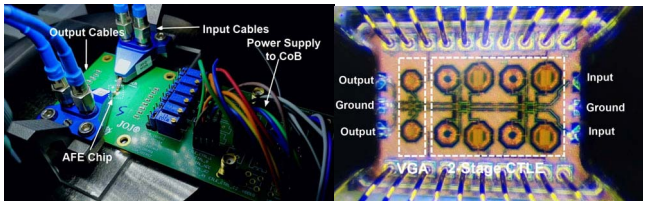
In the conventional design, the VGA gain tuning method is realized by altering R_S in the gm-cell block. However, even small parasitic capacitance at source-degenerated nodes could introduce an undesired peaking at high frequency, resulting in poor in-band flatness, and deteriorating the PAM4 eye diagram. Moreover, conventionally with the increase of VGA gain, its bandwidth will also decrease simultaneously.

In this work, the VGA gain tuning is realized by controlling the feedback resistors R_F of the inverter-based TIA, instead of R_S. By carefully design, the output common-mode voltage of the inverter-based TIA and gm-cell are both set to 650mV, so that only tiny current flows through R_F and the DC operating points will not change when R_F is changed. Besides, common-mode feedback loops at TIAs' outputs with on-chip voltage references are effective to ensure the stability of DC bias voltages.

As shown in Fig. 4, one negative capacitance compensation (NCC) network is applied to fine-tune the frequency response when bandwidth deterioration happens [13]–[15]. The overall transfer function of VGA can be written as:

$$A_{v,AC} = A_{v,DC} \cdot \frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left[\left(\frac{s}{\omega_n}\right)^2+\frac{2\zeta s}{\omega_n}+1\right)} \quad (3)$$

where $A_{v,DC}$ equals to (1), $\omega_{z1} = 1/(R_S C_S)$, $\omega_{z2} = 2\zeta\omega_n$, $\zeta = \frac{(R_D C_{EQ}+g_{m,TIA}L_D)\sqrt{(1+g_{m,TIA}R_D)/(L_D C_{EQ})}}{2(1+g_{m,TIA}R_D)}$, $\omega_{p1} = (1+g_m R_S/2)/(R_S C_S)$, $\omega_{p2} = \sqrt{g_{m,TIA}/(C_{EQ}C_{L2}R_F)}$, $\omega_n = \sqrt{(1+g_{m,TIA}R_D)/(L_D C_{EQ})}$, C_{EQ} is the equivalent loading capacitance after compensation by the NCC network and C_{L2} is the loading parasitic capacitor at the output node of TIA. This transfer function contains two high-frequency poles ω_n and ω_{p1}, and one dominant pole ω_{p2}. To increase the



(a) (b)

Fig. 7. (a) PCB for measurement and (b) microphotograph.

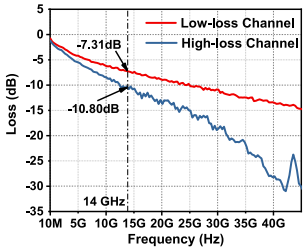
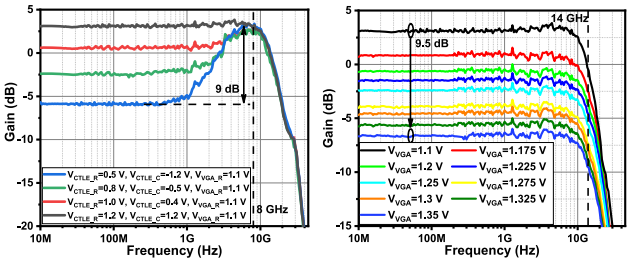


Fig. 8. Measured channel losses.



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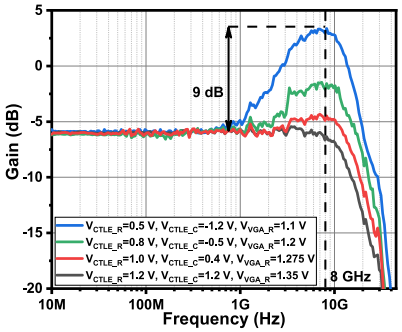

(c)

Fig. 9. Measured frequency response for AFE when (a) only tuning two-stage CTLE, (b) only tuning VGA, and (c) tuning CTLE and VGA simultaneously.

VGA gain, R_F should be larger. However, simply increasing the R_F would also cause the RC constant to be larger, therefore decreasing the VGA bandwidth unexpectedly. The NCC is used to reduce the C_{EQ} to keep the position of the dominant pole ω_{p2} unchanged. Therefore, the decoupling of gain and bandwidth is successfully realized. Post-layout simulation results of the overall AFE with CTLE disabled are shown in Fig. 5(b), which achieves a DC gain tuning range of 9.3 dB and a fixed bandwidth of 15 GHz. The step size of DC gain is about 1.2 dB. Fig. 6 shows the transient post-layout simulation result. Compared with the measured single-ended eye diagram, the simulated differential eye diagram has higher quality.

III. Measurement Results

The proposed AFE is fabricated in the TSMC 40-nm CMOS process. Fig. 7(a) and (b) show the designed evaluation PCB board and the chip microphotograph. The active area of the proposed AFE is 0.32 mm^2 and the total power consumption is 30 mW.

The Keysight N5247B PNA is adopted for the S-parameter measurement. The eye diagram and BER are measured with the Anritsu MP1900A BERT. To test the effectiveness of the CTLE performance, two lossy PCB channels are built. Fig. 8 shows the measured frequency responses of the low-loss channel and the high-loss channel, whose gain losses at 14-GHz Nyquist frequency are 7.3 dB and 10.8 dB, respectively.

Fig. 9(a) demonstrates that the measured CTLE can achieve a fixed peaking frequency at 8 GHz and a 9-dB compensation range by tuning R_S, C_S, and L_F in the second stage CTLE simultaneously, based on the tuning method presented in Section II. Fig. 9(b) shows the measured VGA frequency responses when CTLE is disabled. Fig. 9(c) shows the measured AFE frequency response when tuning CTLE and VGA simultaneously. It successfully demonstrates that the proposed AFE has a fixed peaking frequency.

Fig. 10 shows the measured 56-Gb/s PAM4 eye diagrams with these two different lossy channels. Fig. 10(a) shows

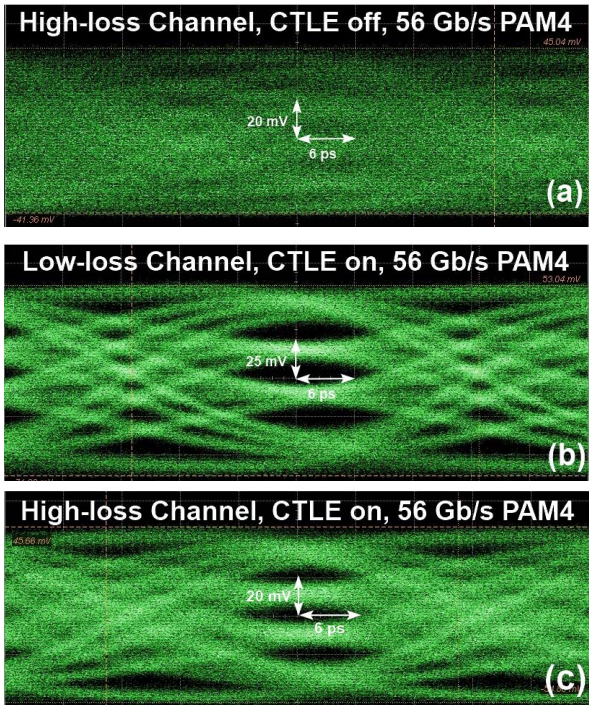

Fig. 10. Measured single-ended 56-Gb/s PAM4 eye diagrams.

that with the two-stage CTLE disabled, the output eye is closed. With CTLE enabled, the measured single-ended 56-Gb/s PAM4 eyes are opened, as shown in Fig. 10(b) and Fig. 10(c).

Fig. 11 shows the measured single-ended 28-Gb/s NRZ eye with equalization (eye diagrams are measured by single-ended due to equipment limitations). In this case, the measured RMS jitter is 1.64 ps. Measured BER bathtub curves across

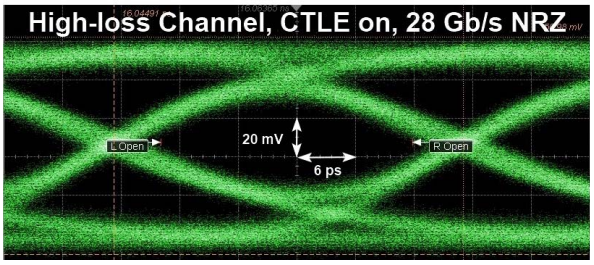

Fig. 11. Measured single-ended 28-Gb/s NRZ eye diagram with high-loss channel.

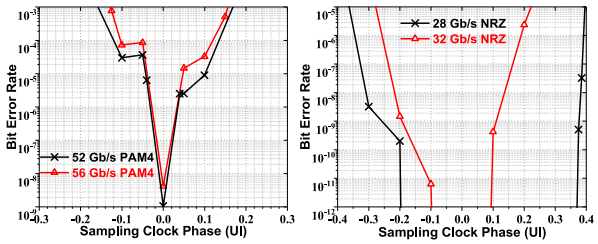

Fig. 12. Measured BER bathtub curves for 52-Gb/s PAM4, 56-Gb/s PAM4, 28-Gb/s NRZ and 32-Gb/s NRZ signals.

TABLE I
PERFORMANCE COMPARISON

	[10]	[11]	[12]	**This Work**
Technology	28-nm CMOS	40-nm CMOS	40-nm CMOS	**40-nm CMOS**
DR (Gb/s)	60	10/8	20	**56**
Data Format	PAM4	NRZ	NRZ	**PAM4**
Equalization	CTLE 2-Tap DFE	CTLE	CTLE	**2-Stage CTLE**
Fixed Peaking Point	No	No	No	**Yes**
Channel Loss (dB)	8.2@ 15 GHz	7.7/17.2@ 5 GHz/4 GHz	18.3@ 10 GHz	**7.3/10.8@ 14 GHz**
BER	PRBS-31 E−6[a] E−12[b]	PRBS-27 E−12	E−12	**PRBS-15 E−8**
Area (mm^2)	0.6705	0.014	/	**0.32**
Power (mW) (EQ/CDR)	66 (39/27)	10	12.8	**30**
Effic. (pJ/bit)[c]	0.65	1	0.64	**0.54**

[a]CTLE only; [b]CTLE + DFE; [c]Without CDR.

different input data rates (52-Gb/s PAM4, 56-Gb/s PAM4, 28-Gb/s NRZ and 32-Gb/s NRZ) are shown in Fig. 12. Although the eye quality can be further improved by optimizing the circuit, the proposed AFE can achieve BER $< 10^{-8}$ from the PRBS-15 data input. Moreover, the decoupling among DC gain, peaking frequency and bandwidth is successfully demonstrated.

Table I summarizes the key performance of the proposed AFE and its comparison with recent published AFEs. This work successfully achieves the fixed peaking frequency and bandwidth when tuning its equalization capability.

IV. CONCLUSION

The measured AFE can successfully compensate for −7.3-dB and −10.8-dB losses at 14 GHz and open the closed 56-Gb/s PAM4 eye with an excellent energy efficiency of 0.54 pJ/bit, BER $< 10^{-8}$. The gm-TIA topology with the source follower structure achieves higher bandwidth, and decouples the trade-offs among DC gain, peaking frequency, and bandwidth.

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