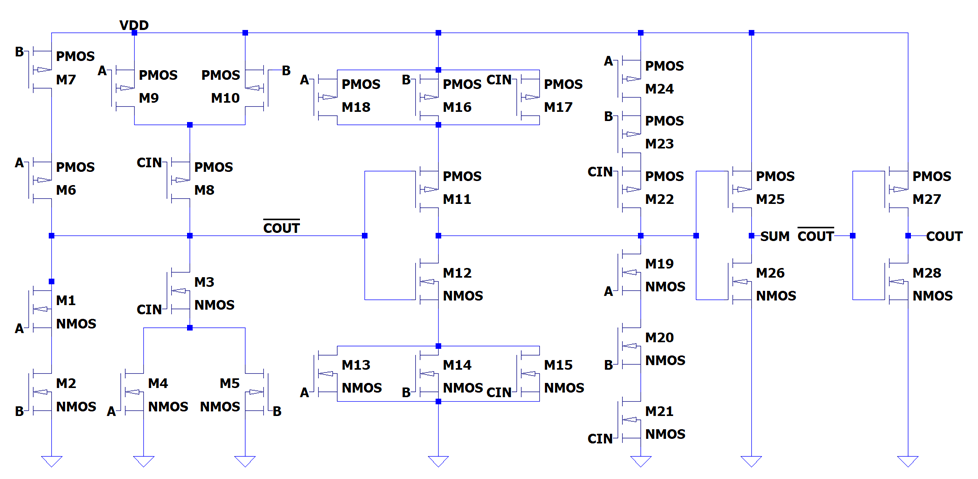
2022 NYCU EE VLSI Lab Report

Lab01 A CMOS Full Adder: Hspice Simulation

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1. **Summary of your Structure**
2. **picture**



1. **Design concept**

~COUT logic :

COUT = A·B + B·CIN + A·CIN

~COUT = ~( A·B + CIN·( A + B ) )

~SUM logic :

if COUT = 0 => (A, B, CIN) could be (1,0,0) or (0,0,0) (in any order)

Case (1,0,0) ~sum = 0 pull low with (A + B + CIN)

Case (0,0,0) ~sum = 1 pull high with (A’ · B’ · CIN’)

if COUT = 1=> (A, B, CIN) could be (1,1,0) or (1,1,1) (in any order)

Case (1,1,0) ~sum = 1 pull low with (A’ + B’ + CIN’)

Case (1,1,1) ~sum = 0 pull high with (A · B · CIN)

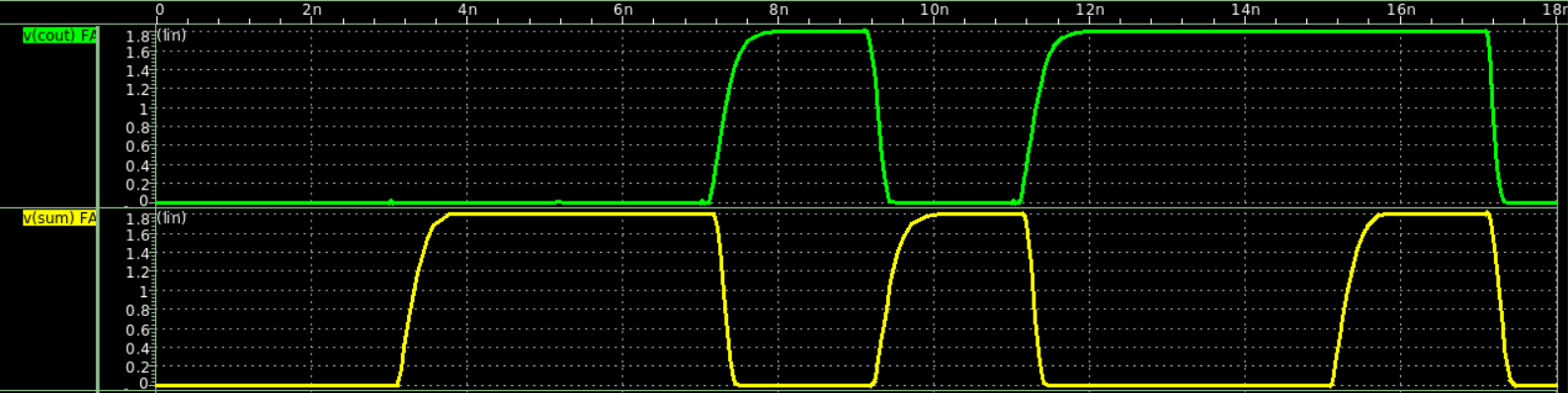
~SUM = ~( ~COUT · (A + B + CIN) + A · B · CIN )

Two inverters : turn ~COUT, ~SUM to COUT, SUM

1. **Output waveform**
2. **wp: 0.24**

**wn: 0.12**

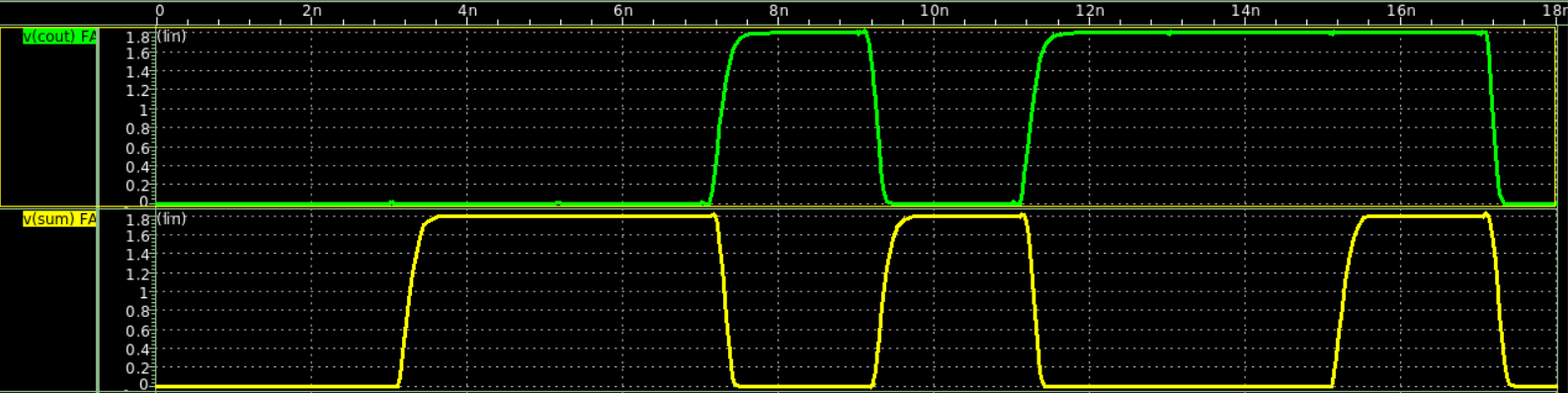
**Output load: 10f**



1. **wp: 0.36**

**wn: 0.18**

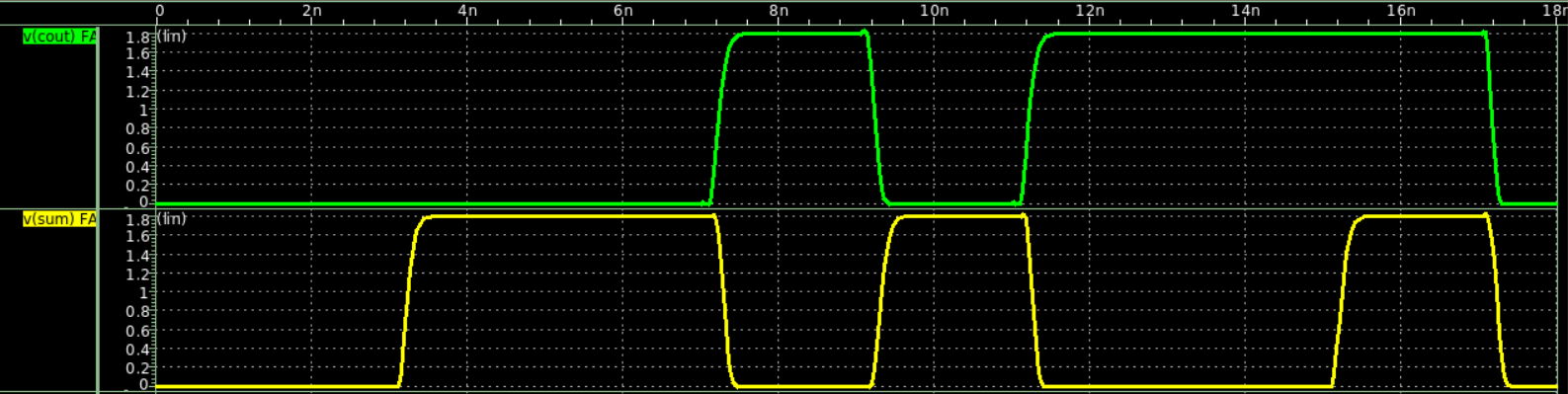
**Output load: 10f**



1. **wp: 0.48**

**wn: 0.24**

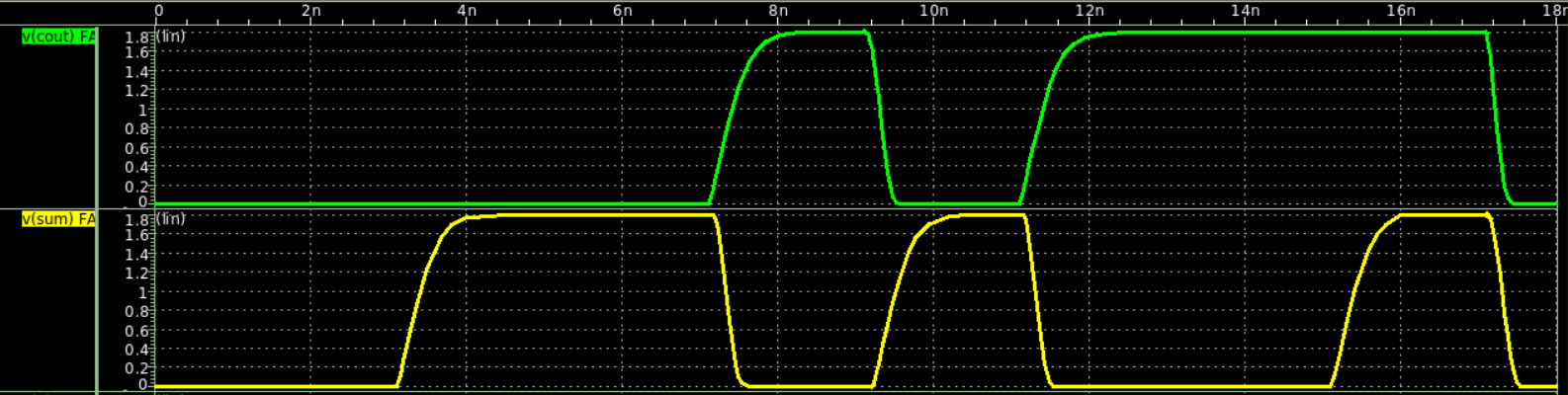
**Output load: 10f**



1. **wp: 0.24**

**wn: 0.12**

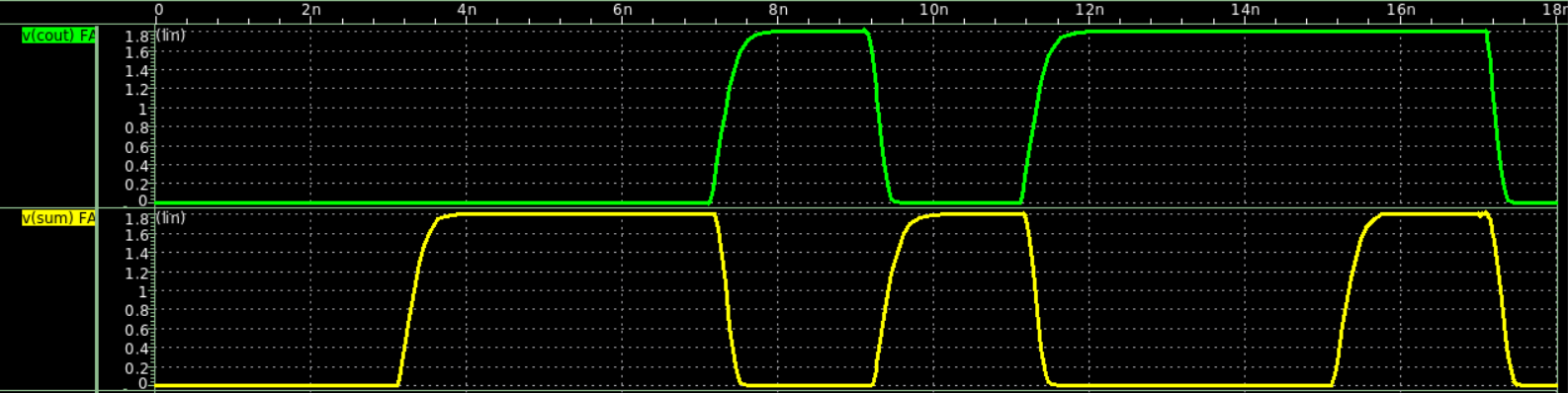
**Output load: 15f**



1. **wp: 0.36**

**wn: 0.18**

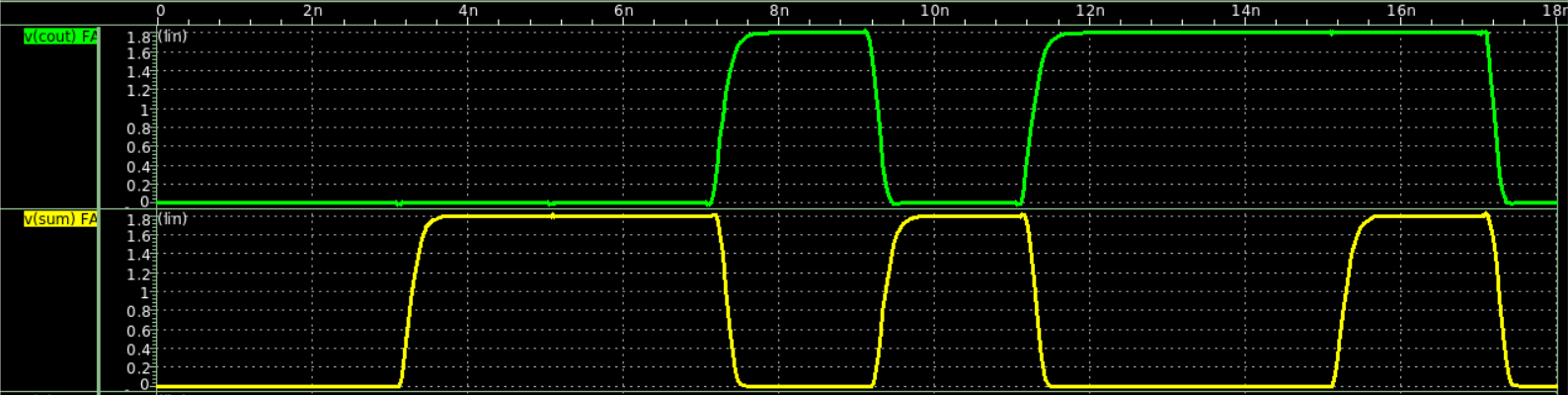
**Output load: 15f**



1. **wp: 0.48**

**wn: 0.24**

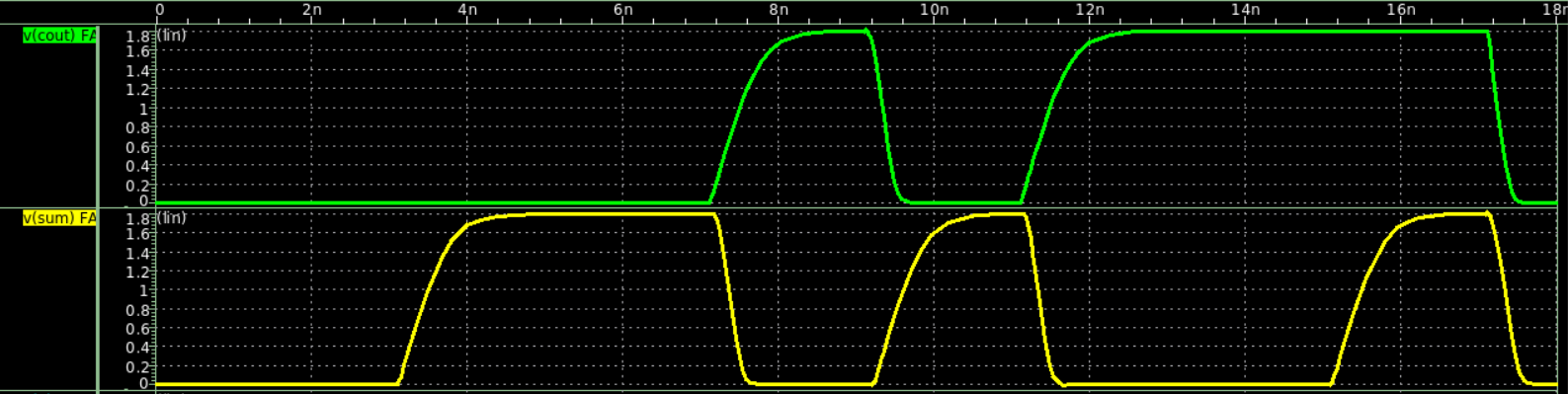
**Output load: 15f**



1. **wp: 0.24**

**wn: 0.12**

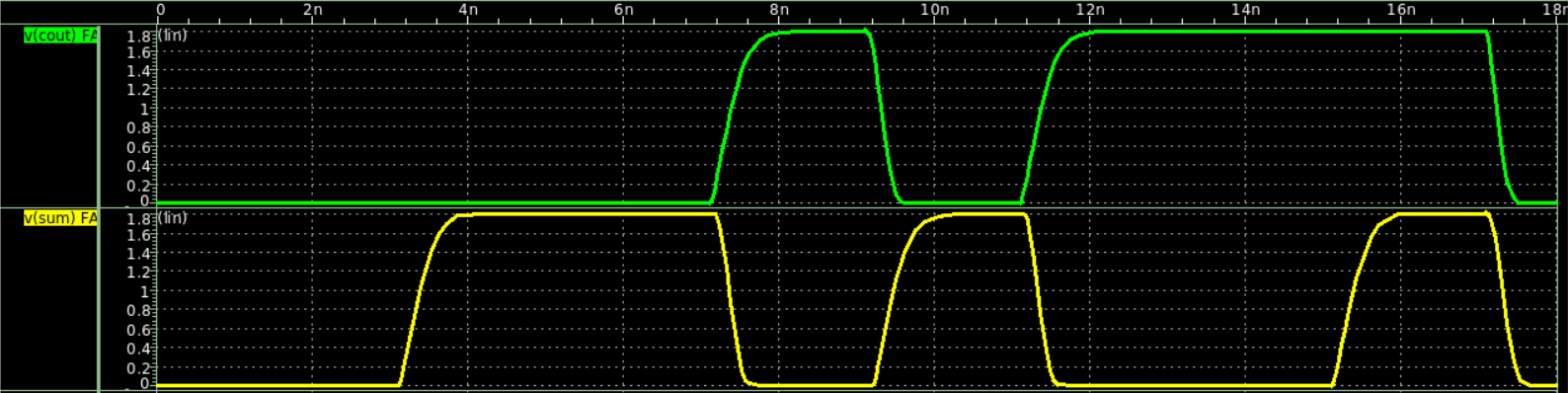
**Output load: 20f**



1. **wp: 0.36**

**wn: 0.18**

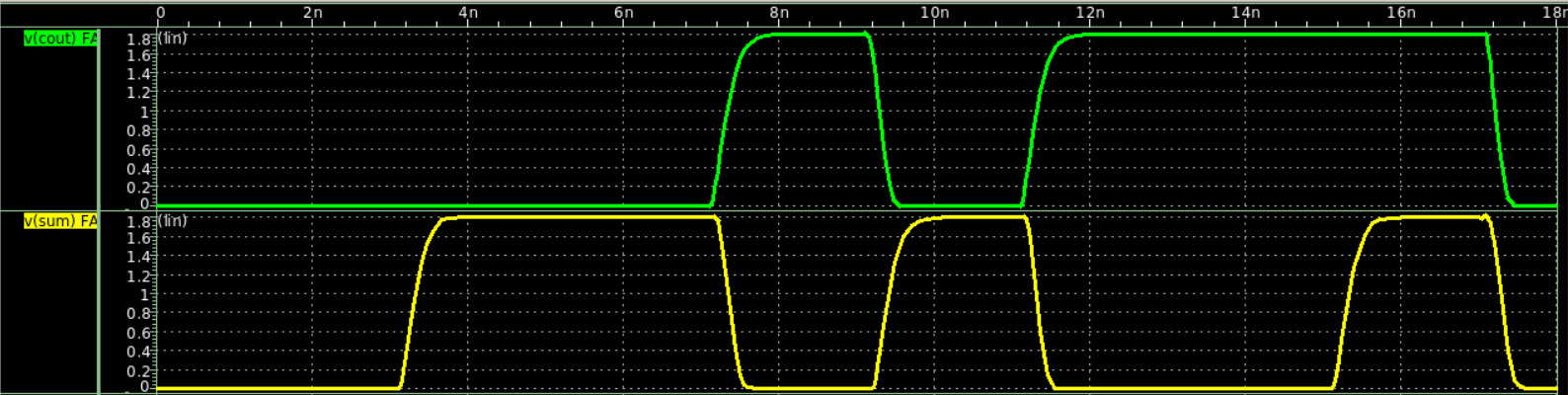
**Output load: 20f**



1. **wp: 0.48**

**wn: 0.24**

**Output load: 20f**



1. **Observations**

**Distortion becomes greater when (TPD becomes greater when) :**

1. **MOS width is smaller (smaller current, slower to charge the output node)**
2. **output load is higher (harder to push through the same amount of current)**
3. **Measurements**
4. **Table**

| **(C,Wn)** | **AVG\_PW** | **TPD** | **TRISE** | **TFALL** |
| --- | --- | --- | --- | --- |
| **(10fF,0.12um)** | 13.7980u | 251.9758p | 391.7264p | 186.9915p |
| **(10fF,0.18um)** | 15.3040u | 209.0278p | 262.3329p | 167.7282p |
| **(10fF,0.24um)** | 16.8445u | 189.4119p | 208.1128p | 152.2583p |
| **(15fF,0.12um)** | 18.3719u | 334.0522p | 563.8529p | 244.6797p |
| **(15fF,0.18um)** | 19.8595u | 262.4846p | 370.5688p | 222.9373p |
| **(15fF,0.24um)** | 21.4026u | 228.8002p | 289.1403p | 199.9067p |
| **(20fF,0.12um)** | 22.9263u | 415.7790p | 741.3519p | 292.1455p |
| **(20fF,0.18um)** | 24.5012u | 315.3306p | 489.5666p | 271.2786p |
| **(20fF,0.24um)** | 26.0399u | 268.8313p | 366.9256p | 245.6471p |

1. **Code (please describe)**

.meas tran avg\_power avg power from 0.1n to 18n

\*\*\*measure average power from 0.1ns to 18ns\*\*\*

.meas tran tprop trig v(a) val='supply/2' rise=2

+targ v(cout) val='supply/2' rise=1

\*\*\*measure TPD from A reaches 0.9v (2nd time) to COUT reaches 0.9v (1st time)\*\*\*

.meas tran tr trig v(cout) val='supply\*0.1' rise=1

+targ v(cout) val='supply\*0.9' rise=1

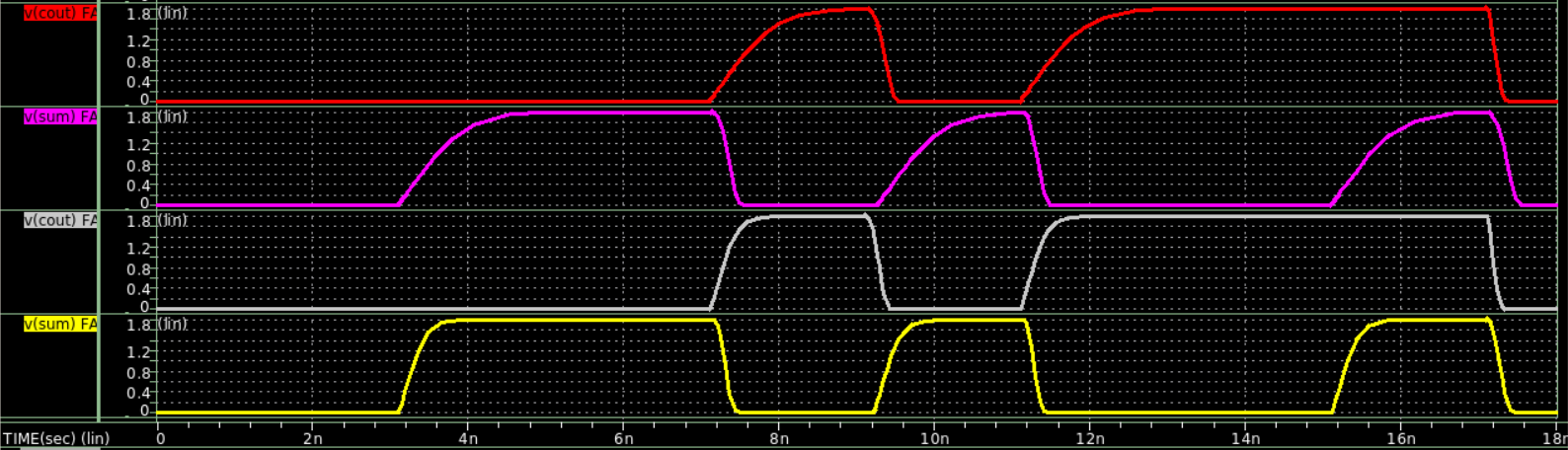
\*\*\*measure rise time from COUT reaches 0.18v to it reaches 1.62v (10% to 90%)\*\*\*

.meas tran tf trig v(cout) val='supply\*0.9' fall=1

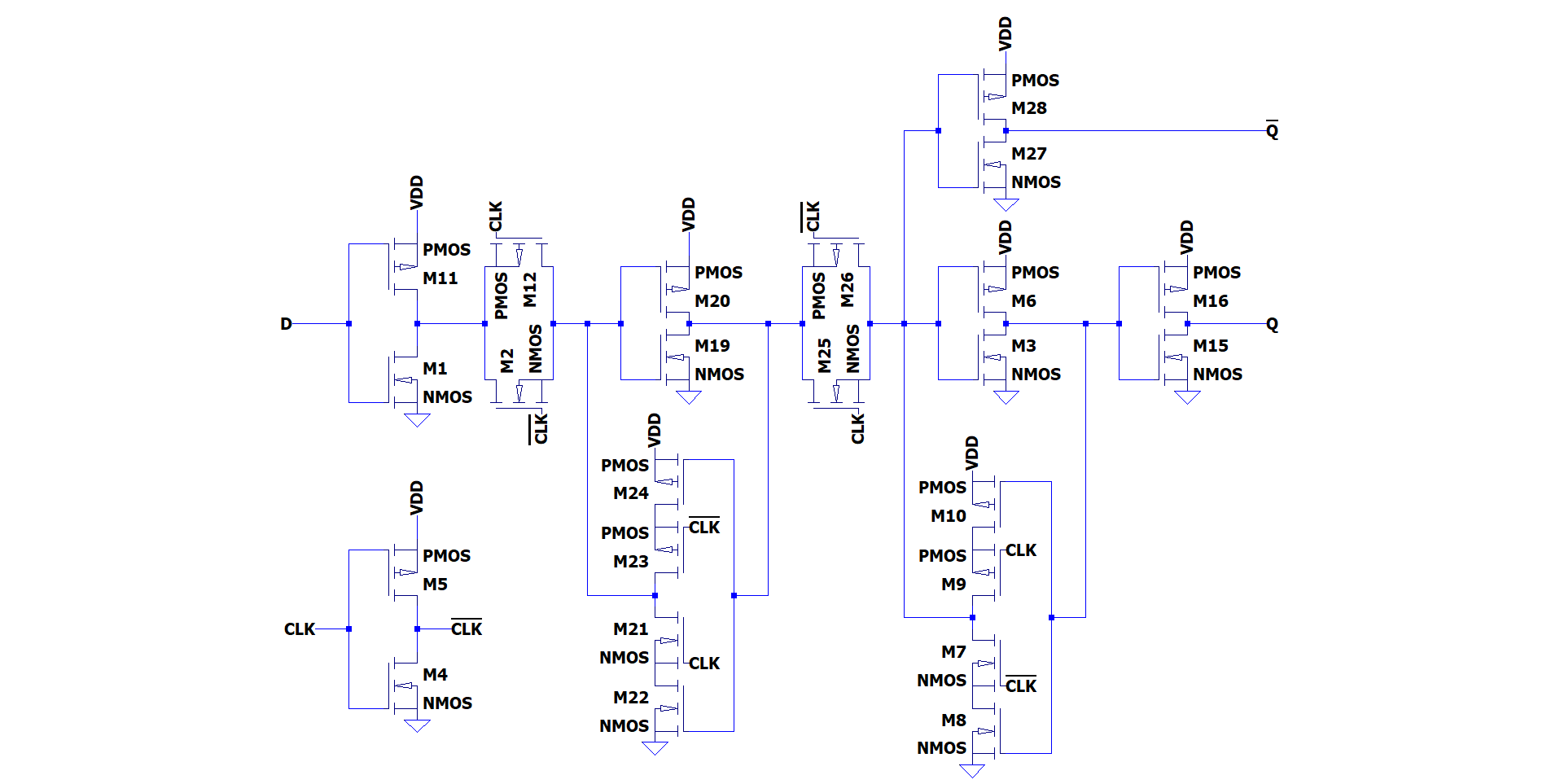
+targ v(cout) val='supply\*0.1' fall=1

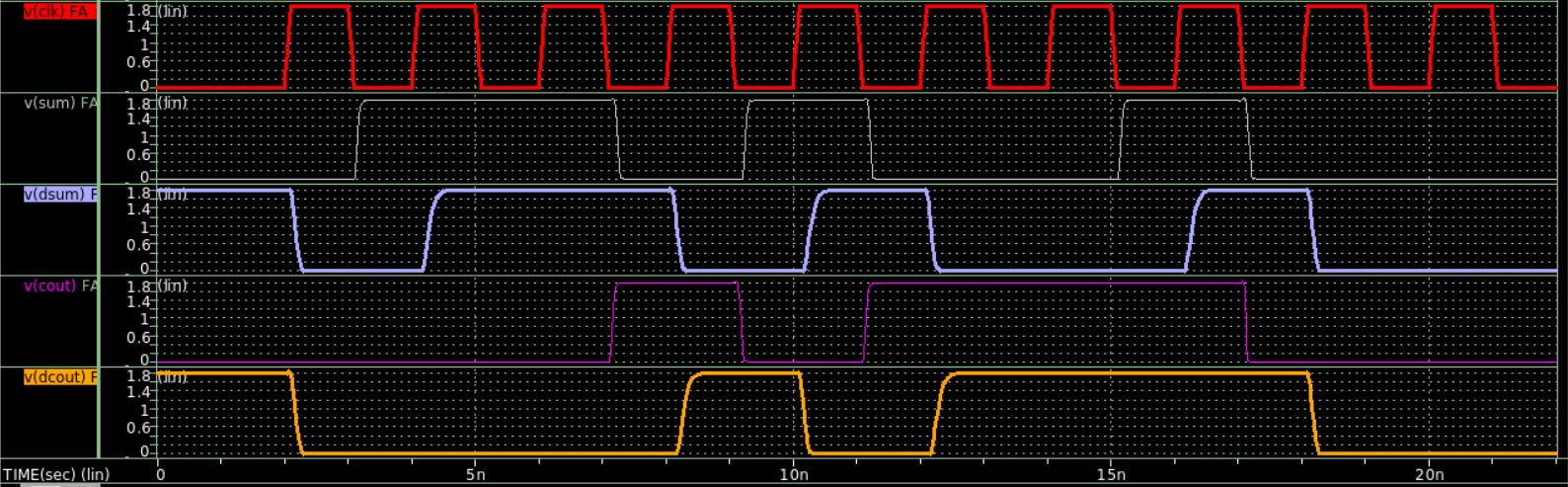
\*\*\*measure fall time where COUT drops from 0.62v to 0.18v (90% to 10%)\*\*\*

1. **Questions**
2. **Explain why there are glitches in FA combinational circuits sometimes, and how to fix it. Is it harmful for your overall design?** Different paths in the circuit might have different propagation delay causing signals to arrive at different times, thus leading to glitches (static-1, static-0, dynamic). To avoid this, either match up each of the input propagation delays (difficult) , or connect a buffer at the end of the circuit to reduce glitches. However, the downside is it takes longer to process (addition of the buffer delay). In my design, I first realize the inverse of SUM and COUT, then connect an inverter at the end, which works the same as adding a buffer to reduce glitches.
3. **Explain how you decide MOSFETs’ width with fixed channel length in your circuit (Hint: explain with mobility of PMOS NMOS, prove it with HSPICE)?** With the ratio of mobility => NMOS : PMOS = 2 : 1 (Approximate) we can set the width ratio Wn : Wp = 1 : 2 ,so that the pull up speed of p-network equals the pull down speed of the n-network towards the output node. With the simulation waveform below we can see the width ratio with Wn : Wp =1:2 has better results than 1:1. (upper 2 being 1:1 and lower 2 being 1:2)



1. **Bonus**

**DFF structure**

**Waveform**

**Glitch at the start :**  At the initial state, cause the DFF has no reset, the outputs are wrong. Once the first positive edge of CLK hits, outputs of both DFFs drop to 0.

| **(C,Wn)** | **AVG\_PW** | **TPD** | **TRISE** | **TFALL** |
| --- | --- | --- | --- | --- |
| **(10fF,0.12um) w/o DFF** | 13.7980u | 251.9758p | 391.7264p | 186.9915p |
| **(10fF,0.12um) w/ DFF** | 73.6974u | 1.2927n | 381.5099p | 146.9912p |
| **(10fF,0.18um) w/o DFF** | 15.3040u | 209.0278p | 262.3329p | 167.7282p |
| **(10fF,0.18um) w/ DFF** | 99.4466u | 1.2470n | 258.0632p | 138.3235p |
| **(10fF,0.24um) w/o DFF** | 16.8445u | 189.4119p | 208.1128p | 152.2583p |
| **(10fF,0.24um) w/ DFF** | 124.8817u | 1.2237n | 199.5162p | 124.0900p |

**From the form above we observe :**

1. This DFF model consumes large portion of power (about 5~8 times more power)
2. TPD inevitably adds [Half clk cycle] + [Tprop of DFF] ~ 1.04 ns
3. Shorter TRISE & TFALL