Project of the Synthesizer with Key input and LFO modulation

Jakub Koc

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Corresponding mail:
jakub.koc04@gmail.com

Abstract.

This work is devoted to the design of a sound synthesizer and includes calculations, simulations, and a complete circuit proposal. The main assumption was to create a prototype that could serve as a foundation for further development and the integration of additional modules in future iterations. This project represents my first attempt to combine two fields at once—music and electronics—which I have tried to describe. Although there had been earlier, informal iterations and initial attempts, this time I aimed to approach the project in a more structured way and describe it in greater detail for other beginner electronics enthusiasts like me.

Key words: Analog Electronics · VCO · 1V/Oct · Exponential Converter · Audio Circuits · PCB Design · Circuit Simulation · Synthesizers

1. Introduction

The origins of modern sound synthesizers are commonly associated with the work of Robert Moog, who introduced the first analog modular synthesizer in the mid-1960s. By combining voltage-controlled oscillators (VCO), filters, and envelope generators, his designs made it possible to generate sound independently of traditional acoustic instruments. This approach opened entirely new sonic possibilities and laid the foundations for electronic sound synthesis as it is known today.

As synthesizers gained popularity and new, previously unheard sounds began to appear in musical compositions, other manufacturers started developing their own unique instruments. Companies such as ARP, Yamaha, Roland, Korg, and many others introduced synthesizers with different architectures, control methods, and characteristic sound signatures. As a result, synthesizers quickly evolved from experimental devices into fully established musical instruments used across a wide range of musical genres.

The next major step in the evolution of synthesizers came with the introduction of digital instruments, enabled by advances in microelectronics and digital signal processing. Digital synthesizers offered improved tuning stability, higher precision, and new synthesis methods, greatly expanding the creative possibilities available to musicians. Although this transition was often associated with a perceived loss of the "warm" character typical of analog sound, careful design techniques allowed these differences to be minimized while providing users with significantly greater flexibility and control.

Alongside commercial development, a strong DIY community began to emerge, consisting of engineers, hobbyists, and musicians designing their own analog synthesizers. In this do-

main, designs are limited almost exclusively by imagination and knowledge of analog electronics. These projects range from large modular systems composed of numerous interconnected blocks, to much more modest constructions with unconventional architectures and distinctive functionality [1].

The aim of this project is to design and analyze an analog sound synthesizer based on classical architecture, with a particular focus on the frequency generation path. The design incorporates a VCO, an exponential converter, a summing stage, and a low-frequency oscillator (LFO), following the 1 V per octave control standard. The subsequent chapters present the theoretical background necessary to justify the adopted design decisions, provide a detailed description of the functional blocks, present simulation results, and outline the hardware implementation, along with a discussion of limitations and possible directions for further development.

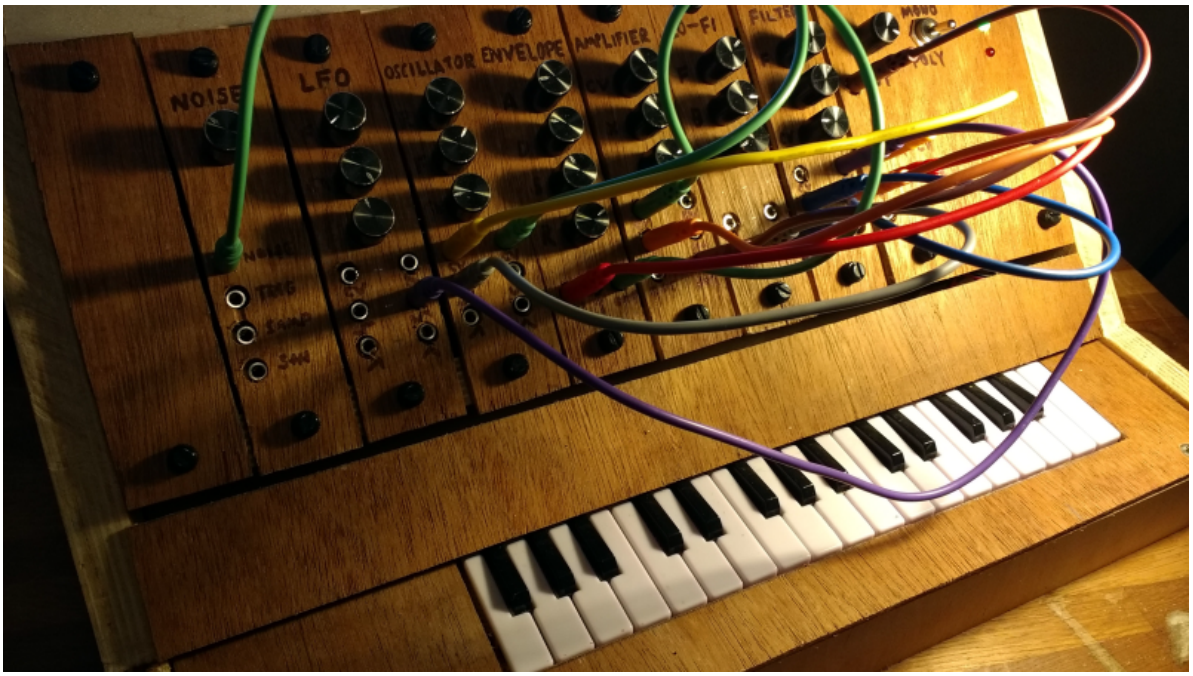

Figure 1: Modular digital synthesizer which combines the modularity of an analog synth with the power of a digital synth [2].

1.1 Project Objectives

The objective of this project is to design, analyze, and simulate an analog voltage controlled sound synthesizer, together with a proposal for its hardware implementation in the form of an electrical schematic and component selection.

The specific objectives of the project are as follows:

- to design an analog sound synthesizer based on a classical block-oriented architecture,
- to develop a frequency generation path based on a VCO,
- to implement an exponential converter enabling frequency control in accordance with the 1 V/oct standard,
- to design a summing stage for control voltages, allowing operation over a range of three octaves,
- to include a LFO intended for modulation of the main oscillator frequency,

- to perform theoretical analysis and circuit-level simulations of the proposed design,
- to present a hardware implementation proposal, including schematic design and component selection.

Detailed experimental evaluation and measurements of the fully assembled hardware are beyond the scope of this work. However, the project anticipates that future iterations will include analyzes and verifications of the completed circuit, including practical measurements and listening tests.

1.2 Functional Requirements

The functional requirements of the designed synthesizer are summarized in Table 1.

Table 1: Functional requirements of the synthesizer.

Parameter	**Requirement**
Power supply	Symmetrical supply ±5 V
Control input connector	3.5 mm jack
Audio output connectors	3.5 mm jack
Frequency standard	Equal-tempered scale
Control voltage standard	1 V/oct
V_{key} voltage range	0 to 1 V
V_{key} step resolution	83.3 mV per semitone
Number of octaves	Three
VCO frequency range	< 130.8 Hz; 987.84 Hz >
Frequency accuracy	Deviation not greater than ±10 cents
LFO enable control	On/off switching
LFO waveform	Sinusoidal
LFO frequency	Approximately 10 Hz
LFO function	Depth of modulation by potentiometer

2. Theoretical Background and Functional Description

This chapter introduces the basic concepts of music theory necessary to understand the design decisions made during the development of the project. In addition, it describes the operating principles of the most complex functional blocks used in the system. Figure 2 presents the block diagram of the synthesizer, with the main blocks highlighted and discussed in this chapter.

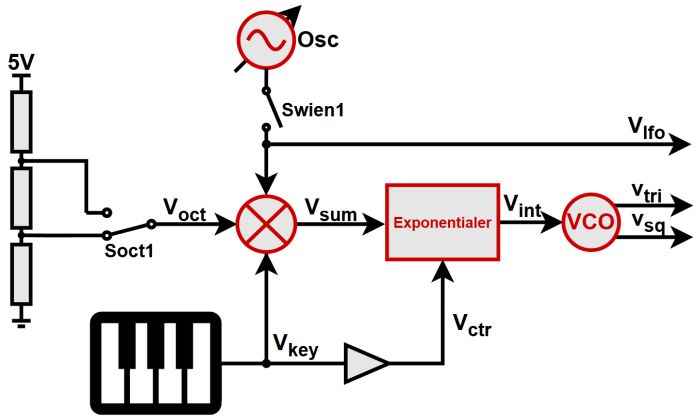

Figure 2: Block Diagram.

The descriptions focus on the idealized operation of each block, architectural considerations, and the equations required for the design process. The analyzed blocks include the VCO, the exponential converter, the summing stage, and the peripheral LFO. A key objective of this chapter is to explain how the VCO interprets the input control signal to generate the needed frequency and how the remaining blocks support this operation.

Most of the figures and equations presented in this chapter were developed by the author. Any external sources are explicitly indicated by footnotes.

2.1 The equal tempered system

Over the centuries, many musical tuning systems have been developed, each defining a different method for determining intervals and assigning frequencies to individual notes. For example, in just intonation, intervals are based on simple integer ratios, whereas the Pythagorean system relies exclusively on pure fifths.

In the nineteenth century, the equal tempered tuning system became widespread, mainly due to the dominance of keyboard instruments [5]. The later development of electronic musical systems and the MIDI standard further reinforced its position, as this tuning system is the simplest to describe in a mathematical way. In equal temperament, the octave is divided into twelve equal logarithmic steps, each corresponding to one semitone, according to the following relation [3, 4]:

$$f_{\mathrm{N}} = f_{\mathrm{o}} \cdot 2^{\frac{N}{12}} \tag{1}$$

Assuming a base frequency f_{o} equal to 16,35 Hz, it is possible to create a table with several octaves:

The 1 V/octave standard is commonly adopted, meaning that each semitone corresponds to a voltage step of approximately 83 mV at the control input, while a full 1 V increase should

Table 2: Frequencies of musical notes across 0 to 7 octaves. Gray columms represents used octaves in this project

Scale	Oct. 0	Oct. 1	Oct. 2	Oct. 3	Oct. 4	Oct. 5	Oct. 6	Oct. 7
C	16,35	32,7	65,4	130,8	261,6	523,2	1046,4	2092,8
C#	17,32	34,64	69,28	138,56	277,12	554,24	1108,48	2216,96
D	18,35	36,7	73,4	146,8	293,6	587,2	1174,4	2348,8
D#	19,45	38,9	77,8	155,6	311,2	622,4	1244,8	2489,6
E	20,26	40,52	81,04	162,08	324,16	648,32	1296,64	2593,28
F	21,83	43,66	87,32	174,64	349,28	698,56	1397,12	2794,24
F#	23,12	46,24	92,48	184,96	369,92	739,84	1479,68	2959,36
G	24,5	49	98	196	392	784	1568	3136
G#	25,96	51,92	103,84	207,68	415,36	830,72	1661,44	3322,88
A	27,5	55	110	220	440	880	1760	3520
A#	29,13	58,26	116,52	233,04	466,08	932,16	1864,32	3728,64
B	30,87	61,74	123,48	246,96	493,92	987,84	1975,68	3951,36

result in a doubling of the frequency [1]. Therefore, one of the main challenges in circuit design is interpreting a linear change at the input as a logarithmic change in frequency, which is achieved using conversion blocks.

The final important aspect is determining how accurate the generated frequency must be so that any deviation remains acceptable to the user. Here, the equal tempered system is again useful, as it divides each semitone into 100 cents [3]. A commonly accepted perceptual tolerance is defined as follows [**?**]:

- < 5 cents – inaudible,
- < 10 cents – audible only to a trained ear,
- < 25 cents – noticeable to most users.

where the frequency deviation expressed in cent can be calculated as [3]:

$$\Delta Interval = 1200 \log_2 \left(\frac{f_\mathrm{o}}{f_\mathrm{ideal}} \right) [cent] \tag{2}$$

2.2 Relaxation Generator (VCO)

The VCO is the core of the entire synthesizer, as it is responsible for generating waveforms whose frequency depends directly on the input control voltage. The quality and stability of this block have the biggest impact on the overall performance of the system. The project focuses on a simple relaxation generator architecture based on an integrator, a Schmitt trigger, and a switching transistor. The main behavior depends on loading and discharging a capacitor, which generates square and triangular waveforms. Variants of this topology have been used in both commercial and DIY analog synthesizers, including designs by Moog and ARP, which can be find in Internet's archives [6].

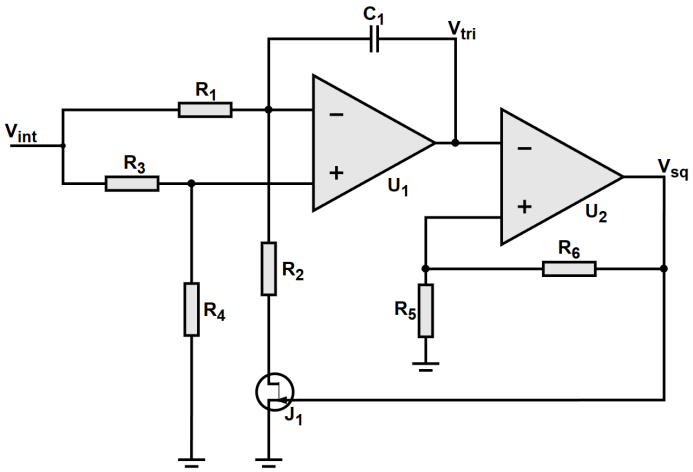

Figure 3: Schematic of VCO.

Being precise, the capacitor is charged by a constant current determined by the input control voltage, which causes the output (V_{tri}) of the first op-amp to decrease linearly over time. When V_{tri} reaches the threshold set by the positive feedback of the second amplifier (Schmitt trigger), the output state (V_{sq}) switches from negative to positive. As a result, the transistor (J_1) turns on, and the direction of the current flowing through the integrator changes. The capacitor then begins to discharge with the constant current, causing the integrator output voltage to increase linearly. When the voltage reaches the opposite threshold of the Schmitt trigger, its output toggles back to the initial state, reversing the current direction once again. This process repeats continuously, producing a symmetrical triangular waveform at the integrator output and a corresponding square waveform at the Schmitt trigger output, as seen in Figure 4.

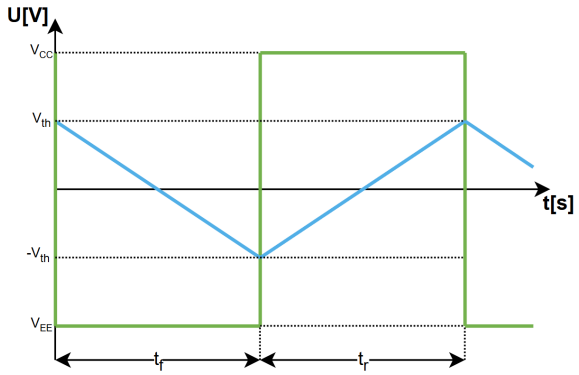

Figure 4: Diagram of VCO's outputs.

The first step of the design is to determine the switching thresholds of the Schmitt trigger, which define both the moments of state transition and the domains of the triangular waveform. These thresholds are set by the supply voltage (It can be either V_{CC} or V_{EE} since they are equal) and resistors R_5, R_6, as expressed (3). It is generally recommended to place the threshold around half of the supply voltage. This choice reduces the risk of op-amp saturation, which can cause non-linearity.

$$V_{\text{th}} = \frac{V_{\text{CC}} \cdot R_6}{(R_5 + R_6)} \tag{3}$$

Once the switching threshold of the Schmitt trigger is known, it becomes possible to derive expressions for the rising (t_r) and falling (t_f) times of the triangular waveform, and consequently for the oscillation frequency (f_o). The falling time is obtained by assuming that the capacitor is charged by a constant current flowing through resistor R_1:

$$t_\mathrm{f} = \frac{V_\mathrm{tri\_pp}}{V_\mathrm{int}} \frac{R_1 C_1}{(1 - \frac{R_4}{R_3+R_4})} \tag{4}$$

while the rising time corresponds to the capacitor being discharged by a constant current flowing through R_2:

$$t_\mathrm{r} = \frac{V_\mathrm{tri\_pp}}{V_\mathrm{int}} \frac{(R_3 + R_4) R_1 R_2 C_1}{(R_4(R_1 + R_2) - R_2(R_3 + R_4))} \tag{5}$$

In the (4) and (5), $V_\mathrm{tri\_pp}$ denotes the peak-to-peak amplitude of the triangular waveform, which is two times V_th. The voltage V_int represents the input control voltage applied to the integrator. At first glance, equations may appear relatively complex. However, if it is assumed that the non-inverting input of the integrator is biased to half of V_int by an appropriate selection of the resistor divider R_3 and R_4, the expressions can be significantly simplified and reduced to the following form:

$$t_\mathrm{f} = \frac{2\Delta V_\mathrm{tri\_pp}}{V_\mathrm{int}} R_1 C_1 \tag{6}$$

$$t_\mathrm{r} = \frac{2V_\mathrm{tri\_pp}}{V_\mathrm{int}} \frac{R_1 R_2 C_1}{(R_1 - R_2)} \tag{7}$$

Finally, the oscillation frequency can be derived by summing the rising and falling time:

$$f_\mathrm{o} = \frac{1}{t_\mathrm{r} + t_\mathrm{f}} = \frac{V_\mathrm{int}}{2V_\mathrm{tri\_pp}(R_1 + \frac{R_1 R_2}{(R_1 - R_2)})C_1} \tag{8}$$

Several important conclusions can be drawn from these expressions. First, to obtain a duty cycle close to 50%, the resistor R_1 should be selected to be twice the value of R_2. Second, the oscillation frequency varies linearly with the input control voltage V_int. Finally, the overall frequency range of the oscillator can be adjusted by proper selection of C_1, R_1, and R_2.

2.3 Exponential Converter

To address the conversion problem discussed in the subsection on the equal tempered system, the nonlinear characteristics of semiconductor devices are used. Components such as diodes and transistors have an exponential current–voltage relationship, which can be used to map linear control signals to exponential responses. In practice, bipolar junction transistors provide a better solution, due to a wider operating range and the possibility of combining pair configurations. The exponential behavior of a bipolar transistor is described by the Ebers–Moll equation [7]:

$$I_\mathrm{c} = I_\mathrm{s} \cdot \left(e^{\frac{V_\mathrm{be}}{V_\mathrm{T}}} - 1 \right) \tag{9}$$

The converter architecture shown in Figure 5 is used as the basis for the design. In this topology, the transistor pair is used, while the operational amplifier and resistors define the biasing conditions. Resistor R_1 sets the reference current I_ref, defined as:

$$I_{\text{ref}} = \frac{V_{\text{cc}}}{R_1} \tag{10}$$

whereas R_2 limits the maximum current flowing through the transistors. To understand why this solution is superior to single-transistor designs, it is useful to consider the following relations [9]:

$$\Delta V_{\text{be}} = \Delta V_{\text{be2}} - \Delta V_{\text{be1}} = V_{\text{T}} \ln\left(\frac{I_{\text{int}}}{I_{\text{ref}}}\right) \tag{11}$$

$$I_{\text{int}} = I_{\text{ref}} \cdot e^{\frac{\Delta V_{\text{be}}}{V_{\text{T}}}} \tag{12}$$

One of the main challenges of simple exponential converters is their dependence on device parameters and temperature, as indicated by (9). The thermal voltage V_{T} increases proportionally with temperature, which can be compensated relatively easily by scaling or trimming. In contrast, the saturation current I_{s} approximately doubles for every 10°C increase in temperature, which can introduce nonlinearity. A major advantage of using a matched transistor pair is that the influence of I_{s} is canceled, as shown in (11), resulting in the output current described by (12).

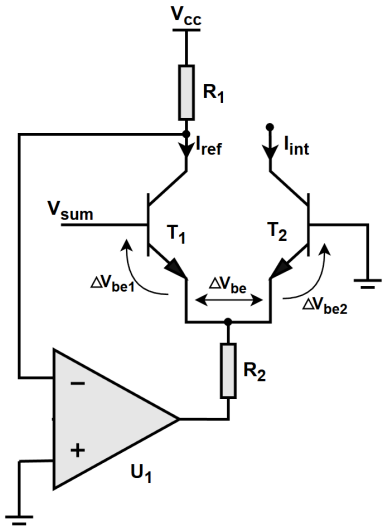

Figure 5: Ideal schematic of exponential converter.

Note that the transistor collector is held at 0 V due to the virtual short between the inputs of the op-amp. Therefore, to ensure proper current transfer through the transistor, the input control voltage must operate in a negative range around 0 to $-V_{\text{BE}}$.

2.4 Summing Amplifier

This part of the design is relatively straightforward. The external control signals V_{key}, the bias voltage corresponding to octave selection V_{oct}, and the modulation signal from the LFO V_{lfo} are summed using an operational amplifier configured as an inverting summing amplifier, as shown in Figure 6.

The inverting configuration is particularly advantageous, as the exponential converter requires a negative control voltage for proper operation.

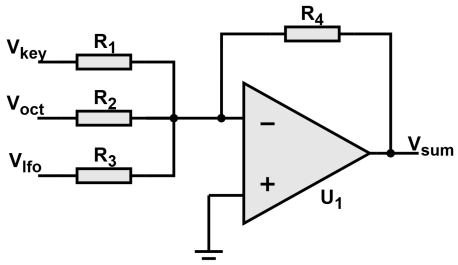

Figure 6: Ideal schematic of summing amplifier.

Since one octave corresponds to a 1 V change in control voltage and the input range of the exponential converter is limited, the input voltage must be appropriately scaled. For this reason, the transfer equation of the summing amplifier is required and is given by:

$$R_4\left(\frac{V_{\text{key}}}{R_1} + \frac{V_{\text{oct}}}{R_2} + \frac{V_{\text{lfo}}}{R_3}\right) = -V_{\text{sum}} \tag{13}$$

where resistors R_1, R_2, and R_3 should be equal in order to provide equal weighting of the summed control voltages.

2.5 LFO (Wien Generator with AGC)

In synthesizers, LFOs are circuits used to introduce modulation of the main carrier signal. In this context, the LFO operates as a peripheral subsystem, and there are no strict requirements. To generate a stable low-frequency signal, a Wien bridge oscillator is used in this project.

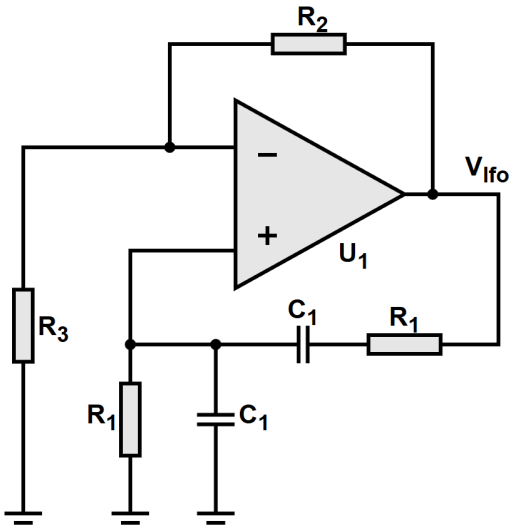

Figure 7: Ideal schematic of wien generator.

The basic Wien bridge oscillator is shown in Figure 7. The circuit is based on an operational amplifier with both positive and negative feedback paths. The positive feedback network determines the oscillation frequency, which is given by [7]:

$$f_{\text{o}} = \frac{1}{2\pi R_1 C_1} \tag{14}$$

while the negative feedback network sets the amplifier gain [7]:

$$A_o = 1 + \frac{R_2}{R_3} \tag{15}$$

In order to design a stable oscillator, two conditions must be met [8]:

- The total phase shift around the feedback loop must be 0°.
- The loop gain must be equal to unity.

The first condition is always satisfied due to positive feedback. The problem arises in the second case, where the condition can only be met by appropriate selection of the resistors in the negative feedback loop. Since the positive feedback network exhibits a gain of 1/3, the amplifier gain must be set to 3. This can be achieved by setting resistor R_2 to be twice the value of R_3. However, due to non-ideal circuit behavior, maintaining the loop gain exactly equal to unity is challenging. A loop gain lower than unity leads to the extinction of the signal amplitude, whereas a gain greater than one increases the amplitude and introduces distortion. Therefore, an automatic gain control (AGC) mechanism is required to generate a stable sine wave, as shown in Figure 8.

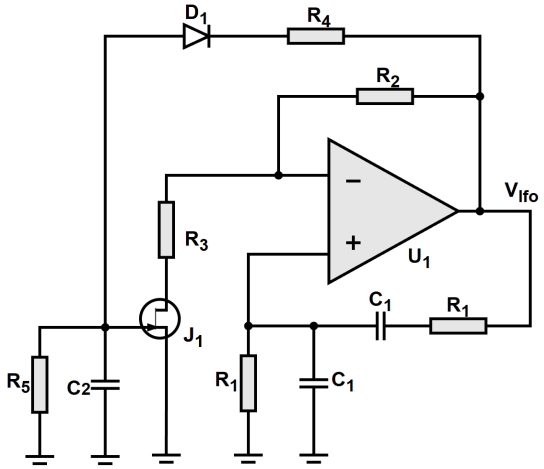

Figure 8: Ideal schematic of Wien generator with AGC.

The AGC implementation is based on a simple and effective principle. Transistor J_1 operates as a voltage-controlled resistor connected in series with R_3, thereby adjusting the generator gain[1]. The feedback loop biases J_1 in such a way that the loop gain is maintained close to three.

Diode D_1 together with resistor R_4 forms an amplitude detector, while R_5 and C_2 generate a smoothed control voltage that defines the gate–source voltage V_{gs} of the JFET. The time constant determined by R_5 and C_2 controls the AGC response speed. For proper operation, the AGC must respond slower than the oscillation period itself, ensuring stable amplitude regulation with minimal waveform distortion.

[1]Since that, the gain calculated by (15) should be a little bit higher than 3.

3. Calculations and simulation Results

This chapter presents the fundamental simulations, the obtained results, and the rationale behind the selection of individual components, together with the schematic diagrams used in the final design. Most of the simulations are transient analyzes and are performed on isolated functional blocks to simplify the interpretation and verification of their behavior. The VCO is analyzed together with the exponential converter due to their strong functional dependency, while the top-level simulation includes all sub-blocks integrated into the complete system. The simulation files and testbench sources from OrCad used in this work are available in the project repository on GitHub [10].

3.1 Exponential Converter

It is convenient to start the analysis with the exponential converter, as it forms the bridge between the summing amplifier and the VCO. The final design of this circuit is shown in Figure 9.

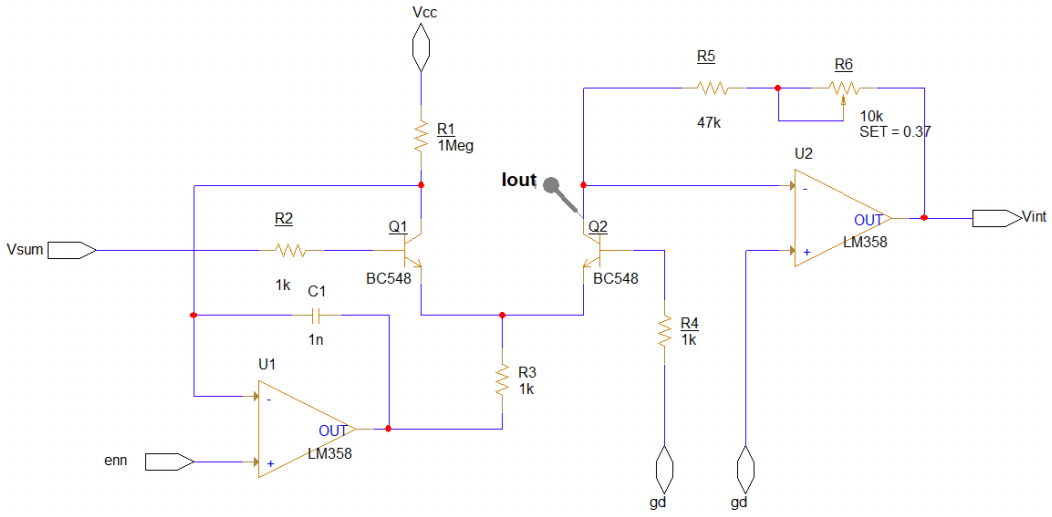

Figure 9: Schematic of exponentialer.

To ensure the stable operation of the circuit, resistors R_2 and R_4 were added to limit the current flowing into the transistor bases, and capacitor C_1 was included for stabilization. Without these components, the circuit may enter an oscillatory state, which is clearly visible in the simulation traces shown in Figure 10.

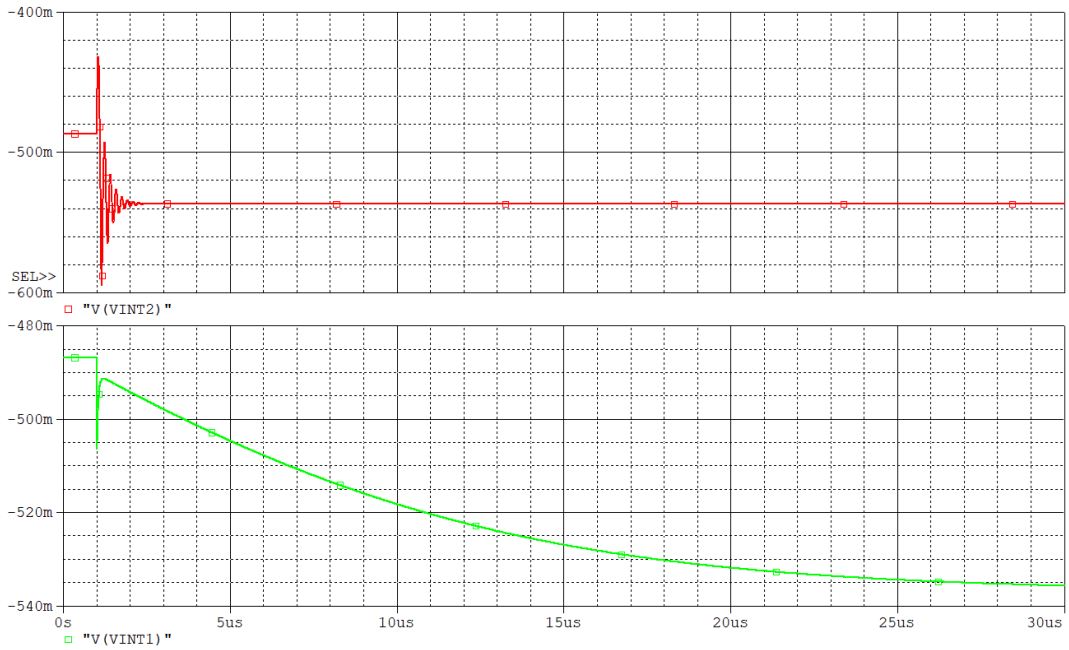

Figure 10: Response to a −50 mV input step given to V_{sum} without capacitor C_1 (V_{int2}) and with it (V_{int1}).

An I2V[2] is added at the output of the exponential converter. Instead of gd, a non-inverting input of U1 pin *enn* was added, which will be explained later. The reference current I_{ref} is set using (10) and resistor R_1 to obtain a value of 5 μA, which provides a suitable operating range. Since no specialized amplifier is required for this stage, the LM358 is used, representing a low-cost solution.

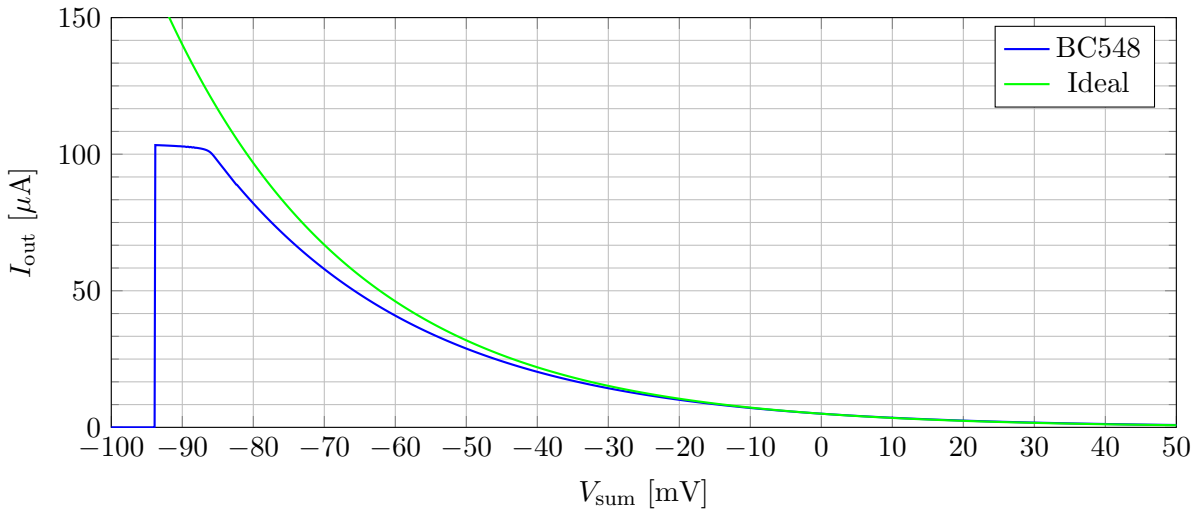

Figure 11: Characteristic I_{out} as a function of V_{sum}

The most critical aspect of the design is the selection of a transistor for the exponential converter, as the entire tuning procedure is referenced to its characteristics. Figure 11 compares the measured response of a BC548 transistor with the ideal characteristic calculated using (12) for $I_{\text{ref}} = 5$ μA. A noticeable discrepancy between the two characteristics can be observed. Equation (12) does not include the full transistor model, which makes these differ-

[2]I2V - Current to voltage converter

ences clearly visible. They can most likely be attributed to the influence of the base resistance r_{be}, finite β and other non ideal parameters.

In practice, the observed deviations are not critical, and the circuit still meets the assumptions presented in Table 3. As a reminder, after applying a constant control voltage increment, the output current is expected to double. For the BC548 transistor pair, this behavior occurs at approximately 19.8 mV, whereas the ideal calculation predicts a voltage step of about 18.7 mV. For easier scaling of the input voltage, the step for the BC548 transistor was shifted to 20 mV, which still provides a solid basis for further design stages.

Table 3: Comparison of output current for BC548 transistor and ideal model

BC548			**Ideal**	
V_{sum} [mV]	I_{out} [μA]	I'_{out} [μA]	V_{sum} [mV]	I_{out} [μA]
-10	7.103	-	-10.0	7.241
-30	14.322	14.206	-28.7	14.475
-50	28.842	28.412	-47.4	28.933
-70	57.941	56.824	-66.1	57.835

Figure 12 presents the final transfer characteristic, set by resistor R_5 such that a control voltage range of 0–5 V corresponds to three octaves. Potentiometer R_6 is used for fine trimming to compensate for frequency deviations caused by component tolerances in the final device.

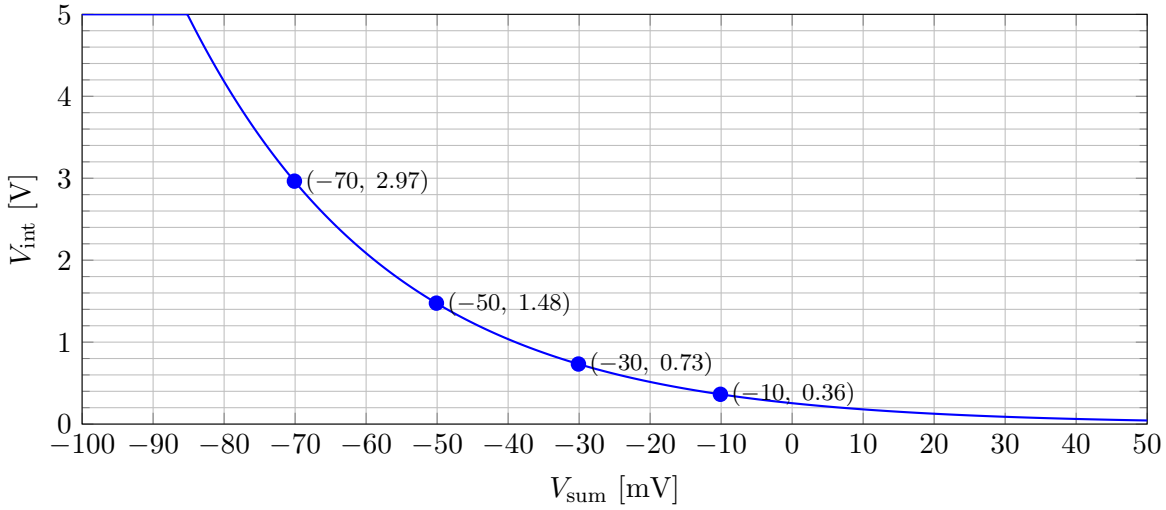

Figure 12: Characteristic V_{int} as a function of V_{sum}

3.2 VCO

The marked points on the transfer curve in Figure 12 define the voltage range in which the VCO is intended to operate. Each point represents a one-octave step, and together they set the usable frequency range of the oscillator. In this design, the lowest control point (-10; 0.36) corresponds to a frequency of 123.48 Hz, while the highest reaches 987.84 Hz according to Table 2. Since the smallest practical control step is 1/12 V, the entire range is shifted accordingly, placing the lowest frequency at the note B rather than C.

In the final hardware design, the MCP602-I/P operational amplifier is used. However, this device was not available for simulation, the AD824 was selected for analysis instead. Both

operational amplifiers exhibit similar key parameters; most importantly, they provide rail-to-rail output capability, which allows the generation of a square wave over the full supply voltage range. Other parameters, such as bandwidth, input offset voltage, or noise are not critical for the correct operation of the circuit.

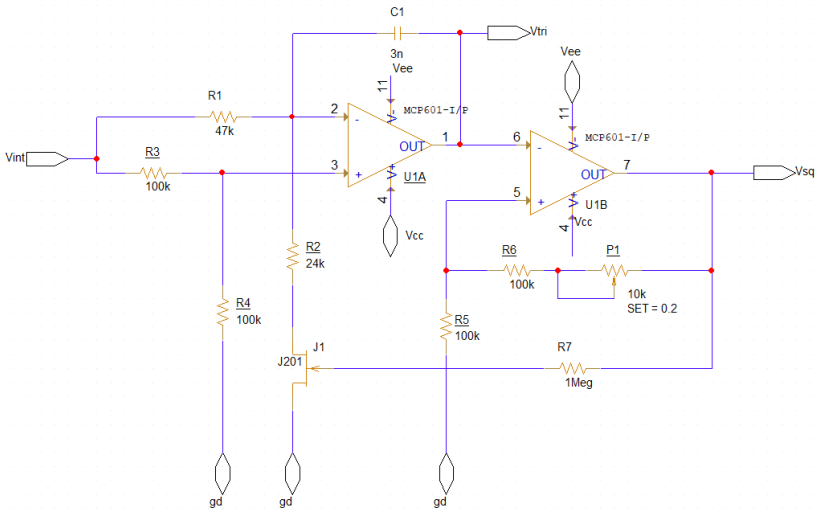

Figure 13: Schematic of VCO.

The design process starts with the Schmitt trigger thresholds, which are determined by resistors R_5 and R_6 according to (3). Both resistors are set to 100 kΩ, resulting in a threshold voltage of approximately 2.5 V. Additionally, potentiometer P_1 is included to correct the offset caused by propagation delays in the feedback loop and the input offset voltage of the operational amplifier.

The next step is to select resistors R_3 and R_4 such that the voltage at the non-inverting input of U_{1A} is equal to half of V_{int}. For this reason, both resistors are also chosen as 100 kΩ.

Another important set of components is formed by resistors R_1 and R_2. As discussed previously, achieving an approximate 50% duty cycle requires R_1 to be twice the value of R_2. Consequently, $R_1 = 47\,\text{k}\Omega$ and $R_2 = 24\,\text{k}\Omega$. With these values, the duty cycle is approximately 49%, which should not be noticeable to the ear.

Finally, capacitor C_1 is selected using (8), yielding:

$$123.48 = \frac{0.36}{2 \cdot C_1 \cdot 5 \cdot \left(47\text{k} + \frac{47\text{k} \cdot 24\text{k}}{47\text{k} - 24\text{k}}\right)} \Rightarrow C_1 \approx 3\ \text{nF} \tag{16}$$

The value of capacitor C_1 is selected while taking into account the availability of standard capacitor values. Therefore, any discrepancy between the calculated value and the implemented component is not critical and can be easily compensated by trimming the potentiometer in the I2V converter of the exponential converter. Table 4 and Figure 14 present the results obtained for the VCO in its final configuration.

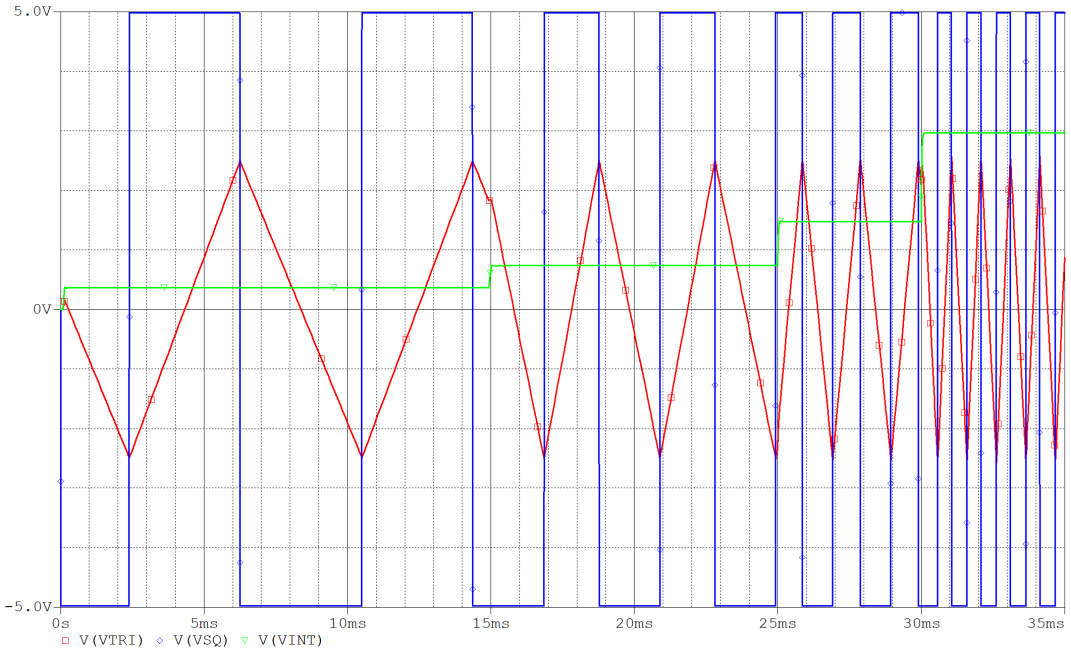

Figure 14: Traces of VCO outputs during different Vsum values.

Table 4: Comparison of output frequency with ideal values and pitch deviation

V_{sum} [mV]	V_{int} [V]	f_{o} [Hz]	$f_{\text{o,ideal}}$ [Hz]	Δf [cents]
-10	0.364	123.35	123.48	-1.86
-30	0.733	247.59	246.96	4.38
-50	1.477	494.24	493.92	1.13
-70	2.966	974.85	987.84	-22.92

At this stage, it is useful to draw some conclusions. The frequency deviation between the VCO output and the ideal characteristic is relatively small for the first two octaves. A deviation of less than 10 cents is typically perceptible only to a trained ear. However, at higher frequencies, the deviation increases and exceeds 20 cents, becoming more noticeable. Although this effect might initially be attributed to the exponential converter, which introduces a control voltage offset, but the root cause lies in the VCO itself.

As shown in Figure 15, increasing the control voltage results in the VCO frequency being progressively lower than the ideal value. This behavior is caused by the rise in the threshold of the Schmitt trigger. At higher frequencies, the circuit changes state at a larger voltage excursion of the triangular waveform. As a result, the effective triangle amplitude Δu_{tri} becomes frequency-dependent, which directly affects the oscillation frequency in (8):

$$f_{\text{o}} = \frac{V_{\text{int}}}{2C_1 \cdot u_{\text{tri\_pp}}(f_{\text{o}}) \cdot \left(R_1 + \frac{R_1 R_2}{R_1 - R_2}\right)} \tag{17}$$

It is also worth mentioning jitter, which was not evaluated in this analysis. Although its presence is certain, it did not introduce any noticeable issues within the scope of the performed investigation. Therefore, in future design iterations, jitter should be analyzed in more detail, plus the frequency dependence of Δu_{tri} should be compensated.

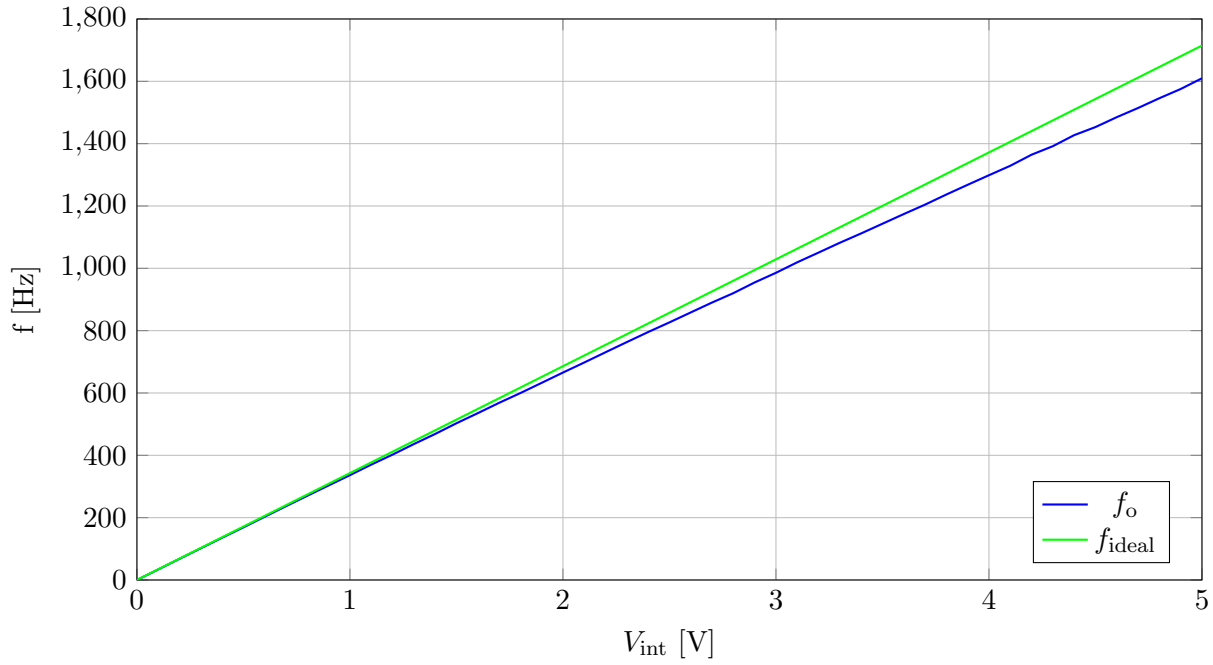

Figure 15: Characteristic f_{o} and f_{ideal} of the VCO as a function of V_{int}

3.3 Summing Amplifier

In this case, a 20 mV step must be converted into a 1 V change; to achieve this, equation (13) is used. The final version of the circuit, including the calculated resistor values, is shown in Figure 16. For this stage, the LM358 operational amplifier was also used as a low-cost solution.

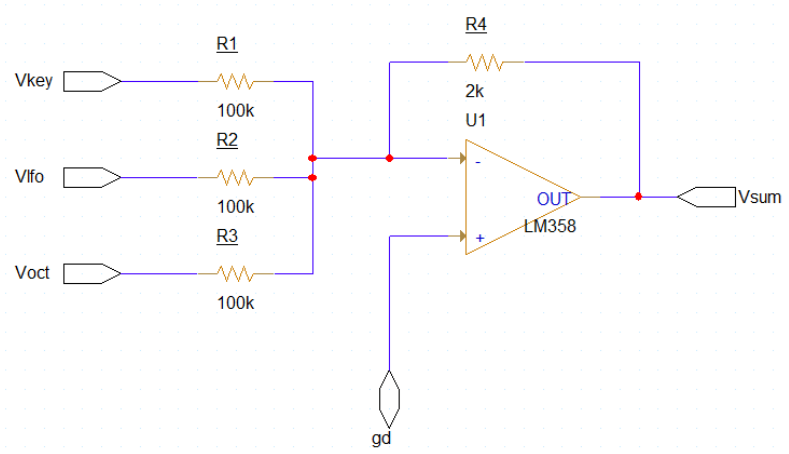

Figure 16: Schematic of summing amplifier.

3.4 LFO

The main assumption is that the LFO must generate a 10 Hz sine wave, which can then be scaled to introduce more or less FM modulation in the main oscillator. The final design is shown in Figure 17.

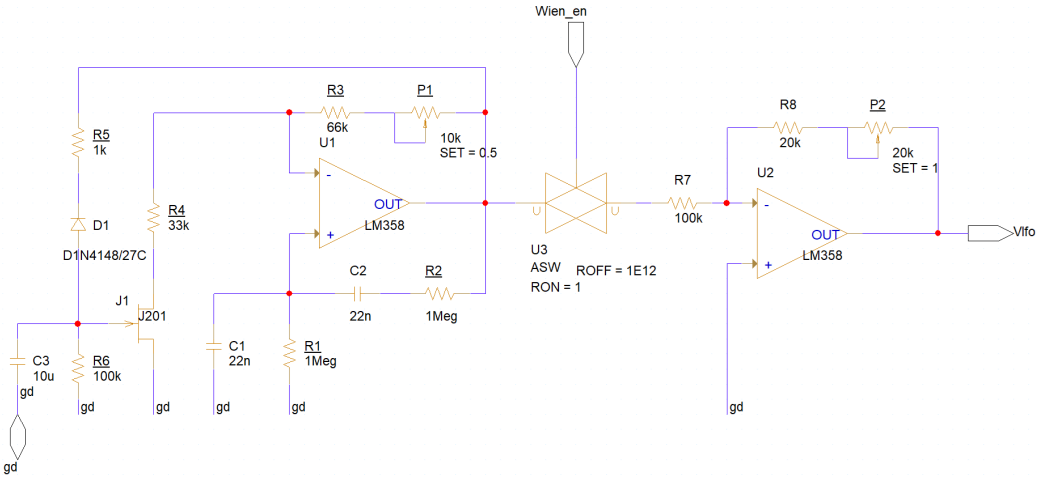

Figure 17: Schematic of Wien oscillator as LFO.

To obtain the desired frequency, equation (14) was used. A capacitor value of 22 nF together with a resistor of 680 kΩ results in a frequency 10.6 Hz. The remaining circuit components were selected to ensure stable operation. Due to component tolerances, the AGC loop may exhibit unstable behavior in certain cases. For this reason, the potentiometer P_1 was added, allowing manual adjustment of the loop gain according to (15) to restore stable operation if required.

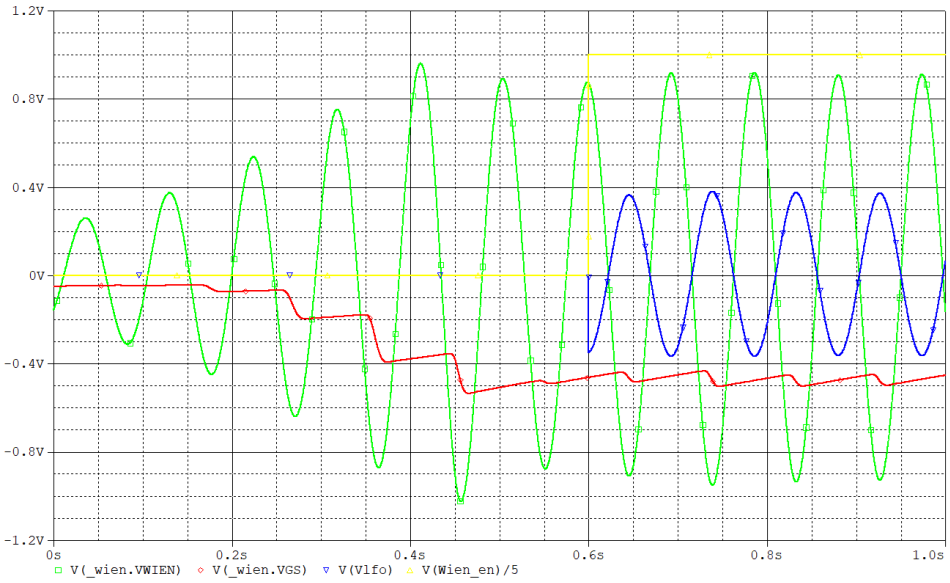

Figure 18: Traces of LFO.

In Figure 18, the most important traces are shown. Green represents the raw output from the Wien oscillator and illustrates how the oscillator is starting and stabilizing. The red one corresponds to Vgs, which controls the JFET's dynamic resistance. The AGC is functioning well and ensures a decent sine wave. To demonstrate that the THD was checked, it was equal to 1.405%.

To control the influence of modulation on the main carrier in the VCO, the op-amp in an inverting amplifier configuration was added, which is connected through the switch U3 that can be easily turned on/off by a user, as represented by the yellow trace. The gain and amplitude of the sine wave can be changed using the potentiometer P2; an example of the

final V_{lfo} signal is shown as the blue waveform.

3.5 Top level simulation

Figure 19 shows the top level view of the synthesizer testbench, which corresponds to the block diagram presented in Figure 2. Three parts are particularly worth emphasizing: the resistor ladder responsible for octave selection, output buffers, and the comparator combined with an inverter stage, which enables the circuit when a key is pressed.

The resistor values were selected to generate control voltages according to Table 4. A buffer stage was inserted between the input of the summing stage and the biasing network to prevent the loading of the resistor ladder.

Two op-amps are connected to the outputs: one configured as a buffer for the signal V_{sq} and the second configured as a non-inverting amplifier for the V_{tri} in order to increase its amplitude toward the supply rails. The gain of this amplifier is set close to two, but slightly below unity to prevent saturation caused by component tolerances.

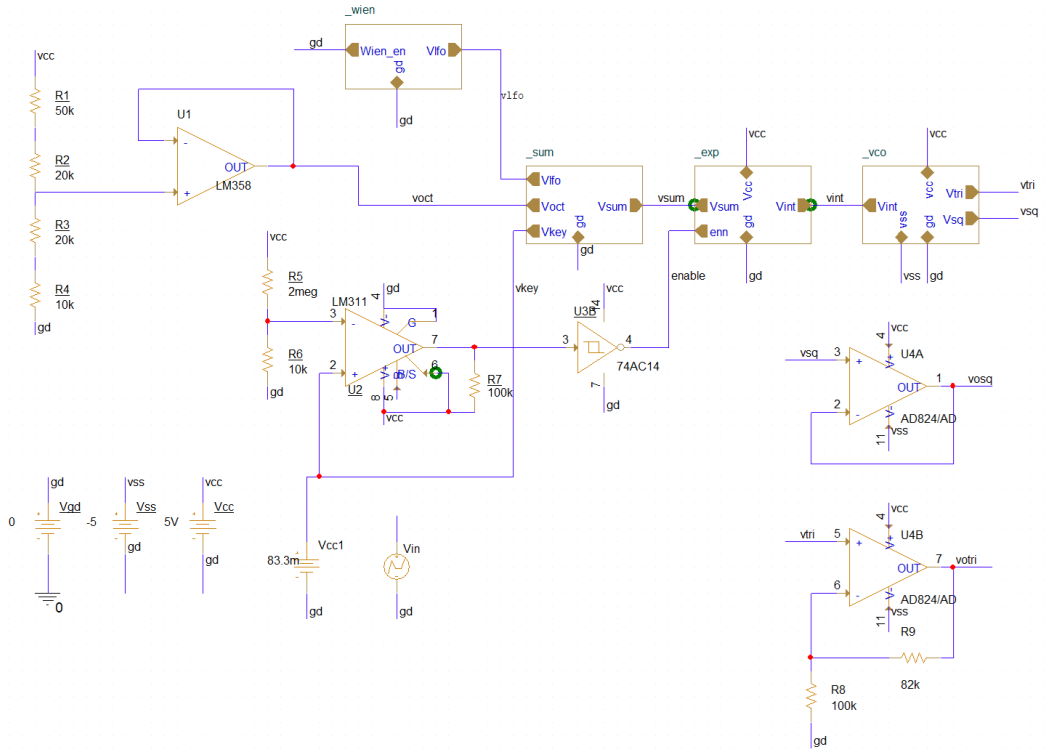

Figure 19: Top level schematic view of the synthesizer.

3.6 Circuit response to input signal

To ensure that the output signal is generated only while an input key signal is present, the V_{key} input is also connected to a comparator with a threshold set to approximately 20 mV. Even the smallest valid input step (83.3 mV) causes the comparator output to switch to a high state. The subsequent inverter then pulls the *enn* control signal to ground.

As shown in Figure 9, the *enn* signal is connected to the non-inverting input of the amplifier, and the circuit operates correctly only when this node is held at zero potential. When no input signal is present, the comparator output remains low, and the inverter pulls *enn* to V_{cc}, which prevents current flow through the transistors in the exponential converter and then into the input of the VCO.

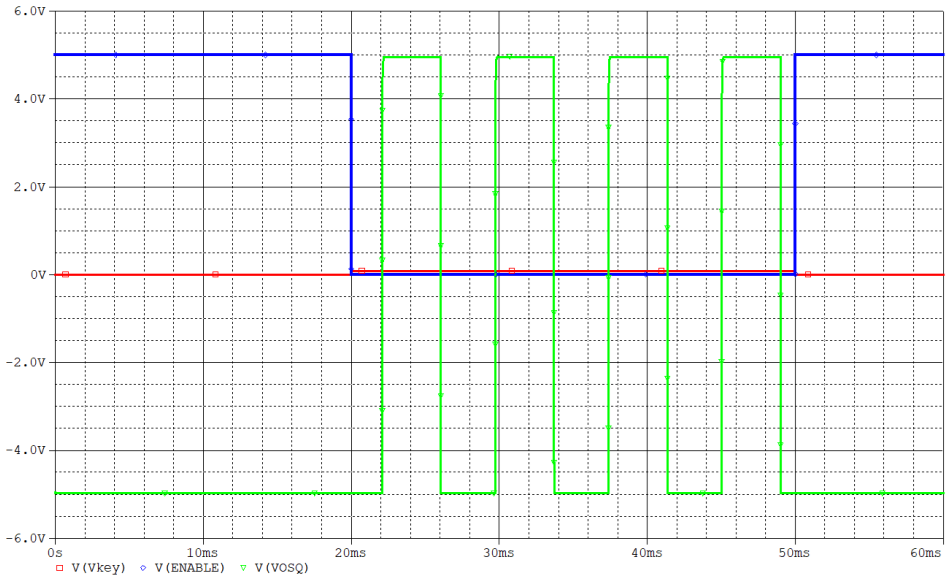

Figure 20: Transient simulation with tested enable press.

As the comparator, a classic LM311 is used together with a pull-up resistor R_7, which also drives the enable pin of the 74AC14 inverter. Both components provide correct operation, as can be observed in the simulation traces shown in Figure 20.

To verify that the design correctly pulls the enable pin to a low logic level (blue trace), the lowest possible voltage was applied to the input V_{key} (red trace). The results confirm that the functional test was successful: the circuit generates an output signal only when a valid control voltage is present at the input.

3.6.1 Vlfo enabled

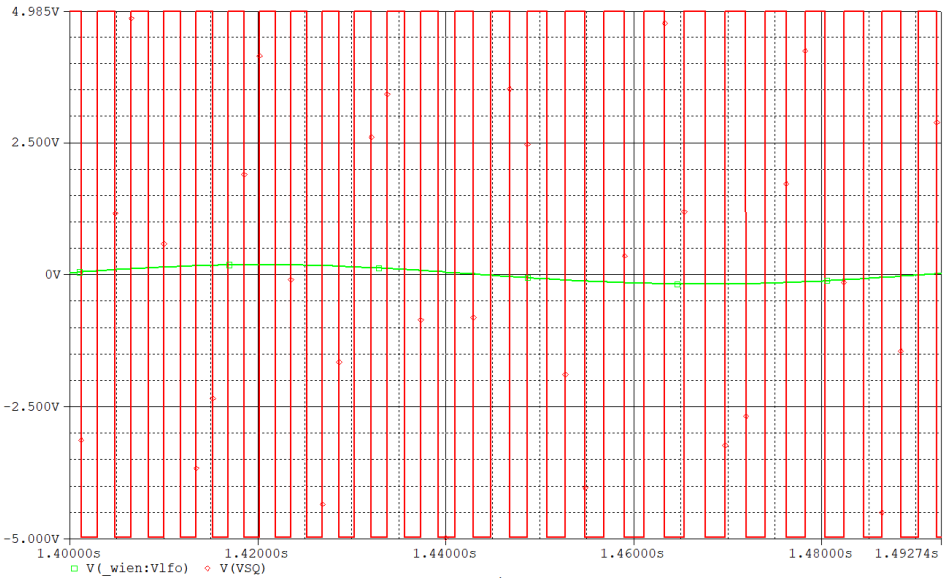

Figure 21: Transient simulation with enabled V_{lfo} and an input voltage of 83.3 mV.

The next tested functionality is the enablement of the LFO signal V_{lfo}, which is intended to modulate the main carrier. It is difficult to determine whether the modulation depth will be satisfactory for the user solely through simulation, it can be evaluated only by listening to the

final design. Figure 21 shows the simulation traces of the V_{lfo} signal together with the V_{sq}. The LFO is enabled by an internal switch controlled via the *Wien_en* pin.

With the applied input voltage, the synthesizer is expected to generate the note C of the fourth octave, corresponding to a frequency of 261.6 Hz, as listed in Table 4. The maximum positive deviation results in a frequency of 299.34 Hz, while the maximum negative deviation yields 231.24 Hz.

If the modulation is not satisfactory, the gain of the amplifier after the output of the Wien generator can be increased to create a wider spread in frequency.

4. PCB Layout and Component Selection

Compared to the simulation schematics, the final design differs only by the addition of switches and input connectors implemented as female jacks. For testing purposes, the VCO is connected via jumpers, allowing it to be electrically separated from the rest of the system. This approach simplifies debugging and standalone testing of the oscillator. The complete solution is shown in Figure 22 as the KiCad schematic and can be find at the GitHub repository [10].

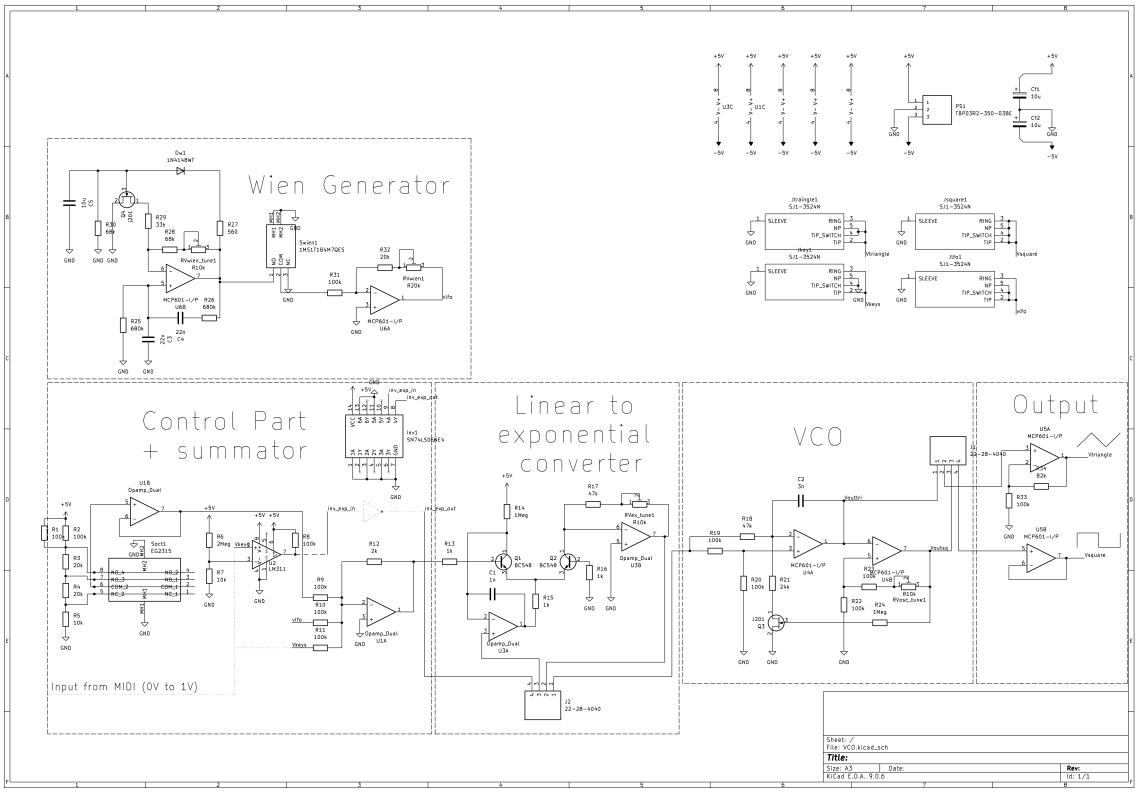

Figure 22: Schematic of the final design in KiCad.

4.1 PCB Design

The PCB layout of the design is relatively straightforward, as the system can be clearly divided into functional blocks. From left to right, the board contains the output buffers, the VCO core, the exponential converter, the summing amplifier, the LFO, and the power supply section. Along one edge of the board, the input connectors and mechanical elements accessible to the user are placed.

Since the device is intended for audio applications and operates exclusively with low frequency signals, high frequency layout effects should not influence the overall functionality.

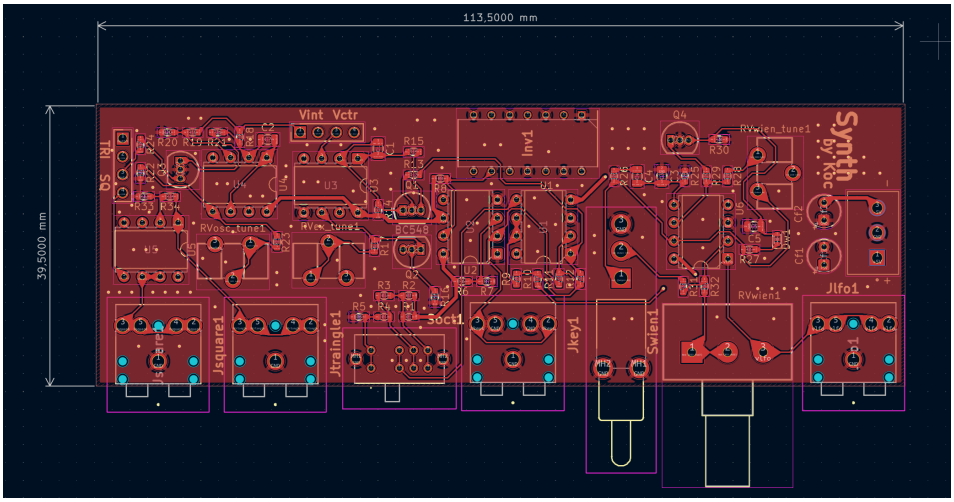

Figure 23: Bottom layer layout of the PCB.

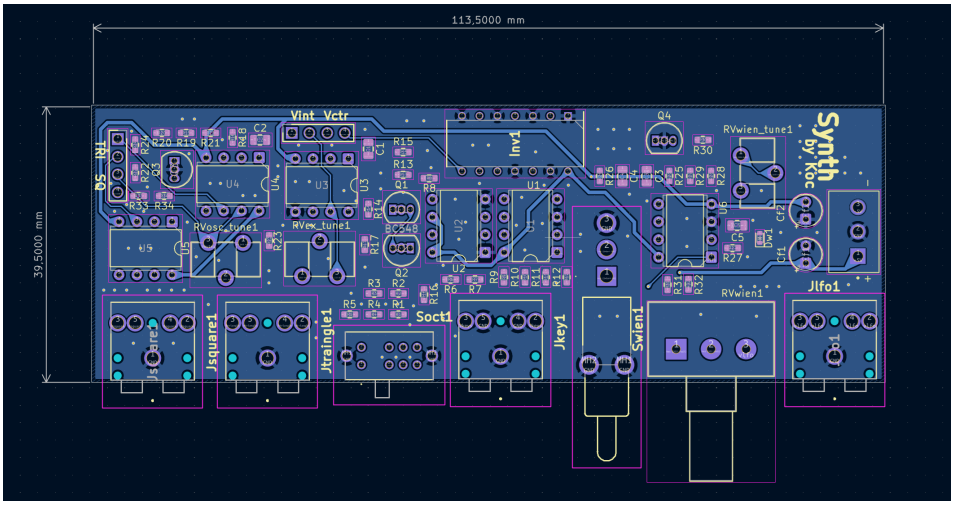

Figure 24: Top layer layout of the PCB.

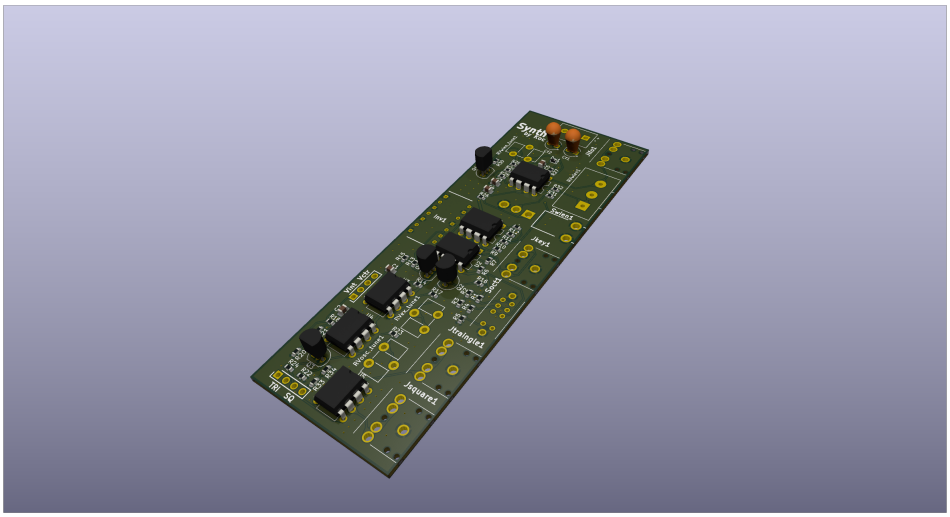

Figure 25: 3D view of the PCB model.

4.2 Component Selection Criteria and BOM

Table 5 lists the components used in the proposed design. Most of them have been discussed earlier, including the active devices such as operational amplifiers and transistors. It is important to note that all passive components should have a tolerance of 1 % or better, as larger tolerances may lead to significant parameter deviations and negatively affect tuning accuracy.

Components such as switches and connectors can be selected according to user preference. Their exact choice is not critical for the functionality of the design and mainly depends on the intended application, user requirements, and available budget.

Potentiometers $RV_{\text{wien\_tune1}}$, $RV_{\text{ex\_tune1}}$, and $RV_{\text{osc\_tune1}}$ are intended for one time trimming to compensate for component tolerances. These elements are mounted on the PCB and are not intended for regular user access. In contrast, potentiometer RV_{wien1} is designed to be accessible from the front panel, allowing the user to adjust the LFO operation during normal use.

Table 5: Bill of Materials (BOM)

Qty	Component	Value / Type	Designators	Footprint
1	Slide Switch	EG2315	Soct1	EG2315
2	Pin Header	22-28-4040	J1, J2	HDRV4W66P0X254 _1X4_1016X249X838P
1	Capacitor	3 nF	C2	C_0805_2012Metric
1	Capacitor	1 nF	C1	C_0805_2012Metric
2	Capacitor	22 nF	C3, C4	C_0805_2012Metric
1	Capacitor	10 μF	C5	C_0805_2012Metric
2	Capacitor	10 μF	Cf1, Cf2	CP_Radial_Tantal_ D4.5mm_P2.50mm
2	OpAmp	LM358	U1, U3	DIP-8_W7.62mm
3	OpAmp	MCP602-I/P	U4, U5, U6	DIP-8_W7.62mm
1	Comparator	LM311	U2	DIP-8_W7.62mm
1	Inverter	SN74LS06NE4	Inv1	DIP794W53P254L 1930H508Q14N
2	BJT	BC548	Q1, Q2	TO-92_Inline
2	JFET	J201	Q3, Q4	TO-92_Inline
1	Diode	1N4148WT	Dw1	D_SOD-523
12	Resistor	100 kΩ	R1, R2, R8, R9, R10, R11, R19, R20, R22, R23, R31, R33	R_0603_1608Metric
2	Resistor	680 kΩ	R25, R26	R_0603_1608Metric
2	Resistor	1 MΩ	R14, R24	R_0603_1608Metric
1	Resistor	2 MΩ	R6	R_0603_1608Metric
2	Resistor	68 kΩ	R28, R30	R_0603_1608Metric
1	Resistor	82 kΩ	R34	R_0603_1608Metric
1	Resistor	33 kΩ	R29	R_0603_1608Metric
3	Resistor	20 kΩ	R3, R4, R32	R_0603_1608Metric
2	Resistor	47 kΩ	R17, R18	R_0603_1608Metric
2	Resistor	10 kΩ	R5, R7	R_0603_1608Metric
3	Resistor	1 kΩ	R13, R15, R16	R_0603_1608Metric
1	Resistor	560 Ω	R27	R_0603_1608Metric
1	Resistor	2 kΩ	R12	R_0603_1608Metric

Qty	Component	Value / Type	Designators	Footprint
3	Pot	10 kΩ	RVex_tune1, RVosc_tune1, RVwien_tune1	Potentiometer_ACP _CA9-H5_Horizontal
1	Pot	20 kΩ	RVwien1	Potentiometer _Alps_RK163 _Single_Horizontal
4	Jack Con	SJ1-3524N	Jtriangle1, Jsquare1, Jkey1, Jlfo1	SJ13524N
1	Terminal	TBP03R2-350-03BE	PS1	CUI_TBP03R2-350-03BE
1	T Switch	1MS1T1B4M7	Swien1	1MS1T1B4M7QES

5. Conclusions

5.1 Summary of the Work

The presented project demonstrates that the proposed analog synthesizer design meets the majority of the initial functional and design assumptions. The system was successfully designed, analyzed, and simulated, resulting in a complete and coherent architecture that is ready for hardware implementation and experimental verification. The adopted block structure, together with the selected components, provides a solid basis for further development and practical use.

The main limitation identified during the analysis concerns the accuracy of frequency generation in the higher part of the operating range, particularly within the second octave. Due to the frequency dependent behavior of the triangular waveform amplitude, the generated frequency increasingly deviates from the ideal, theoretically calculated value, as shown in figure 15. This effect introduces the main source of tuning error in the current design.

5.2 Future Work

Based on the results obtained in this project, several directions for future development can be identified:

- Perform a Monte Carlo analysis to evaluate the influence of component tolerances, identify critical parameters, and determine the required trimming range in the final hardware.
- Conduct a spectral analysis of the output waveforms in order to evaluate harmonic content, signal purity, and the presence of timing jitter.
- Improve the output buffering stage, as the current design does not provide sufficient current capability to directly drive loudspeakers; this may require a dedicated output driver or a modified voltage domain.
- Add capacitors at the outputs to eliminate DC components.
- Validate the complete system under real operating conditions through hardware measurements and listening tests.

References

[1] Ray Wilson. *Make: Analog Synthesizers*. Maker Media, Sebastopol, CA, 2013.

[2] Elliot Williams. The Polyphonic Analog-Digital Synth Project. *Hackaday*, 2018. Available at: https://hackaday.com/2018/10/21/the-polyphonic-analog-digital-synth-project/ Accessed: 2026-01-31.

[3] David Wright. *The Mathematics of Music*. Institute of Physics Publishing, Bristol, 2009.

[4] Donald E. Hall. *Musical Acoustics*. 3rd edition. Brooks/Cole, Pacific Grove, CA, 2002.

[5] Thomas D. Rossing. Tuning and temperament. *Encyclopaedia Britannica*. Available at: https://www.britannica.com/art/tuning-and-temperament/Tuning-and-musical-history Accessed: 2026-01-31.

[6] Kevin Lightner. Moog synthesizer schematics collection. *Hylander Electronics Archive*. Available at: http://www.hylander.com/moogschematics.html Accessed: 2026-01-31.

[7] Paul Horowitz and Winfield Hill. *The Art of Electronics*. 3rd edition. Cambridge University Press, Cambridge, 2015.

[8] B. Pankiewicz. Analogowe układy elektroniczne [*Analog Electronic Circuits*]. Skrypt dydaktyczny, Politechnika Gdańska, Wydział ETI. Available at: http://www.ue.eti.pg.gda.pl/~bpa/aue/aue.pdf Accessed: 2026-01-31.

[9] Thomas Henry Schmitz. Exponential Converter Tutorial. *Schmitzbits Blog*. Available at: https://www.schmitzbits.de/expo_tutorial/ Accessed: 2026-01-31.

[10] J. Koc. Synthesizer with 1V/oct input and LFO. GitHub repository. Available at: https://github.com/Ekstazaa/Synthesizer-with-1V-input-and-LFO.