Case Study of RISC pipelining

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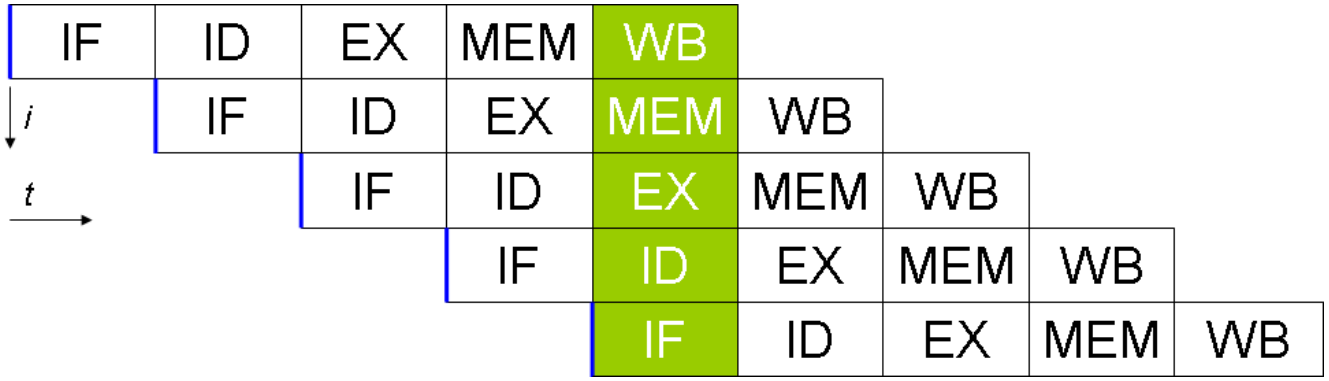
Section- A

RISC pipelining

- Reduced Instruction Set Computer(RISC) Architecture was discovered by John Cocke in 1974.
- RISC is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions which are often found in other types of architecture.
- The new architecture design enabled computers to run much faster than previously.

Stages of RISC pipelining

- Instruction fetch
- Instruction decode
- Execute
- Memory access
- Writeback



Characteristics of RISC Architecture

- The CPU takes less silicon area to implement, and also runs faster.
- Simple Addressing Modes
- Simple Instruction formats
- Complex Operations are executed as sequence of simple instructions.

Advantages of RISC

- Less Design Complexity
- Reducing Design Cost
- Reducing the time between Designing and Marketing

Disadvantages of RISC

- It usually leads to longer programs, which needs larger memory space to store
- Time Consuming
- More Memory Access may be needed