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FPGA-Accelerated Retinex Image Enhancement for Low-Light Conditions

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Abstract: Real-time low-light image enhancement is essential for various applications, including advanced driver assistance systems (ADAS), remote sensing, and object tracking. Among the commonly used techniques, Retinex-based algorithms are particularly effective in restoring visibility in low-light conditions [10] by simulating the way human vision perceives color and brightness. However, these algorithms typically involve complex mathematical computations over large spatial regions, making their hardware implementation challenging and resource-intensive. Due to these difficulties, only a limited number of researchers have focused on addressing this issue. In this context, we propose a novel Retinex-based algorithm that incorporates a low-cost edge-preserving filter for efficient illumination estimation. By making certain approximations to reduce hardware logic resource requirements, our approach ensures a more practical and cost-effective implementation while maintaining the quality of the enhanced image, making it suitable for real-time applications.

Keywords: Retinex based algorithm, Low light image enhancement

1.Introduction:FPGA-based implementations of Retinex algorithms provide an efficient solution for real-time applications. Field-Programmable Gate Arrays (FPGAs) are known for their parallel processing capabilities, low latency, and high flexibility. These features make FPGAs an ideal platform for computationally intensive image processing tasks.

The computational complexity of Retinex algorithms poses challenges for hardware implementation. Conventional methods often rely on iterative or multiscale processing, which can be resource-intensive. Therefore, a low-cost FPGA implementation requires a carefully designed architecture to balance computational efficiency, hardware resource utilization, and image quality. Optimizing the algorithm for FPGA deployment involves simplifications, pipelining, and parallelism, all of which contribute to a faster and more efficient system. One key advantage of using FPGAs for low-light image enhancement is the ability to process high-resolution images in real-time. This capability is crucial in applications like autonomous vehicles [1] and surveillance, where decisions must be made quickly based on enhanced visual data [2]. Moreover, FPGA implementations are highly customizable, allowing for adjustments to the algorithm to meet specific application requirements. Techniques in [4] and [5] use Gaussian filters for illumination estimation, while the LIME technique in [6] enhances low-light images by imposing structural information on the illumination channel, offering an efficient approach for LLIE. This flexibility is particularly valuable in diverse environments, such as indoor and outdoor settings, where lighting conditions can vary significantly.

In addition to real-time performance, FPGA-based Retinex implementations can

achieve significant reductions in power consumption compared to GPU or CPU-based approaches.

The design of a low-cost FPGA implementation involves several considerations, including resource constraints, precision, and memory requirements. For instance, fixed-point arithmetic is often preferred over floating-point to save hardware resources while maintaining acceptable accuracy. Additionally, memory usage must be carefully managed to store intermediate data and ensure smooth data flow throughout the pipeline. These design decisions significantly influence the performance and cost of the final implementation. Over-enhancement, halo artifacts, and color distortion are common issues that must be addressed during implementation. FPGA-based designs [12] can incorporate pre-processing and post-processing modules to mitigate these effects. For example, filtering techniques can smoothen edges and reduce noise, while color correction modules ensure that the enhanced images retain natural color tones. These additional features further enhance the overall image quality.

In practical terms, an FPGA implementation of a Retinex-based algorithm involves several stages, including illumination estimation, reflectance computation, and contrast adjustment. Each stage is mapped to dedicated hardware modules to exploit parallelism. For instance, illumination estimation can be achieved using a Gaussian filter, which is implemented as a series of parallel convolution operations. Similarly, reflectance computation and contrast adjustment are designed to maximize throughput and minimize latency.

Testing and validating the FPGA implementation is a critical step in the development process [13] . The design must be verified using standard image datasets to ensure its effectiveness in enhancing low-light images. Metrics such as Peak Signal-to-Noise Ratio (PSNR), Structural Similarity Index (SSIM), and computational latency are commonly used to evaluate performance [14]. The results are compared against software-based implementations to demonstrate the benefits of the FPGA approach.

2. Proposed Method

2.1. Retinex based algorithm

The **Retinex model** describes an image P(x,y)P(x, y) as the product of **illumination** E(x,y)E(x, y) and **reflectance** R(x,y)R(x, y), where (x,y)(x, y) represents pixel coordinates. In this model, **illumination** signifies light intensity and is expected to be **smooth and free of textures**, while **reflectance** contains the fine details and textures of the image. The goal is to estimate illumination in a way that retains edges while smoothing out textural variations.

The **Retinex model** explains an image as the combination of illumination and reflectance, where illumination represents light intensity and should be smooth without textures, while reflectance contains the detailed textures and edges of the image. The primary objective of this model is to estimate illumination in a way that enhances visibility while preserving fine details.

To begin the enhancement process, a **coarse illumination** map is extracted by identifying the highest intensity value in a local region. However, this initial estimate often introduces blocky artifacts, making it unsuitable for direct reflectance computation. To address this issue, an **edge-preserving filter** is applied. An edge-preserving filter is proposed in [8] for efficient illumination estimation .This filter ensures that illumination remains smooth while maintaining sharp transitions at object boundaries, preventing artificial distortions.

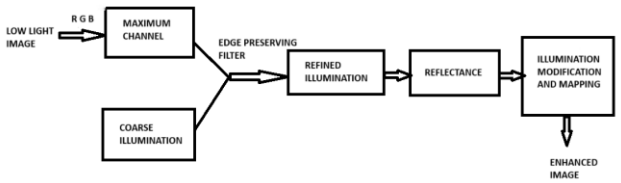
The filter operates based on a **guidance image**, which is derived from the maximum intensity channel of the input image. Instead of averaging over an entire region, which would require significant computational resources, the filter simplifies the process by reducing the dimensionality of the operation. This optimization significantly lowers hardware complexity while still effectively refining the illumination estimation.

One of the key advantages of this approach is its ability to **preserve edges** while eliminating unwanted artifacts. By assigning lower weights to pixels that differ significantly from their surroundings, the filter ensures a natural and visually appealing enhancement. Additionally, the refined illumination [11] values are carefully adjusted to remain within a valid range, preventing unwanted distortions and ensuring that details are well-preserved.

To further improve visibility, the refined illumination undergoes a **contrast enhancement** step [3], which adjusts brightness and improves contrast without introducing unnatural effects. Finally, the enhanced illumination is combined with the reflectance information to reconstruct a **visually enhanced image** that retains fine details while improving brightness and clarity.

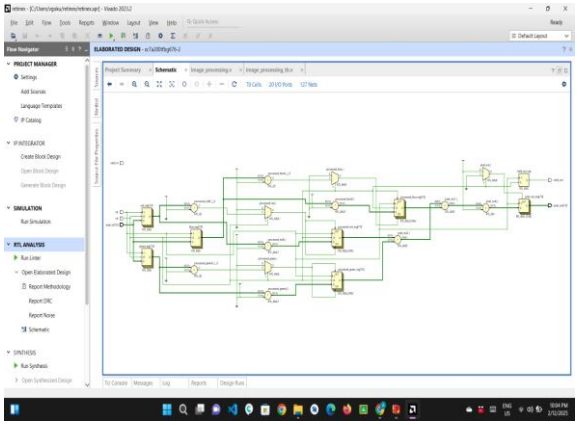
This method is particularly effective for low-light image enhancement, as it ensures a balanced improvement in brightness, contrast, and detail preservation [7], leading to clearer and more visually appealing images.

3 Block diagram



The block diagram illustrates a **Retinex-based low-light image enhancement framework** that improves visibility by estimating illumination and reflectance while preserving essential details. The process begins with a **low-light RGB image input**, where the **maximum intensity channel** is extracted to approximate illumination, based on the assumption that at least one color channel captures sufficient brightness. Simultaneously, a **coarse illumination estimation** is generated as an initial approximation of the lighting conditions. To enhance accuracy, an **edge-preserving filter** is applied, which smooths illumination variations while retaining sharp edges, preventing distortion in the final output. The refined illumination obtained from this step provides a more reliable estimate of the lighting distribution in the image. Next, the system computes **reflectance** using the **Retinex model**, where the original image is divided by the refined illumination, enhancing details while balancing brightness variations. This refined illumination is then **modified and mapped** using a transformation function to adjust brightness and contrast, ensuring a more natural and visually appealing output. The final result is an **enhanced image** with improved clarity [9] and visibility, making it ideal for applications such as **night vision, ADAS, remote sensing, and surveillance**. This efficient approach ensures real-time performance while maintaining computational feasibility, making it well-suited for FPGA and embedded system implementations.

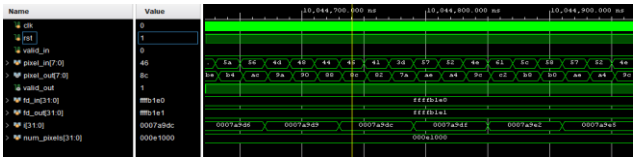
4.Circuit diagram

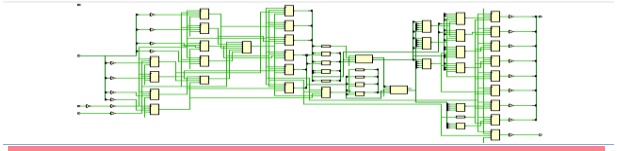


The image displays an **RTL (Register Transfer Level) schematic** of an image processing module designed in **Xilinx Vivado 2023.2**. This hardware implementation appears to be based on the **Retinex model** for image enhancement, as suggested by the project name "retinex." The circuit comprises several key components, including **multipliers (RTL_MULT), registers (RTL_REG), adders (RTL_ADD), and synchronization blocks (RTL_REG_SYNC)**, all working together to process input pixel data efficiently. Multipliers handle intensity scaling and normalization, while adders perform arithmetic operations for contrast enhancement. Registers and synchronization blocks ensure proper data alignment and prevent timing mismatches during real-time processing. The design takes **pixel input values**, processes them through various computational stages, and produces **enhanced pixel output**, with a **valid_out signal** indicating the readiness of the processed data. Optimized for **real-time applications**, this FPGA-based implementation is well-suited for tasks such as **Advanced Driver Assistance Systems (ADAS) and remote sensing**, where effective low-light image enhancement is essential. The structured

design demonstrates a balance between **computational efficiency and image quality**, making it ideal for high-performance applications.

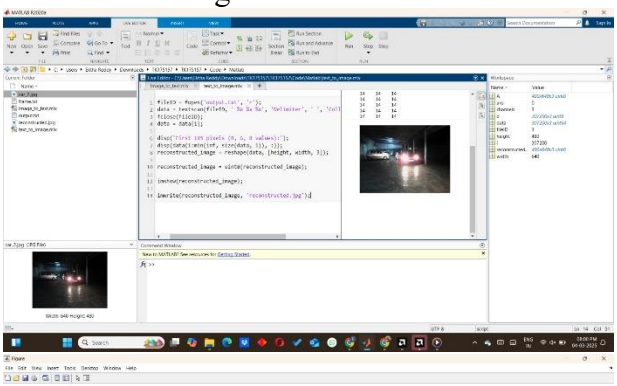
5.Results





As synthesis and implementation complete, DRC violations, timing values, utilization percentages, and power estimates are also populated

Using the matlab tool we can view the output of enhanced images



6.Conclusion

Real-time low-light image enhancement is critical for a wide range of applications, particularly in fields like advanced driver assistance systems, remote sensing, and object tracking. Retinex-based algorithms have proven to be effective in simulating human visual perception to enhance visibility in challenging lighting conditions. However, their complex mathematical computations often present significant challenges in hardware implementation, making them resource-intensive. To address this, our proposed approach introduces a novel Retinex-based algorithm that incorporates a low-cost edge-preserving filter, optimizing the illumination estimation process. By making approximations to reduce hardware complexity, our method ensures an efficient, cost-effective solution while preserving image quality, making it suitable for real-time implementation in practical scenarios.

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