counter Project Status (12/25/2020 - 21:55:57)			
Project File:	counter.xise	**Parser Errors:**	No Errors
Module Name:	counter	**Implementation State:**	Synthesized (Failed)
Target Device:	xc6slx4-2tqg144	• **Errors:**	X 1 Error (0 new)
Product Version:	ISE 14.7	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Current Errors	[-]
Synthesis Errors	
ERROR:HDLCompiler:926: - "E:\ITI intake 41\LABS\VHDL\counter\counter.vhd" Line 18: Multiple wait statements in one process are not supported in this case.	

Current Warnings	[-]
No Warnings Found	

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Dec 25 21:55:56 2020	X 1 Error (0 new)	0	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**
ISIM Simulator Log	Out of Date	Fri Dec 25 20:56:27 2020

Date Generated: 12/25/2020 - 21:55:57