full_adder Project Status			
Project File:	fulladder.xise	**Parser Errors:**	No Errors
Module Name:	full_adder	**Implementation State:**	Programming File Generated
Target Device:	xc6slx4-2tqg144	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Current Errors	[-]
No Errors Found	

Current Warnings	[-]
No Warnings Found	

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	4,800	0%	
Number of Slice LUTs	1	2,400	1%	
Number used as logic	1	2,400	1%	
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	1			
Number used as ROM	0			
Number used as Memory	0	1,200	0%	
Number of occupied Slices	1	600	1%	
Number of MUXCYs used	0	1,200	0%	
Number of LUT Flip Flop pairs used	1			
Number with an unused Flip Flop	1	1	100%	
Number with an unused LUT	0	1	0%	
Number of fully used LUT-FF pairs	0	1	0%	
Number of slice register sites lost to control set restrictions	0	4,800	0%	

Number of bonded IOBs	5	102	4%	
Number of RAMB16BWERs	0	12	0%	
Number of RAMB8BWERs	0	24	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	0	16	0%	
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	200	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	200	0%	
Number of OLOGIC2/OSERDES2s	0	200	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	8	0%	
Number of ICAPs	0	1	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	1.00			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:			

Failing Constraints	[-]
All Constraints Were Met	

Clock Report	[-]
Data Not Yet Available	

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**

Synthesis Report	Current	Fri Dec 25 17:02:46 2020	0	0	1 Info (1 new, 0 filtered)
Translation Report	Current	Fri Dec 25 17:05:31 2020	0	0	0
Map Report	Current	Fri Dec 25 17:05:41 2020	0	0	6 Infos (6 new, 0 filtered)
Place and Route Report	Current	Fri Dec 25 17:05:51 2020	0	0	2 Infos (2 new, 0 filtered)
Power Report					
Post-PAR Static Timing Report	Current	Fri Dec 25 17:05:57 2020	0	0	4 Infos (4 new, 0 filtered)
Bitgen Report	Current	Fri Dec 25 17:16:11 2020	0	0	0

Secondary Reports		[-]
Report Name	**Status**	**Generated**
ISIM Simulator Log	Current	Fri Dec 25 20:45:54 2020
WebTalk Report	Current	Fri Dec 25 17:16:12 2020
WebTalk Log File	Current	Fri Dec 25 17:16:14 2020

Date Generated: 12/25/2020 - 21:52:49