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Master Thesis

Temperature Distribution of an IGBT Chip during Repetitive
Switching Events under Consideration of Front-Side Ageing

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Abstract

In this work, a repetitive switching control pattern has to be established in order to determine the impact of front-side ageing mechanisms on the temperature development of an IGBT chip beyond a single switching event. As topology, a converter like assembly with two IGBT switches and diodes has to be utilized. In fact, a 100 A and 650 V Infineon Econo Pack module will be used. The Device Under Test (DUT) has to be equipped to a proper cooling facility and different methods of temperature sensing have to be evaluated and applied. Front-side ageing mechanisms need to be discussed theoretically, but will be created artificially. The temperature distribution for each ageing state and the development for subsequent ageing steps, is supposed to be evaluated in detail. Further, different switching frequencies have to be performed and the impact on the temperature development has to be compared.

- Preliminary considerations
 - Front-side ageing mechanisms
 - Switching behaviour of a high voltage IGBT
 - Discussion of different temperature sensing methods and Temperature Sensitive Parameters (TSEPs)
- Test setup
 - Implementation and testing of suitable repetitive switching control scheme
 - Assembly of test setup with special consideration of cooling facility, temperature sensing equipment, and power losses
- Measurement
 - Performance of calibration procedures with respect to chosen TSEP
 - Execution of repetitive switching events for different frequencies and ageing states until thermal saturation
 - Creation of artificial front-side ageing with respect to the temperature distribution of the present state
- Evaluation

-
- Temperature development at different positions of the DUT for different ageing states and frequencies with respect to repetitive switching events

Contents

Nomenclature	XII
1 Introduction	1
2 Theory	3
2.1 Switching-Off Behaviour of IGBT	3
2.2 Structure of Power Module	9
2.2.1 Introduction of Standard Module Package	9
2.2.2 Modelling of Front-Side	9
2.3 Degradations on Front-side	11
2.3.1 Bond-Wire Lift-off	11
2.3.2 Reconstruction of Emitter Metallization	15
3 TSEPs	17
3.1 Approaches of Junction Temperature Determining	17
3.1.1 Optical Methods	17
3.1.2 Physical Methods	18
3.1.3 Electrical Methods	18
3.2 Evaluation of TSEPs without Measurement	22
3.2.1 t_{doff} and t_{off}	22
3.2.2 $V_{GE(th)}$	23
3.2.3 dV_{CE}/dt	23
3.2.4 I_{tail}	23
3.3 di_C/dt_max as alternative TSEP	25
3.3.1 Derivation of Temperature Dependency	25
3.3.2 Impact on $R_{G(off)}$	26
3.3.3 Impact on I_C	29
3.3.4 Conclusion	30

Contents

3.4	V_{Miller} as alternative TSEP	30
3.4.1	Derivation of Temperature Dependency	30
3.4.2	Impact on $R_{G(off)}$	32
3.4.3	Impact on I_C	34
3.4.4	Impact on Ageing State	34
3.4.5	Conclusion	35
3.5	$V_{CE(on-sense)}$ as alternative TSEP	35
3.5.1	Derivation of Temperature Dependency	35
3.5.2	Impact on T	36
3.5.3	Conclusion	37
3.6	$V_{CE(on-load)}$ as alternative TSEP	37
3.6.1	Derivation of Temperature Dependency	37
3.6.2	Impact on I_C	38
3.6.3	Impact on Ageing State	39
3.6.4	Summary of Temperature Dependency for $V_{CE(on-load)}$. . .	43
3.6.5	Conclusion	44
4	Calibration	45
4.1	Setup	45
4.2	Approach	46
4.3	Accuracy Evaluation	47
4.3.1	Current Slope and Induced Gate Voltage	47
4.3.2	Self-Heating	48
4.3.3	Inaccuracy of I_C Measurement	49
4.3.4	Parameters for $V_{CE(on-load)} = f(T_j)$ during Calibration and Repetitive Operation	51
4.3.5	Summary of Measurement Deviations	53
5	Repetitive Switching Operation	55
5.1	Test Bench Setup	55
5.1.1	HV	55
5.1.2	PIGBT	56

5.1.3	IGBT Module	56
5.1.4	Clamping Circuit	57
5.1.5	Measuring Probe	59
5.2	Pulse Pattern	60
5.2.1	Aim and Approach	60
5.2.2	Illustration of Waveforms Based on Pulse Pattern	61
5.3	Current Development	63
5.4	Determination of Temperature	64
5.4.1	Case Temperature T_C	64
5.4.2	Junction Temperature T_j	64
5.4.3	Surface and Segment Temperature	66
5.5	Description of Ageing State	68
5.6	Summary of Repetitive Investigation	69
6	Results	71
6.1	I_C and P_{cond}	71
6.1.1	Development of I_C	71
6.1.2	P_{cond}	71
6.2	T_C	73
6.2.1	Development of T_C	75
6.2.2	Comparison 1000 Hz with 500 Hz	75
6.2.3	Explanation for Unexpected Results	75
6.3	T_j	75
6.3.1	Development of T_j	77
6.3.2	Comparison 1000 Hz with 500 Hz	77
6.3.3	Note for Unexpected Results	77
6.4	$T_{surface}$ and $T_{segment}$	77
6.4.1	$SoL - 0$	78
6.4.2	$SoL - 1$	79
6.4.3	$SoL - 2$	80
6.4.4	$SoL - 3$	81

Contents

6.4.5	Comparison of $T_{segment}$ under each SoL	81
7	Summary and Outlook	85
7.1	Summary	85
7.2	Outlook	86
7.2.1	DUT	86
7.2.2	IR-Camera	86
7.2.3	Pulse-Pattern	87
7.2.4	Current Measurement	87
7.2.5	$V_{CE(on-sense)}$ as TSEP	87
A	Appendix	i
A.1	Derivation of Equations	i
A.1.1	Carrier Density and Mobilities	i
A.1.2	Temperature Dependency of $V_{GE(th)}$	ii
A.2	Additional Informations with Respect to Repetitive Investigation . .	iii
A.2.1	Calibration	iii
A.2.2	Repetitive Operation	iii
References		xii

Nomenclature

Abbreviation

Abbreviation	Description
ADC	Analog-Digital Converter
BNC	Bayonet Neill-Concelman Connector
CTE	Coefficient of Temperature Expansion
DCB	Direct Copper Bonded
DUT	Device Under Test
EoL	End of Life
EoU	End of Usability
FWD	Free-Wheeling Diode
GDU	Gate Drive Unit
HS	High-Side
HV	High Voltage
IGBT	Isolated-Gate Bipolar Transistor
IR-Camera	Infrared Camera
LS	Low-Side
MOSFET	Metal-Oxide-Simiconductor Field-Effect Transistor
PCT	Power Cycling Test
PIGBT	Protection IGBT
SMA	Sub Miniature version A
SoL	State of Life
TSEP	Temperature Sensitive Electrical Parameter

Symbols

Symbol	Description	Unit
A	Sensitivity of TSEP	-
B	Offset of TSEP	-
C_{GC}	Miller Capacitance	F
C_{GE}	Gate Capacitance	F
C_{ox}	Oxide Capacitance	F
C_{SC}	Space Charge Capacitance	F
di/dt_{max}	Maximal Current Slope during Turn-Off	A/ μ s
dV_{CE}/dt	Voltage Slope during Turn-Off	V/ μ s
E	Electric Field	V/cm
$E_{g(0)}$	Bandgap at 0 K	V
f	Switching Frequency	Hz
g_{fs}	Transconductance	Ω
I_C	Collector Current	A
$I_{C(calib)}$	Collector Current during Calibration	A
$I_{C(DC+)}$	Current of Busbar Plus	A
$I_{C(rep)}$	Collector Current during Repetitive Operation	A
I_{Load}	Load Current	A
I_{tail}	Tail Current	A
J	Current Density	A/cm ²
L	Length of Channel	cm
L_{par}	Parasitic Inductance	nH
L_{Load}	Load Inductance	H
N_D	Donator Density	cm ⁻³
n_i	Intrinsic Carrier Density	cm ⁻³
n	Density of Free Electrons	cm ⁻³
p	Density of Free Holes	cm ⁻³
P_{cond}	Conductive Power Loss	W
R_{bw}	Bond-Wire Resistance	Ω

$R_{discharge}$	Discharge Resistance	Ω
R_{eE}	Equivalent Resistance between Kelvin and Load Terminal	Ω
$R_{G(int)}$	Internal Gate Resistance	Ω
$R_{G(on)}$	External Gate Resistance during Turn-On	Ω
$R_{G(off)}$	External Gate Resistance during Turn-Off	Ω
R_{par}	Parasitic Resistance of Load Coil	Ω
R_{Seg}	Segment Resistance	Ω
R_{Sum}	Equivalent Resistance within Chip	Ω
R_{Surf}	Emitter Surface Resistance	Ω
$SoL - 0$	State of Life without Bond-Wire Cut	-
$SoL - 1$	State of Life with One Bond-Wire Cut	-
$SoL - 2$	State of Life with Two Bond-Wires Cut	-
$SoL - 3$	State of Life with Three Bond-Wires Cut	-
t_{doff}	Turn-Off Delay Time	μs
t_{off}	Turn-Off Time	μs
t_{on}	Turn-On Time	μs
T_c	Case Temperature	$^{\circ}\text{C}$
T_j	Junction Temperature	$^{\circ}\text{C}$
$T_{segment}$	Segment Temperature	$^{\circ}\text{C}$
$T_{surface}$	Emitter Surface Temperature	$^{\circ}\text{C}$
$V_{CE(off)}$	Collector-Emitter Voltage during Off-State	V
$V_{CE(on)}$	Collector-Emitter Voltage during On-State	V
$V_{CE(on-chip)}$	Collector-Emitter Voltage under Load Current without Package	V
$V_{CE(on-Kelvin)}$	Collector-Emitter Voltage under Load Current, Measured at Kelvin Terminal (see Figure 3.20)	V
$V_{CE(on-load)}$	Collector-Emitter Voltage under Load Current, Measured at Load Terminal (see Figure 2.9(a))	V
$V_{CE(on-sense)}$	Collector-Emitter Voltage under Sense Current	mV

$V_{CE(peak)}$	Maximum of Collector-Emitter Voltage during Turn-Off	V
$V_{CE(on-calib)}$	Collector-Emitter Voltage during Calibration	V
$V_{CE(on-rep)}$	Collector-Emitter Voltage during Repetitive Operation	V
$V_{DC-link}$	Voltage of Power Source	V
V_{drift}	Drift Voltage	V
V_{DS}	Drain-Source Voltage	V
V_F	Forward Voltage	V
V_{FRM}	Maximum of Forward Voltage	V
$V_{GE(off)}$	Gate Voltage of IGBT during Off-State	V
$V_{GE(on)}$	Gate Voltage of IGBT during On-State	V
$V_{GE(th)}$	Gate Threshold Voltage of IGBT	V
V_{GS}	Gate Voltage of MOSFET	V
$V_{GS(th)}$	Gate Threshold Voltage of MOSFET	V
V_{Miller}	Miller Plateau	V
V_j	Build-In Voltage for Forward Voltage	V
V_Z	Zener-Voltage	V
W	Width of Channel	cm
w_B	Width of Space Charge	cm
α	temperature coefficient of resistivity	K ⁻¹
α_{pnp}	Bipolar Current Gain	-
ϵ	Permittivity	F/cm
κ	Channel Parameter	A(cm/V) ²
μ	Carrier Mobility	cm ² /Vs
ψ_B	Fermi Level from Intrinsic Fermi Level	V
τ_{eff}	Effective Carrier Lifetime	s

1 Introduction

Power electronic systems such as inverters and DC-DC converters play an essential role in the power conversion of the renewable energy industries. In order to apply power electronic systems in the automotive, solar and wind industry, they must convert current and voltage into the desired form as efficiently as possible. For this purpose, power semiconductor devices like Insulated Gate Bipolar Transistor (IGBT) are widely utilized as the key component in power electronic systems due to the high voltage and current ratings, conductivity modulation and comparable wide range of frequency.

Nonetheless, it is reported in [YBM⁺¹¹] that power semiconductor devices are concerned as the most fragile components in overall systems. This is because in the application, IGBTs are exposed to repetitive switching events with a certain setting of frequency, duty cycle, and current level. According to the simultaneous presence of current and voltage during switching, conduction, and blocking, the devices heat up. The heat is further transferred towards the back- and front-side of the device. A temperature gradient across the devices, including the applied packaging technology, can lead further to degradation effects or even failures of devices.

The temperature distribution of devices is expected to reach a phase of thermal equilibrium, when the generated thermal power losses meet the cooling capabilities given by the switching duty cycle and the applied cooling techniques at the back- and front-side of the device. Therefore, temperature distribution of IGBT during repetitive switching events influences on its reliability and performance. Furthermore, the determination of temperature distribution of devices is necessary to ensure optimal reliability and operation of power electronic systems. [BLDA13]

The main objective of this work was to investigate the temperature distribution of an IGBT chip during repetitive switching events under consideration of front-side ageing, especially when device reached to and beyond End of Life state.

2 Theory

In this chapter, basic theories with respect to IGBTs are introduced. At first, switching-off behaviour of an IGBT at each time interval is illustrated. After that, module package is depicted. Especially, front-side of the chip is modelled under consideration of bond-wire cut. Moreover, degradation and failures of power module with respect to front-side ageing are mentioned.

2.1 Switching-Off Behaviour of IGBT

An IGBT is made for switching between blocking and conducting state according to the applied gate voltage level. In general, IGBT switches under inductive load condition. In order to obtain the switching behaviour of IGBT device, a test circuit is illustrated in Figure 2.1. As shown in Figure 2.1(a), gate voltage V_{GE} , collector-

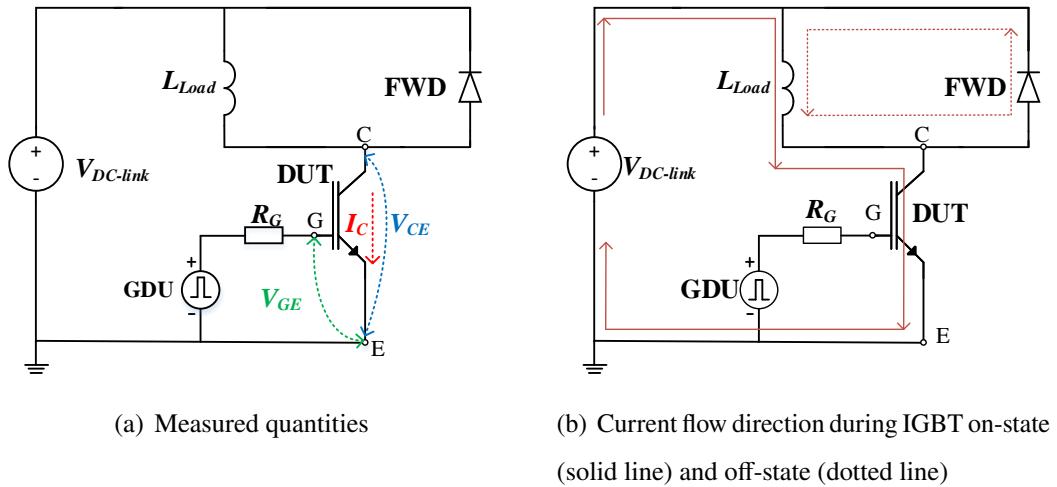


Figure 2.1: Schematic illustration of test circuit with inductive load

emitter voltage V_{CE} and collector current I_C are measured during test. DUT is controlled by gate driver unit (GDU) with an external gate resistor R_G and in series with the inductive load L_{load} . Especially, a freewheeling diode (FWD) is in parallel with the inductive load so current can continue to flow again after IGBT turns off.

Figure 2.1(b) depicts the current flow direction during turn-on and turn-off state

with solid and dotted lines, respectively. When IGBT turns on, current flows from busbar plus through load, DUT and back to busbar minus. Hence, load inductance is charged during turn-on. Load current i_C is determined by Equation (2.1):

$$V_{DC-link} = L_{load} \cdot \frac{di_C}{dt_{on}} \quad (2.1)$$

where $V_{DC-link}$ is the voltage of power source. I_C can be defined by means of on-time t_{on} via pulse program, if $V_{DC-link}$ and L_{load} are fixed.

According to [LSSDD18, BSE12], when analysing the transient switching behaviour, IGBT can be modelled as three capacitances, respective gate capacitance C_{GE} , Miller capacitance C_{GC} and collector-emitter capacitance C_{CE} . The switching operation is approximately equivalent to the charge and discharge phases of C_{GE} and C_{GC} [BSE12]. Figure 2.2(a) depicts these equivalent capacitances. Especially, C_{GC} consists of oxide capacitance C_{ox} and capacitance of space charge region C_{SC} . It can be inferred that C_{SC} depends strongly on the width of space charge. During switching-off, space charge region is expanded due to V_{CE} increasing, which results to C_{SC} decreasing.

Assuming that a single continuous pulse is applied at the gate until i_C equals to a predefined value I_{load} , then the turn-off behaviours of IGBT is described in Figure 2.3. On the contrary, turn-on operation can be determined.

As demonstrated in Figure 2.3, six stages can be extracted during switching-off transient:

- Stage 1: $0 \sim t_1$

IGBT operates at conductive state with on-state gate voltage $V_{GE(on)}$ and on-state collector voltage $V_{CE(on)}$. As shown in Figure 2.2(b), due to the full charged of C_{GE} , electrons are completely accumulated between p -well and n^+ -region. Therefore, an inversion layer is formed and named as MOS-channel. Electrons can flow from emitter via channel and n^- -region to collector. Moreover, as long as V_{CE} exceeds the build-in voltage of pn-junction, holes are able to flow from collector to emitter (see Section 3.5.1). A small space charge region exists between p -well and n^- -region due to the thermal equilibrium. Electrons and holes are fully filled

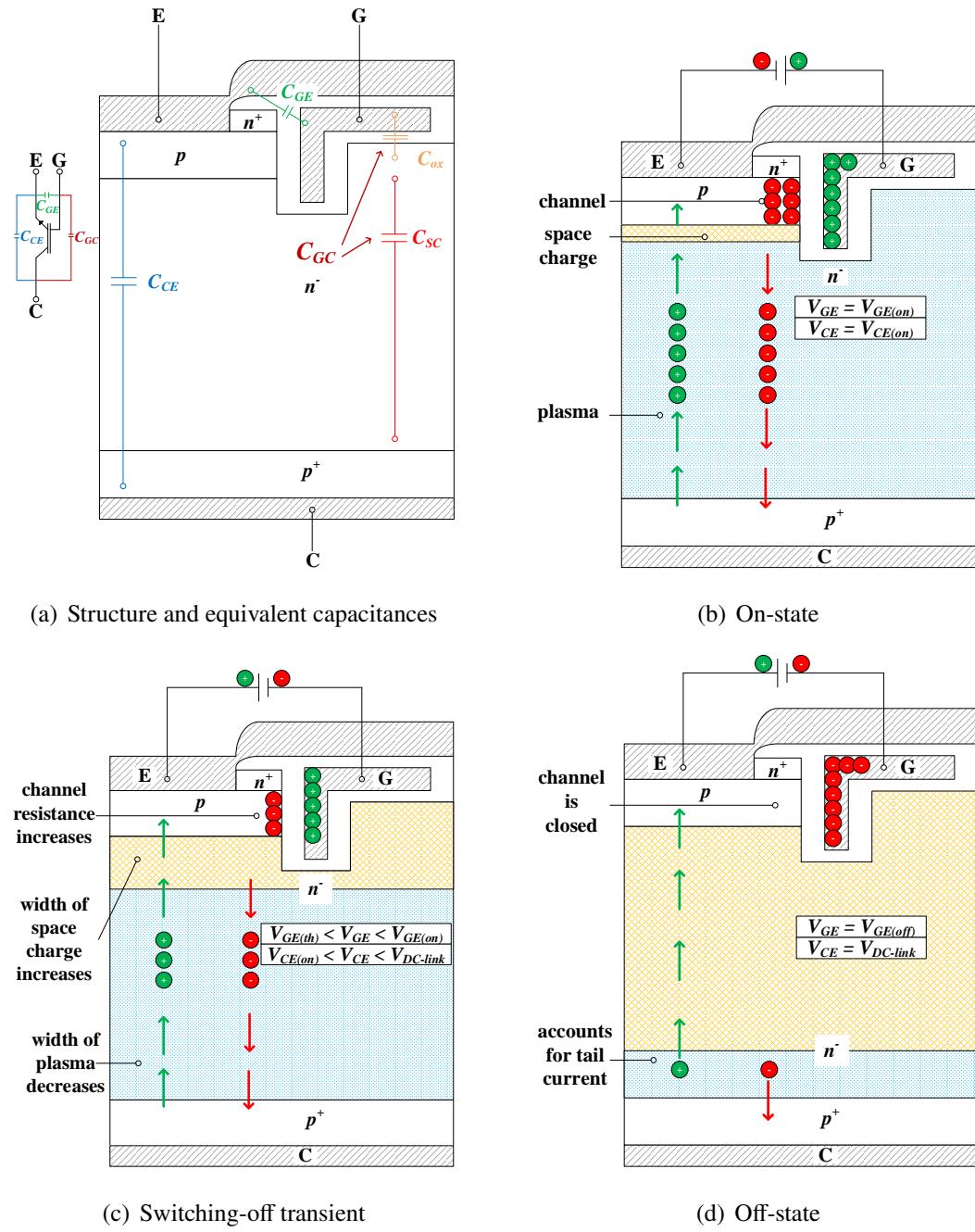


Figure 2.2: Schematic illustration of a trench IGBT and the distribution of plasma and space charge

in n^- -region. These charge carriers are featured as plasma. I_C ramps up due to Equation 2.1.

- Stage 2: $t_1 \sim t_2$

IGBT starts switching off at time point t_1 . C_{GE} begins to discharge and V_{GE} drops, which leads to increasing of channel resistance. As a consequence, V_{CE} increases marginally and the width of space charge region is slightly increased, see Figure 2.2(c). Due to the expansion, C_{GC} decreases. However, the discharge of C_{GE} is predominated in this time interval. Due to the remaining voltage across the load, I_C increases further.

- Stage 3: $t_2 \sim t_3$

At time point t_2 , V_{GE} decreases to Miller plateau V_{Miller} . Apart that, V_{Miller} is the gate voltage, which allows channel further to flow load current. V_{CE} goes steeply up and space charge is further expanded. C_{GC} is discharged and leads to a displacement current. The resulting displacement current charges the gate and counteracts the discharging of GDU. Thus, V_{GE} maintains nearly V_{Miller} .

- Stage 4: $t_3 \sim t_4$

At time point t_3 , since V_{CE} reaches to $V_{DC-link}$, load current is able to commutate towards FWD. Hence, I_C starts to decrease rapidly. As mentioned in [LSSDD18], parasitic inductance L_{par} in the test circuit results to an inductive voltage. Moreover, due to the commutation of FWD, an additional forward voltage spike V_{FRM} overlaps to V_{CE} . Therefore, V_{CE} increases further to maximum $V_{CE(peak)}$. $V_{CE(peak)}$ is given by Equation 2.2:

$$V_{CE(peak)} = |L_{par} \cdot \frac{di}{dt}| + V_{FRM} + V_{DC-link} \quad (2.2)$$

V_{CE} decreases to $V_{DC-link}$ after $V_{CE(peak)}$ and maintains at this value. C_{GC} continues to discharge after t_3 and V_{GE} decreases further.

- Stage 5: $t_4 \sim t_5$

After time point t_4 , I_C drops significant slower than stage 4. Since electrical field of space charge region is completely built up, the remaining charge carriers in n^- -region have to be swept out by recombination. Typically, due to the high lifetime of charge carriers in modern IGBT, this tail current phase can amount to

several microseconds [LSSDD18]. At time point t_5 , V_{GE} decreases to threshold voltage $V_{GE(th)}$. As a result, channel is fully closed.

It has to be remarked that the beginning of tail current I_{tail} varies from structure of device (Punch Through, Non-Punch Through or Field Stop) and operation conditions (such as $V_{DC-link}$ and I_{load}) [CLL⁺17]. As a schematic illustration, an assumption is made that the tail current begins before channel is closed. The tail current will be discussed more in Section 3.2.4.

- Stage 6: $t_5 \sim t_6$

V_{GE} decreases to $V_{GE(off)}$. As illustrated in Figure 2.2(d), V_{CE} stays constant at $V_{DC-link}$, I_{tail} drops slowly.

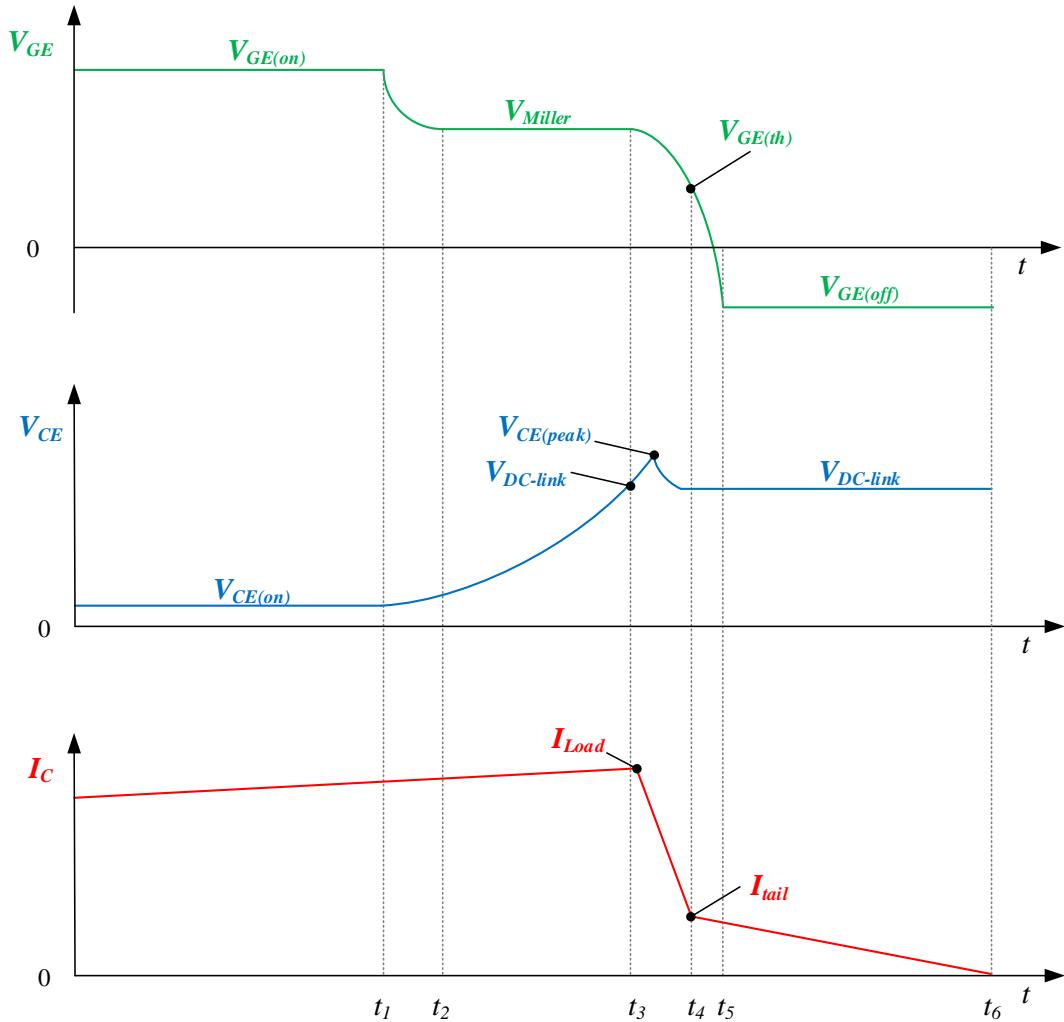


Figure 2.3: Schematic illustration of IGBT switching-off behaviour

Figure 2.4 displays a schematic illustration of output characteristic during switching-off with respect to each stage. Note that inductive over-voltage and reverse recovery are not taken into consideration. Moreover, operating point at each stage is marked. It can be seen that operating point goes to desaturation region during Miller plateau ($t_2 \sim t_3$), which leads to a saturation current $I_{C(sat)}$. $I_{C(sat)}$ is given by Equation 2.3:

$$I_{C(sat)} = \frac{1}{(1 - \alpha_{pnp})} \cdot I_{CH} \quad (2.3)$$

where α_{pnp} is the current gain of equivalent partial transistor in IGBT structure. I_{CH} is current from channel, which is introduced by Equation 2.4:

$$I_{CH} = \frac{\kappa}{2} \cdot (V_G - V_T)^2 \quad (2.4)$$

where κ is a geometry and mobility depended parameter. According to Equation 2.3 and 2.4, it can be inferred that Miller plateau of IGBT can be impacted by channel current. This effect will be discussed more in Section 3.4.

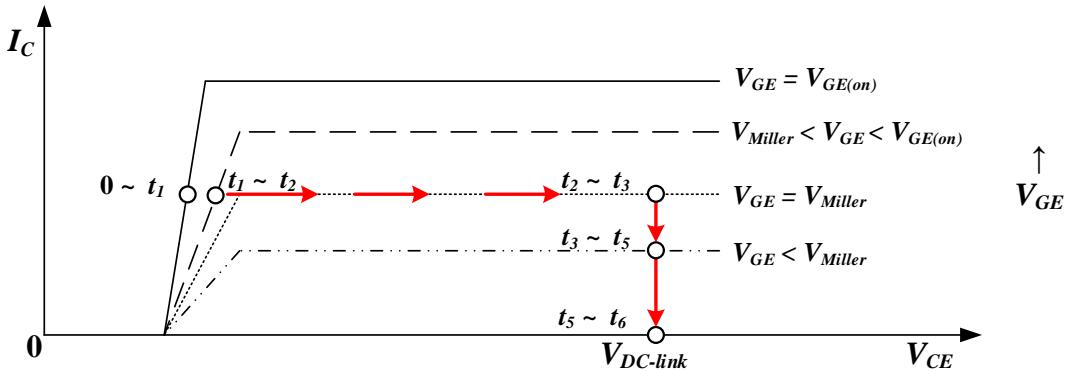


Figure 2.4: Schematic illustration of IGBT output characteristic during switching-off without consideration of inductive over-voltage and reverse recovery current

It can be concluded from the switching-off transient that whether IGBT is at conductive or blocking state, dissipated losses are inevitably generated. The power loss P_{loss} is given by Equation 2.5:

$$P_{loss} = P_{on} + P_{off} + P_{cond} \quad (2.5)$$

where P_{cond} is conductive loss, P_{on} and P_{off} are switching losses during on- and off-state, respectively. Hence, despite at normal switching operation, IGBT suffers from

thermal stress. In this case, may lead to a package-related fatigue [ANB21, SFH⁺11]. In next section, package of power modules is discussed.

2.2 Structure of Power Module

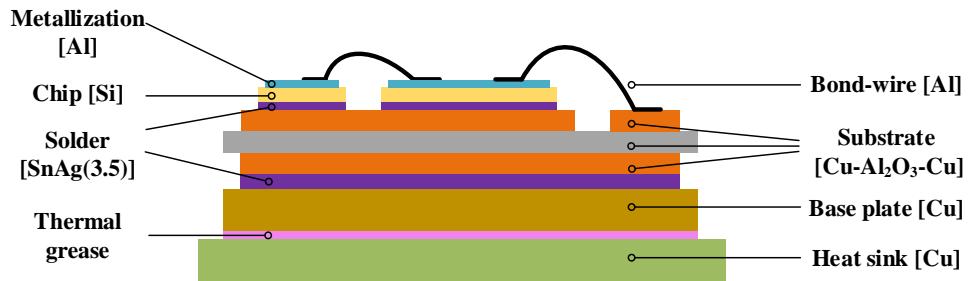
2.2.1 Introduction of Standard Module Package

The layers of a standard module are illustrated in Figure 2.5(a). On the back side, solder is utilized to connect chip, substrate and base plate, respectively. Heat sink is joined to the base plate by a thermal interface material like thermal grease or foil. The design of front-side plays an essential role for current distribution. Especially, due to the high flexibility, low costs and the extensive application experience, aluminium is widely applied as bond-wire material. [HJ97] Diameter and length of bond-wire play an significant role in power devices. Typically, diameter are used in range of 100 μm to 500 μm .

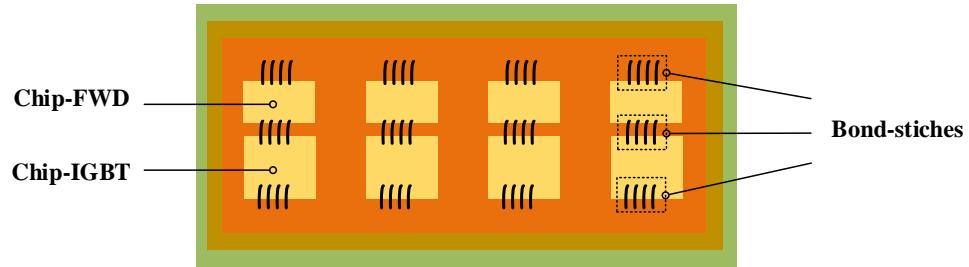
For a purpose of symmetric distribution of current and temperature, as displayed in Figure 2.5(b), stitches are symmetrically bonded on metallization. Therefore, the current capability of power devices is not only limited by the semiconductor chip, but also restricted by the design of the bond-wires. A higher current density demands for thicker and more bond-wires and corresponding stitches. [LSSDD18]

2.2.2 Modelling of Front-Side

Figure 2.6 illustrates an IGBT chip with 3 paralleled segments. GDU is connected with gate and emitter load terminal. The emitter side of chip (i.e., front-side) is especially modelled. During Switching-off, load current flows from emitter side of segment via metallization, bond-wire and finally to emitter load terminal. Gate current flows through the opposite direction. For each segment, metallization, bond-wire and load terminal have equivalent resistances, respective R_{Surf} , R_{bw} and R_E . Moreover, an equivalent resistance exists between two adjacent segments, namely R_{Seg} . It can be concluded that whether in load or gate current loop, they have to flow through additional parasitic resistances, which leads to extra voltage drops and overlay respective at on-state voltage $V_{CE(on-load)}$ and gate voltage V_{GE} . Furthermore, these extra voltage drops vary from the bond-wire state, because the resulting parasitic



(a) Cross section and general materials



(b) Top view

Figure 2.5: Structure of standard module

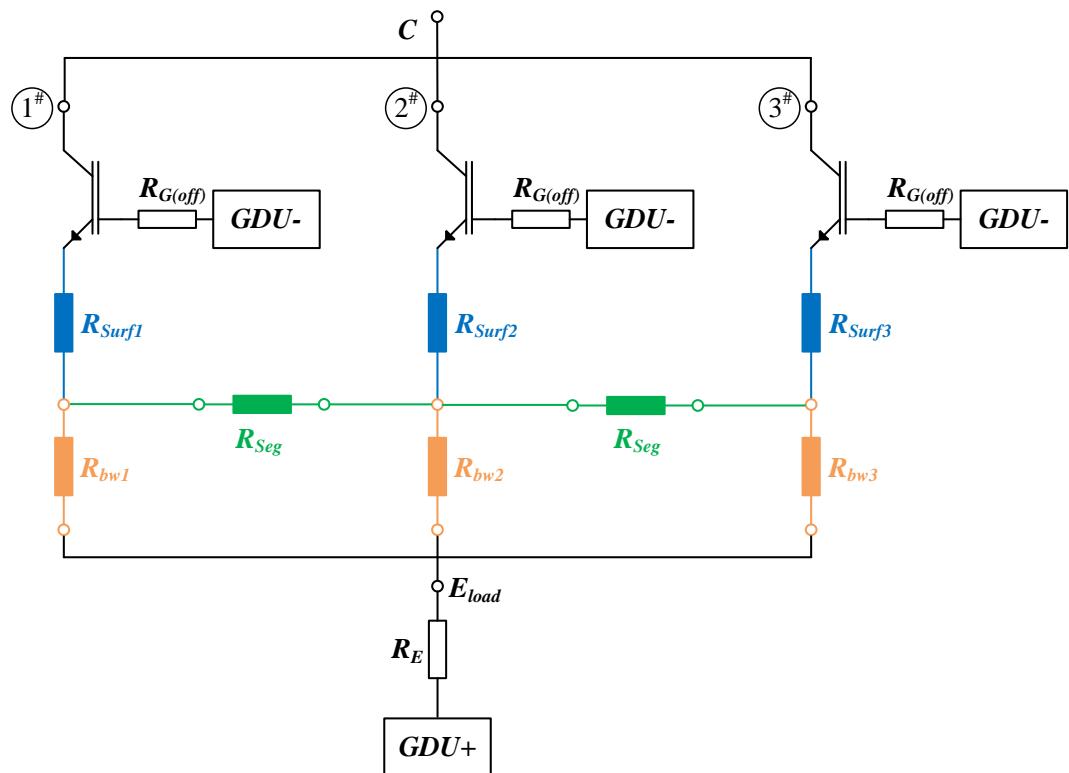


Figure 2.6: Schematic illustration of an IGBT chip model under consideration of emitter side during switching-off

resistances increase with less bond-wire connection. This argument will be illustrated in next section.

2.3 Degradations on Front-side

Interfaces within power module between interconnected layers are exposed to thermal and mechanical impacts during operation, which results to the degradation of power modules and hence the lifetime, reliability and robustness of power modules are reduced. Furthermore, in view of front-side, bond-wire and metallization are main weak points [LSSDD18, ANB21, SFH⁺11, Lut14, WBW⁺13].

2.3.1 Bond-Wire Lift-off

As depicted in Figure 2.5(a), material of layer varies from each other. Each material has characteristic Coefficient of Thermal Expansion (CTE). Figure 2.7 shows several CTEs of various materials at room temperature.

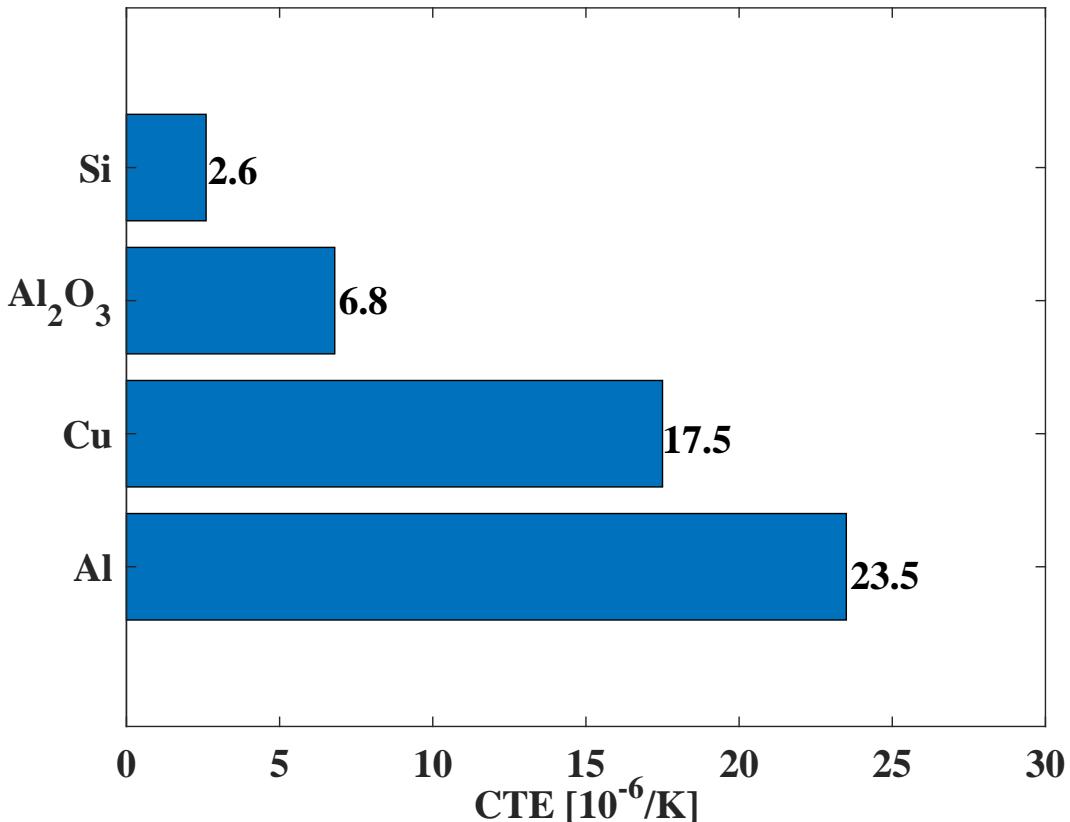
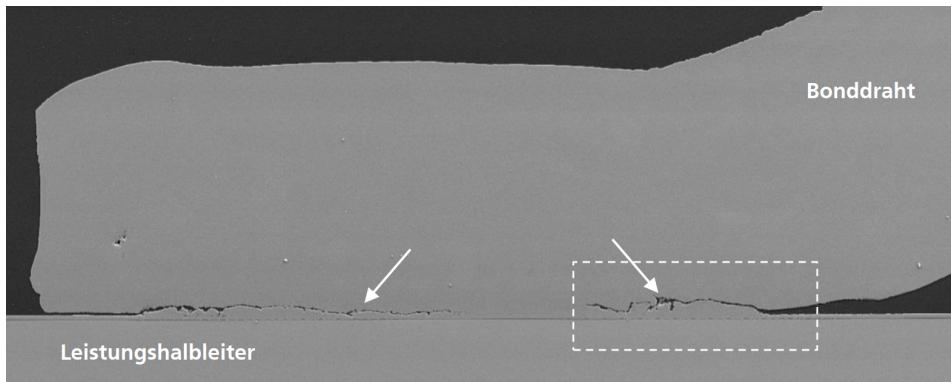


Figure 2.7: Coefficient of thermal expansion at 25°C of materials used in package technologies [LSSDD18]

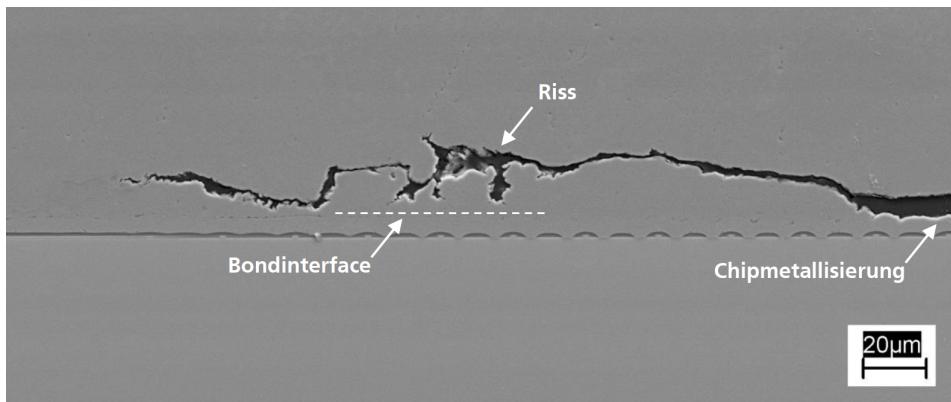
Description

Obviously, large difference exists between chip, metallization and bond-wire. It can be seen that bond-wire has almost 7 times higher thermal expansion than chip during temperature gradients. Since both of them are bonded together due to the bonding process, this thermal expansion is hindered in the area of the bond, in which leads to mechanical stresses and strains. Furthermore, these stresses and strains result to fatigue of the wire material in the bond zone.

Figure 2.8 depicts a typical fault image of bond-wire after thermal strain. Crack occurs firstly in the edge areas of bond-wire, grows towards the bonded area, and finally leads to bond-wire lift-off.



(a) Full view of crack



(b) Zoomed area of a crack in the bond zone

Figure 2.8: Cross-section on a 400 µm Al thick wire bond after thermal stress [Gö13, P.33]

Consequence

If a bond-wires ages, the effective cross-section of the remaining wire is reduced until the complete lift-off. As a consequence, the interconnection resistance of the corresponding segment changes. The current distribution of each segment is affected. Segments with intact bond-wire will conduct more current in comparison to the initial state without bond-wire cut, see [Gö13, NLJ⁺15, DDM20]. In addition, this effect can impact on V_{Miller} and $V_{CE(on-load)}$, see Section 3.4 and 3.6.

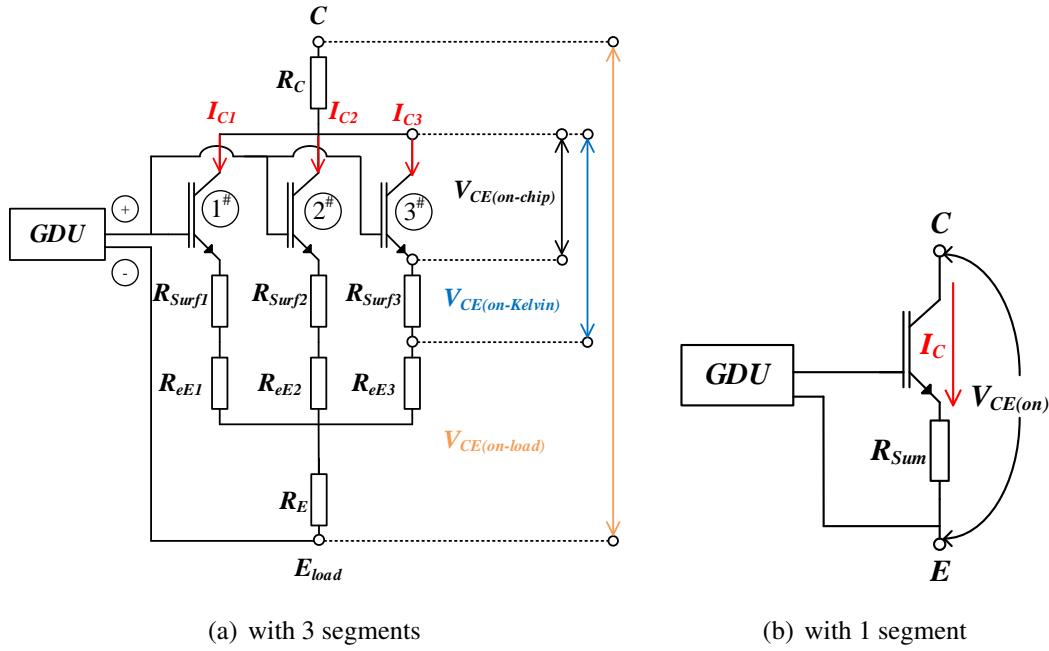


Figure 2.9: Equivalent model of an IGBT chip with respect to $V_{CE(on)}$ measurement under load current and under consideration of various segments

Segment Model

In order to explain this statement, Figure 2.9 is illustrated. Assuming that an IGBT chip includes 3 IGBTs, which account for 3 segments. Moreover, $V_{CE(on-load)}$ is measured (i.e., only emitter load terminal is available). Collector and emitter load terminal has the equivalent resistance R_C and R_E , respectively. Each IGBT has an ideal on-state voltage without package $V_{CE(on-chip)}$, which is only junction temperature and load current dependent. However, in real case, surface resistance has to be taken into consideration, which accounts for $V_{CE(on-Kelvin)}$. Especially, the equivalent resistance between emitter load and Kelvin terminal R_{eE} varies from

bond-wire state and is given by Equation 2.6:

$$R_{eE} = \begin{cases} R_{bw} \parallel R_{Seg} \approx R_{bw} & (\text{bond-wire intact}) \\ f(R_{bw}, R_{Seg}) \gg R_{bw} & (\text{bond-wire defect}) \end{cases} \quad (2.6)$$

where R_{bw} and R_{Seg} are shown in Figure 2.6. Since $R_{Seg} \gg R_{bw}$, when bond-wire is intact, $R_{eE} \approx R_{bw}$ and when defect, $R_{eE} \gg R_{bw}$.

The equivalent resistance within one segment is shown in Figure 2.9(b) and can be given by Equation 2.7:

$$R_{Sum} = R_C + R_{Surf} + R_{eE} + R_E \quad (2.7)$$

Furthermore, $V_{CE(on-Kelvin)}$ and $V_{CE(on-load)}$ can be given by Equation 2.8 and 2.9:

$$V_{CE(on-Kelvin)} = R_{Surf} \cdot I_C + V_{CE(on-chip)} \quad (2.8)$$

$$V_{CE(on-load)} = R_{Sum} \cdot I_C + V_{CE(on-chip)} \quad (2.9)$$

Explanation of Impact on individual Segment

Assume a load current I_C flows through IGBT chip. In normal operation, I_C is determined by load inductance and voltage of power supply. Hence, I_C is independent on ageing and can be given by Equation 2.10:

$$I_C = I_{C1} + I_{C2} + I_{C3} \quad (2.10)$$

However, for individual segment, current distribution varies from bond-wire state. Two cases are discussed according to Figure 2.9(a) with respect to bond-wire of segment 1 intact or defect.

- all bond-wires are intact

In this case, I_C flows symmetrically through each segment, which yields:

$$I_{C1} = I_{C2} = I_{C3} = \frac{1}{3} \cdot I_C \quad (2.11)$$

R_{Sum} of each segment is determined by Equation 2.12:

$$R_{Sum} = R_C + R_{Surf} + R_{bw} + R_E \quad (2.12)$$

- bond-wire of segment 1 defect, segment 2 and 3 intact

R_{Sum} of segment 2 and 3 can be given by Equation 2.12. Since bond-wire of

segment 1 is defect, R_{eE1} is determined by Equation 2.6 and R_{Sum1} can be derived by Equation 2.13:

$$\begin{aligned} R_{Sum1} &= R_C + R_{Surf1} + R_{eE1} + R_E \\ &= R_C + R_{Surf1} + f(R_{Surf2}, R_{Surf3}, R_{Seg}) + R_E \end{aligned} \quad (2.13)$$

It can be inferred that $R_{Sum1} \gg R_{Sum2}$ and R_{Sum3} . According to Figure 2.9(b), applied gate voltage of segment 1 is reduced. As a consequence, segment 1 conduct less current than $\frac{1}{3} \cdot I_C$. Furthermore, segment 2 and 3 have to conduct more current, which leads to the inhomogeneous current distribution of each segment.

2.3.2 Reconstruction of Emitter Metallization

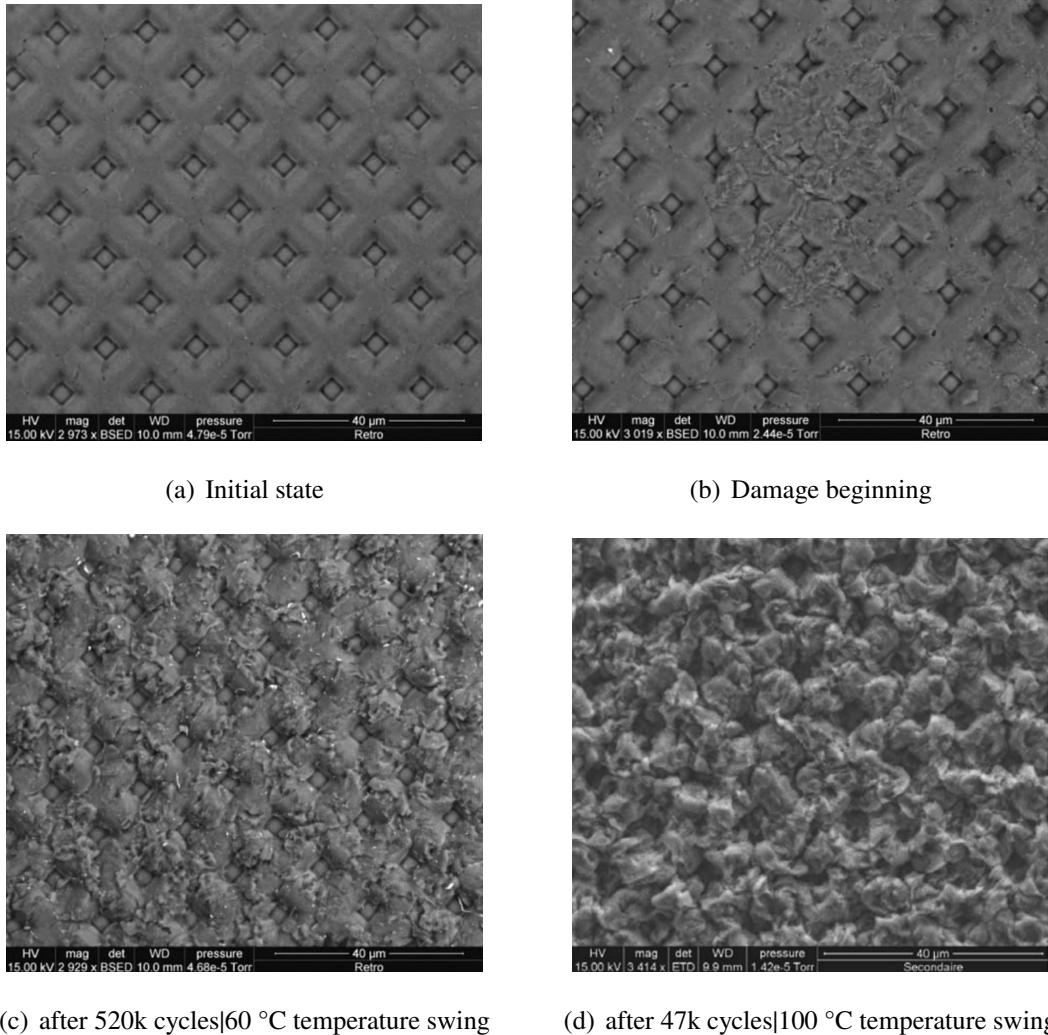


Figure 2.10: Examples of emitter metallization degradations [SFH⁺11, P.4938]

During the IGBT operation, not only bond-wire but also the metallization of chip

should be observed. Conventionally, metallization is made of a vacuum-metallized aluminium layer, which is formed in a grain structure. [LSSDD18]

Owing to the high thermal stress, grains are plastic deformed when the elastic limits are exceeded. In [Cia00], this is the case for junction temperature over 110°C. The plastic deformation can lead to the extrusion of single grains and further causes increasing of R_{Surf} . This phenomenon is introduced as metallization degradation. Figure 2.10 shows the plastic deformation of metallization reconstruction.

To accelerate surface metallization ageing, IGBT is generally exposed under repetitive short circuit events, so that high thermal stress is generated. Various investigations [RBD⁺18, NL13, MKK13, PPL⁺10] found that after IGBT repetitive short circuit operations, not only $V_{CE(on-load)}$, but also $V_{CE(on-Kelvin)}$ is increased despite no bond-wire lift-off. This can be explained by Equation 2.8.

In summary, bond-wire life-off and degradation of metallization lead to increasing of segment resistance and further causes inhomogeneity of current distribution and on-state voltage variation. Thus, $V_{CE(on)}$ can be used for bond-wire damage detection. Moreover, it is reported in [LSSDD18, SFH⁺11, Lut14, Sme10] that if $V_{CE(on)}$ is 5% increased, then device reaches to End of Life state (EoL). Since after that, $V_{CE(on)}$ increases rapidly with ageing, EoL is a critical state for the detection of bond-wire damage state.

3 TSEPs

In this chapter, approaches of junction temperature determining are introduced. Different TSEPs are highlighted investigated. An overview of previous researches is summarized. According to the feasibilities of mentioned TSEPs, on-state voltage under load current, maximal current slope during switching-off and Miller plateau are selected as candidates. After that, basic equations of these TSEPs with dependency on junction temperature and other parameters are derived. Furthermore, measurements are performed with corresponding parameters. Sensitivities, linearities and calibration efforts are investigated. Based on the comparison with these TSEPs, on-state voltage under load current is determined as TSEP for repetitive operation.

3.1 Approaches of Junction Temperature Determining

The junction temperature T_j must be considered in the design of a converter system to ensure optimal reliability and operation. [BLDA14] In general, three T_j parameters are considered in application:

- average junction temperature $T_{j(\text{avg})}$ based on thermal resistance at stationary state;
- temperature swing ΔT_j at non-stationary state;
- maximum junction temperature $T_{j(\text{max})}$ given by manufacturers, where accounts for worst-case scenarios.

Despite thermal characteristics are widely used for estimating T_j , this value cannot be applied in the reality due to various topologies. In order to evaluate T_j , optical, physical and electrical methods are broadly used. These methods will be introduced in detail in following sections.

3.1.1 Optical Methods

In optical methods, gel of power module is removed and surface of chip is uniformly dyed, radiation in the infrared surface of the electromagnetic spectrum can be detected by sensors. Emitted surface thermal energy of chip can be detected and converted to an electrical signal. An IR-image with surface temperature distribution

can be obtained by camera. Various devices are applied for optical methods, such as IR-sensors [ZG10] and IR-camera [DAJ13].

Advantages

By means of optical methods, a high spatial resolution and thus temperature distribution of the whole chip surface can be obviously illustrated. Furthermore, IR-camera has no galvanic contact with module. Therefore, the IR-image record does not affect the device operation or its temperature development.

Disadvantages

Owing to comparable low sampling rate, camera faces the challenge with respect to the synchronization at a certain time point of pulse pattern. Moreover, package has to be modified. Thus, this method is rarely used in the application.

3.1.2 Physical Methods

Typically, physical methods such as thermocouples and thermistors can be utilized for temperature measurement, if it is feasible to access chip directly. [BDPS09] Thermo-voltage can be measured by thermal capacitance of two various materials. Temperature is determined by thermo-voltage according to the Seebeck effect.

Advantages

Temperature can be very precisely measured by thermocouple. Moreover, it is widely used for case temperature measurement [AQG19, LSSDD18] because of the convenient performance.

Disadvantages

Temperature can only be locally measured. In other words, it cannot feature the temperature distribution within a chip with temperature gradient. In addition, response time is comparably low (e.g., for thermocouple is lower than 5 ms [SPP⁺17]) due to the thermal capacitance.

3.1.3 Electrical Methods

Many of electrical properties of semiconductor devices can be strongly temperature-dependent. These parameters are named as Temperature Sensitive Electrical Parameters (TSEPs).

Advantages

TSEPs are broadly used to estimate junction temperature in power electronics due to the good resolution, fast response time and feasible measuring with package.

Disadvantages

However, $T_{j(\text{avg})}$ represents only a ‘global’ or ‘lumped’ value and consequently cannot depict temperature distribution or gradient within whole chips. [Bla04, ADK12] Take an example in [Bla04], the dependency of current density on temperature within diode is shown in Figure 3.1. In actual situation, 5 diodes are parallel and their current densities vary from temperature. However, in modelled situation, an equivalent diode is applied and its current density features mean value. Moreover, the calibration with a changed device state (e.g., ageing), must be taken into consideration [BLDA13].

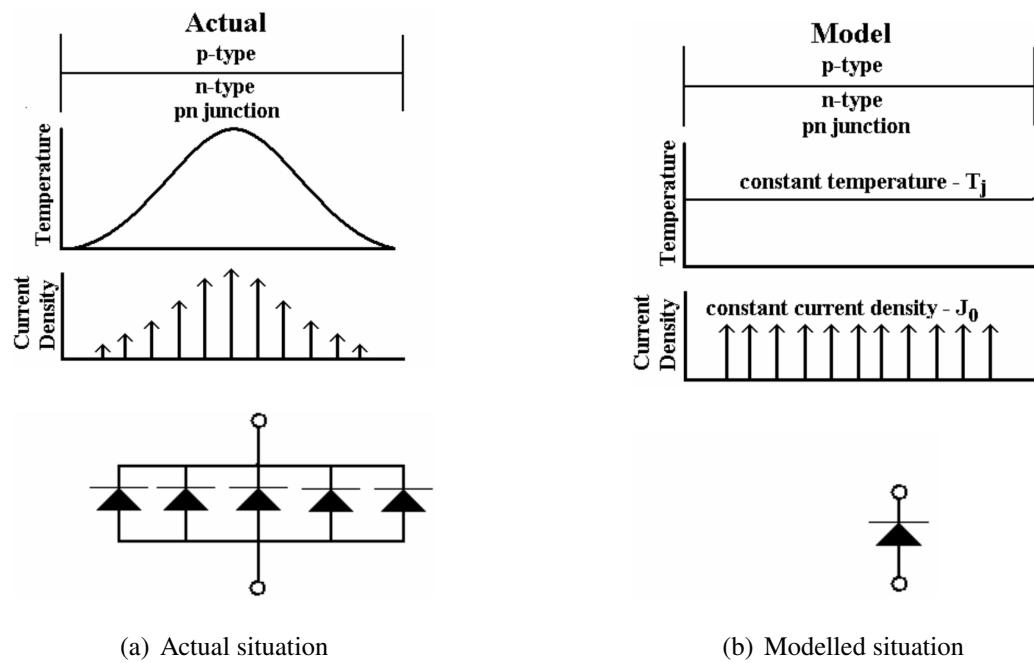


Figure 3.1: An illustration of the various situations for a pn-junction [Bla04, P.71]

Overview of TSEPs in Previous Investigations

Table 3.1 lists several TSEPs mentioned in previous researches. Note that only parameters during on-state and switching-off phase are selected because temperature at switching-on phase cannot characterize the maximal temperature of chip. Moreover, some aspects are especially taken into consideration:

- Dependency
 - Operation-condition-related parameters (such as I_C , $V_{DC-link}$) are concerned.
 - The accuracy of junction temperature may be affected by ageing state.
 - Self-heating issue leads to additional temperature rising and deviation.
- Necessity during repetitive operation
 - Interruption during operation complicates the performance.
 - Package has to be modified if external circuit is necessary.
- Good linearity with temperature increases the accuracy.
- A low calibration effort simplifies the performance.

Table 3.1: Overview of applied TSEPs for IGBTs in previous research

TSEP	Dependency			Necessary during operation?	Linear -ity	Calib -ration effort	Reference	
	Parameter	Front-side ageing	Self-heating?					
$V_{CE(on-sense)}$ ¹	T	no	no	yes	yes	good	medium	[LSSDD18], [SS09], [Sme10], [CPJ ⁺ 21]
$V_{CE(on-load)}$ ²	T , I_C	yes	yes	no	yes	good	medium	[GPT ⁺ 15], [CPJ ⁺ 21]
$V_{GE(th)}$	T	no	no	no	yes	medium	low	[CPJ ⁺ 21], [HMFB15], [BSJ13], [CSML14]

Table 3.1: Overview of applied TSEPs for IGBTs in previous research

TSEP	Dependency			Necessary during operation?		Linear -ity	Calib -ration effort	Reference
	Parameter	Front-side ageing	Self-heating?	Interruption	External circuit			
V_{Miller}	T , V_{GE} , I_C , $R_{G(off)}$, $V_{GE(th)}$, g_{fs}^3	yes	yes	no	yes	medium	high	[CSML14], [CPJ ⁺ 21]
t_{off}^4	T , V_{GE} , I_C , $R_{G(off)}$, $V_{GE(th)}$, g_{fs}	yes	yes	no	no	medium	high	[CSML14], [LLI ⁺ 18]
t_{doff}^5	T , V_{GE} , I_C , $R_{G(off)}$, $V_{GE(th)}$, g_{fs}	yes	yes	no	no	good	high	[CPJ ⁺ 21], [LLI ⁺ 18], [LCS ⁺ 15],
di/dt_max^6	T , I_C , $V_{DC-link}$, $R_{G(off)}$	no	yes	yes	no	medium	high	[LLI ⁺ 18], [CLL ⁺ 16], [CLL ⁺ 17]

Table 3.1: Overview of applied TSEPs for IGBTs in previous research

TSEP	Dependency			Necessary during operation?		Linear -ity	Calib -ration effort	Reference
	Parameter	Front-side ageing	Self-heating?	Interrupt	External circuit			
dV_{CE}/dt^7	T , I_C , $V_{DC-link}$, $R_{G(off)}$	no	yes	yes	no	medium	high	[CPJ ⁺ 21], [BYM ⁺ 11], [LLI ⁺ 18]
I_{tail}	T , I_C , $V_{DC-link}$, $R_{G(off)}$	no	yes	no	no	good	high	[CPJ ⁺ 21], [CLL ⁺ 17], [LLI ⁺ 18]

¹ IGBT on-state voltage under sense current² IGBT on-state voltage under load current³ Transconductance⁴ Turn-off time⁵ Turn-off delay time⁶ Maximal current slope during turn-off⁷ Maximal voltage slope during turn-off

In following sections, these TSEPs are evaluated under consideration of the feasibility during repetitive operation. Several TSEPs without measurement are estimated in Section 3.2, while the remaining TSEPs are assessed in further sections with measurement.

3.2 Evaluation of TSEPs without Measurement

3.2.1 t_{doff} and t_{off}

Turn-off time t_{off} is defined as the sum of storage time, voltage rise time and current fall time during switching off [LSSDD18] (i.e., $t_1 \sim t_6$ in Figure 2.3. Turn-off delay

time is the time from 90% of $V_{GE(on)}$ to 90% of I_{Load} [CSML14]. Neither of them are suitable for repetitive operation of IGBT module because:

- very accurate sensor needed;

t_{doff} varies from 667.5 ns to 764.3 ns in [CSML14]. In order to obtain the delay time precisely, Analog-to-Digital Converter (ADC) of sensors for V_{GE} and I_C measurement must have high resolution.

- tail current and induced gate voltage issue.

As mentioned in Chapter 2, IGBT module has high parasitic inductance, if GDU is connected with load contact, see Figure 2.6. This parasitic inductance results to an induced voltage during switching-off, see Figure 3.13. Hence, it is challenging to estimate the beginning of t_{doff} (i.e., 90% of V_{GE}). Moreover, due to the tail current, the determination of t_{off} is also difficult.

3.2.2 $V_{GE(th)}$

The definition of $V_{GE(th)}$ varies from device and is given individually by manufacturers. Take an example of [Inf13], $V_{GE(th)}$ is defined as the gate voltage that allows 1.6 mA I_C flow through IGBT under the test condition that gate and collector contact are shorted. Despite the low calibration effort and without interruption during repetitive operation, $V_{GE(th)}$ at switching-off phase is not a good choice for IGBT since the zero crossing of the measured current (or the defined I_C value in data sheet) cannot be linked to the gate voltage owing to the tail current.

3.2.3 dV_{CE}/dt

Maximum voltage slope dV_{CE}/dt is defined as the slope from $V_{CE(on)}$ to $V_{DC-link}$ [BYM¹¹] and hence independent on $V_{CE(peak)}$ resulted of stray inductance and V_{FRM} of FWD. However, this TSEP is strongly test condition ($V_{DC-link}$, I_{Load} , etc.) dependent. dV_{CE}/dt shows poor linearity at low $V_{DC-link}$ and I_{Load} in [CPJ²¹, BYM¹¹]. Moreover, dynamic avalanche may affect the slope if high $V_{DC-link}$ is applied [RSPP02, ONSI04]. Thus, dV_{CE}/dt is not concerned as alternative TSEP.

3.2.4 I_{tail}

The definition of tail current can be rarely found in literatures. Despite a significant current slope change during swiching-off phase of IGBT, the beginning of tail current

is difficult to estimate. According to [CPJ⁺21], a uniform time point at $t = 301.68 \mu\text{s}$ is selected as the beginning of tail current.

Two mechanisms with respect to current falling model are mentioned in [CLL⁺17], respective extraction of storage carries and recombination of minority carries. According to this, two stages are characterized for transient collector current falling model and shown in Figure 3.2:

- At stage 1, the extraction of storage carries is predominated, J_{Load} falls to a specified current density J_{C_PT} .
- At stage 2, tail current occurs, where recombination of minority carries dominates.

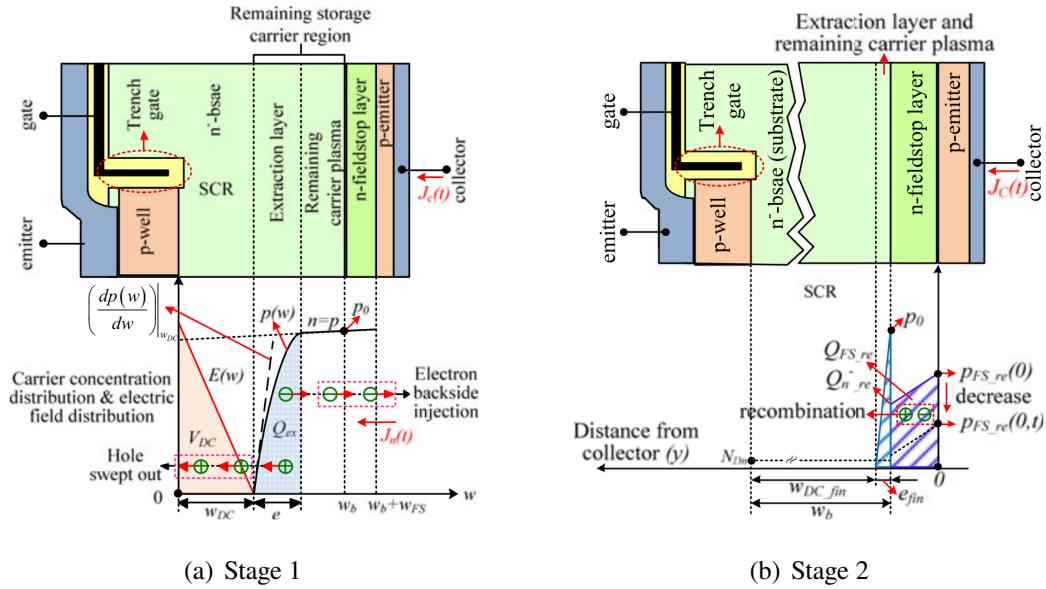


Figure 3.2: I_C falling transition [CLL⁺17, P.6398-6399]

Moreover, the upper limit bus voltage V_{DC_max} for a specified J_{Load} is defined.

Various stages are shown by different $V_{DC-link}$:

- Both stages take place, if applied $V_{DC-link}$ is lower than V_{DC_max} ;
- On the contrary, only stage 2 can be found during switching-off.

The measurement results under various stages and $V_{DC-link}$ are shown and compared in Figure 3.3.

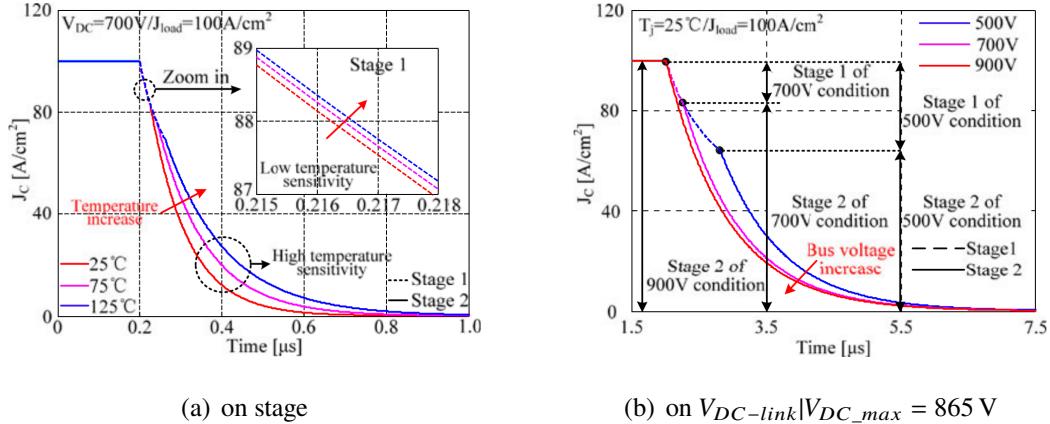


Figure 3.3: Temperature dependency during I_C falling transition [CLL⁺17, P.6400-P.6401]

It can be seen in Figure 3.3(a) that tail current shows better temperature sensitivity than maximum of current falling slope. However, at high $V_{DC-link}$ under the fixed J_{load} in Figure 3.3(b) ($V_{DC-link} = 700$ V and 900 V), it is difficult to distinguish the beginning of tail current.

Above all, tail current is strongly operation condition dependent and challenging to estimate. Hence, tail current is not suitable as alternative TSEP.

3.3 di_C/dt_{max} as alternative TSEP

3.3.1 Derivation of Temperature Dependency

As mentioned in [CLL⁺17], maximum of I_C falling slope di_C/dt_{max} accounts for the slope of stage 1 (i.e., J_{C1}). Its temperature dependency on parameters is shown in Figure 3.4. In short, the density of the plasma is increased with temperature, which leads to a longer turn-off time (see Appendix A.1.1). In other words, di_C/dt_{max} decreases with temperature.

As shown in Table 3.2, di_C/dt_{max} is $V_{DC-link}$, $R_{G(off)}$ and I_{Load} dependent. Since $V_{DC-link}$ is fixed during repetitive operation, only the latter two parameters are investigated with measurement in the following sections.

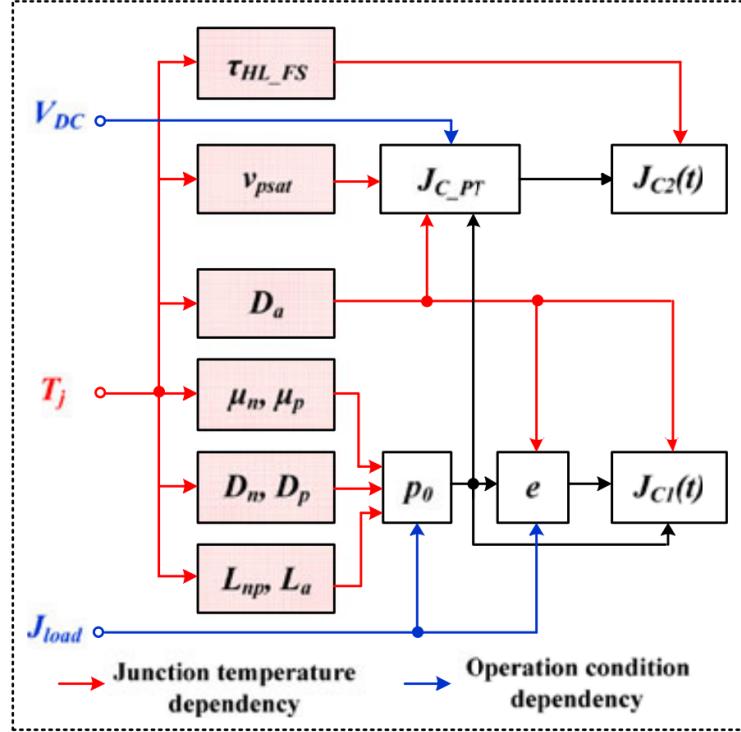


Figure 3.4: Temperature dependency of di_C/dt_{max} on parameters [CLL⁺17, P.6400]

3.3.2 Impact on $R_{G(off)}$

Figure 3.5 illustrates dependency of di_C/dt_{max} on $R_{G(off)}$. Three regions are divided according to the value of $R_{G(off)}$:

- At small value, di_C/dt_{max} is controlled by plasma and changes marginally;
- In the middle range of $R_{G(off)}$, di_C/dt_{max} increases at first until maximum and then decreases. This region is named as semi-controlled region;
- At large value of $R_{G(off)}$, di_C/dt_{max} decreases with $R_{G(off)}$ and named as $R_{G(off)}$ controlled region.

Principle of each region should be explained in detail.

Plasma Controlled Region

V_{GE} drops rapidly, which resulted to fast close of channel. Electrons from channel are quickly swept out and hence are rarely able to compensate with holes from plasma p . According to Poisson's equation yields:

$$\frac{dE}{dx} = \frac{q}{\epsilon} \cdot (N_D + p) \quad (3.1)$$

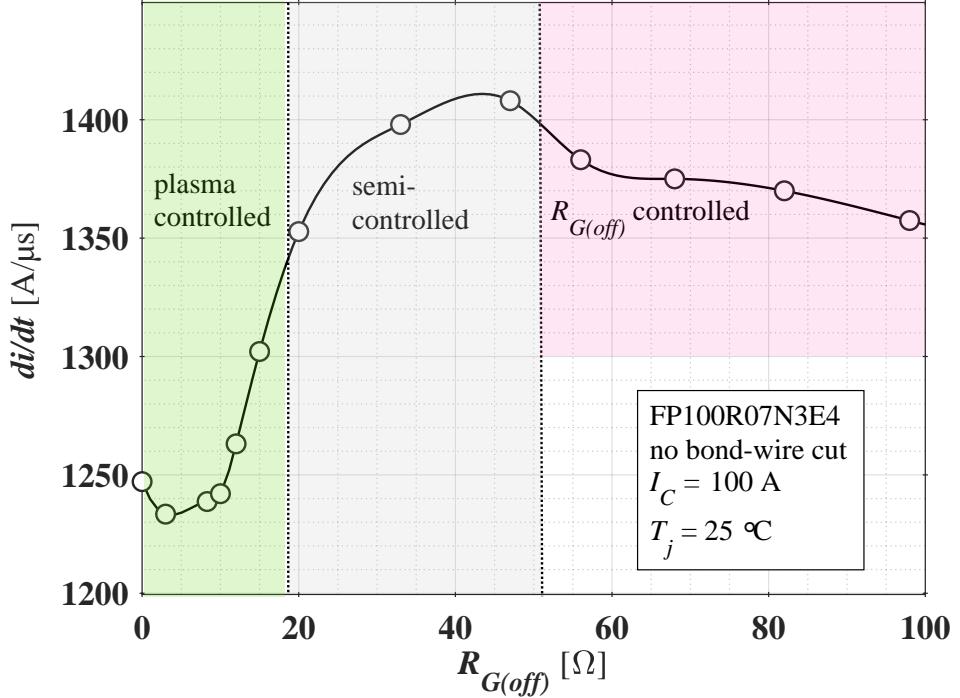


Figure 3.5: Measurement results of di_C/dt_{max} with various $R_{G(off)}$

where E is the electric field, x is the length of space charge region, q is elementary charge, ϵ is dielectric constant, and N_D is the donator density in n^- -region. It can be seen from Equation 3.1 that the additional p from plasma results to a high dE/dx . Furthermore, $V_{DC-link}$ is given by Equation 3.2:

$$V_{DC-link} = \int_0^{W_{RLZ}} E dx \quad (3.2)$$

Hence, once V_{CE} reaches to $V_{DC-link}$, I_C starts falling, electrical field are completely built-up. However, due to the high dE/dx , still much plasma remains and leads to a relative low di_C/dt_{max} . Figure 3.6 depicts the electrical field and plasma distribution during switching-off transition with small $R_{G(off)}$.

Semi-Controlled Region

$R_{G(off)}$ increases in semi-controlled region, which means channel closes slower. Thus, more electrons from channel n can be compensated with holes from plasma. It yields:

$$\frac{dE}{dx} = \frac{q}{\epsilon} \cdot (N_D + p - n) \quad (3.3)$$

Therefore, the remained plasma decreases with increasing $R_{G(off)}$, which causes increasing of di_C/dt_{max} , as displayed in Figure 3.7. Furthermore, it can be inferred

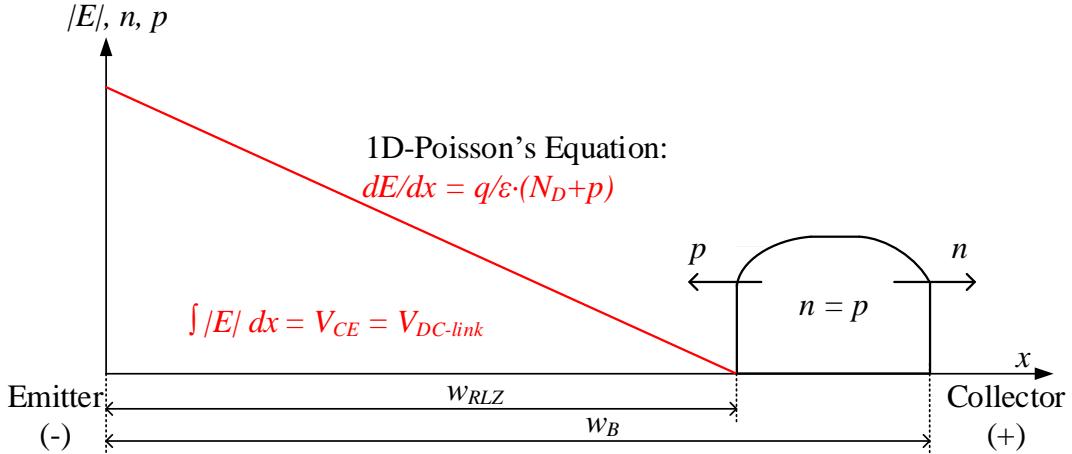


Figure 3.6: Schematic illustration of electric field and plasma distribution during switching-off at small gate resistor

that there is a maximum of di_C/dt_{max} corresponds to a middle-range value of $R_{G(off)}$. After that, $R_{G(off)}$ is predominated and plasma plays less role. In this case, current falling time is proportional to gate resistor [LSSDD18]. A higher value of $R_{G(off)}$ leads to di_C/dt_{max} decreasing.

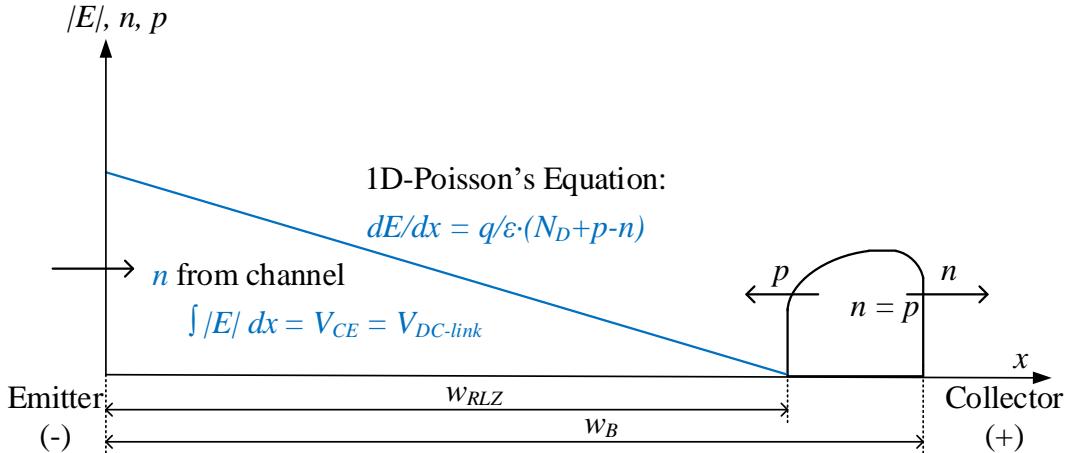


Figure 3.7: Schematic illustration of electric filed and plasma distribution during switching-off at medium range gate resistor

$R_{G(off)}$ Controlled Region

At large gate resistor, holes from plasma could be compensated totally by electrons from channel. Electric field mode is similar to MOSFET. Thus, di_C/dt_{max} is decreased with larger gate resistor.

3.3.3 Impact on I_C

In order to investigate the dependency of di_C/dt_{max} under various I_C , three measurements are performed and depicted in Figure 3.8. di_C/dt_{max} is calculated from 90% to 60% of load current in order to exclude the start of the tail current.

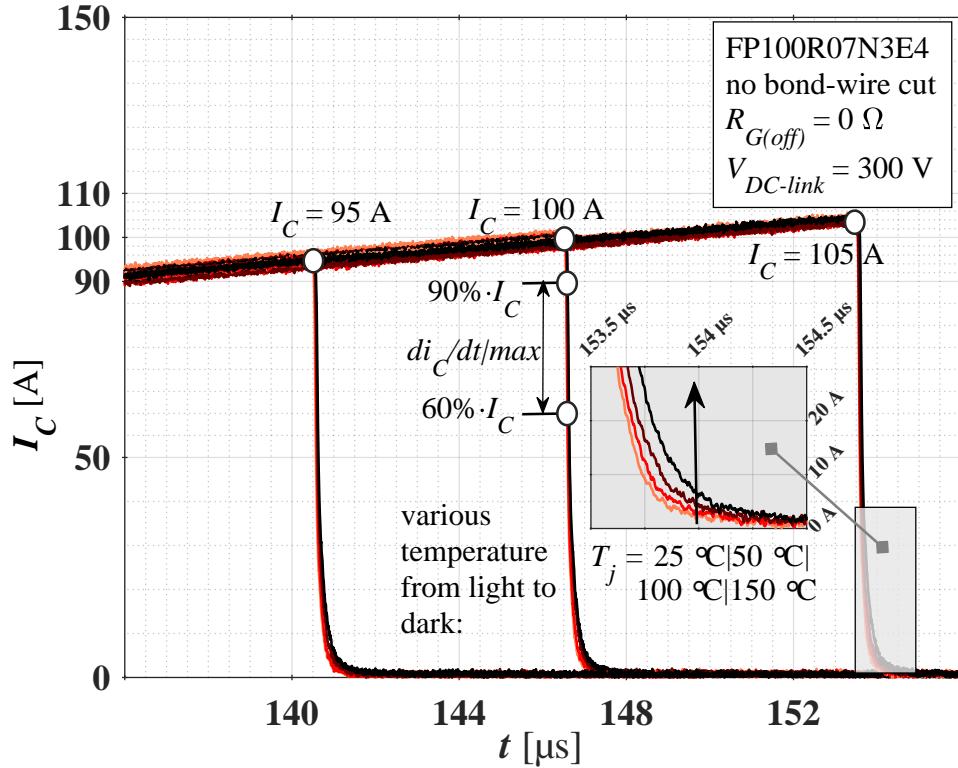


Figure 3.8: Determination of di_C/dt_{max} under different load current

A linear calibration curve can be given under various temperatures according to Equation 3.4:

$$TSEP_{Calib} = A \cdot T_j + B \quad (3.4)$$

where A accounts for sensitivity and B is the offset, which is independent on temperature. The calibration results are shown in Figure 3.9. It can be seen that:

- di_C/dt_{max} decreases with T_j and depends strongly on I_C .
- A very poor linearity with T_j is illustrated owing to the large difference between measured data and the fitted curve.

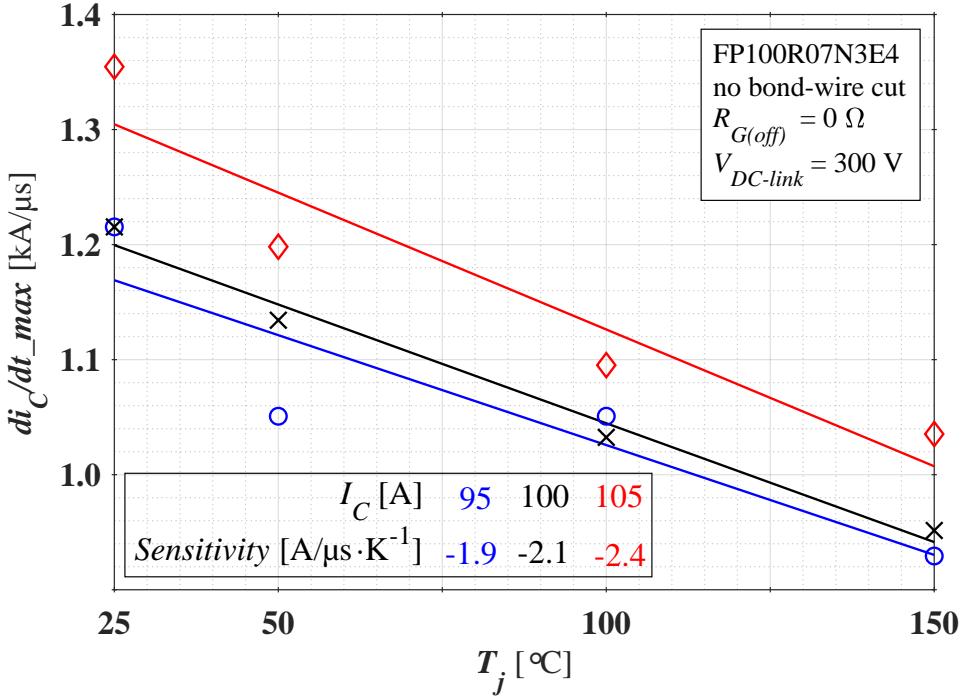


Figure 3.9: Measured calibration curve of di_C/dt_max under various I_C

3.3.4 Conclusion

It can be concluded that di_C/dt_max is not suitable as a TSEP for this work. On the one hand, calibrating for each scaled current is time intensive. On the other hand, it shows poor linearity.

3.4 V_{Miller} as alternative TSEP

3.4.1 Derivation of Temperature Dependency

According to [LSSDD18], Miller plateau is defined by Equation 3.5:

$$V_{Miller} = V_{GE(th)} + \frac{I_C}{g_{fs}} \quad (3.5)$$

where both $V_{GE(th)}$ and g_{fs} are temperature dependent. Nonetheless, their temperature behaviours are opposite.

Temperature Dependency of $V_{GE(th)}$

According to [SN07], the temperature dependency of $V_{GE(th)}$ can be introduced by Equation 3.6:

$$\frac{dV_{GE(th)}}{dT} \approx \frac{1}{T} \cdot \left(\psi_B - \frac{E_{g(0)}}{2q} \right) \cdot \left(2 + \frac{1}{C_{ox}} \cdot \sqrt{\frac{\epsilon_s \cdot q \cdot N_A}{\psi_B}} \right) \quad (3.6)$$

where ψ_B is the Fermi level from intrinsic Fermi level (i.e., middle bandgap), $E_{g(0)}$ is the band gap at 0 K, C_{ox} is oxide capacitance, ϵ_s is permittivity of semiconductor and N_A is the acceptor density. The complete derivation is shown in Appendix A.1.2. It can be seen that $V_{GE(th)}$ decreases with temperature.

Temperature Dependency of g_{fs}

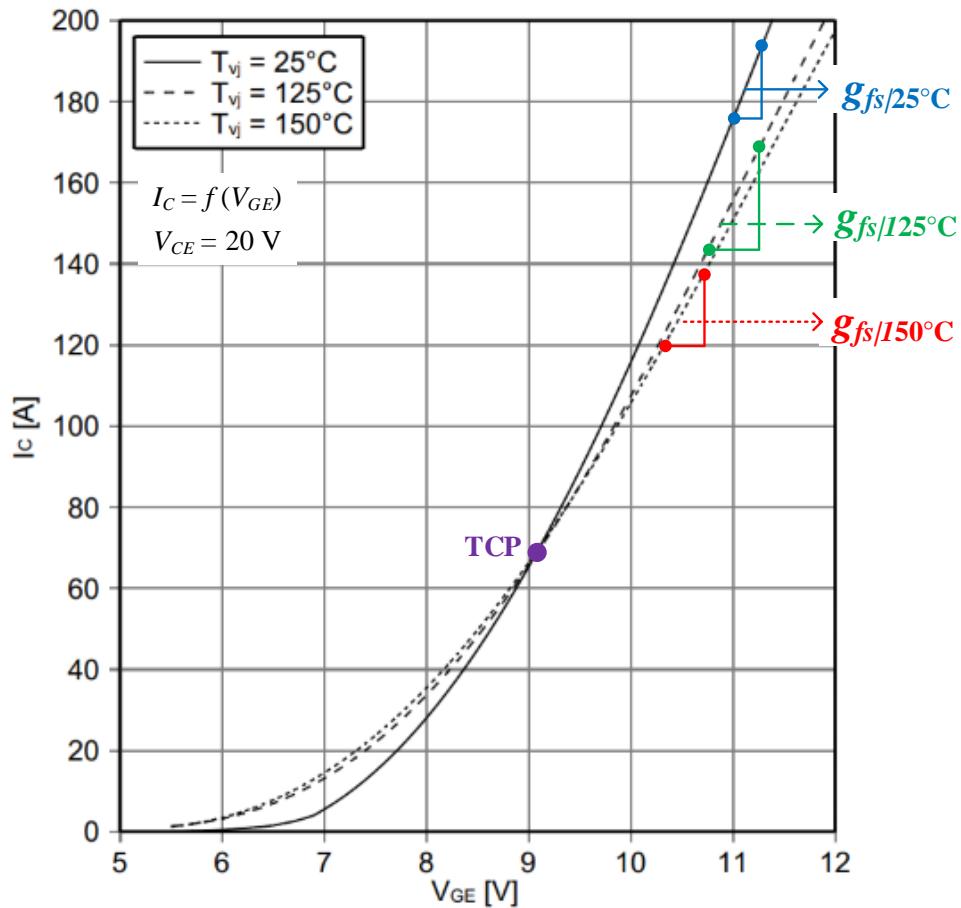


Figure 3.10: Example of a transfer characteristic [Inf13, P.7]

Transconductance g_{fs} is given by Equation 3.7:

$$g_{fs} = \kappa \cdot (V_{GE} - V_{GE(th)}) \quad (3.7)$$

where κ is given by:

$$\kappa = \frac{W \cdot \mu_n \cdot C_{ox}}{L} \quad (3.8)$$

where W and L is the width and length of channel, respectively. Hence, temperature dependency of g_{fs} varies from κ and $V_{GE(th)}$. Both of them decrease with temperature and lead to opposite result:

- If $V_{GE(th)}$ is predominated, g_{fs} increases with temperature.
- On the contrary, g_{fs} decreases with temperature if κ dominates.

Figure 3.10 illustrates the transfer characteristic of [Inf13] as an example. It can be shown that g_{fs} decreases with temperature in this case.

All in all, temperature dependency of V_{Miller} varies from $V_{GE(th)}$ and g_{fs} . While $V_{GE(th)}$ leads to V_{Miller} decreasing, g_{fs} causes V_{Miller} increasing with temperature. Measurement results in [HZL19] are consistent with this inference.

Moreover, V_{Miller} is I_C , $R_{G(off)}$ and ageing state dependent, see Table 3.2. In the following sections, impact of these parameters are investigated.

3.4.2 Impact on $R_{G(off)}$

Firstly, the simulative results of an IGBT are illustrated in Figure 3.11 under different external $R_{G(off)}$ without consideration of integrated gate resistance R_{int} . It can be seen that:

- The duration of Miller plateau increases with $R_{G(off)}$.
- V_{Miller} stays nearly constant at different external resistance. In other words, despite switching-off velocity of channel can be impacted by $R_{G(off)}$, it has no impact on Miller plateau voltage level.

Nevertheless, owing to the integrated gate resistance of power module, measured V_{Miller} includes enormous error if external $R_{G(off)}$ is applied with small value. Figure 3.12 demonstrates the setup of gate voltage measurement.

It can be seen that measured V_{GE} is the sum of gate voltage at chip $V_{GE(real)}$ and voltage drop over R_{int} . Thus, if R_{ext} (i.e., $R_{G(off)}$) is big enough, then $V_{GE(measure)}$ is nearly equal to $V_{GE(real)}$. Nonetheless, if R_{ext} is as small as R_{int} , then $V_{GE(measure)}$

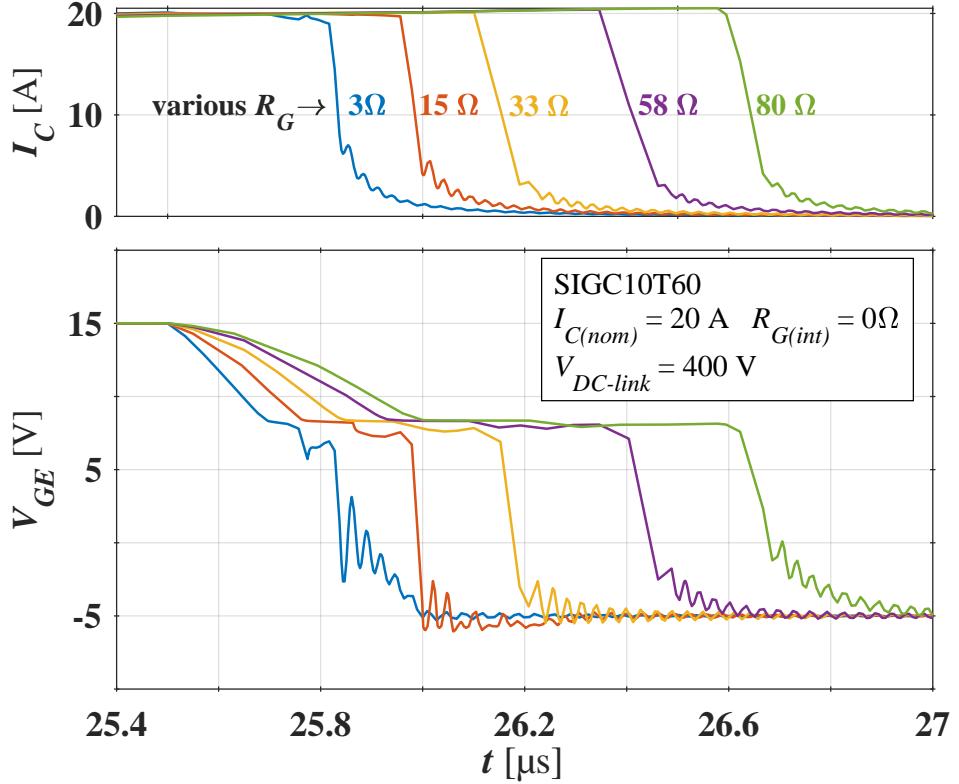


Figure 3.11: Simulative results of V_{Miller} with various $R_{G(off)}$

is large error included due to voltage drop over R_{int} . In application, a fast-switching behaviour is necessary in order to reduce dissipated power. Hence, in most cases, a small $R_{G(off)}$ value is selected. However, this can lead to measurement deviation if integrated gate resistance is not negligible.

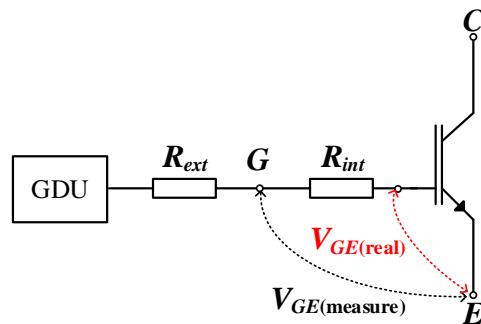


Figure 3.12: Schematic illustration of gate voltage measurement under consideration of integrated gate resistance

3.4.3 Impact on I_C

Dependency of V_{Miller} on I_C is displayed in Figure 3.13. It can be seen that V_{Miller} increases significantly from 100 A to 200 A. Equation 3.5 accounts for the explanation of this result.

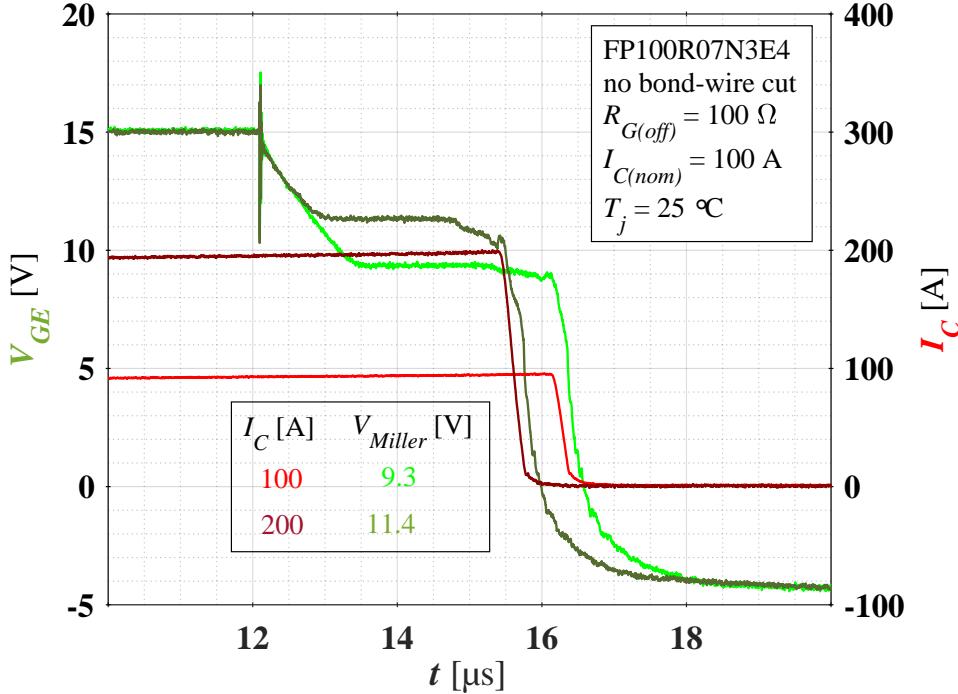


Figure 3.13: Measurement results of V_{Miller} under various I_C

3.4.4 Impact on Ageing State

Figure 3.14 shows V_{Miller} under different ageing state. It has to be remarked that bond-wire was cut artificially instead of bond-wire lift-off after Power Cycling Test (PCT). Since the ageing of PCT is predominately affecting the external chip connections, the Miller capacitance C_{CG} should not be influenced. [LHD⁺21] Nonetheless, owing to the ageing effect, distribution of load current is no more homogeneous (see Section 2.3.1). For IGBT cells with intact bond-wire, according to Equation 3.5, V_{Miller} increases with higher current. A simulation with respect to bond-wire cut is performed in [Bä20]. According to this simulative result, since all cells are paralleled, maximum of V_{Miller} should be measured. Therefore, V_{Miller} increases with ageing.

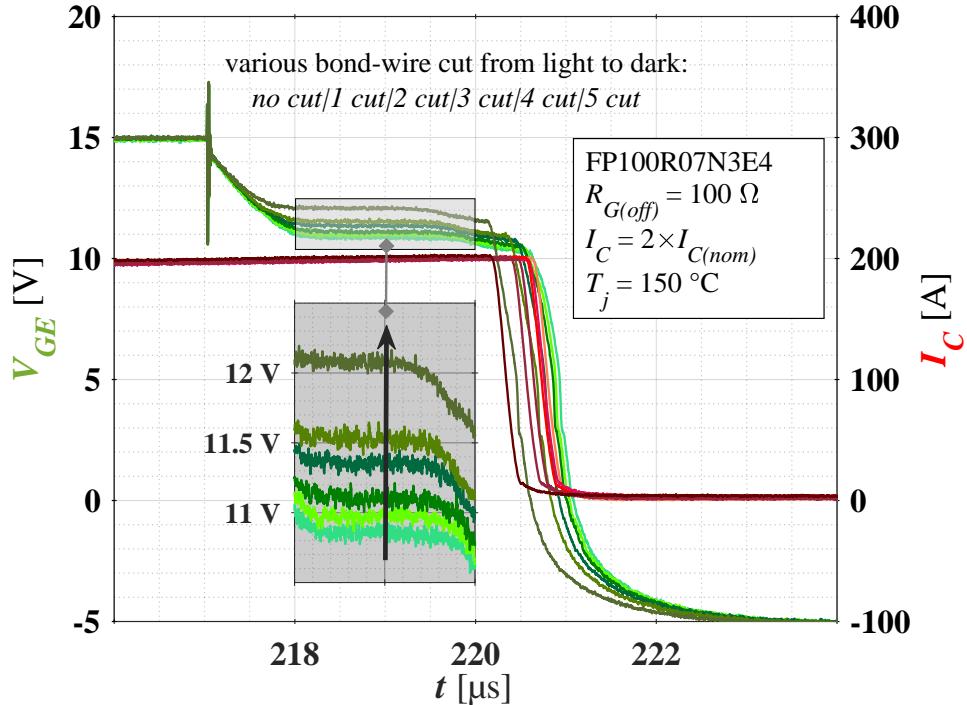


Figure 3.14: Measurement results of V_{Miller} under various ageing state

3.4.5 Conclusion

It can be inferred by the dependency investigations that V_{Miller} is not suitable as a TSEP to use because:

- Small $R_{G(off)}$ is applied in the application.

V_{Miller} cannot be measured precisely due to the integrated gate resistance.

- V_{Miller} shows strong dependency on I_C and ageing state.

Since I_C is not constant during repetitive operation (see Section 5.3), it increases the calibration effort extensively.

3.5 $V_{CE(on-sense)}$ as alternative TSEP

3.5.1 Derivation of Temperature Dependency

When IGBT is on, holes flow from collector via n^- -region to emitter and electrons flow on the opposite direction. In this case, IGBT is equivalent as a pin-diode. Figure 3.15 illustrates carrier density profile of pin-structure during on-state. Build-in voltage exists between p^+n -junction and n^+n -junction due to the space charge region of junctions at thermal equilibrium. Nevertheless, only part of them contributes to

forward voltage and named as V_j because rest of them is used to reduce potential steps at junctions [SN07]. Therefore, V_j is given by Equation 3.9:

$$V_j = V_{p^+n} + V_{nn^+} = \frac{k \cdot T}{q} \cdot \ln \left(\frac{p_L \cdot n_R}{n_i^2} \right) \quad (3.9)$$

where p_L and n_R are holes from left side (i.e., collector side) and electrons from right side (i.e., emitter side).

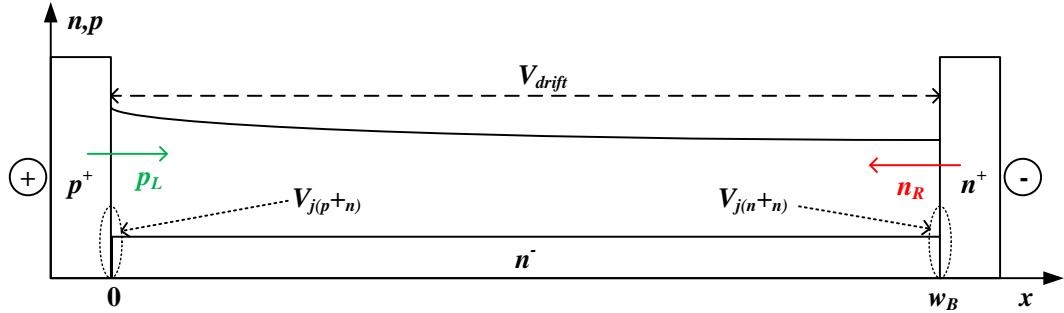


Figure 3.15: Carrier density profile of IGBT during on-state

Apart from that, resistive voltage due to the majority carrier currents at high current densities V_{drift} is included. Hence, the forward voltage V_F is given by Equation 3.10:

$$V_F = V_j + V_{drift} \quad (3.10)$$

It can be inferred from Equation 3.9 that V_j decreases with temperature. Moreover, $V_F \approx V_j$ can be derived according to Equation 3.10 if IGBT conducts under sense current due to the negligible V_{drift} . Therefore, $V_{CE(on-sense)}$ decreases with temperature.

3.5.2 Impact on T

$V_{CE(on-sense)}$ as a TSEP is widely used in PCT due to the independency of ageing state and self-heating [LSSDD18, SS09]. Figure 3.16 shows the calibration curve of an IGBT module. Typically, a current density of 100 mA/cm^2 is selected. It can be seen that $V_{CE(on-sense)}$ shows very good linearity over a wide temperature range.

However, in order to measure $V_{CE(on-sense)}$, the blocking phase of DUT has to be interrupted. Further, a certain delay time has to be considered, before the TSEP can

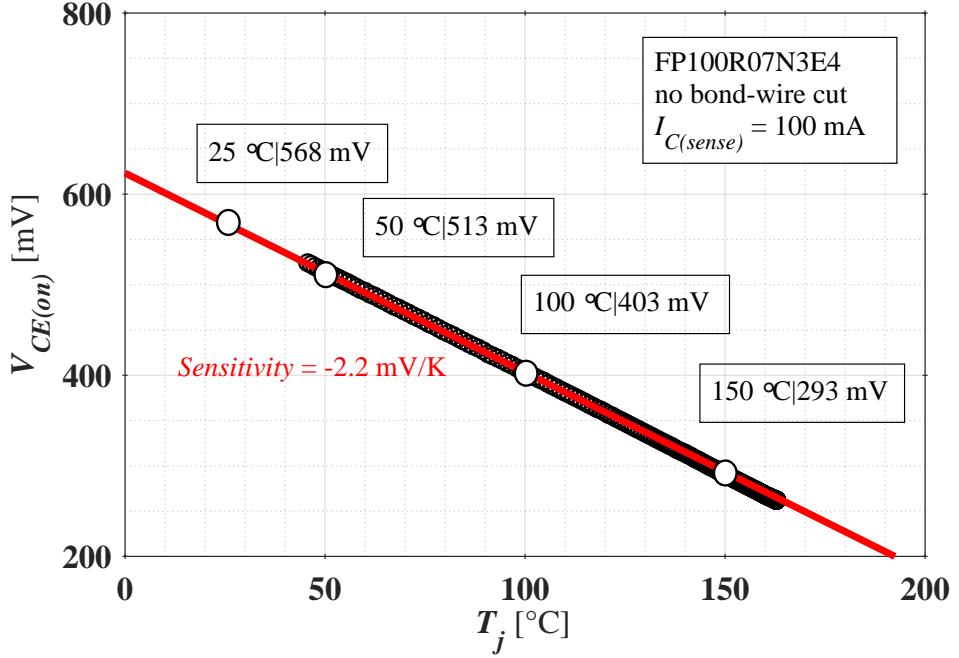


Figure 3.16: Measured calibration curve of $V_{CE(on-sense)}$ under 100 mA I_C

be recorded. This delay is determined by the sense current settling time and the tail current turn-off time and accounts for a couple of micro seconds for IGBTs. During this time, the junction temperature decreases already and therewith decreases the accuracy of the temperature determination method. [HFB⁺16] A detailed simulation model is further necessary to take this delay time into account and find the real maximum temperature right before turn-off.

3.5.3 Conclusion

It can be concluded that $V_{CE(on-sense)}$ is not feasible to be applied during repetitive operation, because device is either blocking a high voltage or conducting a high current. In order to measure $V_{CE(on-sense)}$, repetitive operation has to be interrupted.

3.6 $V_{CE(on-load)}$ as alternative TSEP

3.6.1 Derivation of Temperature Dependency

As introduced in Equation 3.10, V_{drift} plays an essential role when IGBT conduct under load current. V_{drift} is given by Equation 3.11:

$$V_{drift} = \frac{w_B^2}{(\mu_n + \mu_p) \cdot \tau_{eff}} \quad (3.11)$$

where w_B is the base width and τ_{eff} is the effective lifetime of carrier.

Based on Equation 3.11, opposing effects have to be considered with respect to the temperature dependency of $V_{CE(on-load)}$:

- Mobilities decrease with temperature, which leads to V_{drift} increasing;
- Carrier lifetime increases with temperature, which causes V_{drift} decreasing.

Figure 3.17 displays an output characteristic of [Inf13] as an instance. It can be seen

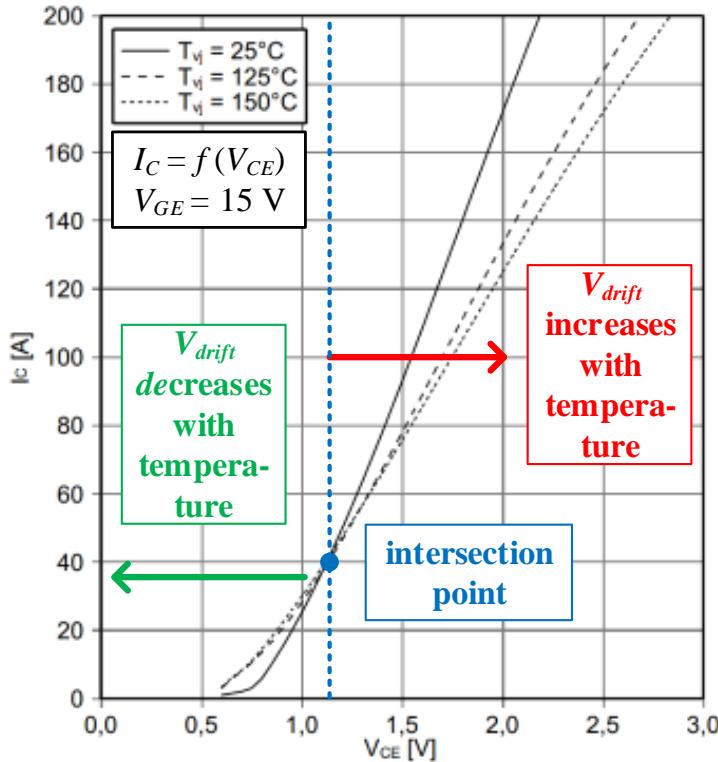


Figure 3.17: Example of an output characteristic [Inf13, P.7]

that $V_{CE(on-load)}$ strongly depends on I_C . In addition, an intersection point occurs at $I_C = 40 \text{ A}$. The temperature dependency of $V_{CE(on-load)}$ varies from load current:

- For a fixed I_C below 40 A, $V_{CE(on-load)}$ decreases with temperature;
- $V_{CE(on-load)}$ increases with temperature beyond 40 A.

Moreover, as mentioned in Table 3.2, the impacts of I_C and ageing state are investigated in following sections.

3.6.2 Impact on I_C

Figure 3.18 depicts calibration curves of $V_{CE(on-load)}$ under various I_C with 500 Hz switching frequency. It can be seen that:

- $V_{CE(on-load)}$ shows positive temperature coefficient under selected load current. Therefore, the sensitivity increases with I_C .
- $V_{CE(on-load)}$ shows good linearity with T_j .

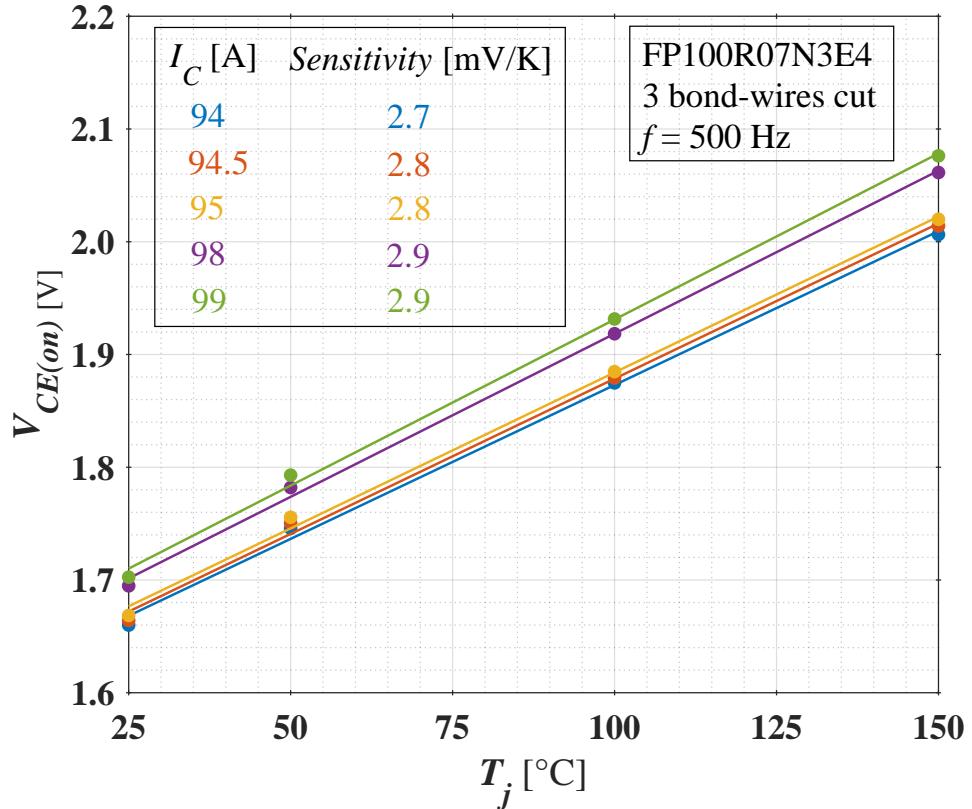


Figure 3.18: Measured calibration curve of $V_{CE(on-load)}$ under various I_C

3.6.3 Impact on Ageing State

IGBT Module

Figure 3.19 depicts calibration curves of an IGBT module under various number of bond-wires (i.e., front-side ageing state). It can be inferred that the sensitivity increases significantly with ageing state under a fixed switching frequency and I_C .

Nonetheless, it has to be remarked that the measured IGBT module has no Kelvin contact (i.e., bond-wires included) at emitter side, see Figure 5.2. Thus, according to Equation 2.8 and 2.9, the measured $V_{CE(on-load)}$ has an additional voltage drop over bond-wires, which leads to measurement error.

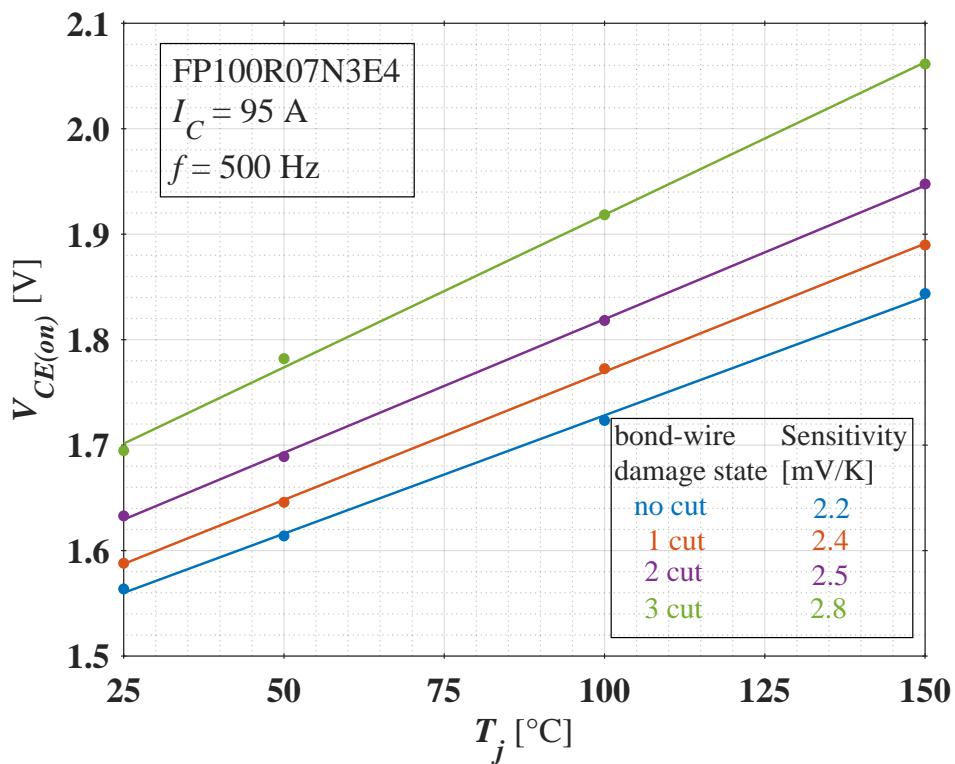


Figure 3.19: Measured calibration curve of $V_{CE(on-load)}$ under various ageing state with 500 Hz switching frequency

DCB Chip

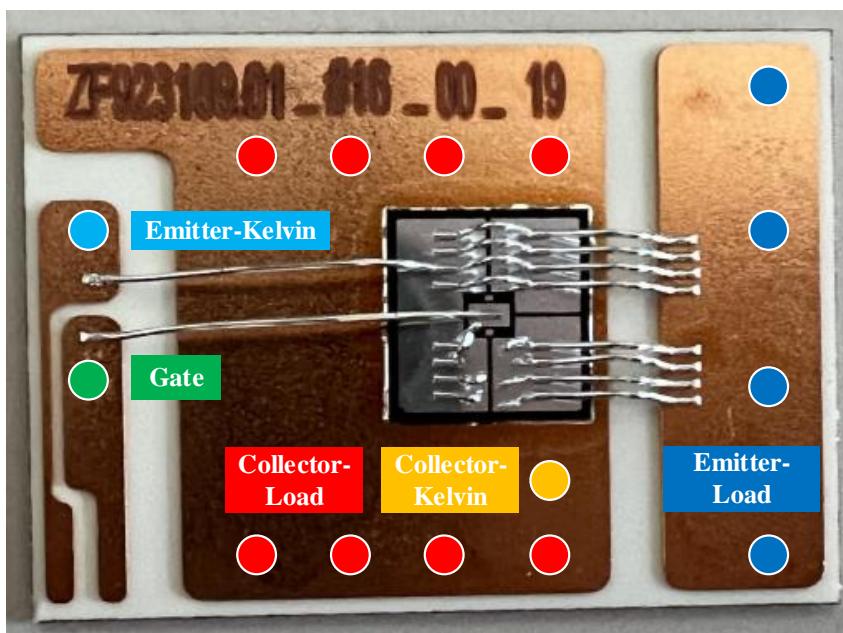


Figure 3.20: Layout of an IGBT chip with DCB package

As a comparison, calibration under nominal load current ($I_C = 150$ A) is performed by a Direct Copper Bonded (DCB) IGBT chip, with which $V_{CE(on)}$ can be measured both at Kelvin (i.e., $V_{CE(on-Kelvin)}$) and load contact (i.e., $V_{CE(on-load)}$). The layout of DCB chip is displayed in Figure 3.20.

Figure 3.21 illustrates the measurement results of DCB IGBT chip at various emitter contact. The sensitivity and offset of calibration curve are listed in Table 3.2.

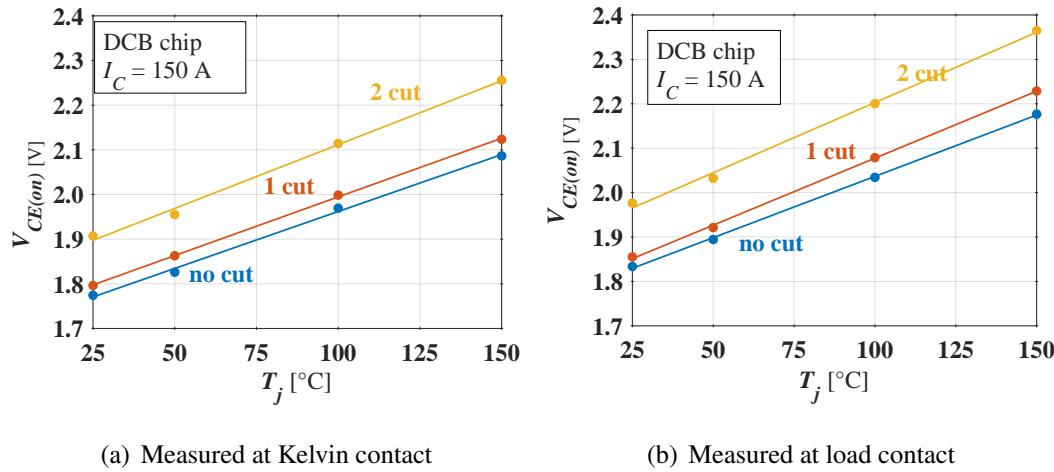


Figure 3.21: Measured calibration curves of a DCB IGBT chip at various emitter contact with ageing

Table 3.2: Sensitivity and offset of calibration curves with a DCB IGBT chip under each ageing state at respective Kelvin and load contact

Bond-wire state		no cut	1 cut	2 cut
Sensitivity [mV/K]	Kelvin	2.5	2.6	2.9
	Load	2.8	3	3.2
Offset [V]	Kelvin	1.71	1.73	1.83
	Load	1.76	1.78	1.89

It can be concluded from Table 3.2 that:

- Under each ageing state, sensitivity and offset at load contact are higher than at Kelvin contact all the time.
- Sensitivity and offset at each Kelvin and load emitter contact increase with ageing.

Explanation of Variation under Kelvin Contact

Since $V_{CE(on)}$ increases due to ageing, offset is correspondingly rises. In order to explain the increasing increase of sensitivity, output characteristics are performed with Kelvin contact under initial and 2 bond-wire cut state respective at room temperature and 150 °C. Curves are displayed in Figure 3.22.

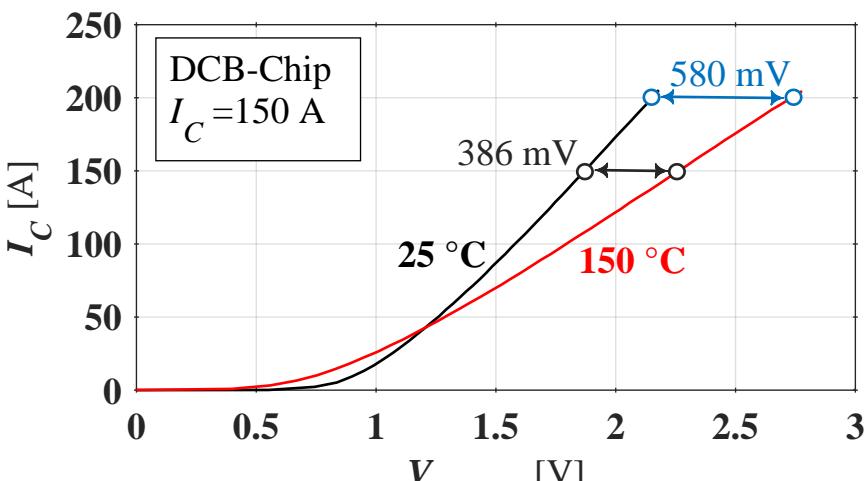
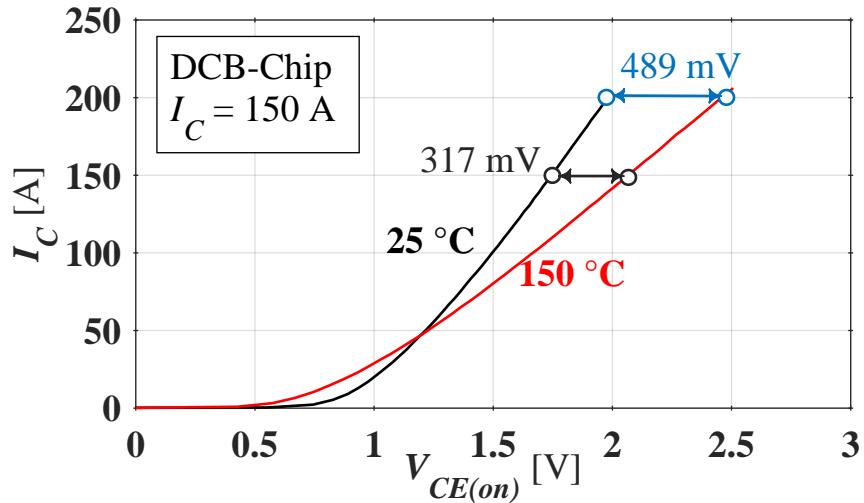


Figure 3.22: Measured output characteristic of a DCB IGBT chip at Kelvin contact under various ageing state

It can be seen that after ageing:

- $V_{CE(on-Kelvin)}$ increases at fixed temperature.

- $V_{CE(on-Kelvin)}$ rises more with temperature at fixed load current.

It can be further inferred that owing to ageing:

- $V_{CE(on-chip)}$ increases at fixed temperature.
- Segments with intact bond-wires conduct more current, which results to higher $V_{CE(on-chip)}$ and hence the sensitivity increases.

Explanation of Variation under Load Contact

In view of load contact, the sensitivity is higher than Kelvin contact under the fixed ageing state in Table 3.2. Therefore, it can be inferred that the additional resistance R_{eE} in Equation 2.6 is also temperature dependent. Take the equivalent resistance within one segment R_{Sum} into consideration, its temperature dependency is given by Equation 3.12:

$$R_{Sum} = R_{Sum(RT)} \cdot (1 + \alpha \cdot \Delta T) \quad (3.12)$$

where $R_{Sum(RT)}$ is the resistance at room temperature, α is the temperature coefficient of resistivity and ΔT is the temperature difference. Moreover, R_{Sum} increases with ageing and leads to higher voltage drop, which overlays on $V_{CE(on-load)}$. This effect will worsen when IGBT is exposed at high temperature.

Since the sensitivity is $V_{CE(on-chip)}$ and R_{Sum} dependent, recalibration has to be performed for each ageing state.

3.6.4 Summary of Temperature Dependency for $V_{CE(on-load)}$

In summary, temperature dependency of $V_{CE(on-load)}$ under consideration of load current level (i.e., operation condition) is shown in Figure 3.23.

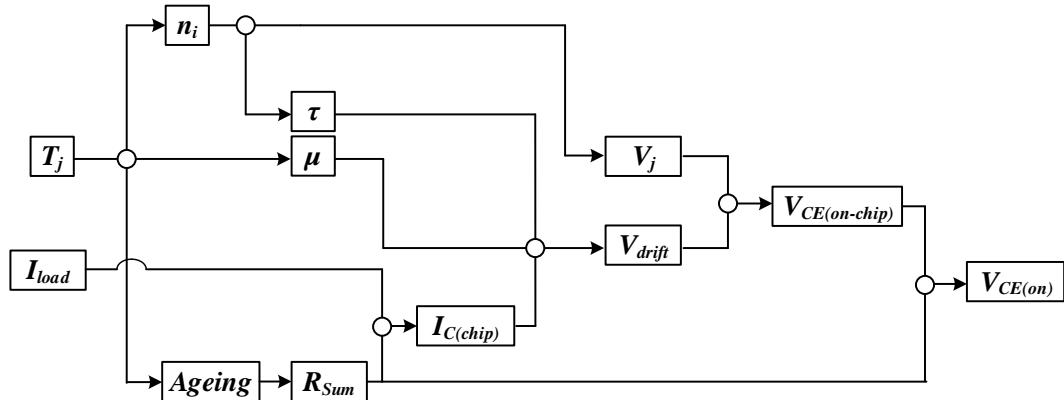


Figure 3.23: Temperature dependency of $V_{CE(on)}$

3.6.5 Conclusion

Compared with other alternative TSEPs, $V_{CE(on-load)}$ has very good linearity with T_j . By means of clamping circuit (see Section 5.1.4), $V_{CE(on-load)}$ can be measured with I_C simultaneously. However, recalibration is necessary after each ageing state.

All in all, $V_{CE(on-load)}$ is utilized as TSEP in this work for the determination of junction temperature. Moreover, optical method (IR-camera) and physical method (thermocouple) are also used for the determination of surface and case temperature, see Section 5.4.

4 Calibration

In this chapter, approach of temperature calibration based on $V_{CE(on-load)}$ as TSEP is introduced. Especially, the calibration accuracy is evaluated.

4.1 Setup

DUT is placed on a temperature adjustable heat plate and module baseplate is heated. Four stepped temperatures are selected for temperature calibration, respective 25 °C, 50 °C, 100 °C and 150 °C. In addition, before each calibration, $V_{CE(on-sense)}$ is utilized as TSEP to ensure that T_j equals to T_c during calibration. The DUT is turned on, a current source with 100 mA sense current is connect with collector and emitter. $V_{CE(on-sense)}$ is measured by multimeter. Value of $V_{CE(on-sense)}$ at each stepped temperature is given in Figure 3.16. For each stepped temperature, DUT is calibrated at 500 Hz and 1000 Hz, respectively. Pulse pattern for calibration is shown in Table 4.1. Values for each time duration are shown in Appendix, see Table A.2.

Table 4.1: Pulse pattern for calibration at specified switching frequency

GDU	$t_1 \sim t_2$	$t_2 \sim t_3$	$t_3 \sim t_4$
HS	on	off	on
LS/DUT	on	on	on

According to Table 4.1, 3 stages are shown during calibration:

- Stage 1: $t_1 \sim t_2$ (first turn-on phase)

Both HS- and LS/DUT-IGBT are on. I_C is hence ramped-up from 0 to the desired current level.

- Stage 2: $t_2 \sim t_3$ (free-wheeling phase)

I_C is free-wheeled in LS/DUT, because HS-IGBT is off. Especially, this duration is set to half of the switching period in repetitive operation in order to perform 50% duty cycle.

- Stage 3: $t_3 \sim t_4$ (second turn-on phase)

Both HS- and LS/DUT-IGBT are turned-on and I_C ramps-up again to desired current level.

It has to be remarked that time points from t_2 to t_4 are only utilized for the verification of self-heating issue. For the calibration itself, pulse pattern is independent on the switching frequency and hence, only first turn-on phase should be considered.

4.2 Approach

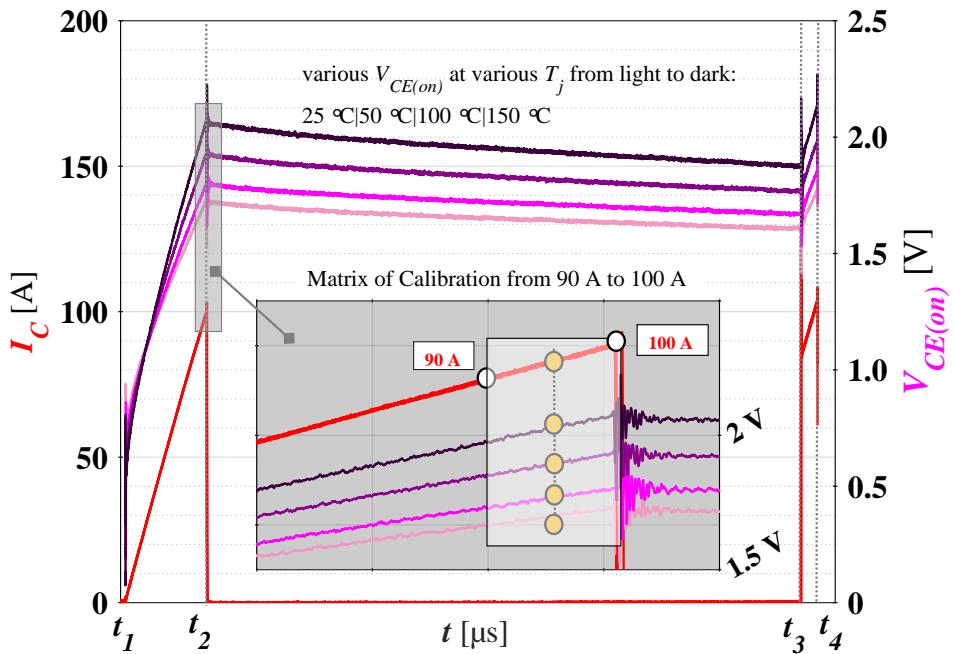


Figure 4.1: Waveforms of $V_{CE(on-load)}$ and I_C based on Table 4.1 during calibration for a repetitive switching under the current level of 100 A

Figure 4.1 depicts waveforms of I_C and $V_{CE(on-load)}$ at 4 stepped temperatures based on Table 4.1 with a 100 A nominal current. Since Rogowski coil is wound on busbar plus, only ramp-up phase of current can be detected (see Section 5.2 and 5.3).

It can be seen that $V_{CE(on-load)}$ rises with temperature under fixed I_C . As displayed in zoomed area, white dots account for minimum and maximum of current, respective 90 A and 100 A. Furthermore, current is scaled with 0.1 A increment. As a result, calibration vector of current $\vec{I}_{C(calib)}$ with 101 elements can be determined.

Along the dot line that for each current value at each time point, 4 $V_{CE(on-load)}$ values (yellow dots in zoomed area) can be found. Therefore, calibration matrix of on-state

voltage $\vec{V}_{CE(on-calib)}$ with 4×101 elements can be determined. The obtained curves $V_{CE(on-load)} = f(I_{Load}, T_j)$ are in the end linear fitted by a Savitzky-Golay filter.

4.3 Accuracy Evaluation

In order to evaluate calibration accuracy, several potential impact factors are investigated.

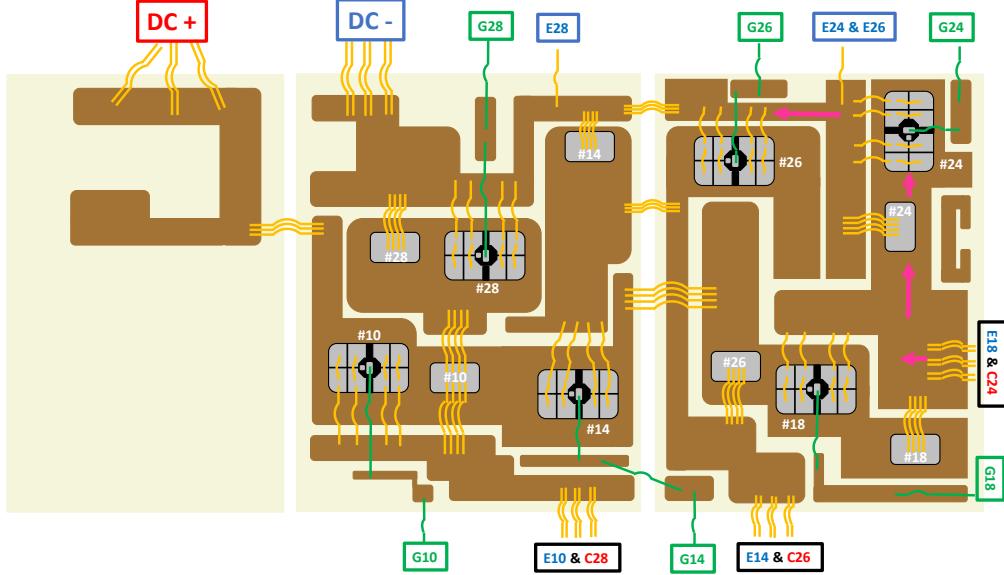


Figure 4.2: Front-side layout of used module and current flow direction of DUT, including common source

4.3.1 Current Slope and Induced Gate Voltage

Figure 4.2 depicts the layout of DUT. Subsystem #14 and #24 are selected as HS and LS/DUT, respectively. The current flow direction is shown in red arrow. Since only load contact is available for the DUT, the common source of DUT is high. According to Figure 4.1, current slope exists at first turn-on phase during calibration (i.e., time point $t_1 \sim t_2$). This current slope leads to a positive induced gate voltage and thus, applied V_{GE} at chip is reduced. In addition, this induced voltage is part of the measured $V_{CE(on-load)}$. To investigate this effect, two measurement were performed.

Current Slope

DUT was calibrated by AC (clamping circuit) and DC (curve tracer), respectively. The results are shown in Figure 4.3. Note that the offset at fixed temperature results

of different adapter for $V_{CE(on-load)}$ measurement. It can be seen that sensitivity is not changed.

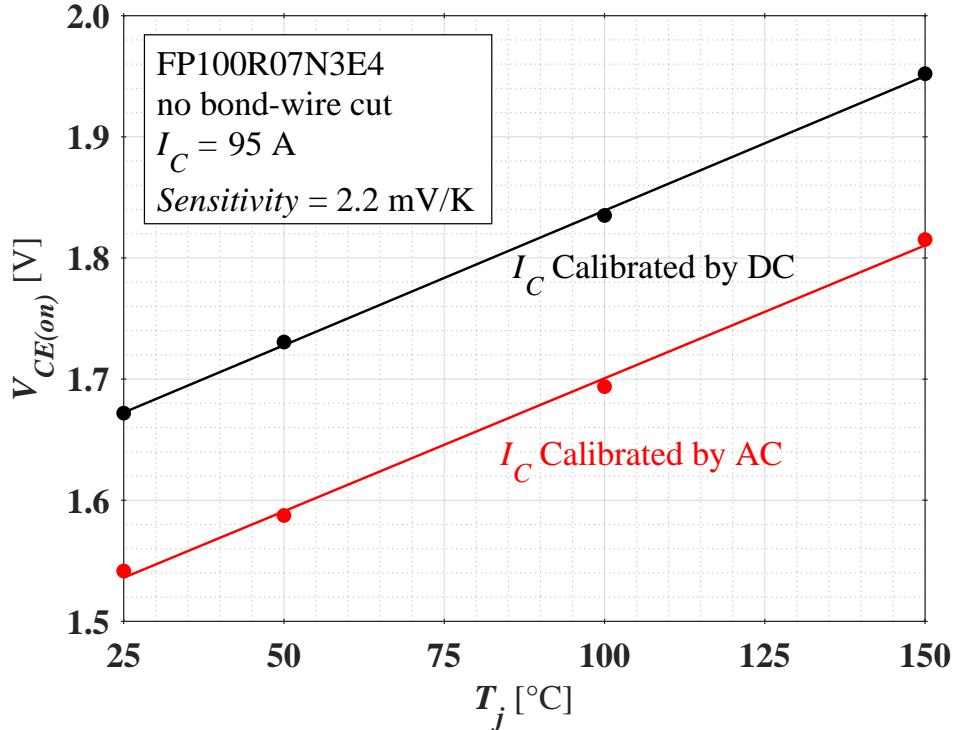


Figure 4.3: Impact of di/dt on calibration

Induced Gate Voltage

DUT was calibrated by DC (curve tracer) at $V_{GE} = 15$ V and 14.5 V to qualitatively perform the effect of induced gate voltage. Measurement results are shown in Figure 4.4. It can be seen that sensitivity changes marginally.

Conclusion

It can be concluded that owing to the current slope, V_{GE} decreased marginally during calibration and impact on $V_{CE(on-load)}$. However, this measurement deviation due to induced gate voltage is almost temperature independent and hence, belongs to systematically error during repetitive operation.

4.3.2 Self-Heating

As displayed in Figure 4.1, calibration matrix is selected at first turn-on phase. Before second turn-on phase, DUT is self-heated during free-wheeling phase due to the power loss during conduction. As a consequence, temperature is increased and further leads to $V_{CE(on-load)}$ rising.

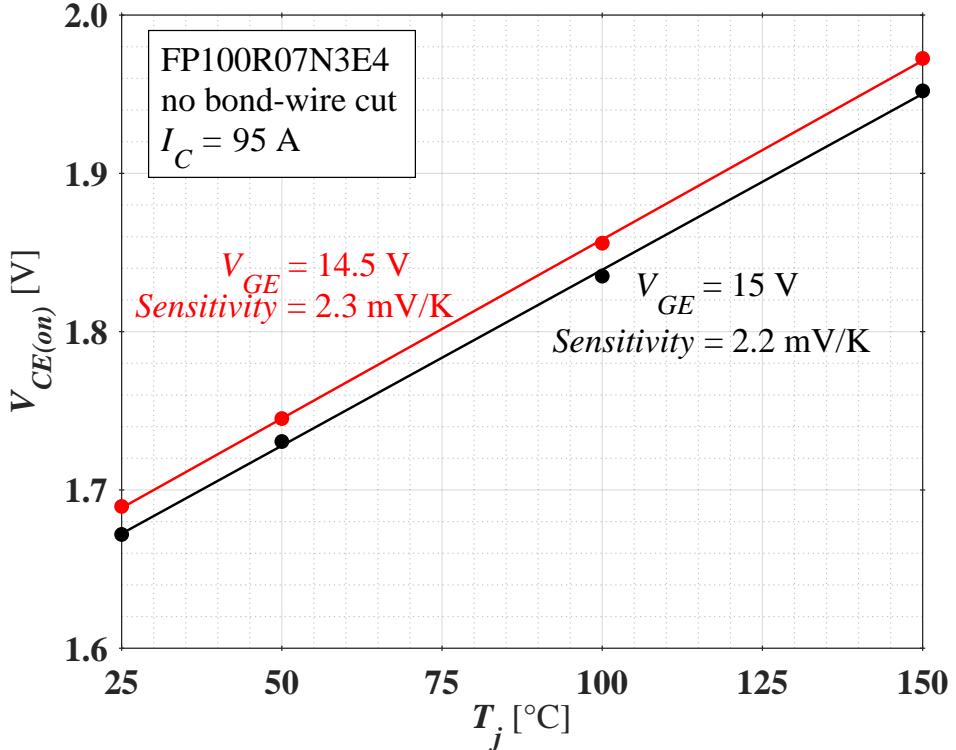


Figure 4.4: Impact of induced gate voltage on calibration

To investigate the impact of self-heating on calibration, a calibration matrix at second turn-on phase is performed. The results are depicted in Figure 4.5. It can be revealed that under 95 A load current, self-heating results to 5 K increasing of T_j .

Moreover, in view of first turn-on phase, a load coil with low inductance should be selected and the time point t_2 in Table 4.1 should be as small as possible, so that the self-heating issue at first turn-on phase can be negligible.

4.3.3 Inaccuracy of I_C Measurement

In this work, Rogowski was applied for I_C measurement, see Section 5.1.5. Figure 4.6 shows a calibration waveforms of I_C and $V_{CE(on-load)}$ at 25 °C. Especially, I_C is calibrated by Rogowski and shunt resistor, respectively. Since shunt resistor features a higher bandwidth, no delay time and is not affected by voltage slopes, it can be assumed that by shunt resistor measured I_C approximates more to expected.

It can be seen that for the fixed current value, $V_{CE(on-load)}$ calibrated by shunt resistor is smaller than Rogowski. As a consequence, T_j determined by shunt resistor is 5 K higher than determined by Rogowski, see Figure 4.7. Therefore, T_j is underrated,

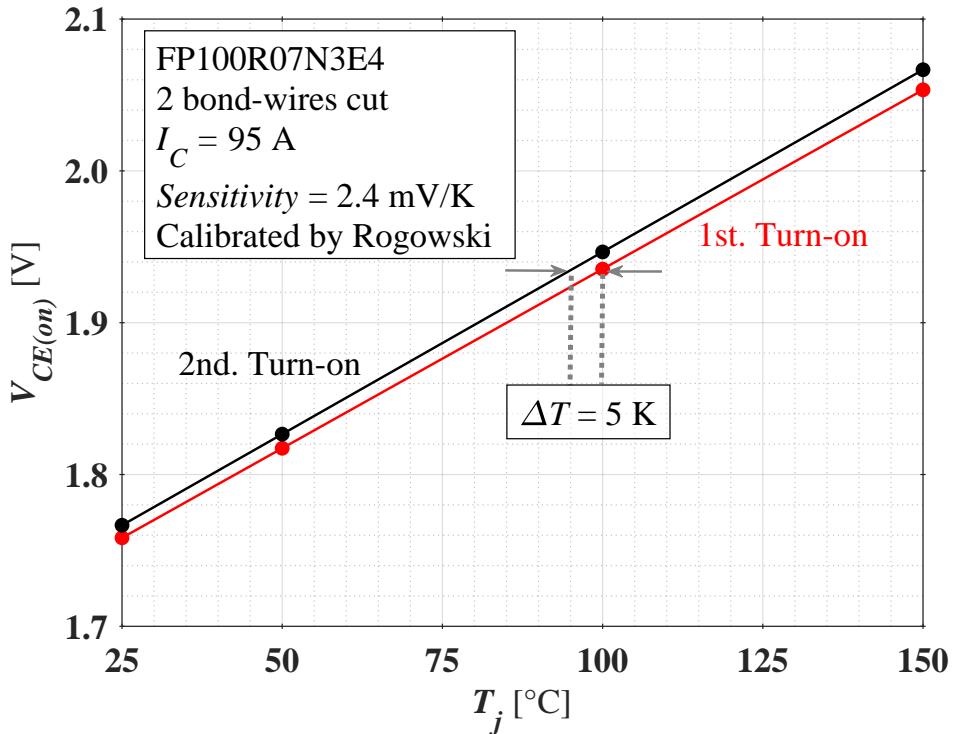
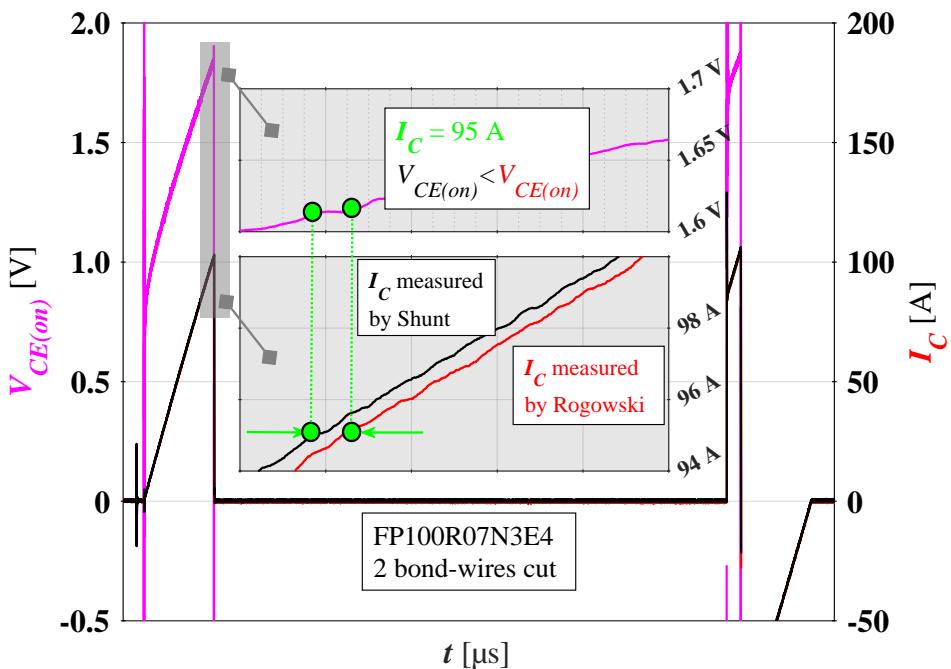


Figure 4.5: Impact of self-heating on calibration

Figure 4.6: Waveforms of $V_{CE(on-load)}$ and I_C measured by Rogowski (red) and shunt (black) at 25 °C

when a Rogowski coil is used.

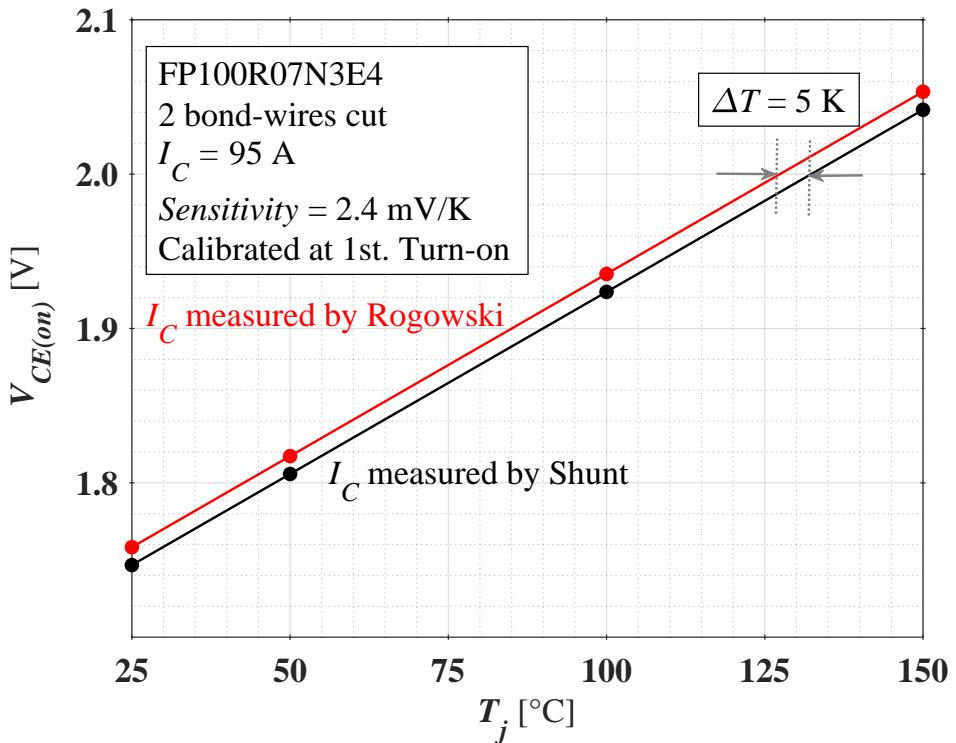


Figure 4.7: Impact of measurement equipment for I_C on calibration

4.3.4 Parameters for $V_{CE(on-load)} = f(T_j)$ during Calibration and Repetitive Operation

During calibration, $V_{CE(on-load)}$ is measured at fixed temperature and I_C . Then, according to Equation 3.4, the sensitivity A and offset B are derived. During repetitive operation, each I_C matches a $V_{CE(on-load)}$ value. Substitute this $V_{CE(on-load)}$ to calibration curve, junction temperature T_j is estimated, see Figure 5.11.

However, these by calibration determined parameters may differ from repetitive operation because for a fixed I_C :

- DUT was passive heated during calibration, hence despite the ageing state, temperature distribution is homogeneous.
- During repetitive operation, however, the power loss is consistently generated within each segment and leads to temperature rising. Owing to the ageing state, temperature distribution of DUT is no longer homogeneous. According to Equation 2.9 and 3.12, R_{Sum} increases and further for a fixed temperature, $V_{CE(on-load)}$ is higher than calibration. It can be assumed that a higher sensitivity and offset can

be determined during repetitive operation.

Figure 4.8 depicts the parameters for a fixed current during calibration and repetitive operation, respectively. It can be seen that for a fixed $V_{CE(on-load)}$ measured during repetitive operation, T_j estimated by calibration curve is overrated.

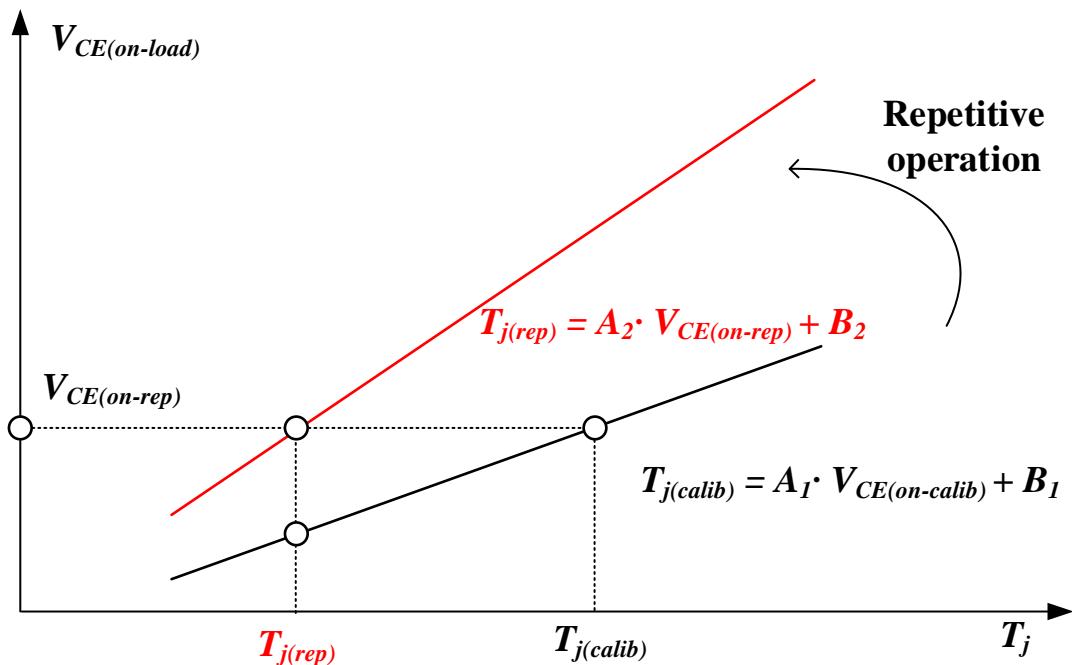


Figure 4.8: Schematic illustration of parameters for calibration and repetitive operation

4.3.5 Summary of Measurement Deviations

It can be concluded that measurement deviations consist of:

- systematically deviations, which are temperature independent
 - Current slope during calibration leads to a induced voltage, which further results to a smaller V_{GE}
 - Inaccuracy of I_C measurement due to the Rogowski coil leads to an offset of $V_{CE(on-load)}$ in calibration curve for a fixed current. Furthermore, temperature is underrated by using Rogowski
- dynamic deviations, which are temperature dependent
 - Self-heating issue should be avoided during calibration. To do that, several strategies are proposed
 - * I_C and $V_{CE(on-load)}$ should be calibrated at first turn-on phase in Table 4.1
 - * Load coil should be selected with small inductance;
 - * The duration of I_C ramps-up should be short
 - Owing to the inhomogeneous temperature distribution during repetitive operation, the sensitivity and offset determined by calibration may no longer suitable. However, it is difficult to verify the parameters for repetitive operation. Only calibrated parameters are available. Hence, temperature may be overrated

All in all, whether systematically or dynamic error, it is difficult to neither qualitative or quantitative determine which deviation is predominated. Because only one chip was tested in this work and hence there is no other results as comparison. However, it is necessary to list all possible impacts on calibration.

5 Repetitive Switching Operation

In this chapter, test bench setup is introduced. Switching principle and current development are explained. Three temperatures are determined during repetitive operation. Methods of temperature determination are illustrated.

5.1 Test Bench Setup

Figure 5.1 depicts the applied circuit for repetitive operations. A single-phase H-bridge circuit was used. The measured quantities are shown with dotted lines. It can be seen that 5 parts are included in this circuit, respective high voltage supply (HV), protection IGBT (PIGBT), HS-IGBT, LS-IGBT as DUT and clamping circuit for $V_{CE(on-load)}$ measurement. HS- and LS-IGBT corresponded to 2 subsystems of a complete six pack IGBT module, see Figure 4.2. The setup of each part is illustrated in detail in following sections.

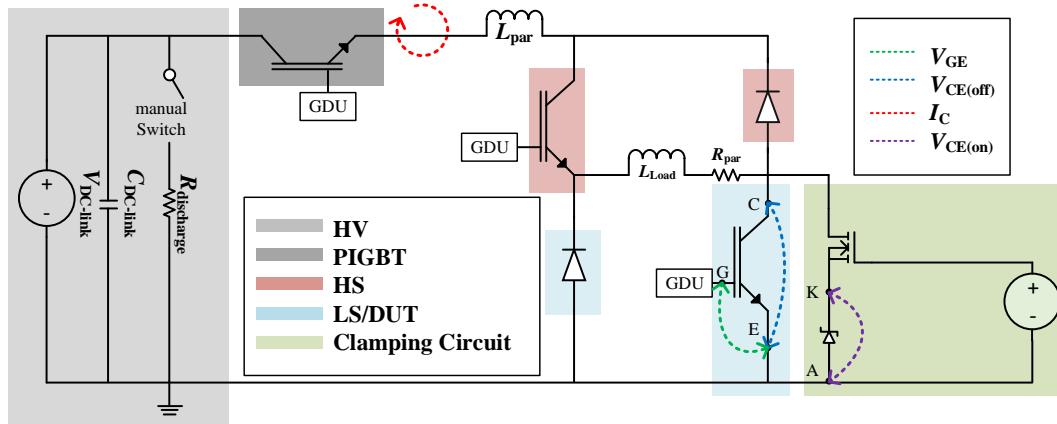


Figure 5.1: Schematic illustration of the performed circuit for repetitive operations

5.1.1 HV

The DC-link voltage $V_{DC-link}$ is determined via a high voltage source and buffered by a capacitor $C_{DC-link}$. For the performed measurement, a voltage of $V_{DC-link} = 300\text{ V}$ and a total capacitance of $C_{DC-link} = 2.26\text{ mF}$ were specified. The buffer capacitor can be discharged by the discharge resistance $R_{discharge}$ when the manual switch turns on.

5.1.2 PIGBT

A 1.5 kA and 4.5 kV IHM IGBT module with V_{CE} failure detection was utilized as PIGBT. Collector of PIGBT was connected with busbar plus of buffer capacitor and emitter with tested module. To limit the short circuit saturation current in case of failure, a low gate-voltage of 8 V was applied.

5.1.3 IGBT Module

A 100 A and 650 V IGBT EconoPIMTM3 module [Inf13] was used for the measurement. Layout of this module and the additional adapter are shown in Figure 5.2. $DC+$ was connected with emitter of PIGBT, while $DC-$ connected with busbar minus of buffer capacitor. Parasitic inductance of circuit L_{par} is calculated by 112.5 nH. Moreover, a choke with magnetic core coil $L_{load} = 337 \mu\text{H}$ and $10 \text{ m}\Omega$ parasitic resistance R_{par} was used between emitter of HS-IGBT (red area) and collector of LS/DUT-IGBT (blue area).

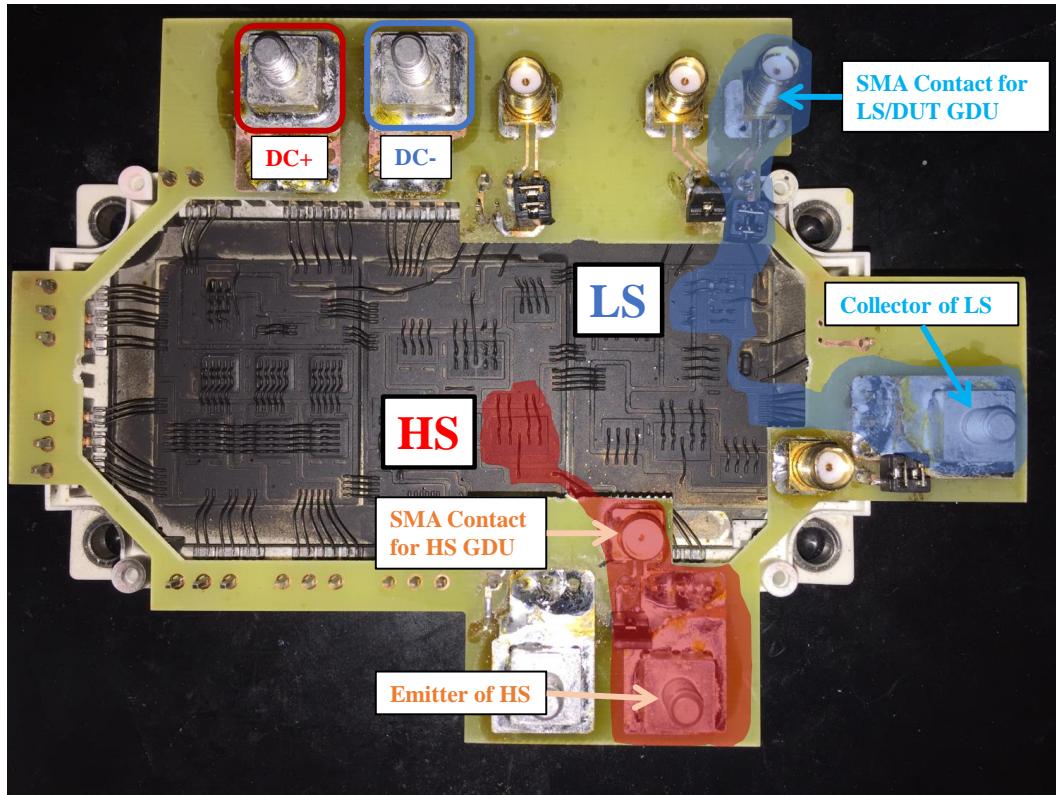


Figure 5.2: Layout and terminal of tested IGBT module

Two gate drivers were utilized for HS- and LS/DUT-IGBT, respectively. The GDUs

were connected with Sub Miniature version A (SMA) connector. It has to be remarked that both HS and LS/DUT have a common path with the load current due to the bond-wires. Despite this, in case of the LS/DUT, the L_{CS} was much lower than HS, see Figure 4.2.

The on-state gate-voltage $V_{GE(on)}$ and off-state gate-voltage $V_{GE(off)}$ were configured by 15 V and -5 V, respectively. External gate resistors $R_{G(on)}$ and $R_{G(off)}$ of 0Ω were selected in order to obtain a fast-switching behaviour.

To operate DUT on a normal operation as shown in data sheet, I_{Load} was specified as nominal current with 100 A.

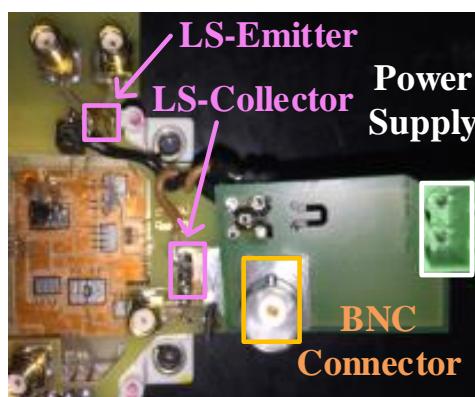
In addition, gel was removed and surface was dyed with black thermo-coating in order to guarantee equal emission coefficients all over the surface, which was investigated by IR-camera.

5.1.4 Clamping Circuit

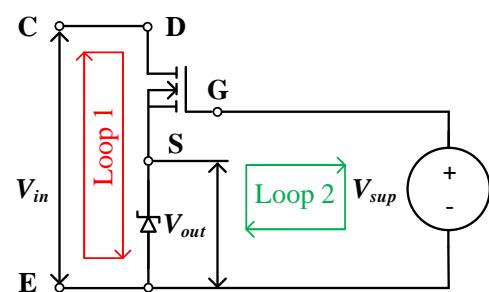
Setup

Since $V_{CE(off)}$ is normally more than several hundred times higher than $V_{CE(on-load)}$, the clamping circuit is broadly used for $V_{CE(on-load)}$ measurement because it can block the $V_{CE(off)}$, which is measured by a high voltage range probe. By means of a low voltage range probe, the measurement accuracy of $V_{CE(on-load)}$ increases.

[LEJ17]



(a) Layout of front-side



(b) Schematic illustration of back-side circuit

Figure 5.3: Clamping circuit for $V_{CE(on-load)}$ measurement

As depicted in Figure 5.3(a), clamping circuit is parallel soldered between collector and emitter of DUT. An additional power supply V_{sup} with 6 V is applied in circuit.

$V_{CE(on-load)}$ is measured via a Bayonet Neill–Concelman (BNC) connector with $75\ \Omega$, which is directly connected to oscilloscope. Figure 5.3(b) illustrates the circuit schematic. A BSP 125 n-channel MOSFET with 600 V blocking voltage and 1.9 V threshold gate voltage $V_{GS(th)}$ and a Zener diode with 9 V Zener voltage V_Z are performed in circuit.

Principle

To illustrate the principle of clamping circuit, $V_{CE(on-load)}$ is concerned as input voltage V_{in} , and the voltage drop over Zener diode is output voltage V_{out} . Based on Kirchhoff circuit laws, two equations are derived from Figure 5.3(b) in loop 1 and 2:

$$V_{in} - V_{out} - V_{DS} = 0 \quad (5.1)$$

$$V_{GS} + V_{out} - V_{sup} = 0 \quad (5.2)$$

Depending on whether DUT is blocking or conductive during repetitive operation, two stages of clamping circuit are specified by V_{CE} and are shown in Figure 5.4.

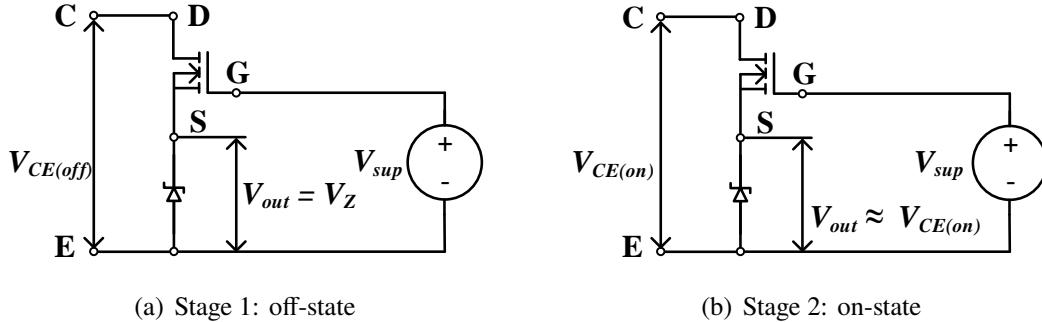


Figure 5.4: Schematic illustration of clamping circuit principle

- Stage 1: off-state

$V_{in} = V_{CE(off)}$. Since $V_{CE(off)} > V_Z$, loop 1 is active and $V_{out} = V_Z$. However, according to equation 5.2, in this case $V_{GS} < V_{GS(th)}$. Hence MOSFET is off and no current flows through MOSFET.

- Stage 2: on-state

$V_{in} = V_{CE(on)}$ and $V_{CE(on)} < V_Z$. According to Equation 5.2, $V_{GS} > V_{GS(th)}$ and MOSFET is able to open. Nevertheless, in this case loop 1 is inactive and current could rarely flow through MOSFET. Hence, based on Equation 5.2, $V_{DS} \approx 0\ \text{V}$ and $V_{out} \approx V_{CE(on)}$.

It can be concluded that, while DUT is blocking, $V_{CE(off)}$ is clamped by MOSFET and when DUT is conductive, $V_{CE(on-load)}$ is almost equivalent to voltage drop over Zener diode. Therefore, the clamping circuit is feasible for $V_{CE(on-load)}$ measurement.

5.1.5 Measuring Probe

V_{GE} , $V_{CE(off)}$, I_C and $V_{CE(on)}$ were simultaneously measured by a 400 MHz and 12-bit oscilloscope during repetitive operation. Passive probes were applied for V_{GE} , $V_{CE(off)}$ and $V_{CE(on)}$ measurement. Informations about probes are shown in Appendix, see Table A.3. Especially, for current measurement, several methods are applied in power electronics:

Shunt Resistor

As mentioned in Section 4.3.3, shunt resistor shows more accuracy than Rogowski coil, see Figure 4.6. In addition, its accuracy is independent on current slope. However, two aspects must be taken into consideration if shunt resistor is used.

- The shunt resistor adds parasitic inductance and resistance into the load commutation loop. Dissipated power is generated when current flows through shunt resistor, which leads further to the increasing of temperature over shunt resistor.
- It complicates the measurement due to a fixed ground potential. Oscilloscope is isolated by an isolation transformer. Hence, the BNC connector of oscilloscope is the uniform reference point in the circuit. Once shunt resistor is applied for I_C measurement, other probes must have the same reference point, which is hardly performed in realistic.

Therefore, shunt is not feasible for repetitive operation.

Clamp Ammeter

Compared with shunt resistor, reference point of clamp ammeter is isolated. Unfortunately, two cables with 16 mm diameter were used for repetitive switching investigation and were not suitable for existing clamp ammeter.

Rogowski Coil

Due to the simple feasibility, Rogowski coil was used for I_C measurement in this work. Moreover, two measurement strategies were proposed after some pre-measurements by Rogowski:

- The measurement position of coil must be rigorously fixed for each measurement due to voltage slope interferences.
- Rogowski coil is wound with busbar plus instead of measuring current directly under DUT due to:
 - the current course with too low di/dt during free-wheeling
 - the package limitation without possibly damaging the DUT bond wires or shade the surface
 - the comparable constant du/dt at $C_{DC-link}$ reduces the electrostatic coupling between the coil and the electrode being measured and further increases the measurement reliability [Iwa15]

These two strategies could strive to ensure that I_C curve not shift vertically during the free-wheel phase of current and each I_C measurement is reproducible.

5.2 Pulse Pattern

As displayed in Table 5.1, a pulse pattern with 50% duty cycle was performed during repetitive operations with two specified switching frequencies. Switching frequency f was specified by 500 HZ and 1000 HZ, respectively.

Table 5.1: Performed pulse pattern for repetitive switching operations with specified switching frequency

Period	$1/2f$			$1/2f$
GDU	t_1	t_2	t_3	t_4
PIGBT	on	on	on	on
HS	on	off	on	on
LS/DUT	on	on	on	off

5.2.1 Aim and Approach

The aim of this pulse was that:

- DUT could be switched-off at nominal load current by each record of oscilloscope.
- The specified pulse pattern keeps the current level within the load almost. Hence, power losses during repetitive operation consist of conduction losses of coil and

switches (i.e., PIGBT, HS- and LS/DUT-IGBT). In this way, the losses approaches to the switching losses of an inverter in the application.

This pulse pattern was continuously generated by LabVIEW program during operations. After overall 20 minutes operation, PIGBT was manually switched-off and hence repetitive operation was ended.

5.2.2 Illustration of Waveforms Based on Pulse Pattern

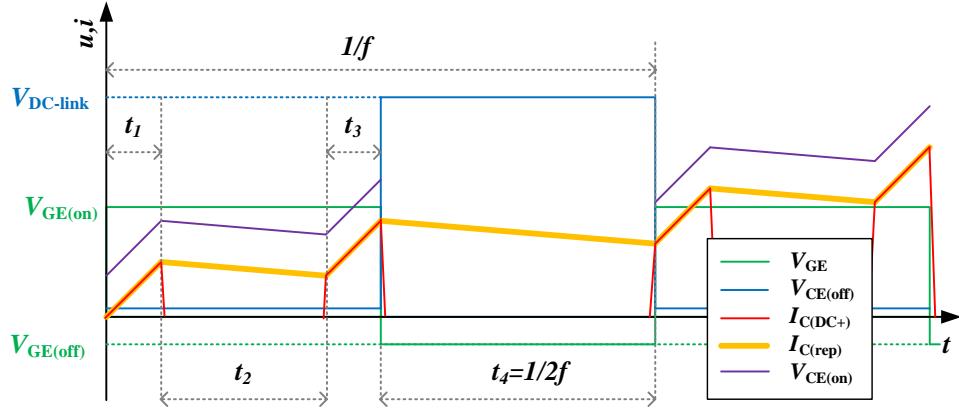


Figure 5.5: Schematic illustration of waveform by performed pulse pattern within one period during repetitive operation

Figure 5.5 illustrates the current and voltage waveforms of LS/DUT, which is based on performed pulse pattern in Table 5.1. Note that y-axis is not scaled. Moreover, load current I_C is characterized by two current curves. Red line is the current at busbar plus $I_{C(DC+)}$, which could be detected by Rogowski. Bold orange line represents the current $I_{C(rep)}$, which flows continuously in circuit.

It can be seen that current ramps-up during time interval t_1 and t_3 , and free-wheeling during t_2 and t_4 . Current during free-wheel stages are neglected by Rogowski, while during ramp-up stages could be detected. Figure 5.6 illustrates flow direction of I_C at each stage. Moreover, each stage is depicted in detail as follows.

- Stage 1: t_1

HS-IGBT and DUT are both on, which results to $I_{C(DC+)} = I_{C(rep)}$. $I_{C(DC+)}$ is ramped-up from zero. $V_{CE(on-load)}$ is I_C dependent and thus ramped-up with I_C . Moreover, current slope is determined by R_{par} and on-state voltage drop of PIGBT, HS-IGBT and DUT. As an example, Equation 5.3 describes slope of current until

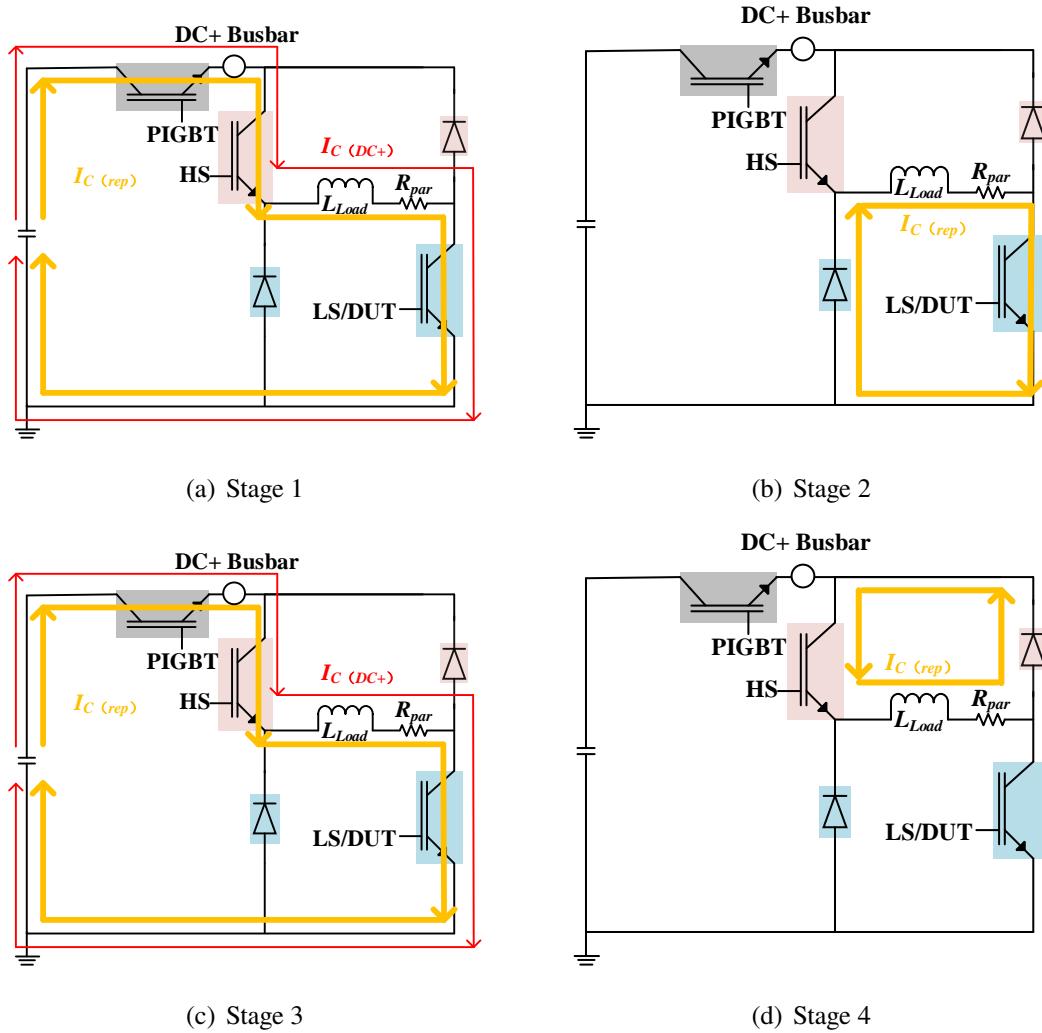


Figure 5.6: Various stages of performed current flow direction by repetitive pulse pattern within one period

time point t_1 :

$$V_{DC-link} - V_{CE(on)}PIGBT - V_{CE(on)}HS - V_{CE(on)}LS/DUT - i_C \cdot R_{par} = L_{load} \cdot \frac{di_C}{dt} \quad (5.3)$$

- Stage 2: t_2

HS-IGBT is off and DUT is on, thereby $I_{C(DC+)}$ is unable to be detected by Rogowski and $I_{C(rep)}$ is free-wheeling in LS/DUT, coil and LS-FWD. Therefore, $I_{C(rep)}$ decreases slowly and $V_{CE(on)}$ drops.

- Stage 3: t_3

HS-IGBT and DUT are on, $I_{C(DC+)} = I_{C(rep)}$. $I_{C(DC+)}$ ramped-up again as mentioned in Equation 5.3.

- Stage 4: t_4 HS-IGBT is on and DUT is off, $I_{C(DC+)}$ is unable to be detected and $I_{C(rep)}$ is free-wheeling in HS-IGBT, coil and HS-FWD. Hence, I_C is decreased. Since no current flows through DUT, $V_{CE(on-load)}$ drops to zero. Especially, Stage 4 is specified by half of switching period in order to implement a 50% duty cycle of DUT.

5.3 Current Development

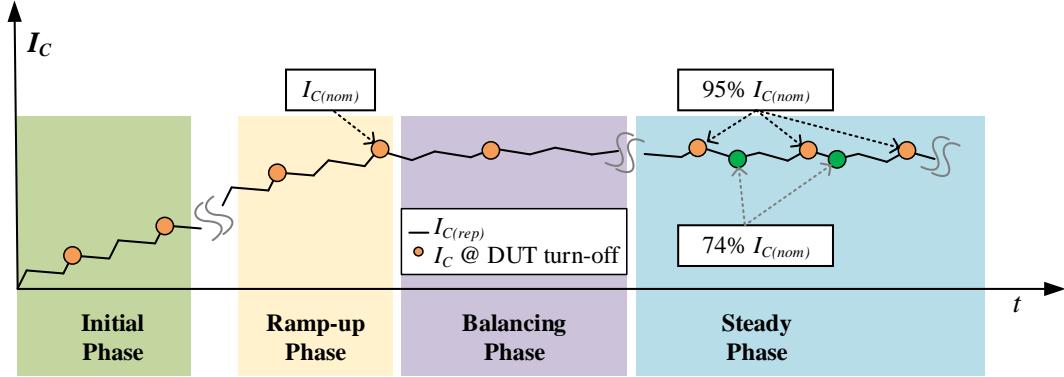


Figure 5.7: Schematic illustration of load current development during repetitive switching operations

A schematic illustration for the development of load current during repetitive operation is shown in Figure 5.7. Note that current and time are not scaled. Switching-off waveforms of DUT between stage 3 and 4 in Figure 5.5 are recorded by oscilloscope. Black lines represent $I_{C(rep)}$. Orange dots account for the current right before DUT turn-off (i.e., time point t_3 in Table 5.1), while green dots correspond to current levels, when the DUT turns-on (i.e., time point t_1 in Table 5.1). Based on current level, four phases are specified in Figure 5.7.

- Initial phase, where I_C starts rising from zero.
- Ramp-up phase, where I_C ramps-up to desired current level (i.e., nominal current in this work).
- Balancing phase

Owing to high load current, the generated power losses lead to temperature rising. Furthermore, increased temperature caused higher $V_{CE(on)}$ of PIGBT, HS-IGBT and LS/DUT. As described in Equation 5.3, current can be decreased from nominal current because both on- and off-time of DUT are fixed by pulse pattern.

- Steady phase

According to pre-measurements, the rising slopes of current from stage 1 and 2 were equal to decreasing slopes of current from stage 2 and 4 after about 100 pulses. After that, current could be turned off at 95% of nominal current at each period. However, it has to be remarked that the mean value of $I_{C(rep)}$ is only around 82% of nominal current. In other words, the equivalent I_C , which flows through DUT during on-time, is lower than the desired current level.

5.4 Determination of Temperature

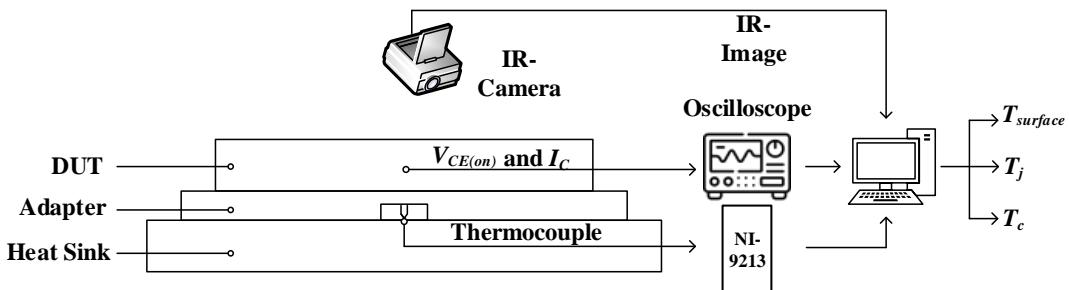


Figure 5.8: Schematic illustration of setup for temperature determination during repetitive operation

Case, junction and surface temperature were observed during repetitive operations. Setup was shown in Figure 5.8. Determination of each temperature is introduced in following sections.

5.4.1 Case Temperature T_c

A K-type thermocouple was placed directly below Cu-plate to measure thermo-voltage every one second, see Figure 5.8. Furthermore, a NI-9213 driver was utilized to convert analog voltage signal into digital signal, so that case temperature could be obtained by LabVIEW program.

5.4.2 Junction Temperature T_j

Sequence Mode for Waveform Record

A LeCroy HRO 64Zi oscilloscope [Tel17] was utilized to measure V_{GE} , $V_{CE(off)}$, I_C and $V_{CE(on)}$ during repetitive operations. Especially, a so-called sequence mode was performed for the waveforms. In sequence mode, the completed waveform consists

of fixed-size segments. Those segments, corresponding to recorded oscilloscope waveforms, are further called slices, in order to have a clearly different notation to the segments at the emitter surface of the DUT.

Table 5.2 displays the settings for repetitive operations with specified switching frequency overall 20 minutes. The principle of sequence mode and slices determination are shown in Appendix, see A.2.2.

Table 5.2: Sequence mode settings for repetitive operations overall 20 minutes

Switching frequency [Hz]	Interval between two slices [s]	Number of slices during repetitive operation
500	2	600
1000	1	1200

T_j Determination

Figure 5.9 depicts 3 slices of measured waveforms during repetitive switching operating with 500 Hz frequency under the ageing state with 1 bond-wire cut.

According to Table 5.2, slice 1, 100 and 600 accounted for operating time at 0.002 s, 2 s and 20 min, respectively. In view of each slice, signals were triggered by $V_{CE(off)} = 200$ V at time point $t = 0$ μ s and recorded with overall 1 μ s length. $V_{CE(on)}$ curves within time interval -0.6 μ s to -0.4 μ s are zoomed with grey background.

It can be seen from Figure 5.9 that with increasing slices, current drops from nominal current to a steady value (i.e., 94.5% of nominal current) and $V_{CE(on)}$ is increased. $I_{C(rep)} - V_{CE(on-rep)}$ value pair of each slice is marked with a white dot at a uniform time point $t = -0.5$ μ s. Thus, $\vec{I}_{C(rep)}$ and $\vec{V}_{CE(on-rep)}$ vectors can be obtained within repetitive operation of overall 20 minutes.

In the end, T_j can be determined by substituting $\vec{I}_{C(rep)}$ and $\vec{V}_{CE(on-rep)}$ into calibration matrix, see Figure 5.11.

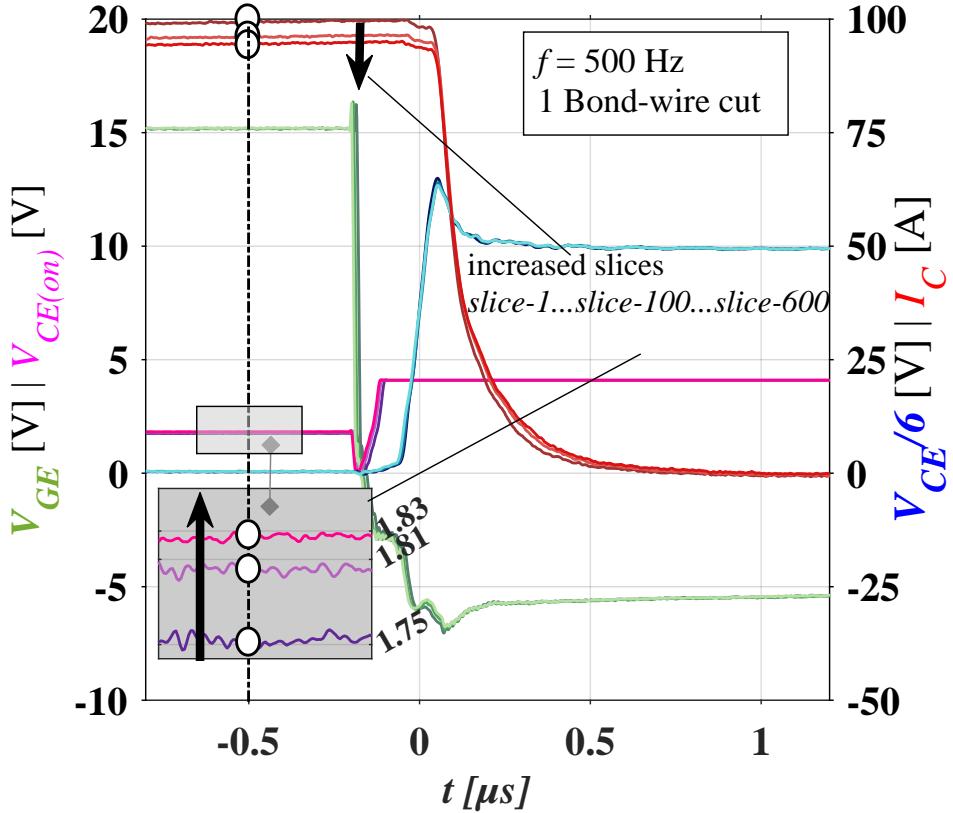


Figure 5.9: Three selected slices within one repetitive operation overall 20 minutes

5.4.3 Surface and Segment Temperature

A FLIR 300 series IR-camera was placed over DUT in order to record surface temperature $T_{surface}$ every 2 seconds, see Figure 5.8. Figure 5.10 depicts the determination of surface and segment temperatures.

It has to be remarked in Figure 5.10 that:

- Owing to the lack of synchronization with pulse pattern, IR-camera was not able to feature the surface temperature precisely at the moment, when repetitive switching operations were recorded.
- $T_{surface}$ and T_j can only be compared to a certain extend.
- The evaluation of $T_{surface}$ and T_j should be traded individually, not among each other.

Surface Temperature $T_{surface}$

Figure 5.10(a) displays the emitter segmentation of DUT and the chronology of bond-wire cuts. DUT is divided into 8 segments and each segment is numbered.

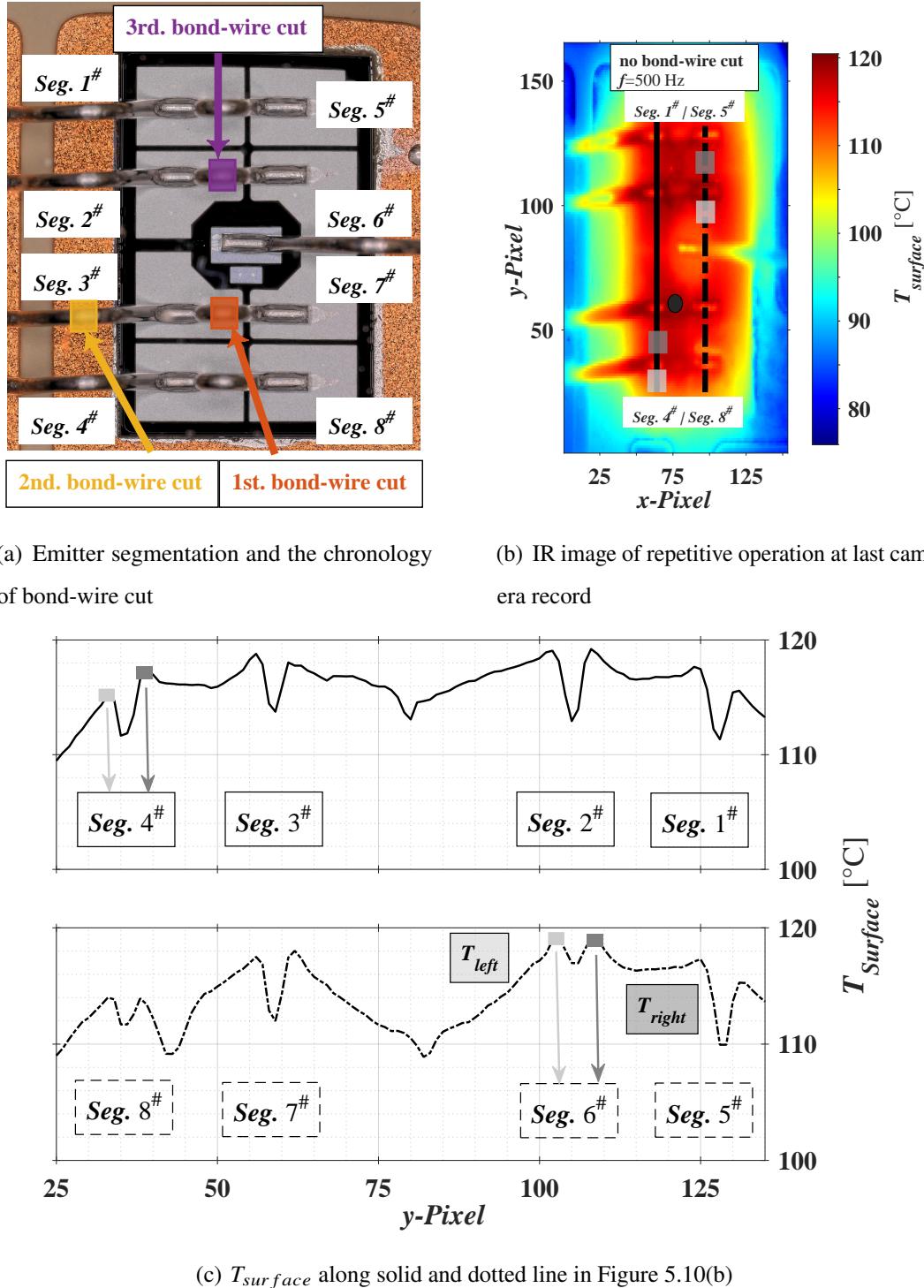
Figure 5.10: Determination of $T_{surface}$ and $T_{segment}$

Figure 5.10(b) shows an IR image of DUT surface temperature distribution with 500 Hz switching frequency at initial state without bond-wire cut, which was recorded by last frame of IR-camera. The highest temperature was marked with the black dot.

Furthermore, along the direction of y-pixels, two black lines are pointed from bottom to top, which are placed in the middle of segments. Solid line crosses 4 segments, starting from segment 4 to 1, while dotted line points from segment 8 to 5. Moreover, two grey rectangle boxes are marked on each bond-wire side within segment 4 and 6, respectively. According to this, segment temperature can be derived.

Segment Temperature $T_{segment}$

$T_{surface}$ along solid and dotted line are shown in Figure 5.10(c). The large dent in the centre of the chip indicates the gate contact region with no active metallization underneath. The smaller dents in the profile are due to the shading effect of the bond-wires, which have a lower temperature than the chip surface. [SS09]

Thus, it can be inferred that from left to right, small dents indicate segment 8 to 5 along dotted line. Light and dark grey boxes are named as T_{left} and T_{right} , respectively. $T_{segment}$ was determined according to Equation 5.4:

$$T_{segment} = \frac{T_{left} + T_{right}}{2} \quad (5.4)$$

5.5 Description of Ageing State

After repetitive operation at initial state without bond-wire cut, according to the result of IR image, bond-wire over the hottest segment was cut. Then, a new calibration was performed with one bond-wire cut. This process was repeated until DUT reached End of Usability (EoU) state. In this work, EoU relates to 3 bond-wires cut.

It can be seen that each ageing state of DUT corresponds to a new State of Life (SoL). To simplify the description of ageing process, several variables of SoL with respect to the number of bond-wire cut are shown in Table 5.3. In addition, the increasing of $V_{CE(on)}$ for each SoL is included.

Table 5.3: Description of DUT ageing state for each repetitive operation

Variable	Number of bond-wire cut	$V_{CE(on)}$ at $I_C = 100 \text{ A}$	Increasing of $V_{CE(on)} [\%]$
$SoL - 0$	0	1.6017	0
$SoL - 1$	1	1.6268	1.6
$SoL - 2$	2	1.6761	4.6
$SoL - 3$	3	1.7412	8.7

5.6 Summary of Repetitive Investigation

Figure 5.11 summarizes all the steps for repetitive investigations by means of $V_{CE(on-load)}$ as TSEP. To illustrate these steps, an example is used with 500 Hz.

- Calibration
 - Due to the limitation of static pulse pattern, $I_{C(rep)}$ decreases during repetitive operation. Hence, $V_{CE(on-load)}$ is calibrated by a $\vec{I}_{C(calib)}$ vector with 101 values of scaled $I_{C(calib)}$.
 - Calibration matrix of sensitivity and offset are derived with each scaled $I_{C(calib)}$.
- Repetitive Operation
 - Vector of $V_{CE(onrep)}$ and $I_{C(rep)}$ are determined in each slice by a uniform time point at conductive state, where indicates the maximal chip temperature before turn-off.
 - Substituting $\vec{V}_{CE(rep)}$ and $\vec{I}_{C(rep)}$ into calibration matrix, $T_{j(rep)}$ of each slice is obtained.
- Bond-wire Cut
 - Bond-wire is cut after each repetitive operation according to the hottest surface temperature.
 - Recalibration for the new SoL and repetitive operation are further performed.
 - Investigation stops when DUT reaches to EoU state.

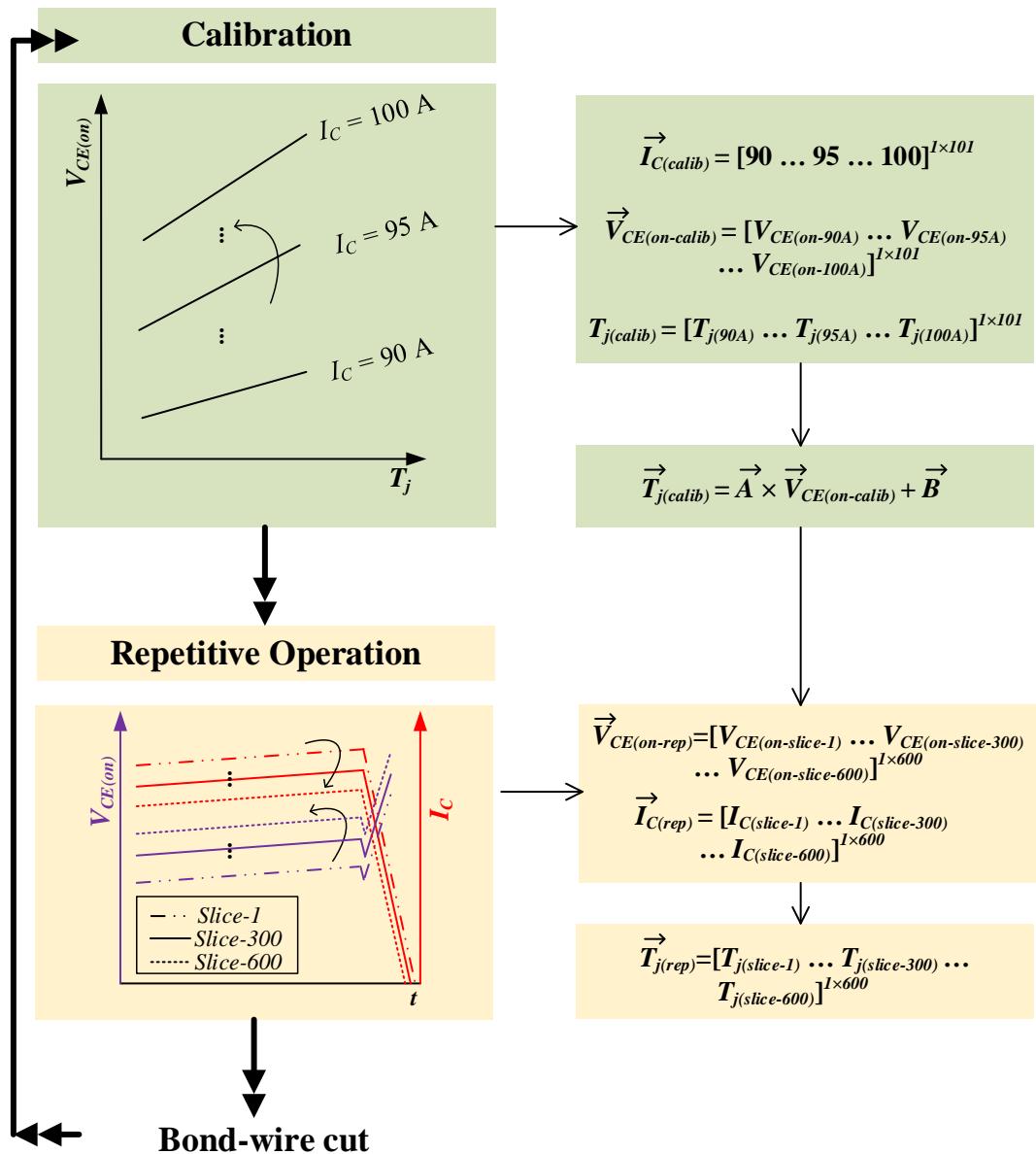


Figure 5.11: Summary of implementation for repetitive switching investigation with 500 Hz

6 Results

In this chapter, temperatures during repetitive operation are evaluated. First of all, the developments of current and conductive power loss P_{cond} are displayed to show that temperature of each ageing state is comparable. After that, case, junction and surface temperatures under each SoL with 500 Hz frequency are illustrated. In addition, temperatures at 500 Hz are compared with 1000 Hz. The impact of ageing state and frequency on temperature and its distribution is determined.

6.1 I_C and P_{cond}

6.1.1 Development of I_C

The development of I_C during all repetitive switching operations with 500 Hz under each SoL are shown in Figure 6.1. Since pulse pattern cannot be changed during operation, a pre-measurement under each aged state overall 5 minutes was performed in order to adapt the current to initial state without bond-wire cut as close as possible. Values of pulse pattern for repetitive switching operations under each SoL is shown in Appendix, see Table A.4.

I_C under each SoL with 500 Hz are shown in Figure 6.1. It can be seen that:

- Under a fixed SoL, I_C dropped from nearly nominal current to steady state with 94.5 A after 15 minutes operation.
- the maximal current fluctuation ΔI at steady state is 0.5 A.

6.1.2 P_{cond}

According to [LSSDD18], P_{cond} is determined by Equation 6.1:

$$P_{cond} = V_{CE(on)} \cdot I_C \quad (6.1)$$

Development of P_{cond}

It can be seen in Figure 6.2 that:

- P_{cond} increases with ageing due to the nearly constant I_C but increased $V_{CE(on)}$.

- For a fixed SoL, P_{cond} decreases marginally at beginning and stays nearly constant after 5 minutes.

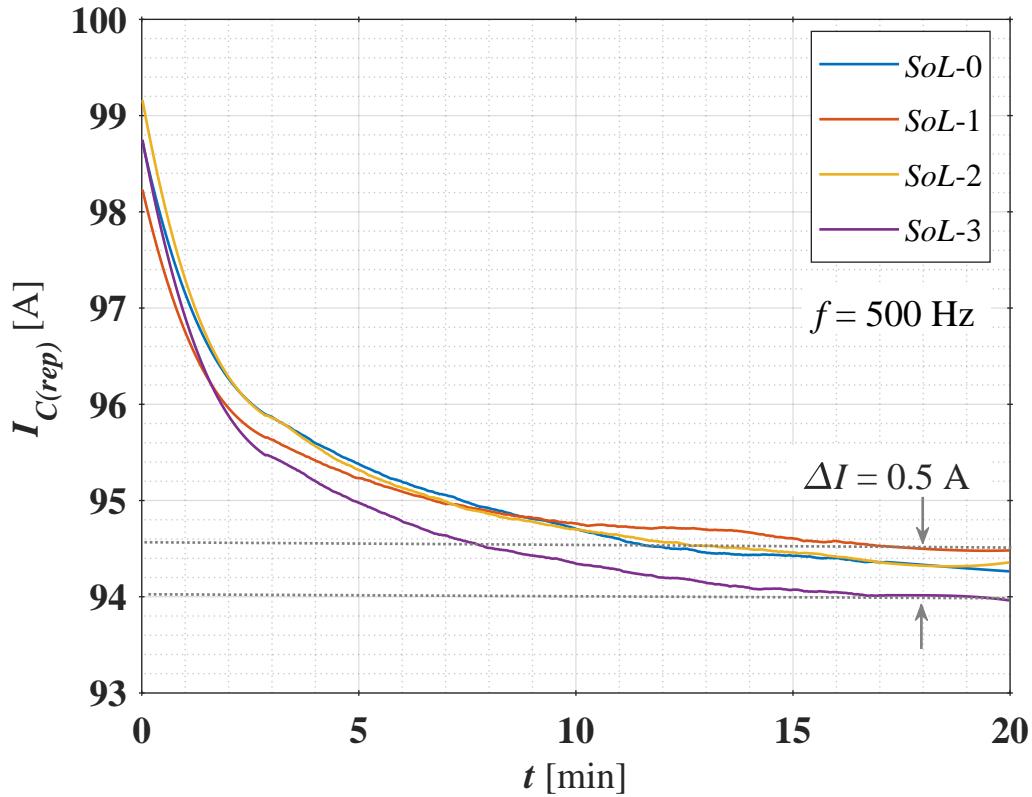


Figure 6.1: Development of I_C during repetitive operations under various SoL

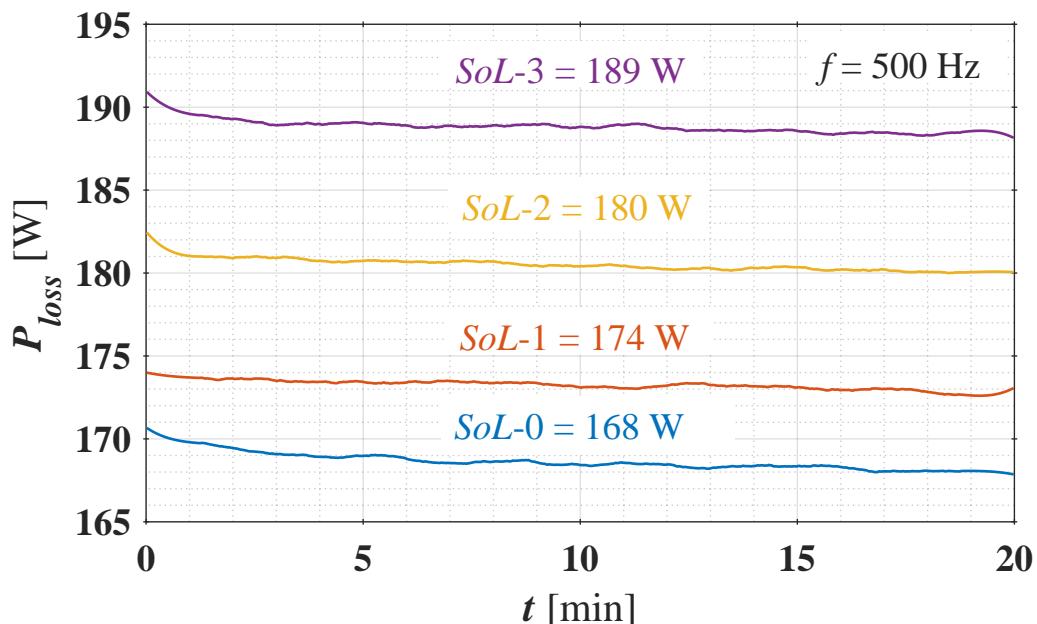


Figure 6.2: Development of P_{cond} under each SoL

Comparison 1000 Hz with 500 Hz

Steady value of P_{cond} under each SoL with 500 Hz is compared to 1000 Hz and shown in Figure 6.3.

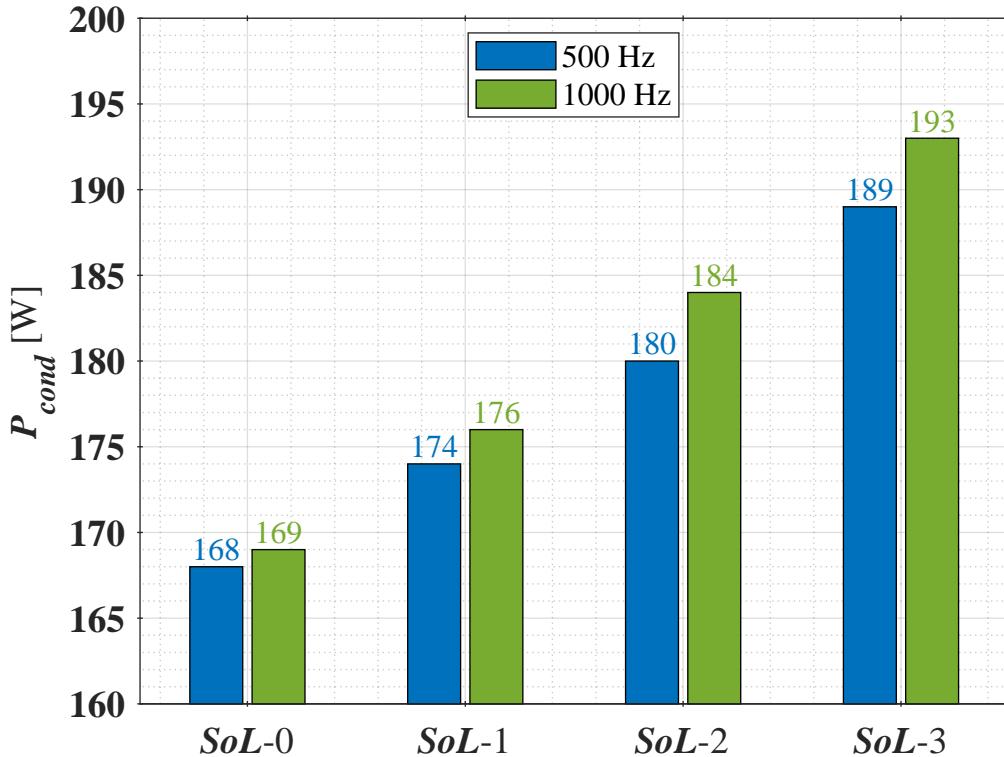


Figure 6.3: Comparison of P_{cond} at steady state under each SoL with 500 Hz and 1000 Hz

It can be seen that:

- P_{cond} with 1000 Hz increases with ageing from 169 W to 193 W.
- Under each SoL, P_{cond} with 1000 Hz is higher than with 500 Hz due to:
 - the doubled frequency, which increases the temperature of device and further results to a higher $V_{CE(on)}$;
 - the 0.5 A higher value of $I_{C(rep)}$ at steady state (i.e., 95 A) with 1000 Hz.

6.2 T_C

Developments of T_c under each SoL is depicted in Figure 6.4.

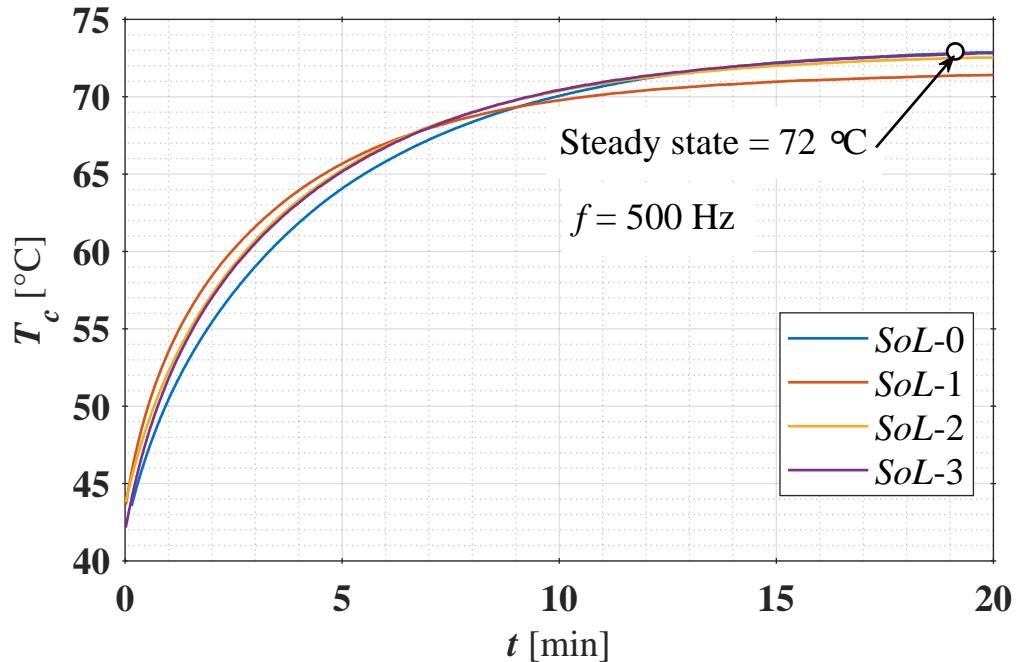


Figure 6.4: Developments of T_c under each SoL

T_c at steady state with 500 Hz and 1000 Hz are compared and shown in Figure 6.5.

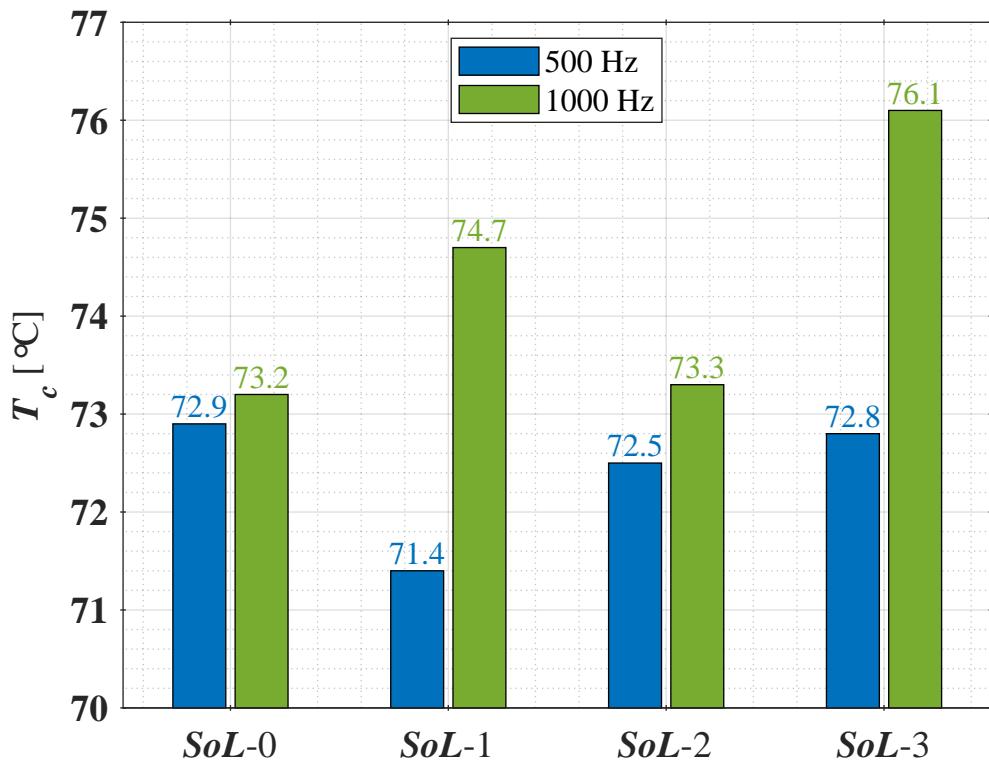


Figure 6.5: Comparison of T_c at steady state under each SoL with 500 Hz and 1000 Hz

6.2.1 Development of T_C

It can be seen in Figure 6.4 that:

- Under a fixed SoL, T_c increases with time from nearly 40 °C and reaches to steady value around 72 °C after 15 minutes operation.
- The steady value of T_c varies from 71.4 °C to 72.9 °C, but not increasing with ageing all the time.
- Various temperature gradient for various SoL:
 - flattest under $SoL = 0$;
 - steepest under $SoL = 1$;
 - no significant change under $SoL = 2$ and $SoL = 3$.

6.2.2 Comparison 1000 Hz with 500 Hz

It can be concluded in Figure 6.5 that compared with 500 Hz:

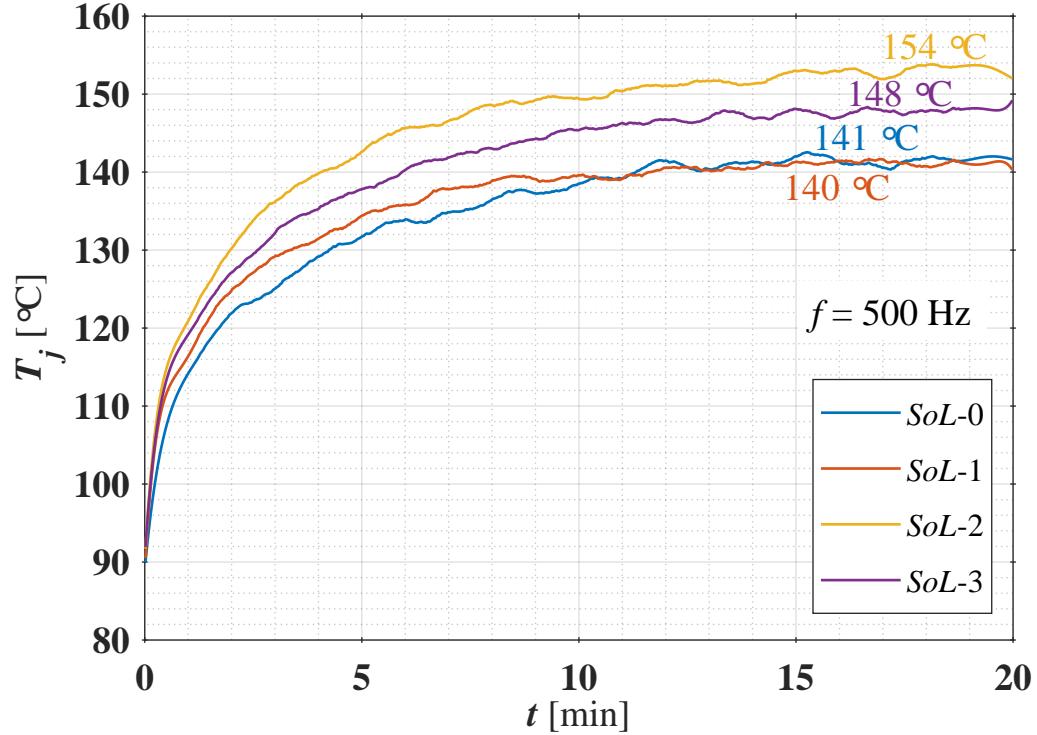
- Steady value of T_c with 1000 Hz is higher under a fixed SoL owing to more P_{cond} .
- T_c at steady state with 1000 Hz varies from 73.2 °C to 76.1 °C.
- Steady values of T_c with 1000 Hz do not show a replicable behaviour of increasing with ageing.

6.2.3 Explanation for Unexpected Results

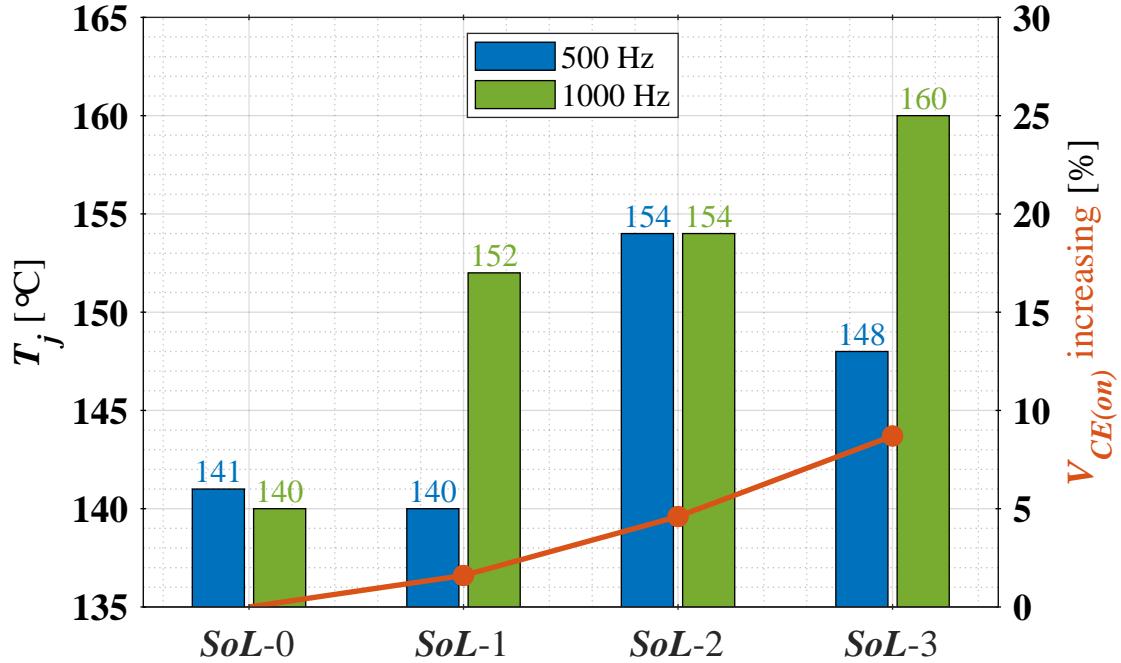
A thermocouple is placed under the power module within a adapter plate, close to HS-IGBT, see Figure 5.2. As a consequence of the spatial distance between thermocouple and DUT, measured T_c cannot characterize the case temperature of DUT precisely.

6.3 T_j

Developments of T_j under each SoL is depicted in Figure 6.6.

Figure 6.6: Development of T_j under each SoL

T_j at steady state with 500 Hz and 1000 Hz are compared. Moreover, the increasing of $V_{CE(on)}$ under each SoL is included and shown in Figure 6.7.

Figure 6.7: Comparison of T_j under each SoL with 500 Hz and 1000 Hz

6.3.1 Development of T_j

It has shown in Figure 6.6 that:

- T_j starts rising from nearly 90 °C and reaches to steady state after about 15 minutes.
- Steady value of T_j varies from 140 °C to 154 °C.
- Various behaviours of T_j under each SoL:
 - Compared with initial state, T_j decreases marginally under $SoL - 1$;
 - T_j increases significantly under $SoL - 2$;
 - T_j decreases obviously under $SoL - 3$.
- Temperature gradient before 15 minutes shows the same trend as T_j at steady state.

6.3.2 Comparison 1000 Hz with 500 Hz

It can be concluded in Figure 6.7 that compare with 500 Hz:

- Steady value of T_j varies from 140 °C to 160 °C.
- Value of T_j at steady state increases with ageing, large increasing exists from $SoL - 0$ to $SoL - 1$ and $SoL - 2$ to $SoL - 3$;
- DUT reaches to End of Life (EoL) state under $SoL - 2$. However, T_j increase marginally from $SoL - 1$ to EoL.

6.3.3 Note for Unexpected Results

Since $V_{CE(on-load)}$ increases with ageing, more power loss is generated and hence the rising of T_j is expected. However, it has to be remarked that T_j under EoU state (i.e., $SoL - 3$) is lower than under EoL state (i.e., $SoL - 2$) with 500 Hz. In this work, only one chip was tested. Thus, the results has no comparison with other chip under the same test condition. Moreover, the IR-camera has no synchronisation with pulse pattern. Therefore, T_j cannot be compared directly with $T_{segment}$. Furthermore, the possible explanation for unexpected results cannot be given.

6.4 $T_{surface}$ and $T_{segment}$

Distribution of $T_{surface}$ and according to Figure 5.10(c) and Equation 5.4 determined $T_{segment}$ under each SoL are shown respective in Figure 6.8, 6.9, 6.10 and 6.11. In each Figure, 8 segments are divided by white boxes, which are associated with Figure 5.10(a). White 'x' shows no more bond-wire contact over the according segment.

Black dot depicts the hottest point on emitter surface.

6.4.1 $SoL - 0$

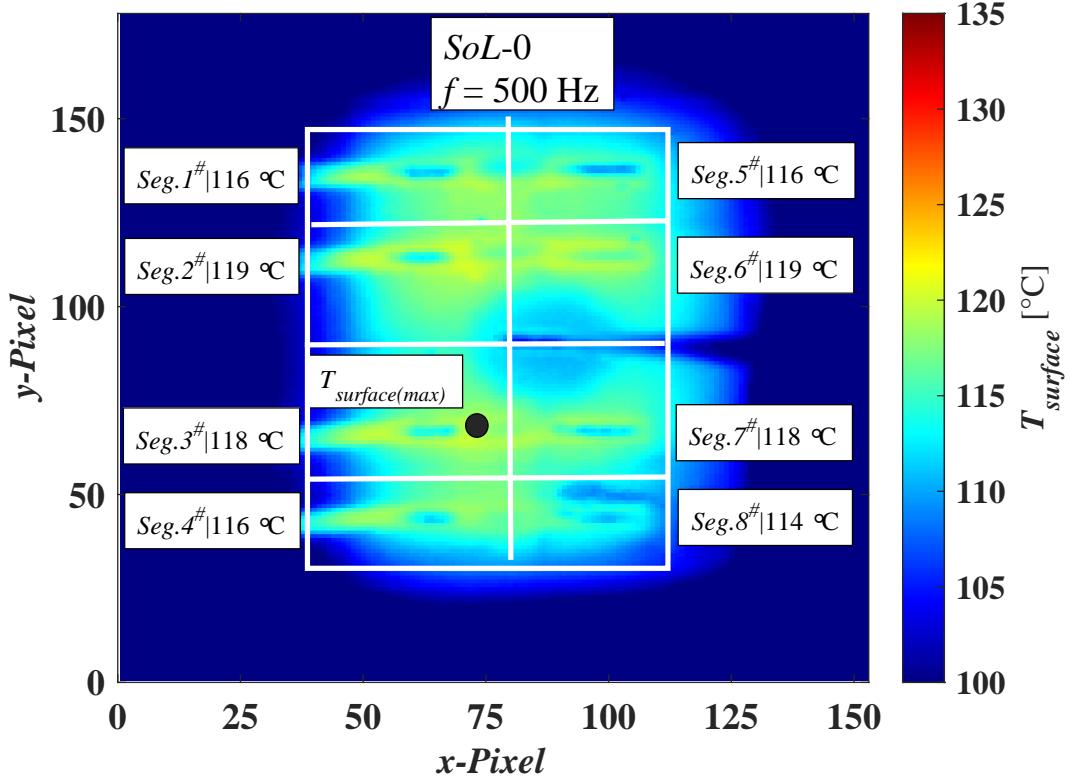


Figure 6.8: $T_{surface}$ and $T_{segment}$ under $SoL - 0$

It can be seen in Figure 6.8 that under $SoL - 0$ without bond-wire cut:

- $T_{segment}$ varies from $114\text{ }^{\circ}\text{C}$ to $119\text{ }^{\circ}\text{C}$.
- The maximal asymmetric difference of segment temperature is 5 K.
- Segment 1, 4 and 5, which are located at the edge of the chip, have the same temperature with $116\text{ }^{\circ}\text{C}$.
- Segment 8 has the lowest temperature due to the long distance of ideal geometric load current path, see Figure 4.2.

6.4.2 SoL – 1

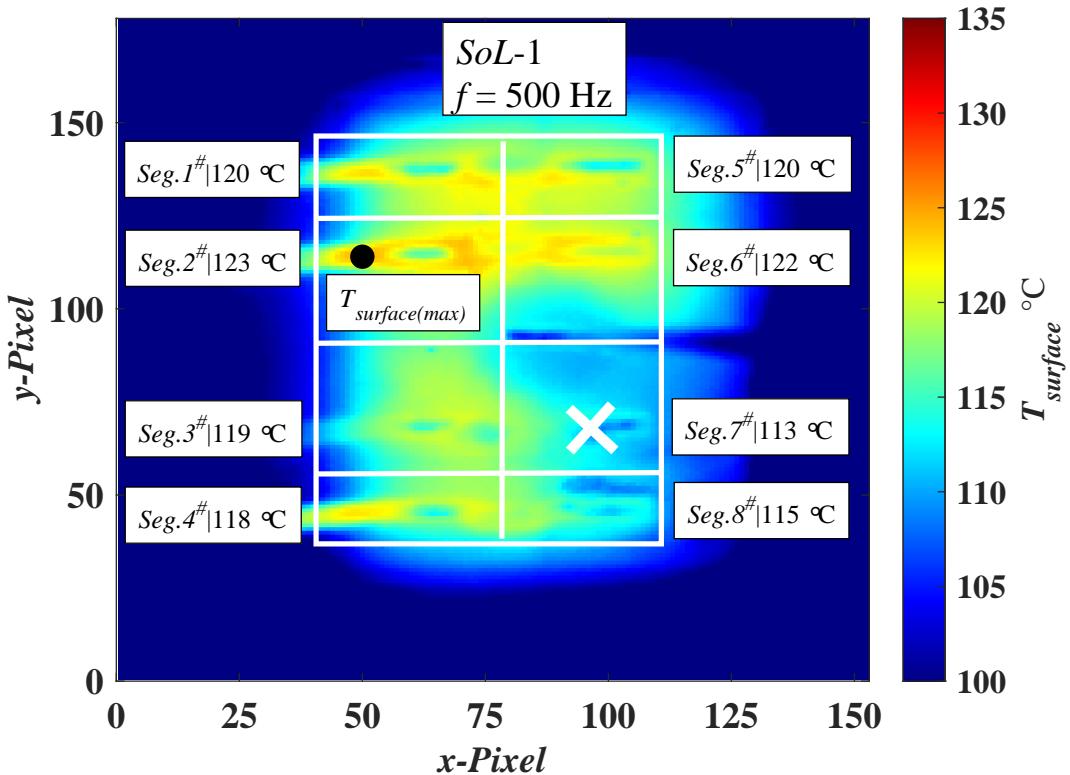


Figure 6.9: $T_{surface}$ and $T_{segment}$ under $SoL - 0$

It has shown in Figure 6.9 that under $SoL - 1$ with 1 bond-wire cut:

- $T_{segment}$ varies from 113°C to 123°C .
- The maximal asymmetric difference of segment temperature is 10 K .
- Segment 7 has the lowest temperature after bond-wire cut, because gate current has to flow through more resistance, in order to go back to emitter, see Figure 2.9. This results to the reduction of V_{GE} in segment 7. As a consequence, less load current flows and power loss is decreased.

6.4.3 SoL - 2

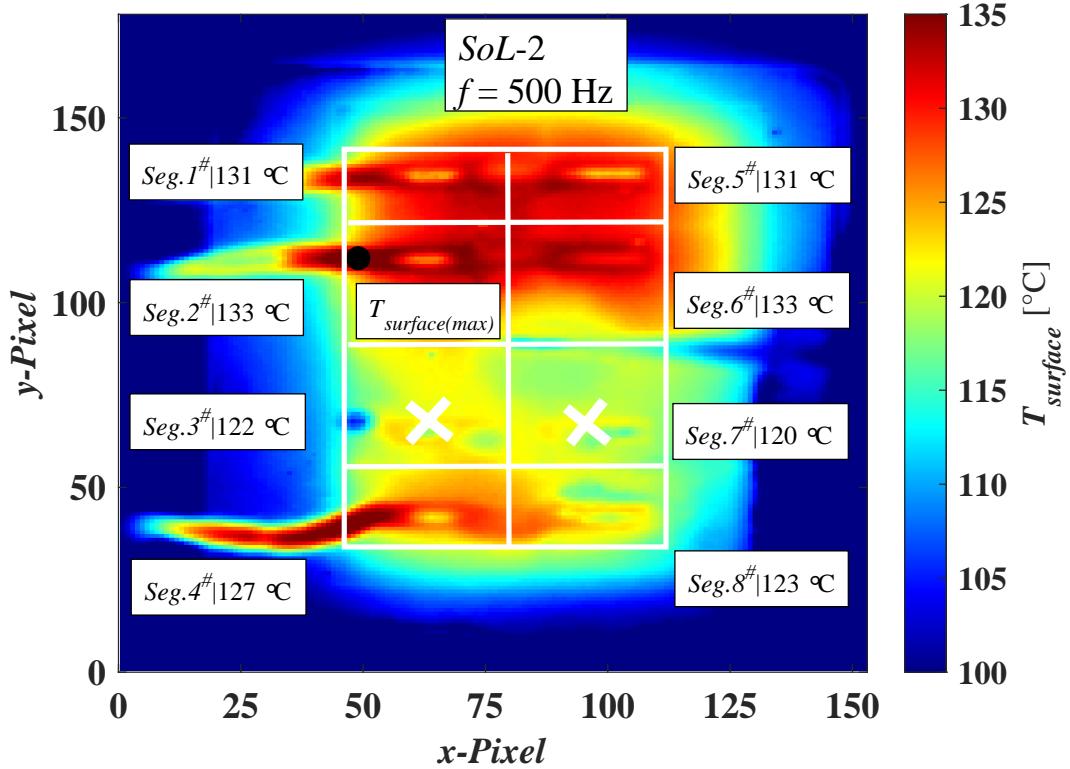


Figure 6.10: $T_{surface}$ and $T_{segment}$ under $SoL - 0$

It can be inferred in Figure 6.10 that under $SoL - 2$ with 2 bond-wires cut:

- $T_{segment}$ varies from $120\text{ }^{\circ}\text{C}$ to $133\text{ }^{\circ}\text{C}$.
- The maximal asymmetric difference of segment temperature is 13 K.
- Since segment 3 and 7 have no more bond-wire contact, they have the low temperature with $122\text{ }^{\circ}\text{C}$ and $120\text{ }^{\circ}\text{C}$, respectively.

6.4.4 $SoL - 3$

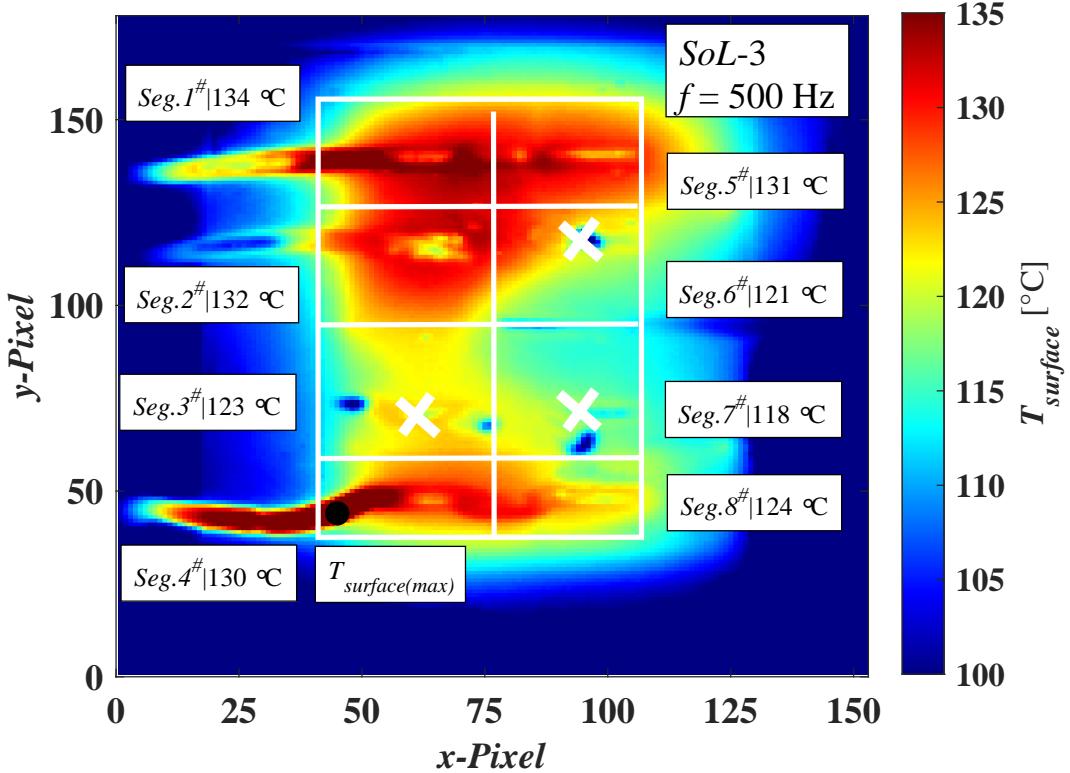


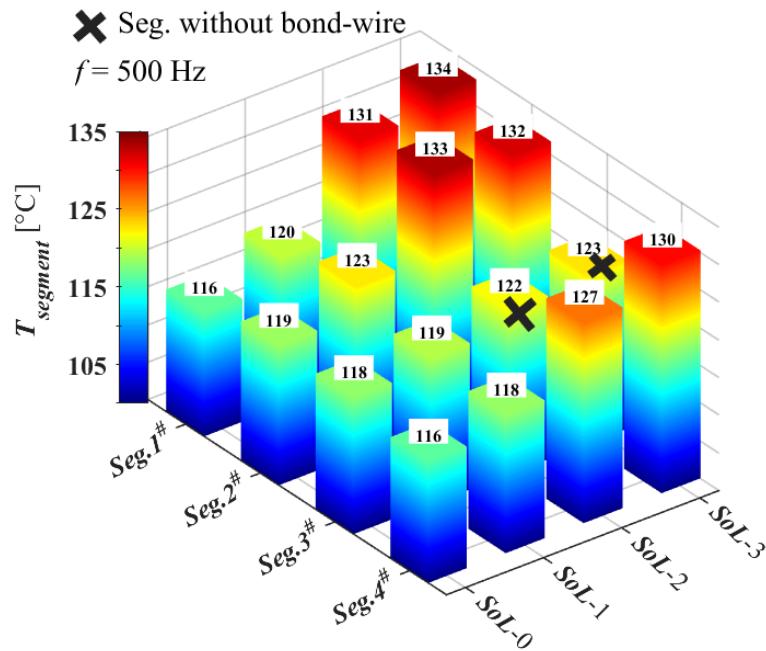
Figure 6.11: $T_{surface}$ and $T_{segment}$ under $SoL - 0$

It can be inferred in Figure 6.11 that under $SoL - 3$ with 3 bond-wires cut:

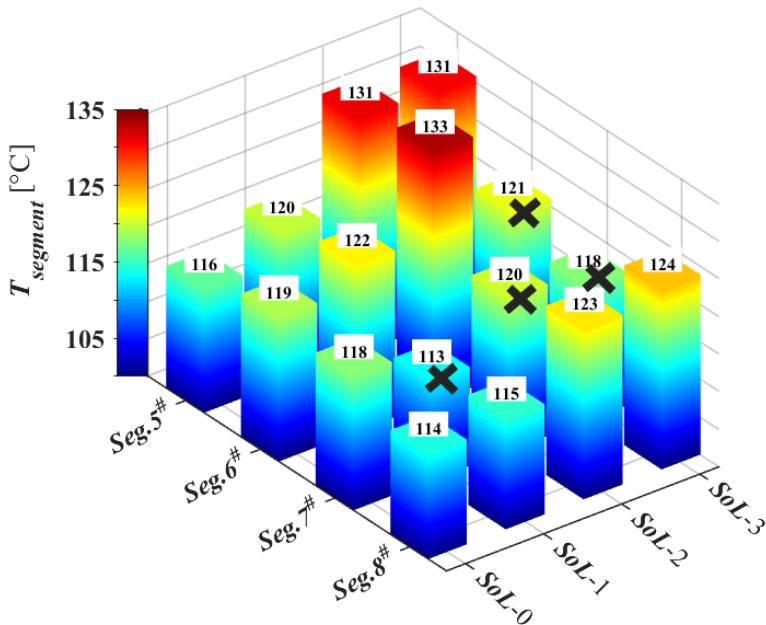
- $T_{segment}$ varies from 118 °C to 134 °C.
- The maximal asymmetric difference of segment temperature is 16 K.
- Since segment 3, 6 and 7 have no more bond-wire contact, they have the low temperature and vary from 118 °C and 123 °C, respectively.

6.4.5 Comparison of $T_{segment}$ under each SoL

Figure 6.12 depicts each $T_{segment}$ under each SoL with 500 Hz. Moreover, the maximum, minimum and mean value of $T_{segment}$ under each SoL are compared with 1000 Hz and 500 Hz and shown in Figure 6.13.



(a) Segment 1-4



(b) Segment 5-8

Figure 6.12: Overview of $T_{segment}$ under each SoL

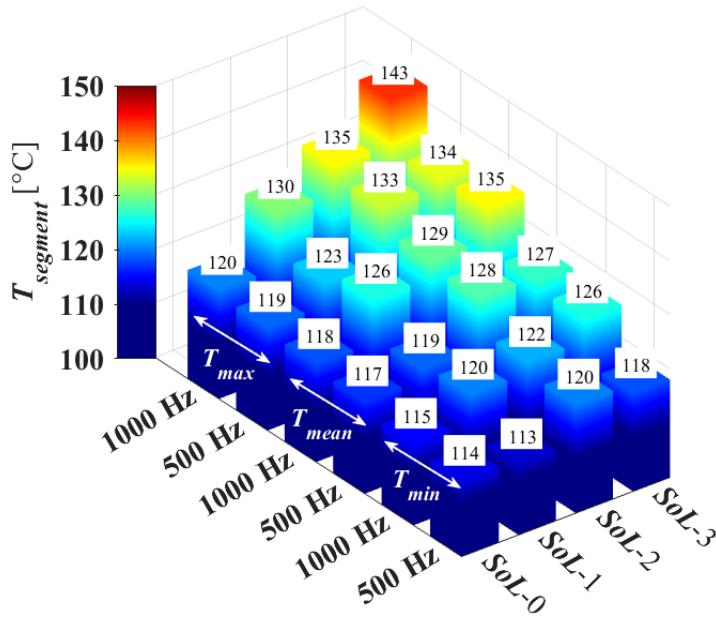


Figure 6.13: Comparison of characterized value for $T_{segment}$ with 500 Hz and 1000 Hz

Overview of $T_{segment}$ under each SoL with 500 Hz

It can be concluded in Figure 6.12 that:

- $T_{segment}$ with bond-wire contact are increasing with ageing all the time.
- $T_{segment}$ without bond-wire contact are substantially lower than segments with intact contact under each SoL.
- Temperature of segment 3 increases with ageing despite its bond-wire is cut under $SoL - 3$.
- Temperature of segment 7 is the lowest under each SoL since its bond-wire is cut.
- The highest temperature of segment varies from SoL:
 - until EoL (i.e., $SoL - 2$): segment 2 and 6;
 - after EoL (i.e., $SoL - 3$): segment 1.
- Temperature of segment 6 decreases steeply after EoL.
- Asymmetric distribution of segment temperature exists at all times, maximum of temperature difference increases significantly with ageing.

Comparison of characterized value for $T_{segment}$ with 500 Hz and 1000 Hz

It can be inferred in Figure 6.13 that:

- All characterized $T_{segment}$ with 1000 Hz are higher than with 500 Hz under each SoL.
- Mean value of $T_{segment}$ shows various variation with frequency:
 - with 1000 Hz: increases all the time with ageing;
 - with 500 Hz: increases until EoL and decreases under EoU.
- Steady value of T_j shows the same variation trend as mean value of $T_{segment}$.

7 Summary and Outlook

7.1 Summary

The main aim of this work was to investigate the temperature distribution of an IGBT chip during repetitive operation under consideration of ageing with respect to bond-wire on the front-side.

First of all, basic theories with respect to switching-off behaviour, package of power module and degradation on front-side were introduced. After that, several methods for temperature determination of power semiconductors were illustrated. TSEP for junction temperature determination was especially investigated.

To perform repetitive switching events, an inverter circuit with single phase was built. Two subsystems of an IGBT module were utilized as HS and LS/DUT, respectively. IGBT was switched off at nominal current with two different switching frequencies and a fixed duty cycle of 50%. Repetitive operation lasted overall 20 minutes for each ageing state so that all investigated temperatures could reach to the steady state. The switching principle of pulse pattern for the specified repetitive switching operation was depicted. Several limitations for this performance were shown. Unlike power cycling test, bond-wires were artificially cut to obtain different state of life with respect to front-side ageing of IGBT chip.

To estimate the temperature distribution of chip during repetitive switching operation, three temperatures were observed, namely case temperature measured by thermocouple, surface temperature determined by infrared camera and junction temperature determined by TSEP. Typically, several alternative TSEPs were explained, performed and compared. After that, IGBT on-state voltage under load current was utilized as TSEP for this work. Its calibration principle and the method of junction temperature determination were described. In particular, the potential impact factors and accuracy of calibration were discussed.

Finally, the developments of case, surface and junction temperatures were displayed with various states of life and two specified switching frequencies, respectively. Results were depicted and analyzed. An outlook on future research was given.

It can be concluded according to results that:

- No obvious variation could be extracted from case temperature owing to the measurement performance.
- Junction and segment temperatures were significantly affected by each state of life and frequency.
- Mean value of segment temperature shown the same variation trend as junction temperature at each state of life.
- Inhomogeneity of segment temperature was increasing with ageing.

7.2 Outlook

This work has shown a feasible and application-oriented method for the temperature determination under the repetitive switching operation. The following section shows which further investigations and optimization options are available.

7.2.1 DUT

In this work, a subsystem of IGBT module was utilized as DUT. Its Kelvin contact included bond-wire and equivalent resistance of collector and emitter terminals. These additional resistances resulted to a higher on-state voltage and further to the overrated junction temperature.

To eliminate the impact on bond-wire on on-state voltage measurement, DCB chips is necessary in further investigations.

Current was measured at busbar owing to the module package. With DCB chips, current can be measured directly under DUT.

7.2.2 IR-Camera

In this work, IR-camera was not synchronized with pulse pattern during repetitive operations. Thus, surface temperatures determined by IR-camera could not characterize whether DUT was at conductive, blocking or switching phase.

For further investigations, IR-camera should be associated with pulse pattern so that surface temperatures could be recorded right at the uniform time point, where selected for junction temperature determination. Furthermore, by TSEP determined T_j and by IR-camera determined $T_{segment}$ can be compared directly.

7.2.3 Pulse-Pattern

In this work, pulse pattern was not changeable during repetitive operations. Therefore, current was decreased with time due to the temperature increasing, which further resulted to slightly different current development under each state of life.

For further investigations, pulse pattern should be adjustable during repetitive operations so that DUT could turn-off at nominal current all the time and the development of current under each state of life should be the same.

7.2.4 Current Measurement

This work has shown that Rogowski coil was not suitable for DC and AC measurement with slight slope and hence was placed at busbar plus.

For further investigations, Pearson probes could be suitable for DC (or AC with slight slope) measurement during conduction state and shunt for high slopes during switching.

7.2.5 $V_{CE(on-sense)}$ as TSEP

As mentioned in Section 3.5.2, on-state voltage under sense current shows very good linearity and can avoid self-heating issue. A possible setup is shown in Figure 7.1.

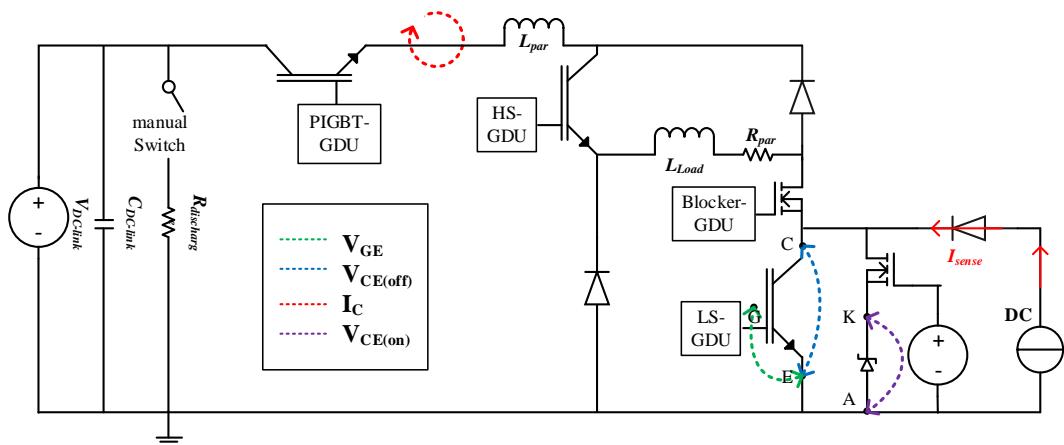


Figure 7.1: Schematic illustration of the performed circuit for $V_{CE(on-sense)}$ as TSEP

Compared with the setup of $V_{CE(on-load)}$ as TSEP, an additional MOSEFT as blocker is in series with DUT. A DC current source is parallel with DUT and generates a sense current I_{sense} .

Table 7.1 depicts the specified pulse pattern for temperature determination by means of $V_{CE(on-sense)}$ as TSEP. Every several pulses $t_{4.1} \sim t_{4.3}$ are applied instead of t_4 . $V_{CE(on-sense)}$ can be extracted during time interval $t_{4.2}$.

Table 7.1: Pulse pattern for repetitive operations by means of $V_{CE(on-sense)}$ as TSEP

Period	1/2f			1/2f			
	t_1	t_2	t_3	t_4	$t_{4.1}$	$t_{4.2}$	$t_{4.3}$
GDU	on	on	on	on	on	on	on
PIGBT	on	off	on	on	on	on	on
HS	on	off	on	on	on	on	on
LS/DUT	on	on	on	off	off	on	off
Blocker	on	on	on	on	on	off	on

A Appendix

A.1 Derivation of Equations

A.1.1 Carrier Density and Mobilities

Intrinsic carrier density n_i is shown in Equation A.1:

$$n_i^2 = N_C \cdot N_V \cdot e^{-E_g/kT} \quad (\text{A.1})$$

where N_C and N_V is density of states at the bottom of the conduction band and density of states at the top of the valence band, respectively. E_g is bandgap, k donates the Boltzmann constant and T is absolute temperature. Mobilities μ in Silicon is given by Equation A.2:

$$\mu = \mu_\infty + \frac{\mu_0 - \mu_\infty}{1 + \left(\frac{N}{N_{ref}}\right)^\gamma} \quad (\text{A.2})$$

where μ_0 and μ_∞ are limiting values for low and high concentrations, N_{ref} is the concentration at which the mobility adopts the mean value between limiting values, N donates the carrier concentration n or p . All these parameters are temperature depended. Table A.1 lists parameters for electrons and holes, respectively.

Table A.1: Temperature depended parameters for mobilities in Silicon [LSSDD18]

Parameter		μ_0	μ_∞	$N_{ref} \cdot 10^{16}$	γ
Unit		cm^2/Vs	cm^2/Vs	cm^{-3}	1
Carrier Type	Electrons	$1412 \cdot (300/T)^{2.28}$	$66 \cdot (300/T)^{0.9}$	$9.7 \cdot (T/300)^{3.51}$	$0.725 \cdot (300/T)^{0.27}$
	Holes	$469 \cdot (300/T)^{2.1}$	$44 \cdot (300/T)^{0.8}$	$24 \cdot (T/300)^{4.13}$	$0.7 \cdot (300/T)^{0.00}$

Figure A.1(a) depicts temperature dependency of n_i . Figure A.1(b) shows μ at two different doping densities, where represent n^- -region and p-base region of IGBT, respectively. It can be seen that n_i increases with temperature and on the contrary, μ decreases with temperature.

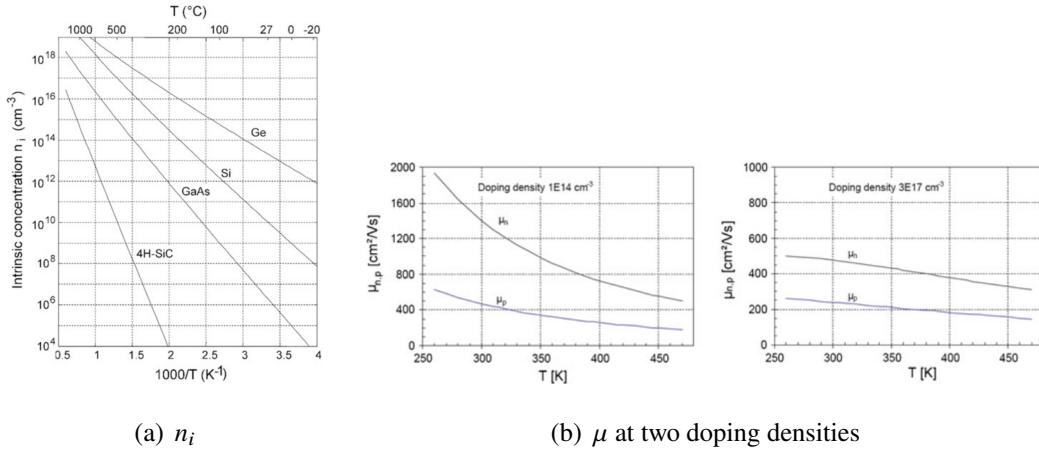


Figure A.1: Temperature dependency of carrier parameters in Silicon [LSSDD18, P.23, P.45]

A.1.2 Temperature Dependency of $V_{GE(th)}$

In general, threshold voltage V_T with respect to FET structure is given by the sum of initial flat-band voltage, voltages across the semiconductor ($\approx 2 \cdot \psi_B$) and the oxide layer. [SN07] It can be described by Equation A.3:

$$V_T = V_{FB} + 2 \cdot \psi_B + \frac{\sqrt{2 \cdot \epsilon_s \cdot q \cdot N_A \cdot (2 \cdot \psi_B)}}{C_{ox}} \quad (\text{A.3})$$

where V_{FB} is from non-zero shifted flat-band voltage due to the fixed oxide charges Q_f and the work-function difference ϕ_{ms} between the gate material and the semiconductor. Hence, V_{FB} is introduced by Equation A.4:

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} \quad (\text{A.4})$$

Since ϕ_{ms} and Q_f are essentially independent of temperature [SN07], differentiating Equation A.3 with respect to temperature yields:

$$\frac{dV_T}{dT} = \frac{d\psi_B}{dT} \cdot \left(2 + \frac{1}{C_{ox}} \cdot \sqrt{\frac{\epsilon_s \cdot q \cdot N_A}{\psi_B}} \right) \quad (\text{A.5})$$

where ψ_B is given by:

$$\psi_B = \frac{k \cdot T}{q} \cdot \ln \left(\frac{N_A}{n_i} \right) \quad (\text{A.6})$$

Furthermore, differentiating Equation A.6 with respect to temperature yields:

$$\frac{d\psi_B}{dT} \approx \frac{1}{T} \cdot \left(\psi_B - \frac{E_{g(0)}}{2q} \right) \quad (\text{A.7})$$

Substituting Equation A.7 to A.5 yields:

$$\frac{dV_{GE(th)}}{dT} \approx \frac{1}{T} \cdot \left(\psi_B - \frac{E_g(0)}{2q} \right) \cdot \left(2 + \frac{1}{C_{ox}} \cdot \sqrt{\frac{\epsilon_s \cdot q \cdot N_A}{\psi_B}} \right) \quad (\text{A.8})$$

A.2 Additional Informations with Respect to Repetitive Investigation

A.2.1 Calibration

Table A.2: Time duration for calibration respective 500 Hz and 1000 Hz in Table 4.1

Time [μs]	t_1	t_2	t_3		t_4		t_5	t_6
			500 Hz	1000 Hz	500 Hz	1000 Hz		
Value	10	5	133	973	122	487	5	5

A.2.2 Repetitive Operation

Probes

Table A.3: Probes for repetitive operation

Probe	V_{GE}	$V_{CE(off)}$	I_C^*	$V_{CE(on)}$
Type	passive	passive	differential	passive
Attenuation	10:1	100:1	100:1	1:1
Frequency [MHz]	500	400	16	200

* Peak current = 600 A

Principle of Sequence Mode for Waveform Record

Due to the limited record length, oscilloscope was not feasible to record all the data from each switching operation. Hence, the sequence mode of oscilloscope was used in this work. The completed waveform consists of fixed-size slices. Only the switching-off phase was saved within one slice. Therefore, measurements and evaluations can be made on selected slices using the full resolution of the used time base. For each slice, time base was 200 ns and sampling rate was 500 MS/s.

Moreover, hold-off for a certain amount of slices was performed between two slices, and hence time was utilized to provide enough time for the oscilloscope to store the data and to limit the generated data size.

Determination of Slices

Take 500 Hz in Table 5.2 as an instance, the determination of each slice is shown in Figure A.2. The duration of each pulse during measurement was 0.002 s. At first pulse, signal was triggered at $V_{CE} = 200$ V. After the first trigger, oscilloscope started recording first slice at the 1000th pulse, because 999 events were ignored by Hold-off function. In other words, slice was recorded for every 2 s. Hence, after 20 minutes operations, 600 slices were recorded in total.

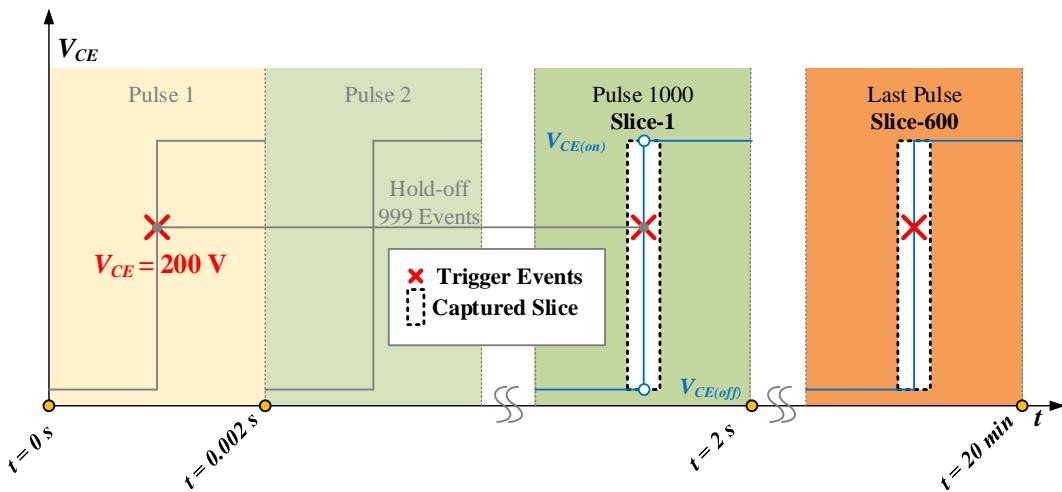


Figure A.2: Schematic illustration of slices determination by using sequence mode during repetitive operations with 500 Hz switching frequency

Values of Pulse Pattern for Each Ageing State

Table A.4: Values of pulse pattern for each ageing state

Time [μs]	t_1		t_2		t_3		t_4	
f [Hz]	500	1000	500	1000	500	1000	500	1000
$SoL - 0$	16	7.4	974	486.6	10	6	1000	500
$SoL - 1$	17.2	7.9	972.8	486.1				
$SoL - 2$	17.5	8	972.5	486				
$SoL - 3$	17.7	8.2	972.3	485.8				

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