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# Influence of Magnetic Coupling Effects between Load and Gate Commutation Loop on the Short Circuit Behavior

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## Abstract

Magnetic coupling effects have to be considered for neighboring inductive parasitics and overlapping commutation loops, and become more pronounced for transients with high current slopes. This paper shows the influence of coupling effects on the short circuit transients of semiconductor switches. Utilizing a special adapter, different coupling magnitudes, orientations, and origins could be displayed. Depending on the coupling, a softer or more dangerous short-circuit dynamic could be the consequence. Measures against coupling effects are summarized.

## 1 Introduction

The integration of a power semiconductor switch into a load- and gate-loop comes along with parasitic inductances. The inductances are inherent to conducting paths and enclosed commutation loops that are used to access the device terminals. According to the demand [1] to increase the switching speed of power devices and increasing the power density, hence reducing the distance between different commutation loops, the inductances cannot be treated individually.
In this work, the influence of coupling mechanisms between load- and gate-loop is addressed. In addition, the impact of physical distance between coupling inductances and measures against coupling effects are addressed.

## 2 Short circuit measurements subjected by magnetic coupling effects

### 2.1 Measurement adapter without pre-existing common-source inductance

The utilized measurement adapter realized as 3-level PCB (printed circuit board) stack is depicted in Fig. 1 with corresponding electrical circuit.

Starting at the bottom-level, Fig. 1c), a semiconductor switch on DCB (direct copper bonded) was soldered at the back-side and wire-bonded on the front-side on a DCB substrate. In this work, a 3.3 kV MOSFET and a 1.7 kV IGBT were used. The DCB offers landing areas for DC ±, Gate and Sense contacts. Given by the bond layout, a negligible inherent common-source inductance $L_{CS}$ is given. The intermediate-level, Fig. 1b), hosts the contact pins for DC ±, Gate and Sense contacts. In order to measure as close as possible at the real chip contacts, the gate measurement $V_{GE/S}$ was included on this level, too. $V_{GE/S}$ was measured for all different GDU (gate drive unit) connection positions. The top-level, Fig. 1a), was designed to keep the DC ± pins in place, without having electrical contact. Gate and Sense contacts were connected and guided to 4 different GDU positions # 1 to # 4. The gate trace was placed on the back-, and the sense trace on the front-side of the PCB. A simplified equivalent circuit diagram for the stacked 3-level setup is depicted in Fig. 1d). Here, the investigated coupling mechanism is implied between $L_G$ and $L_{Par\_low}$. It has to be mentioned, that other coupling relations, are also present for this setup. For example between the high- and low-potential contact-pins from Eq. (2)b) to b). However, this coupling effects are constant throughout the investigation of different GDU positions.
The inductance $L_{CS^*}$ is the effective inductance, which the gate and load commutation loop have in

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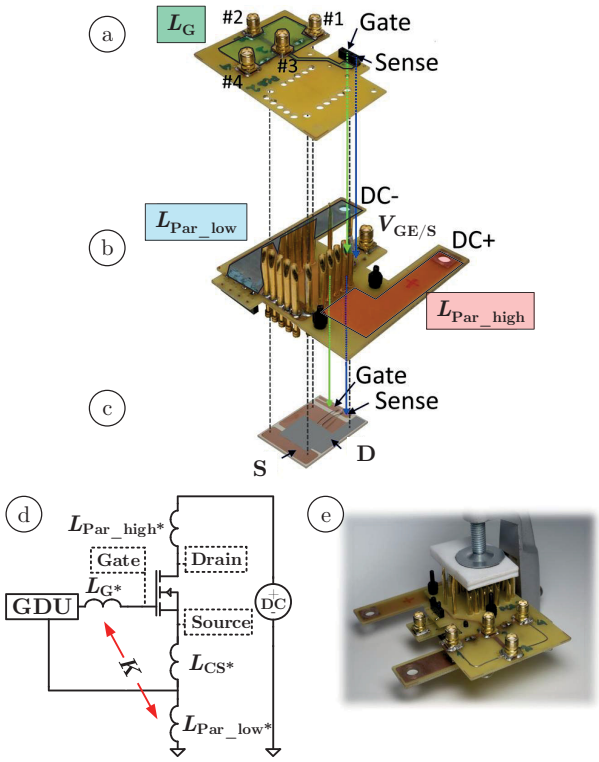


**Fig. 1:** 3-level test setup without common-source inductance. a) Top-level with different GDU positions #1 - #4, b) Intermediate-level with load terminals for DC-Link connection, c) Bottom-level with semiconductor switch on DCB substrate d) resulting circuit including dominant coupling mechanism, e) stacked 3-level test setup

common and is composed according to Eq. (1).

$$\begin{aligned} L_{\mathrm{CS}^*} &= L_{\mathrm{CS}} \pm M \\ L_{\mathrm{G}^*} &= L_{\mathrm{G}} \pm M \\ L_{\mathrm{Par\_low/high}^*} &= L_{\mathrm{Par\_low/high}} \pm M \end{aligned} \tag{1}$$

Hereby, the inductance values including a * are the effective inductances during dynamic transients. Those are taking the pre-existing inductances, indicated without * and given by the trace geometry, and the mutual inductance M, which represent the impact of coupling mechanisms K, into account. The parasitic inductances $L_{par\_high/low}$ within the load commutation loop remain constant for all upcoming presented tests. However, the gate loop inductances $L_G$ and thus the coupling mechanisms K could be varied by choosing a different GDU position. A further variation of $L_G$ was possible by adjusting the top-level as shown for different variants in Fig. 2.

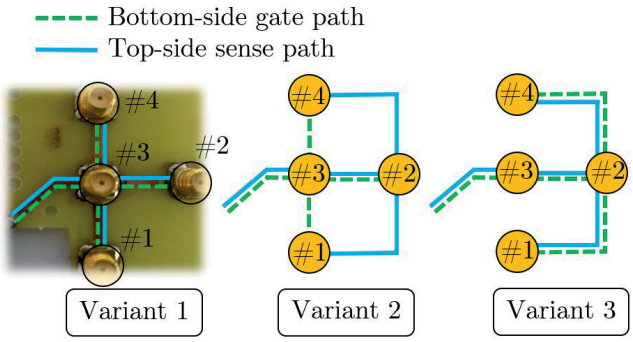


**Fig. 2:** Different variants for the top-level PCB (Fig. 1a)

## 2.2 Determination of parasitic inductances and coupling effects

The parasitic gate inductance $L_G$ for different GDU positions at the top-level differs in case of different trace layouts according to Fig. 2. For position #2 and #3, no changes of $L_G$ are expected. However, for #1 and #4 the trace layout plays a major role:

- Variant 1 has the lowest $L_G$ value, due to small loop areas between gate and sense trace
- Variant 2, the loops are bigger and the traces are longer, a higher $L_G$ value follows
- Variant 3, has a slightly higher parasitic inductance due to longer traces in comparison to variant 1

This qualitative observations could be proven by measurements according to the following principle:

- For a designated GDU position within the setup of Fig. 1, a voltage pulse was applied
- A defined capacitance of some nano farad was placed between the contact pins for gate and sense on the bottom level Fig. 1a)
- An oscillation resulted with a damped, however defined frequency according to the Thomson's equation:

$$f = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{2}$$

- From this frequency, and the known capacitance value, the inductance could be calculated

| GDU position | Variant 1 | | Variant 2 | | Variant 3 | |
|---|---|---|---|---|---|---|
| | $L_G$ in nH | $L_{CS^*}$ in nH | $L_G$ in nH | $L_{CS^*}$ in nH | $L_G$ in nH | $L_{CS^*}$ in nH |
| #1 | 105 | -0.8 | 158 | -2.4 | 145 | -0.3 |
| #2 | 105 | -0.3 | 105 | -0.3 | 105 | -0.3 |
| #3 | 90 | -0.3 | 90 | -0.3 | 90 | -0.3 |
| #4 | 105 | 0.4 | 158 | 1.8 | 145 | -0.3 |

**Tab. 1:** Measurement results of parasitic inductances $L_G$ and effective common-source inductance $L_{CS^*}$ for different GDU positions # 1 to # 4 and different PCB variants

The results are listed in Tab. 1. No load current was applied during the determination of $L_G$, hence no coupling between gate and load commuation loop had to be considered.

To determine the coupling orientation, namely a positive or negative feedback, between inductances of different commutation loops, as implied in Fig. 1d) is a little more complicated.

An approach is depicted Fig. 3. In Fig. 3a) the equivalent electrical circuit for the 3-level test setup is displayed. Highlighted are the gate and sense traces and important parasitic inductances. In order to determine the coupling orientation between inductances, the theory of transformers might be helpful.[2]

1. Selection of a current, e.g. $I_{Load}$, through the inductance of interest, e.g. $L_{Par\_low}$ and drawing the resulting magnetic field lines (red) along the conducting path following the right-hand rule. The result is depicted in Fig. 3b).
2. According to Fig. 3d), the coupling with $L_G$ is supposed to be investigated. The area of this inductance, where the magnetic field from the first step couples in, is depicted in Fig. 3c).
3. Within the area surrounded by $L_G$, a voltage is induced. This voltage forces a current to flow through $L_G$, which has to follow Lenz's law. Hence, this current has an orientation through $L_G$, that the resulting magnetic field is counteracting the root cause of the induction. The current and corresponding magnetic field lines are exemplary drawn in violet in Fig. 3c).

It is important to note, that the current displayed in Fig. 3c) and d) is not the gate current, which results out of the interacting between chip and GDU. Instead, this current has to treated as notional value in order to determine the inductance orientation. This orientation can be determined by a little dot next to the inductance symbol, according to the rule:

- Inducing inductance (e.g. $L_{Par\_low}$): The dot is placed where the current enters the inductance
- Induced inductance (e.g. $L_G$): The dot is placed where the current leaves the inductance

The result is shown in Fig. 3d) for the electrical circuit. An equivalent illustration is given by Fig. 3e), where the coupling is considered with effective values according to Eq. (1). The difference between Fig. 3d) and e) is given by the mutual inductance M, which represents positive or negative coupling with a value greater, equal, or smaller zero. For the specific case in Fig. 3, a negative feedback with a mutual inductance greater than zero should result. This estimation could be proven by measurements utilizing the method presented by [3] and [4]. The measurement circuit and evaluation principle is depicted in Fig. 4.

The results are listed in Tab. 1. Two things have to be pointed out.

1. According to the preliminary consideration that the pre-existing inductance $L_{CS}$ is negligible small for the setup in Eq. (2), the measured effective inductance $L_{CS^*}$ can be treated as mutual inductance M in good approximation.
2. The mutual inductance is different between variant 1 and 3, although the area between gate and sense trace is almost identical. This can be explained as follows: For variant 3, the area of $L_G$, where the magnetic field from $L_{Par\_low}$ couples in, is more far away and has another angle towards the magnetic field lines.
3. The obtained negative values for $L_{CS^*}$ are difficult to imagine. However, they follow the impact of coupling mechanisms as explained before according to the literature [2].
4. A basic positive feedback with negative mutual inductance is obtained with this setup due to the 45° angled trace leading towards GDU position # 3, which all positions have in common.

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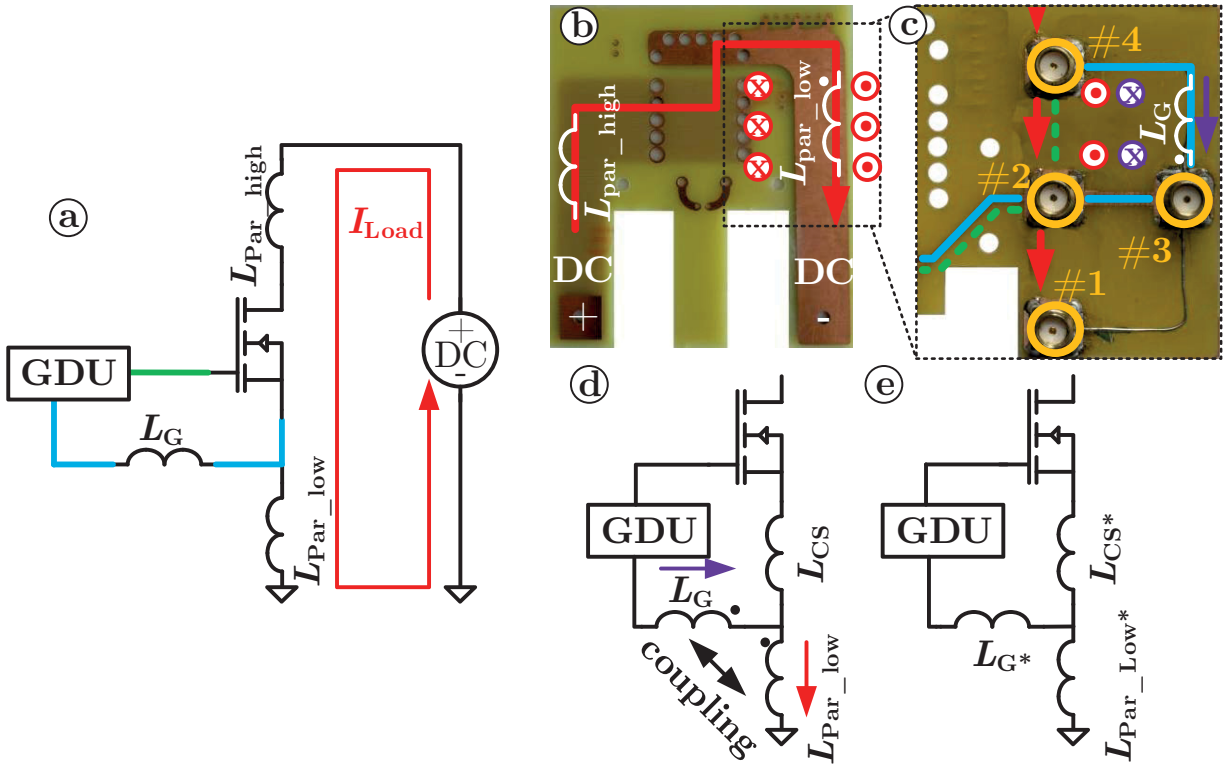


**Fig. 3:** Approach to determine the coupling orientation qualitatively. Example PCB variant 2, GDU at position # 4. a) electric equivalent circuit of the measurement adapter with highlighted gate and sense traces, b) intermediate-level PCB including the load current path, resulting magnetic field lines, and parasitic inductances, c) top-level PCB including notional current (violet) and corresponding magnetic field lines, d) coupled inductances for the chosen example, e) equivalent circuit to d)

## 2.3 Measurement results

After the determination of the parasitic inductances and coupling effects, the measurement results with the 3-level setup can be evaluated. Initially, the measurements were performed with a SiC MOSFET because of a low input capacitance, higher transconductance and therewith faster current slope in comparison to the available Si IGBTs. Hence, the above discussed coupling effects should be most visible. The obtained short circuit type 1 waveforms for different GDU positions and variant 2 top-level PCB are depicted in Fig. 5.

According to Tab. 1, the worst case scenario by taking the mutual inductance into account, was chosen. The applied DC-Link voltage was set to a low value in order to prevent the SiC MOSFET from thermal destruction during the short circuit duration. The gate voltage was chosen low in order to limit the danger of thermal destruction of the device under test. In addition, the applied gate voltage was close to the TCP (temperature compensation point) in order to limit thermal induced effects to a minimum. The turn-off resistance had to be chosen high due to oscillation effects, which are explained later in this work. A lower resistance resulted in a destructive short circuit event (not shown here).
The results are following the expectation of the previous section and the measurement results from Tab 1. Position # 1 is subjected by a positive feedback, with negative mutual inductance, that accelerates the short circuit turn-on like a small common-source inductance would do as shown by [5]. In contrast, position # 4 reveals a smoother short circuit turn-on. The totally consumed energy $E_{SC}$, as well as maximum $dI_D/dt_{max}$ during turn-on, are summarized in Fig. 5.
Evaluating this exemplary measurement: The SiC MOSFET had to withstand about 80 % more short circuit energy and was subjected by a 6.5-times

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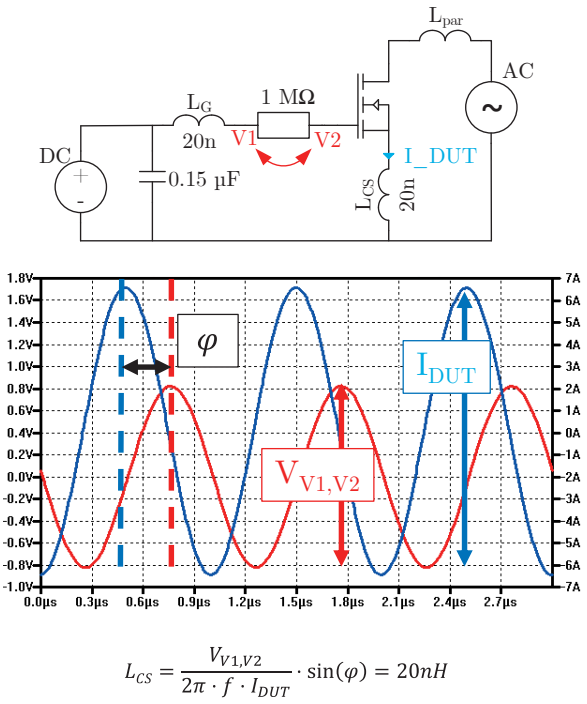


$$L_{CS} = \frac{V_{V1,V2}}{2\pi \cdot f \cdot I_{DUT}} \cdot \sin(\varphi) = 20nH$$

**Fig. 4:** Circuit, corresponding waveform and exemplary evaluation of the effective common-source inductance $L_{CS}$, according to [3] and [4]

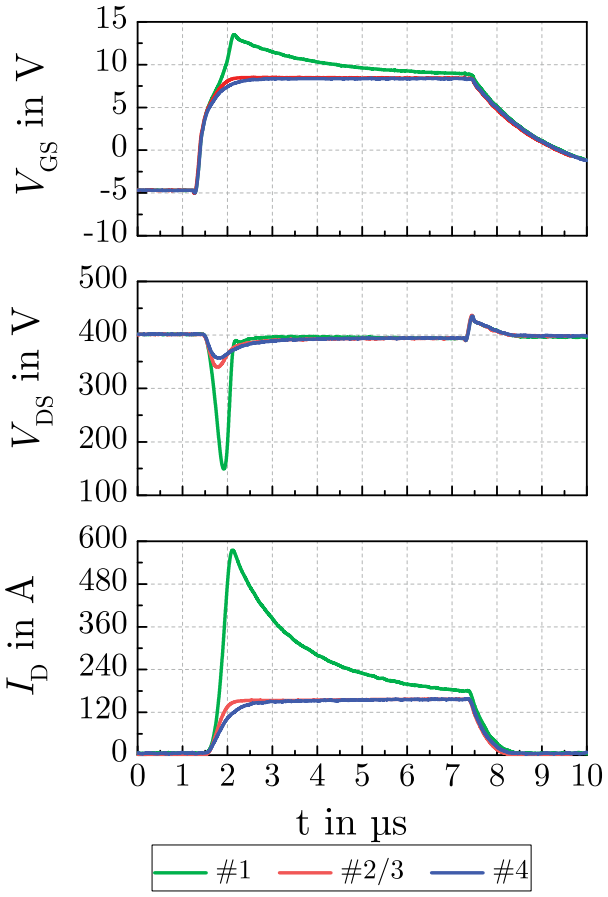


**Fig. 5:** Short circuit type 1 for different GDU position #1,2,4 with PCB variant 2.
(SiC MOSFET | 5 mm distance between top- and intermediate PCB | $R_{Gon}$=27 Ω | $R_{Goff}$=330 Ω | $V_{Gon}$=8 V | $V_{DC}$=400 V)

higher slope, while the GDU was connected at position #1 with strong positive feedback, in comparison to position #4 with negative feedback.

## 2.4 Reduction of coupling effects by distance and shielding layer

Following the expectations of magnetic induction theory [2], the coupling between two inductances can be reduced by increasing the distance or by adding a conductive shield in between. In Fig. 6, the damping influence of a higher distance and an additional copper-laminated PCB in between is shown. With a higher distance and the additional shield, the short circuit course given for a GDU at position #1 equals the position #2 Fig. 5, where a negligible coupling was present. The shield was realized by an additional PCB layer, placed between Fig. 1a) and b), with a floating copper-laminated surface.

## 2.5 Influence of gate resistance

For the following investigations, a Si IGBT was used, because of a higher inherent short circuit robustness in comparison to the available SiC MOSFET.

The selection of $R_G$ is essential to prevent the semiconductor switch from drastic oscillations, as shown in Fig. 7.

In principle, a small $R_G$ value enables faster switching, but increases the susceptibility to oscillations, due to an under-damped gate-loop according to [6]. A too small value enables the GDU to pull- the gate voltage up or down with a high slope $dv_G/dt$. This causes a high current slope $di_C/dt$, in turn a high inductive over- or undershoot of $V_{CE}$, and finally a capacitive charging or discharging current with the gate. The tendency of the switch to oscillate increases.

Increasing the gate resistance damps the oscillation remarkably. A design guideline of $R_G$ is given in

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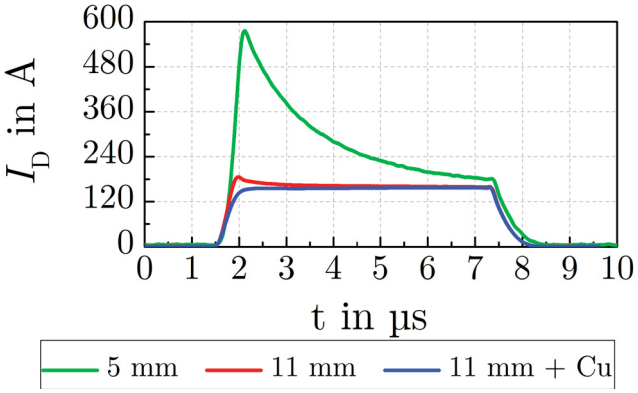


**Fig. 6:** Influence of distance (5 mm or 11 mm) between top- and intermediate-level of the 3-level setup and an additional shielding layer. (Variant 2 PCB, GDU position # 1, measurement conditions according to Fig. 5)

the literature [7] according to the following equation:

$$R_G \geq 2\zeta \cdot \sqrt{\frac{L_G}{C_{GS}}} \tag{3}$$

The damping ratio ζ describes the amplitude reduction between consecutive oscillations. According to the literature [8], a factor of ζ=1 corresponds to a solid rule of thumb to provide proper damping. However, this is only applicable for small coupling factors. As shown in section 3, greater coupling factors K request a higher damping ratio ζ. In Fig. 7, a damping ratio of 1.5 can be calculated for the case of $R_{Gon}$=$R_{Goff}$=5.6 Ω, which is not sufficient to damp the gate loop.

The influence of coupling effects is much more pronounced during turn-on, then for the turn-off transition. This can be explained as follows: The gate voltage course is determined by the GDU and the feedback from the inductive coupling. With a high voltage difference between GDU output and gate potential, the gate driver can supply a higher gate current, hence dominate the gate voltage course.

- During turn-on, the voltage difference towards the gate voltage steady-state decreases. However, the current level and in case of oscillations, the current slope increases. The slope of the current, which is coupled into the gate circuit by the mutual inductance, dominates the gate course.
- During turn-off, the voltage difference is high at the beginning. Means, the gate driver can sink a high gate current to shape the gate course. In addition, the current amplitude decreases due to the lowering of the gate voltage level. After passing the threshold voltage, the load current is already at a very low level, which cannot excite an oscillation through inductive coupling anymore.

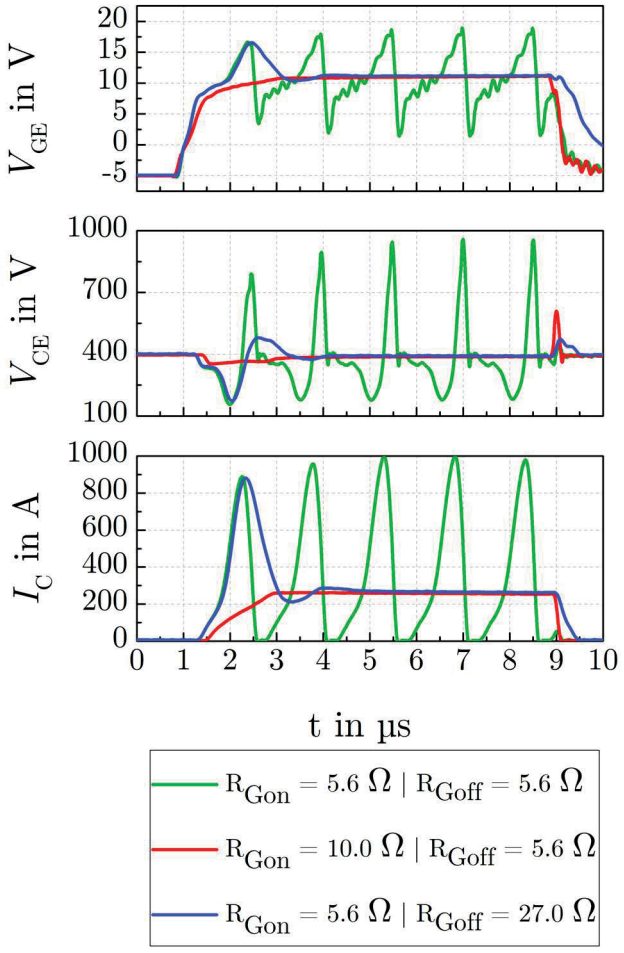


**Fig. 7:** Collector current and gate voltage for different gate resistor combinations.
(Variant 2 PCB, GDU position # 1
Si IGBT | 5 mm distance between top- and intermediate PCB | $V_{Gon}$=11 V | $V_{DC}$=400 V)

## 2.6 Influence of the applied voltage level

Another parameter, that influences the tendency of oscillations is the applied voltage level, Fig. 8. A voltage difference of about 2 % applied beforehand in addition to the DC-link capacitor, causes a dramatically different short circuit behavior. The reason for this is difficult to quantify according to the following aspects:

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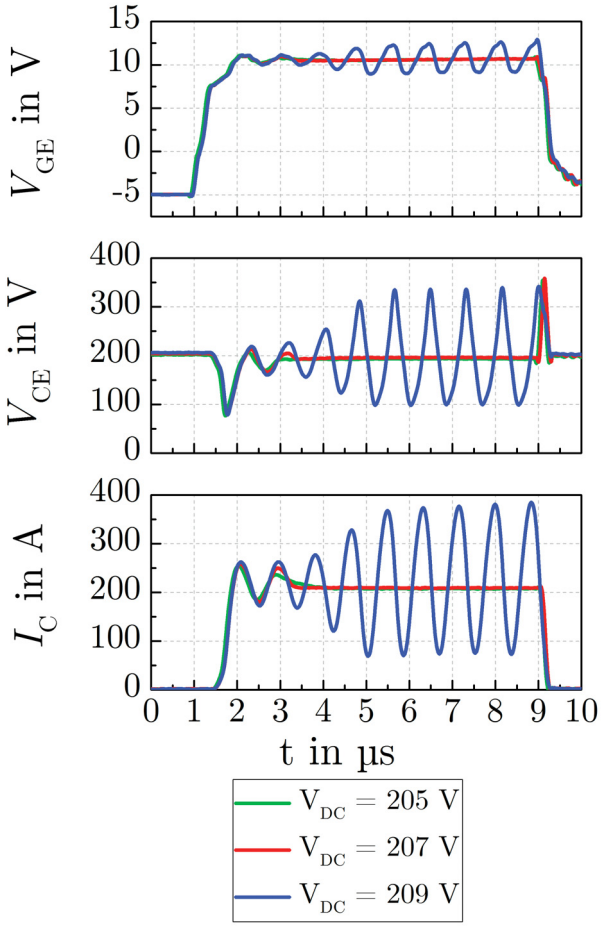


**Fig. 8:** Short circuit type 1 for variant 2 PCB and GDU position # 1 with different DC voltages.
(Si IGBT| 5 mm distance between top- and intermediate PCB | $R_{Gon}$=$R_{Goff}$=5.6 Ω | $V_{Gon}$=11 V)

- The oscillation frequency obtained by Eq. (2) does not correlate with the parasitic capacitance, and inductance values that were determined during the tests. Another oscillation source seems to superimpose with the gate commutation loop.
- Superimposing oscillations with voltage dependency could have two source:

1. Inductive superimposition: Due to the coupling between $L_{Par\_low}$ and $L_G$, a mutual inductance M is inserted into the commutation loop. M transfers the slope of the load current into the gate commutation loop. This feedback is amplified, if the slope of the load current increases. The slope increases, when the amplitude of the short circuit current is increased by keeping the same oscillation frequency. The short circuit current increases slightly according to a wider space-charge region that builds up at higher DC voltage levels.
2. Capacitive superimposition: The oscillating load current induces an oscillating voltage between collector and emitter, due to the parasitic inductances $L_{Par\_high/low}$. The corresponding voltage slope sources and sinks a current through the miller capacitance into the gate. Also the miller capacitance is voltage dependent.

| GDU position | $L_G$ in nH | $L_{CS*}$ in nH |
|---|---|---|
| #1 | 248 | 11.5 |
| #2 | 220 | 11.5 |
| #3 | 180 | 9.4 |
| #4 | 160 | 9.4 |
| #5 | 220 | 8.0 |
| #6 | 248 | 8.0 |

**Tab. 2:** Different parasitic gate and effective common-source inductances for different GDU connection points # 1 to # 6 for the setup in Fig. 9.

All in all, the oscillation sources are superimposed and overcame a critical excitation level, that could not be damped anymore by the given gate resistance. A more precise evaluation requires a more detailed insight into all parasitic components of the setup and device itself.
A theoretical approach to determine a critical voltage level for a given application, was presented by [6].
Even though, that the investigated voltage level may not represent the normal application case, it has to be highlighted, that slight variants of voltage levels may cause drastically different oscillation behaviors.

## 2.7 Results for a measurement adapter with pre-existing common-source inductance

Another PCB setup was utilized to demonstrate the effect of coupling mechanisms, when a common-source inductance $L_{CS}$ is pre-existing due to the geometrical interconnection of conducting traces. The setup is shown in Fig. 9. Measured inductances are listed in Tab. 2.

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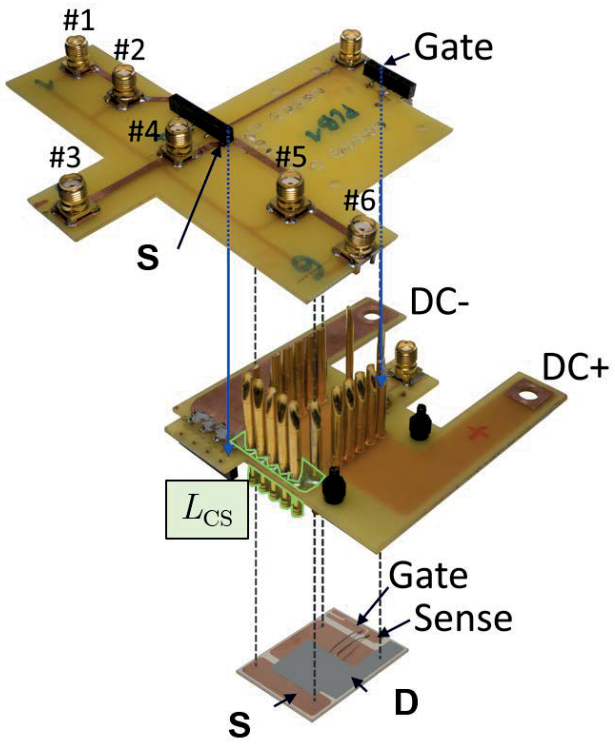


**Fig. 9:** 3-level PCB with pre-existing geometrical common-source inductance $L_{CS}$.

This setup is distinguished to show the influence of coupling effects between all parasitic inductances, which are present in a common semiconductor switch integration. Namely, parasitic inductances of the main commutation loop $L_{Par\_high/low}$, of the gate loop $L_G$, and the pre-existing geometrical common-source inductance $L_{CS}$. The coupling mechanisms are rather complex for this setup, because 6 coupling relations, as depicted in [4], have to be considered between all parasitic inductances. The individual contribution of each coupling pair is difficult to separate, however, the overall impact is measurable. The effective common-source inductance, respecting all coupling contributions, is given for all GDU positions in Tab. 2. The corresponding gate loop inductances are given, too. Both were measured according to the same principle described in section 2.2. According to the geometric layout of the intermediate- and top-level, $L_{CS}$ is equal for all GDU positions. According to the measurements and the perpendicular arrangement of GDU position #3 and #4, with respect to the load commutation loop, it is assumed, $L_{CS}$ is assumed to be 9.4 nH.

The measurement results presented in Fig. 10 can

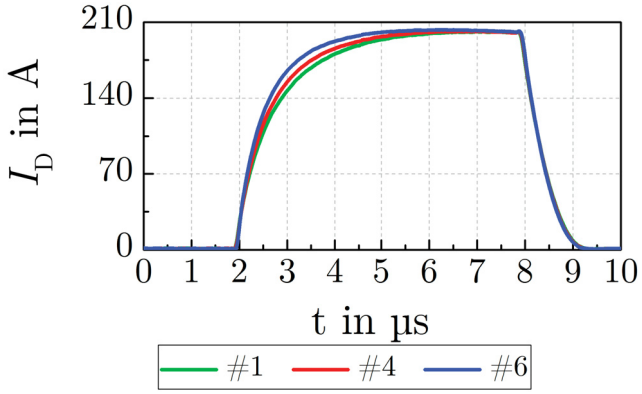


**Fig. 10:** Short circuit current obtained for the 3-level setup according to Fig. 9 at different GDU positions #1, 4, 6. $V_{GS}$ was measured close to the chip independently of the GDU position. (SiC MOSFET| 5 mm distance between top- and intermediate PCB | $R_{Gon}$=3.3 Ω | $R_{Goff}$=330 Ω | $V_{Gon}$=9 V | $V_{DC}$=400 V)

be evaluated as follows:

- According to the obtained effective common-source inductances, as listed in Tab. 2, the short circuit turn-on for position #6 is, taking position #4 as reference, faster.
- The results for position #2, #3, and #5 are not depicted, due to the high similarity to #1, #4, and #6, respectively.
- The additional inductance $L_G$ between #6 to #5, #3 to #4, and #1 to #2 does not influence the measurement result.

It can be concluded, that the effect of coupling is also present in setups with pre-existing common-source inductances.

## 3 Simulation of coupling effects

Coupling effects can also be reproduced and studied with electrical circuit simulators (e.g. *LTSpice*, or *SIMetrix*). Therefore, a coupling factor K between two inductances has to be defined between -1 and 1 to represent a positive or negative feedback. The exemplary simulation shown in Fig. 11 is supposed to demonstrate the meaning of the K value.

A coupling factor is established between $L_G$ and $L_{Par\_low}$ with different magnitudes. In fact, K has to

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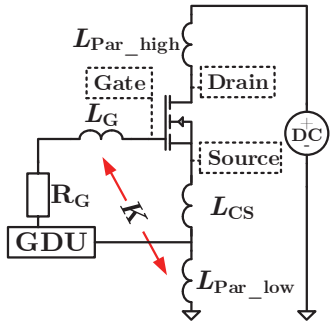


| Setup | A | B | C | D |
|---|---|---|---|---|
| $L_G$ in nH | 20 | 22 | 20 | 25 |
| $L_{Par\_low}$ in nH | 20 | 22 | 20 | 25 |
| $L_{CS}$ in nH | 4 | 2 | 4 | 0 |
| $K$ | -0.1 | 0 | -0.25 | 0 |

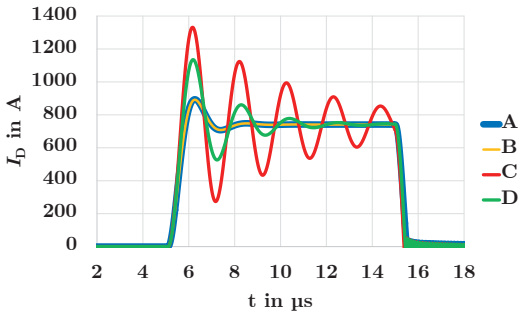


**Fig. 11:** Simulation model, setup parameter set and resulting drain current for an exemplary short circuit type 1 event. The drain current course for setup A is depicted with a thicker line in order to visualize the equality with setup B.

be interpreted as follows: A coupling K between $L_G$ and $L_{Par\_low}$ with a positive feedback and a value of -0.1 (setup A in Fig. 11) generates a mutual inductance M with an value of 10 % of the corresponding inductances. Following the theory [2], M is considered in the electric circuit simulator as follows:

$$\begin{aligned} K \propto L_G \leftrightarrow L_{Par\_low} : -0.1 \\ L_{CS^*} = L_{CS} - M \\ L_{G^*} = L_G + M \\ L_{Par\_low^*} = L_{Par\_low} + M \end{aligned} \tag{4}$$

When a K-value is entered into the simulator (setup A), the simulator is taking the effective values, indicated by *, into account.
The comparison between setup A and B in Fig. 11 verifies, that instead of implementing a K-value, also the converted values according to Eq. (4) can be used in order to consider coupling effects.
Earlier in this work, negative common-source inductances were measured, which are not easy to imagine. As shown with setup C and following the calculation principle, a negative common-source inductance would follow. That the negative common-source inductance in setup C causes an even faster turn-on, and more oscillating current as a non-existing common-source inductance in setup D, is also shown.
For the simulation in Fig. 11, a gate resistance $R_G$=3 Ω was applied while a model with gate-source capacitance $C_{GS}$=100 nF was used. Taking Eq. (3) into account, a simulation with a damping ratio of $\zeta$>3 was performed. An even higher $\zeta$ would be necessary to damp the oscillation successfully, in case of a positive feedback and hence low effective common source inductance $L_{CS^*}$.

Presuming a detailed insight into the capacitances and inductances of the setup, electrical simulation are a powerful option to reproduce coupling effects.

## 4 Design considerations for lowering coupling effects

It was shown, that the three-dimensional design of gate- and load-commutation loops may lead to coupling effects. Corresponding to the investigated short circuit events, these effects can be

+ Beneficial: Less consumed short circuit energy
- Hazardous: Increased susceptibility to oscillations, faster short circuit transients

In order to prevent coupling effects to take place, the following design considerations should be applied:

- Design of commutation loops in a strip-line setup with minimized inherent stray inductance, according to [9].
- Right-angled alignment of overlapping or nearby commutation loops according to the evaluation with different GDU positions in section 2.3
- Usage of a sufficiently large gate resistance with respect to the effective common-source inductance $L_{CS^*}$
- Reconsideration of higher distances or shielding layers between commutation loops

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## 5 Conclusion

It could be shown that the gate driver position and hence the resulting coupling orientation between gate and load commutation loops can affect the short behavior remarkably. An approach to determine the nature of a coupling feedback was presented and could be proven by measurements. The influence of gate resistors and the applied voltage level on the short circuit waveform and measures against coupling effects were presented and discussed in detail. That electrical simulations are a useful tool to interpret coupling effects could be presented.

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