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Faculty of Electrical Engineering and Information Technology
Chair of Power Electronics

Temperature Distribution of an IGBT Chip during Repetitive Switching Events under Consideration of Front-Side Ageing

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Course of Study	Electro-Mobility
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Date	01.06.2022

Outline

Motivation

01 | Operation of device

- repetitive switching
- $I_{C(nom)}$
- frequency

02 | Temperature determination

- case → T_c
- junction → T_j
- surface → $T_{surface}$

03 | Front-side ageing

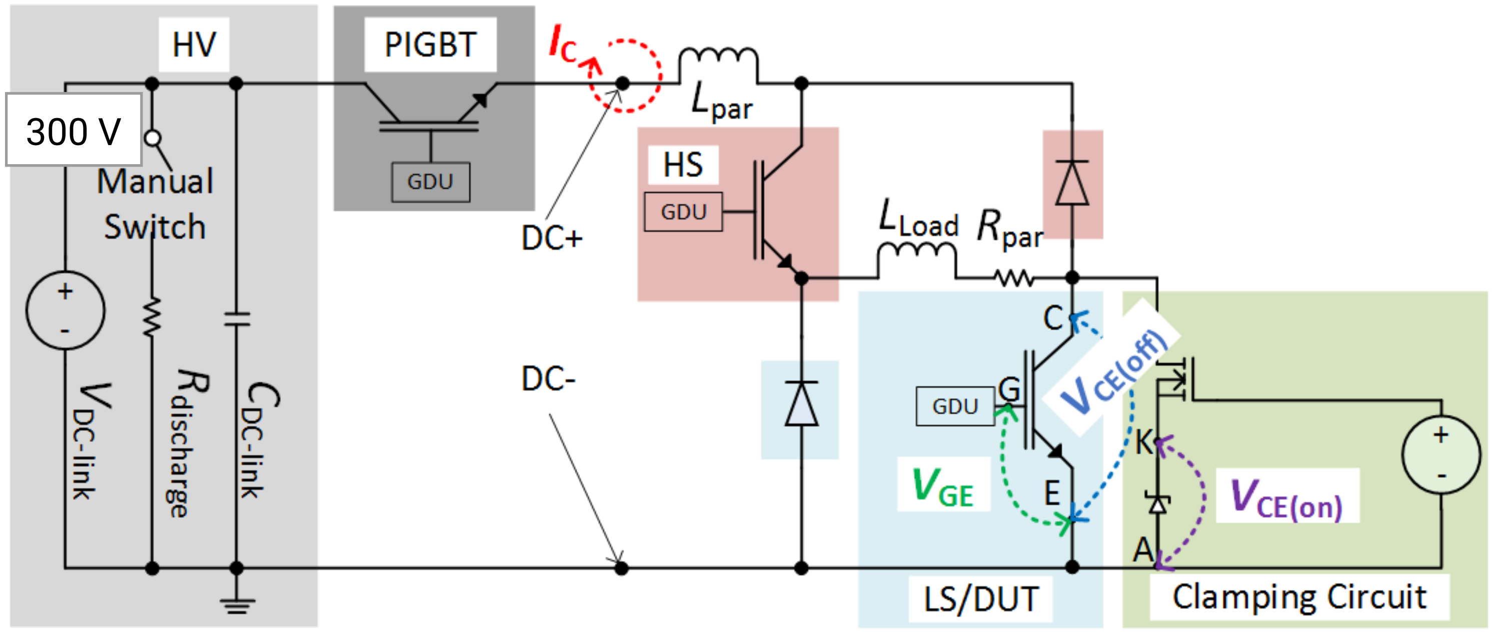
- bond-wire-loop cut-off

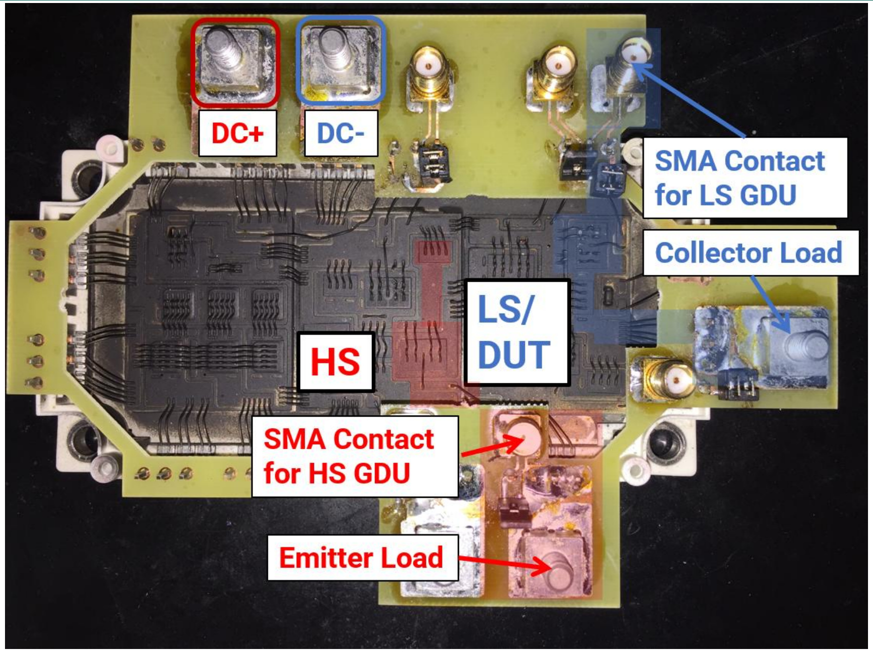
Goal | Dependency of temperature

- ageing state
- f (500 | 1000 Hz)

Outline

Circuit and DUT





Operation condition

- R_G = 0 → fast switching
- $I_{c(nom)}$ @ turn-off (100 A)
- 20 min operation → steady T

Test circuit

- $V_{CE(on)}$ measured by clamping circuit
- I_C measured @ DC+

DUT | Adapter

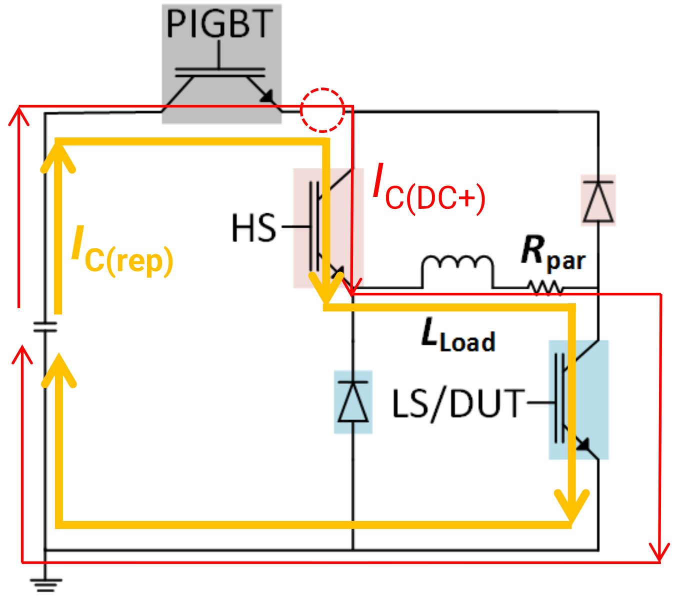
- removed gel & dyed surface → IR-camera
- Emitter contact of DUT → bond-wire included

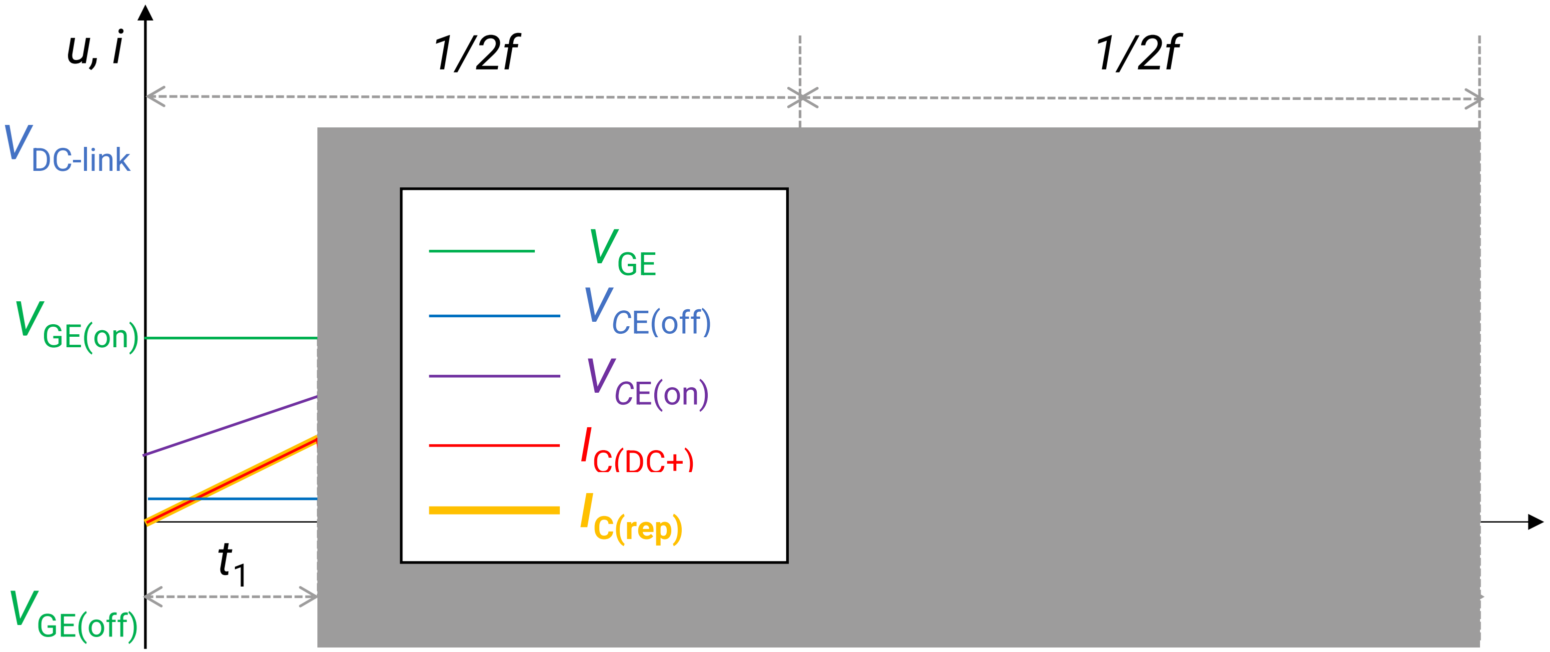
Outline

Pulse pattern | t_1

GDU	t_1	t_2	t_3	t_4
PIGBT	on	on	on	on
HS	on	off	on	on
LS/DUT	on	on	on	off

Circuit





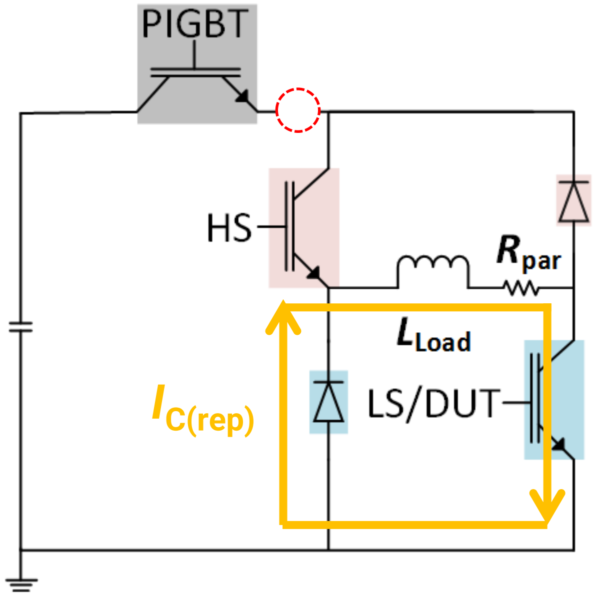
Waveform

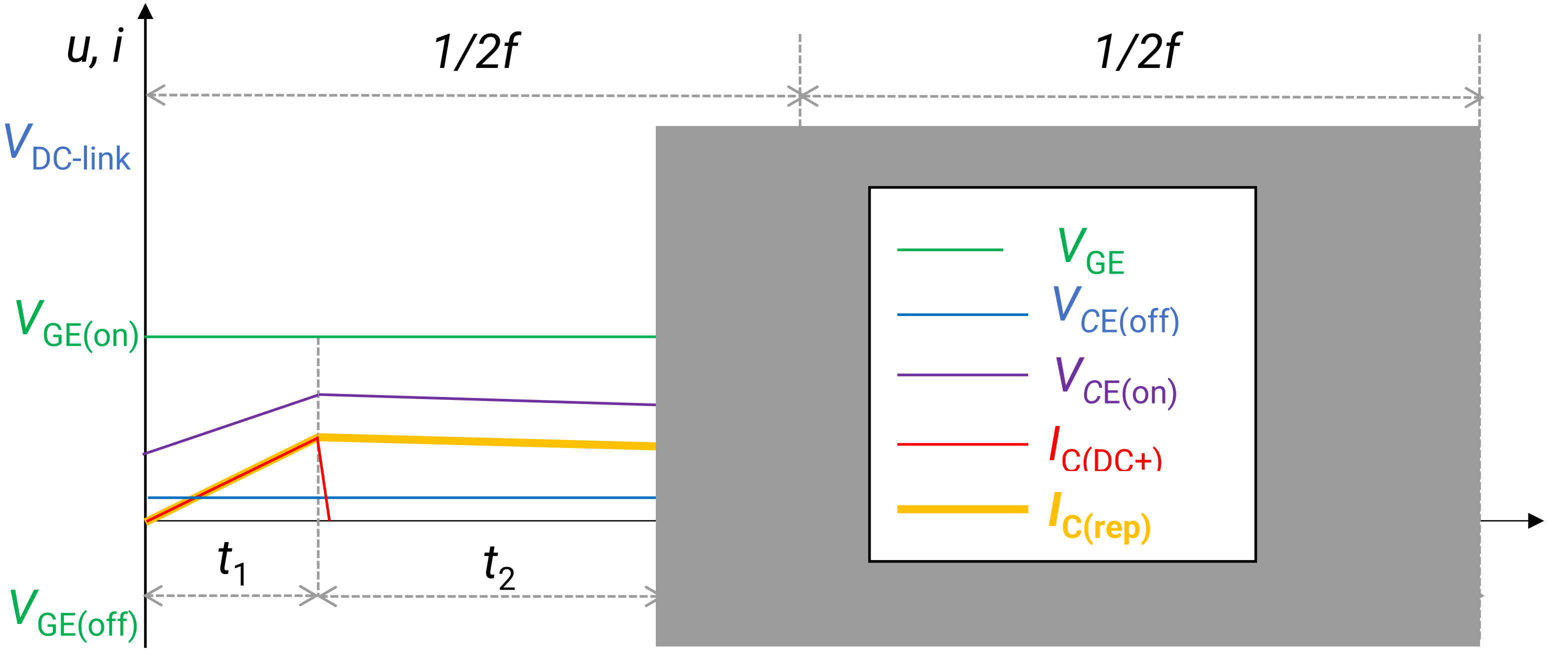
- HS & DUT both on
  - ➢ I_C ramps-up
  - ➢ $V_{CE(on)}$ increases with I_C

Pulse pattern | t_2

GDU	t_1	t_2	t_3	t_4
PIGBT	on	on	on	on
HS	on	off	on	on
LS/DUT	on	on	on	off

Circuit





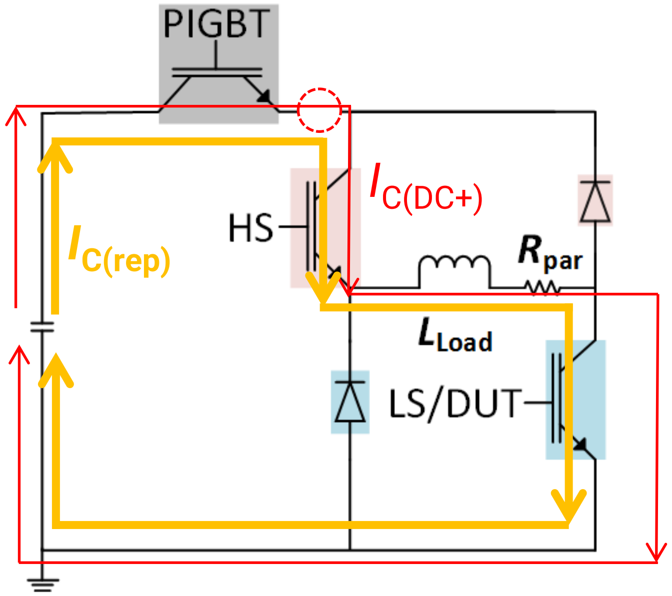
Waveform

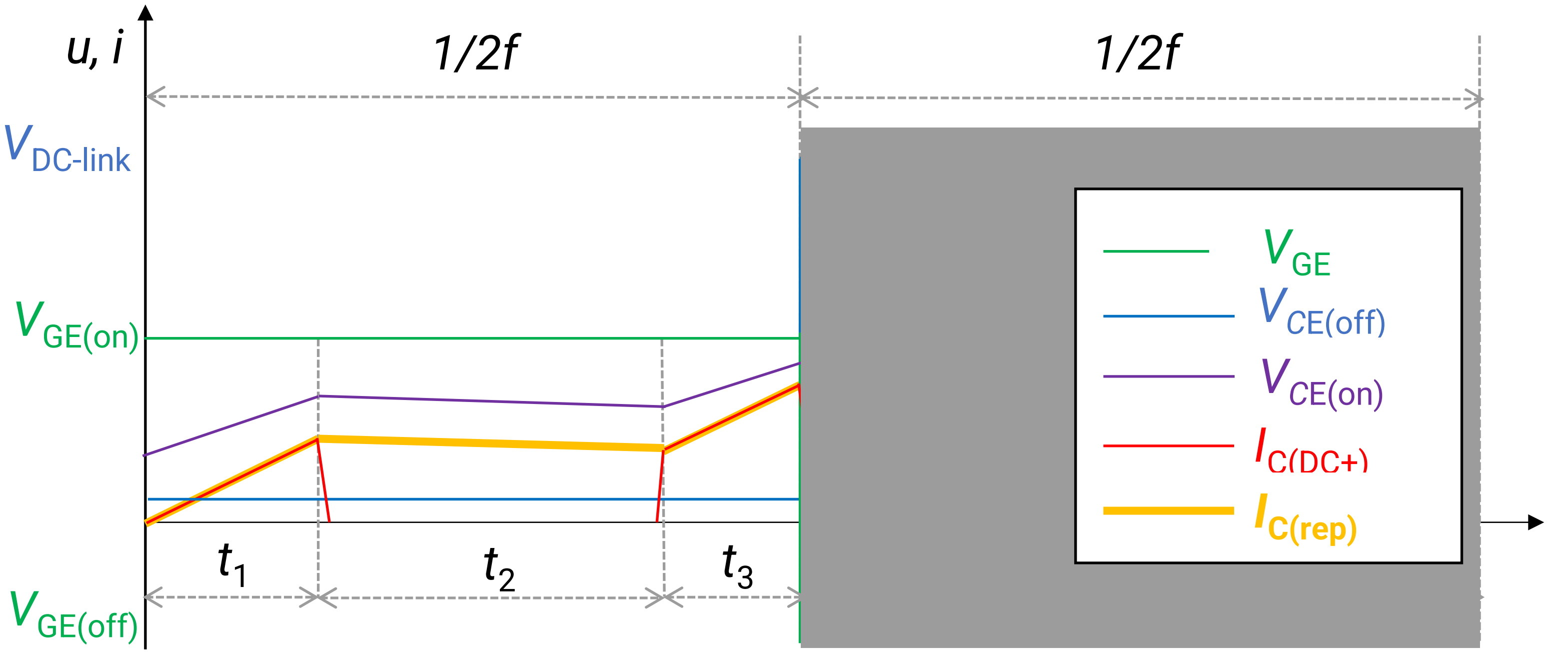
- HS off & DUT on
  - ➢ $I_{C(rep)}$ in LS free-wheeling
  - ➢ $V_{CE(on)}$ decreases with I_C

Pulse pattern | t_3

GDU	t_1	t_2	t_3	t_4
PIGBT	on	on	on	on
HS	on	off	on	on
LS/DUT	on	on	on	off

Circuit





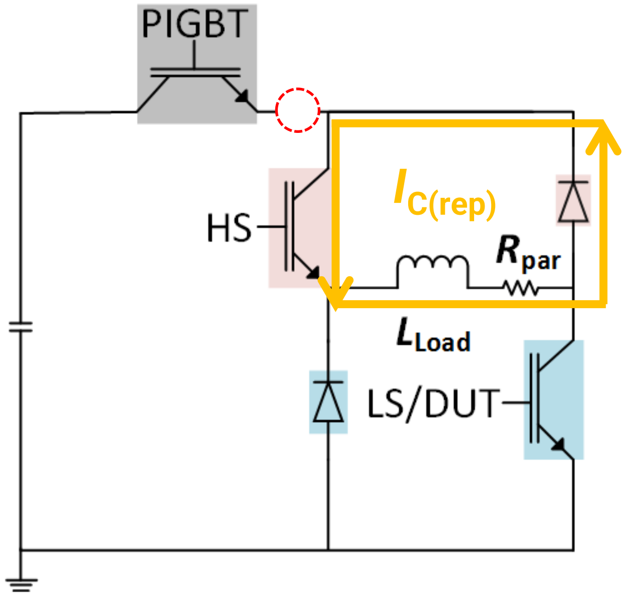
Waveform

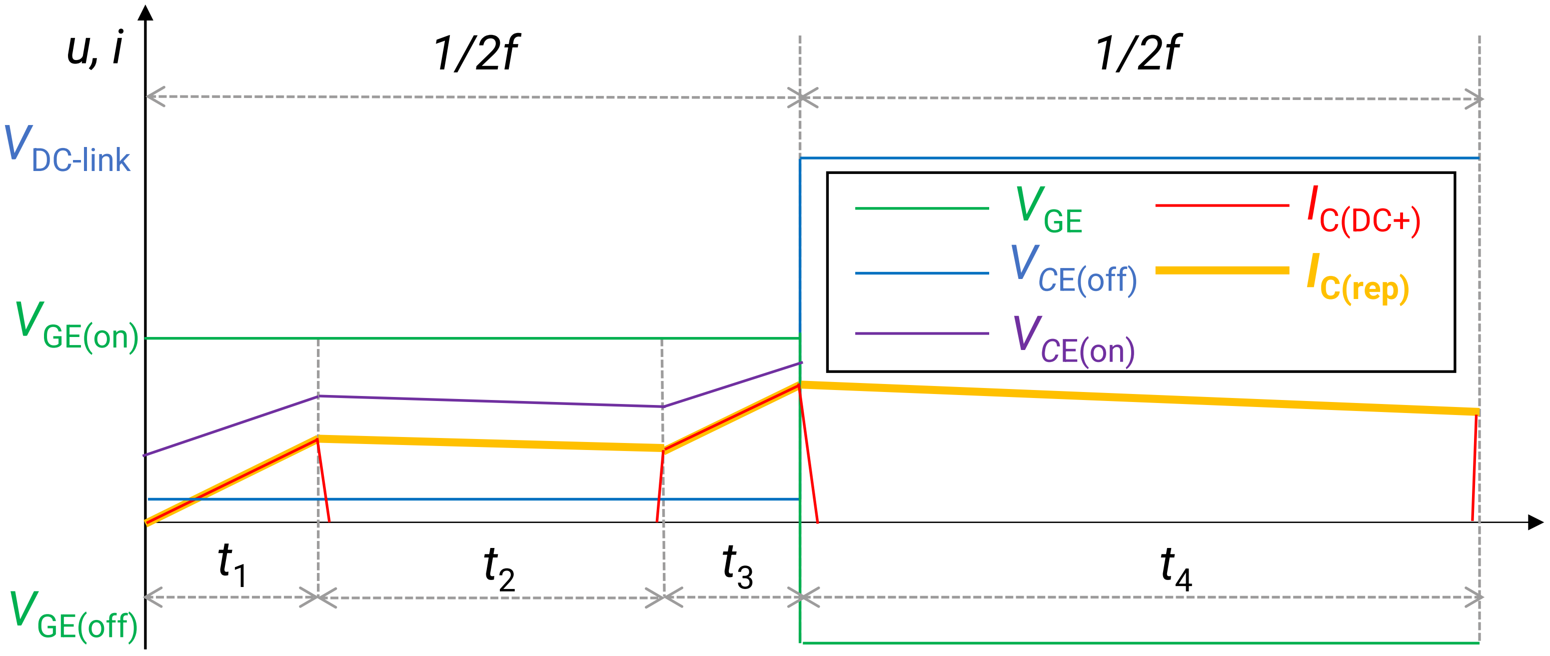
- HS & DUT on
  - ➢ $I_{C(rep)}$ ramps-up
  - ➢ $V_{CE(on)}$ increases with I_C

Pulse pattern | t_4

GDU	t_1	t_2	t_3	t_4
PIGBT	on	on	on	on
HS	on	off	on	on
LS/DUT	on	on	on	off

Circuit



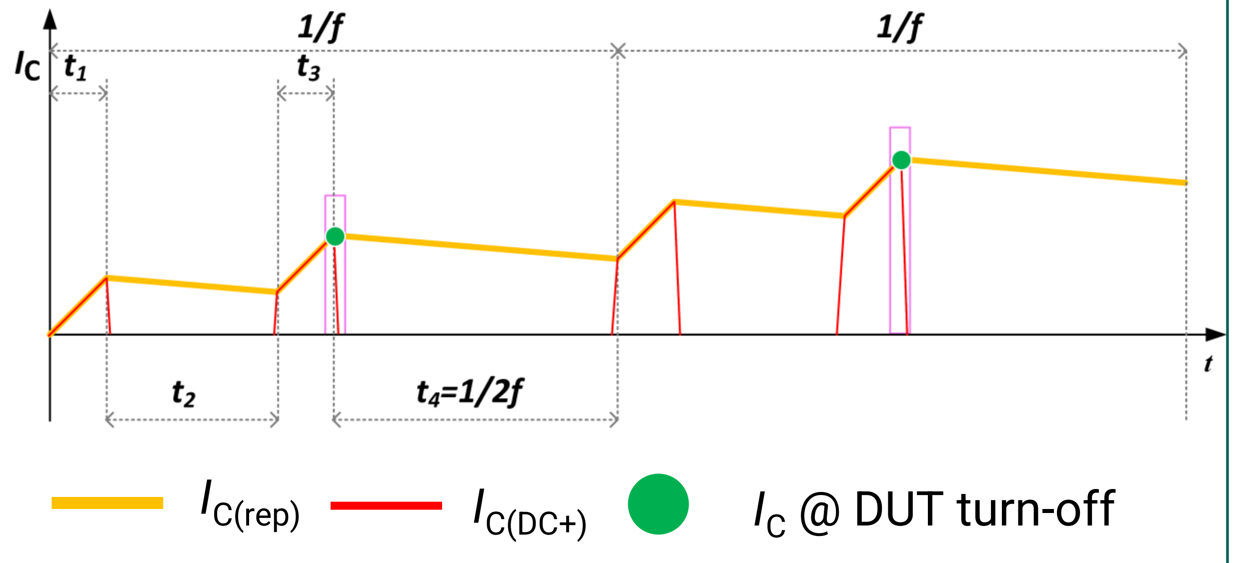


Waveform

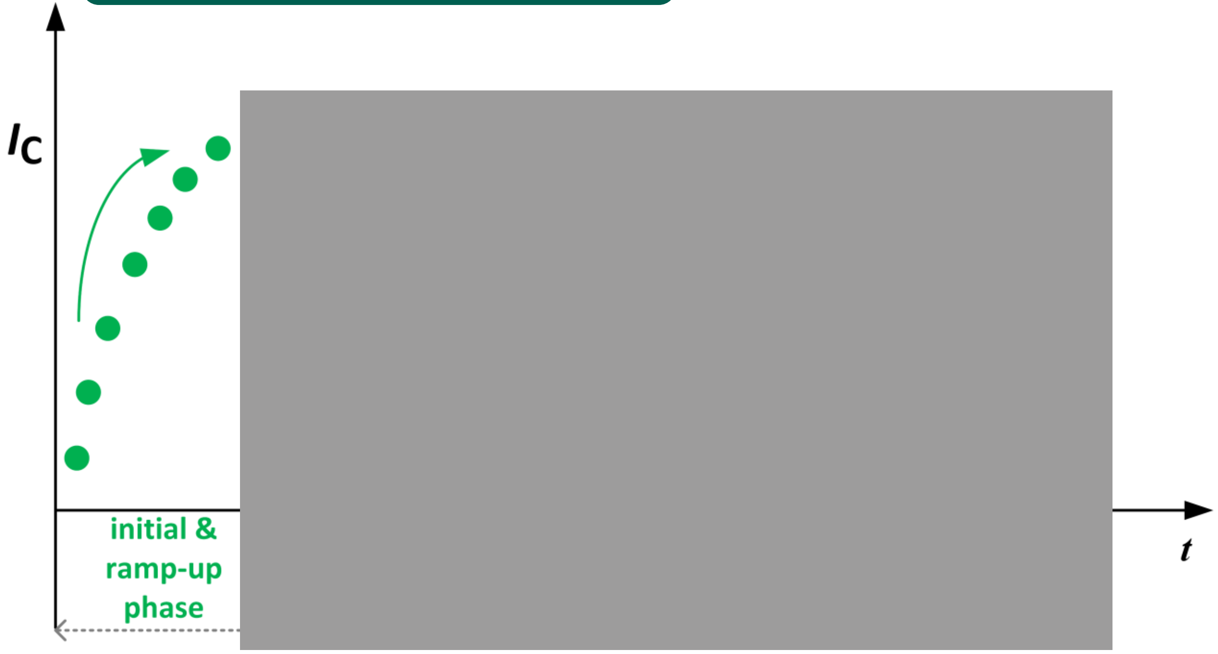
- HS on & DUT off
  - ➢ $I_{C(rep)}$ in HS free-wheeling
  - ➢ DUT → 50% duty cycle

Development of I_C | initial & ramp-up phase

Record of I_C



Initial & ramp-up



Development of I_C | balancing phase

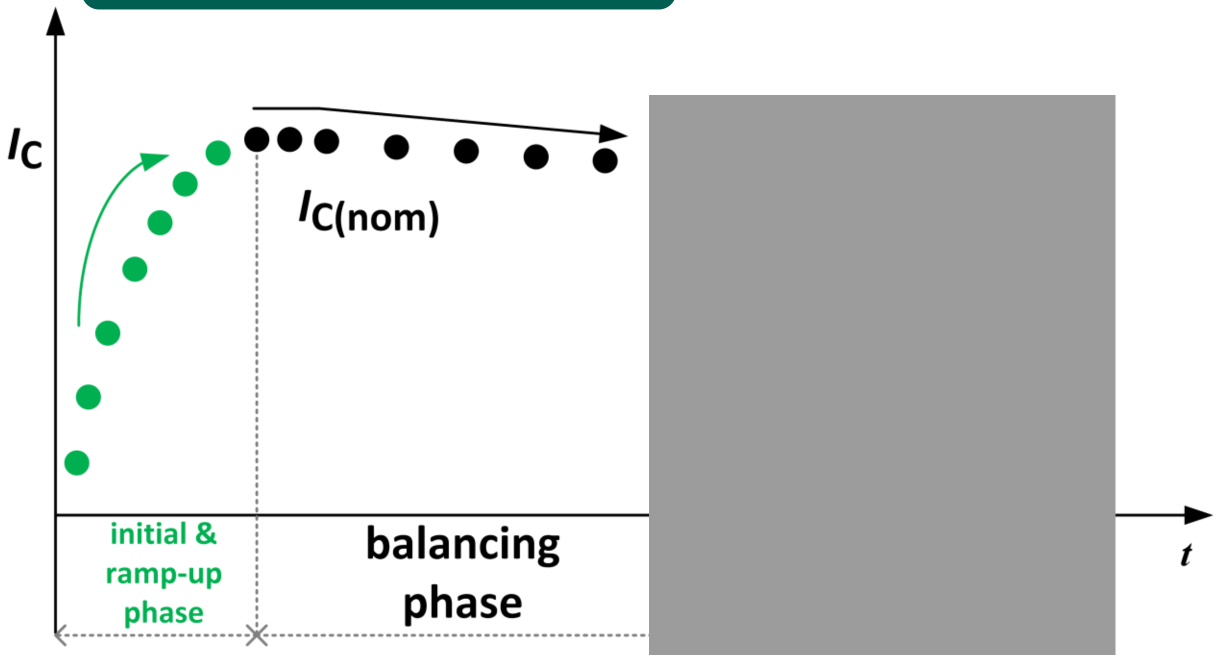
Derive of I_C

$$V_{DC\text{-}link} - \sum V_{CE(on)} - i_C \cdot R_{par} = L_{Load} \cdot di_C / dt$$

- $V_{DC\text{-}link}$, L_{Load} & dt = const.
- $P \uparrow \rightarrow T \uparrow \rightarrow V_{CE(on)} \uparrow$

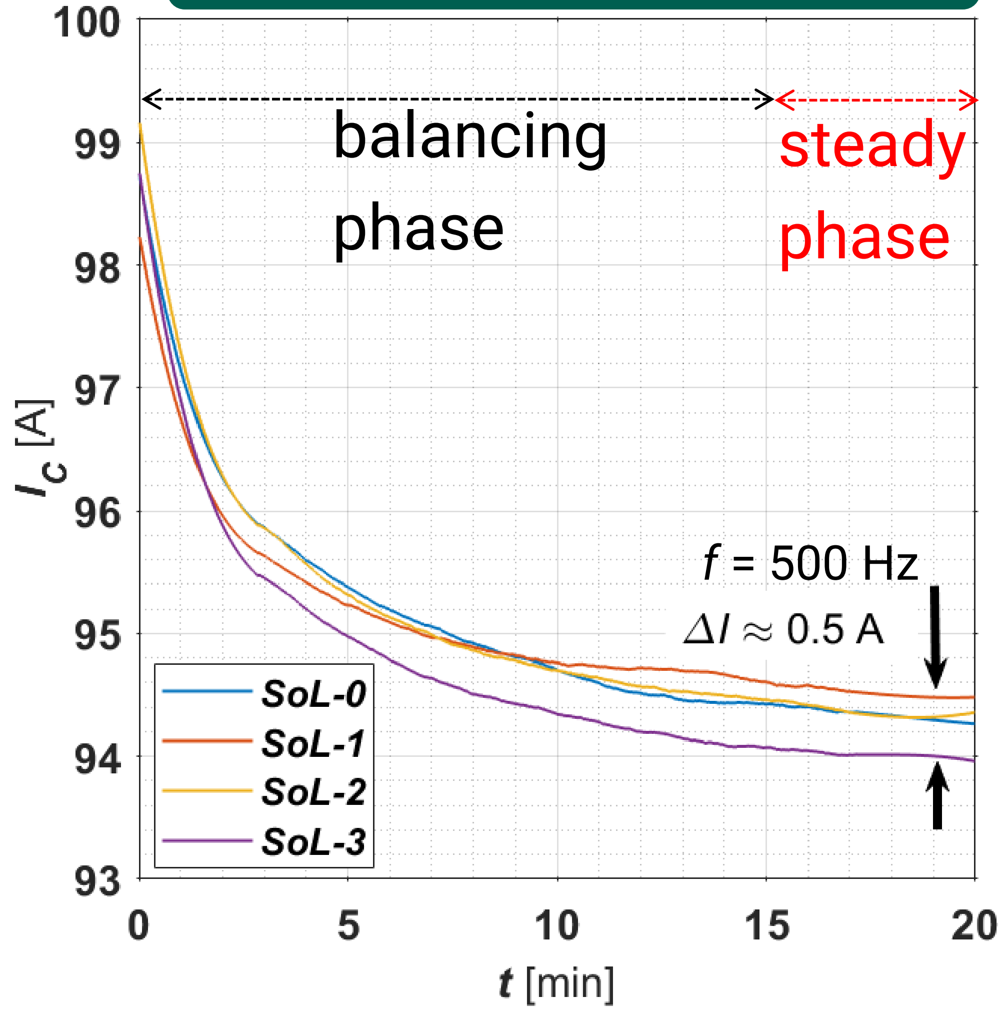
➢ $I_{C(rep)} \downarrow$

Balancing phase



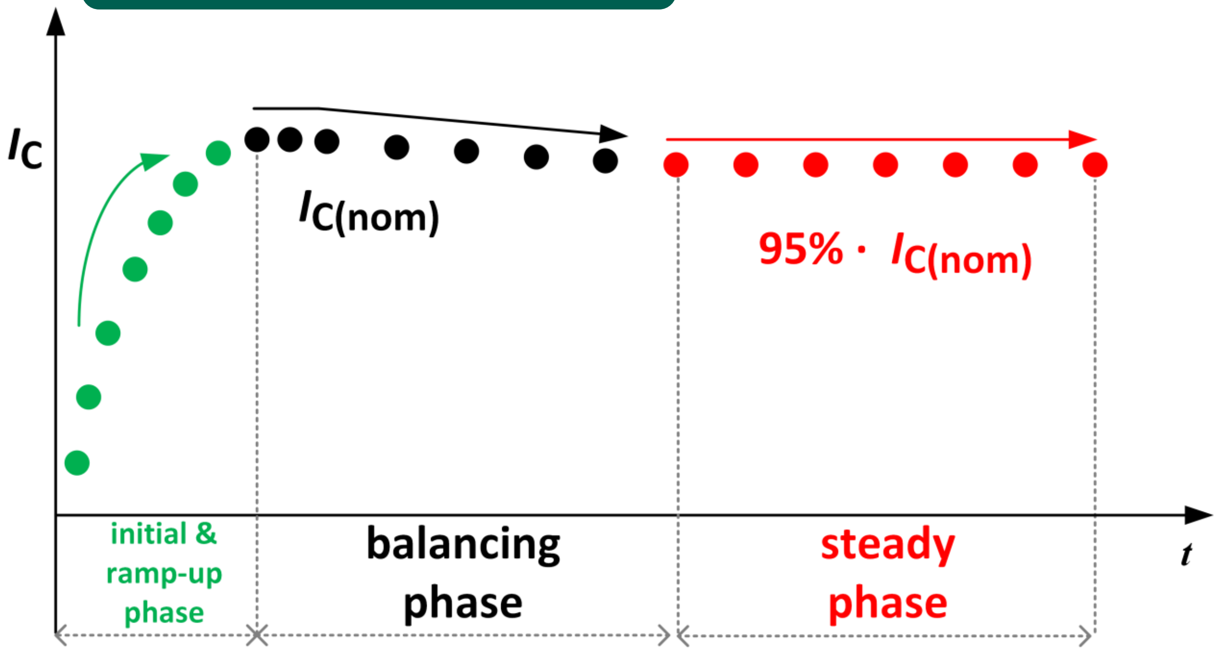
Development of I_C | measurement results

Measurement results of I_C



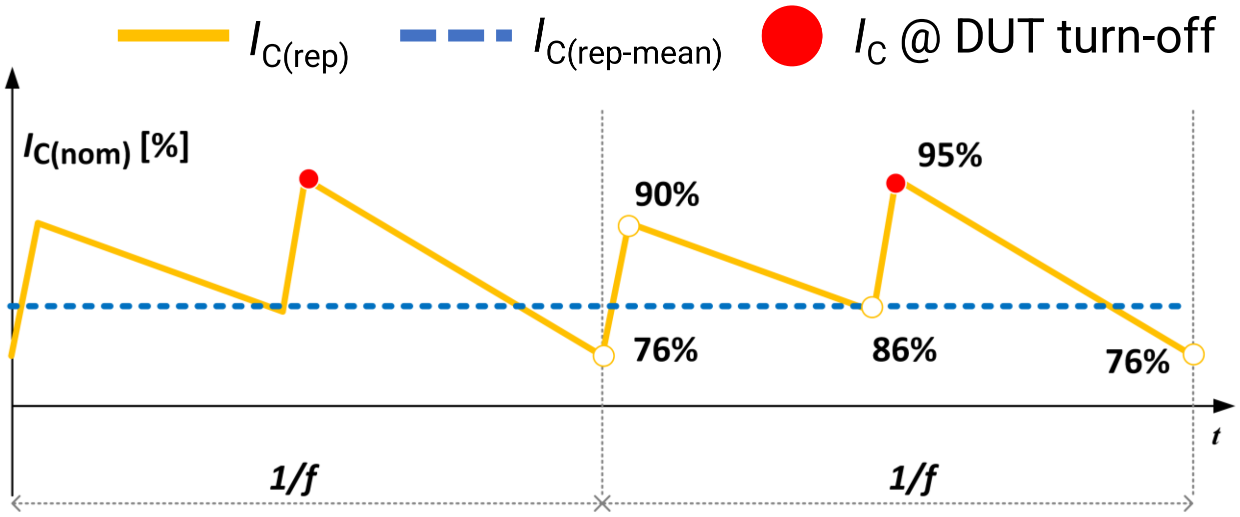
SoL = State of Life

Steady state

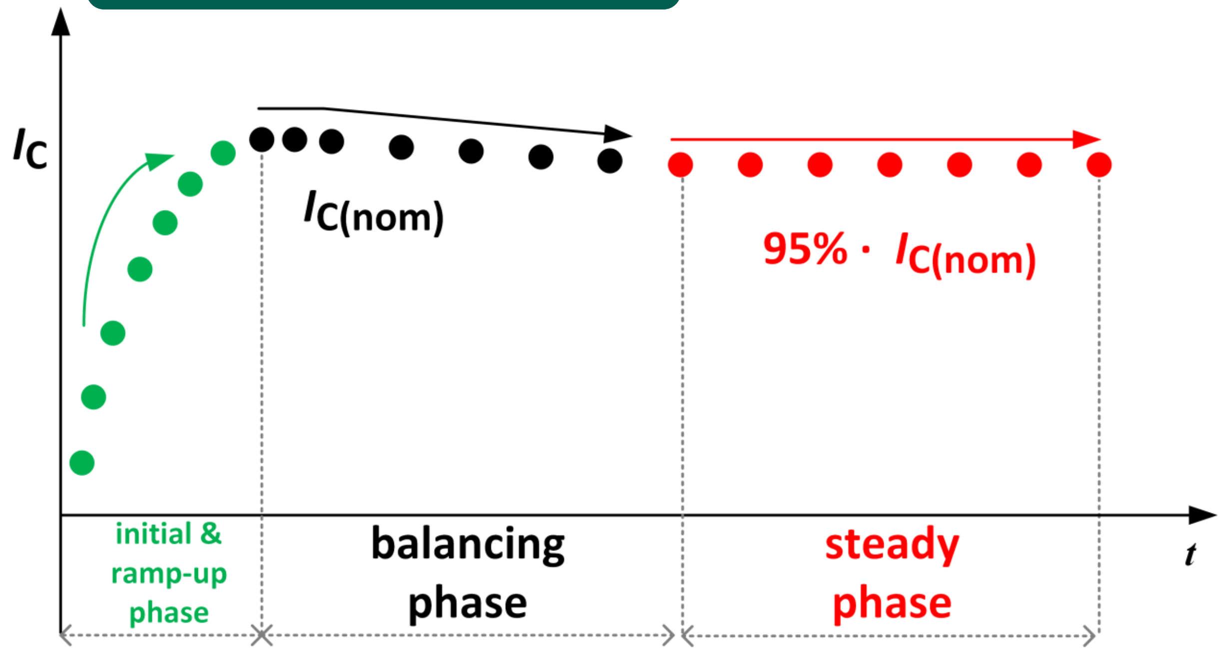


Development of I_C | $I_{C(rep\text{-}mean)}$

Mean value of I_C at steady state



Development of I_C



Performance of pulse pattern

- DUT switches off at 95% · $I_{C(nom)}$
- P_{loss} more like an real inverter approached:
  - R_{par}
  - conductive loss of switches ($V_{CE(on)} \cdot I_C$)

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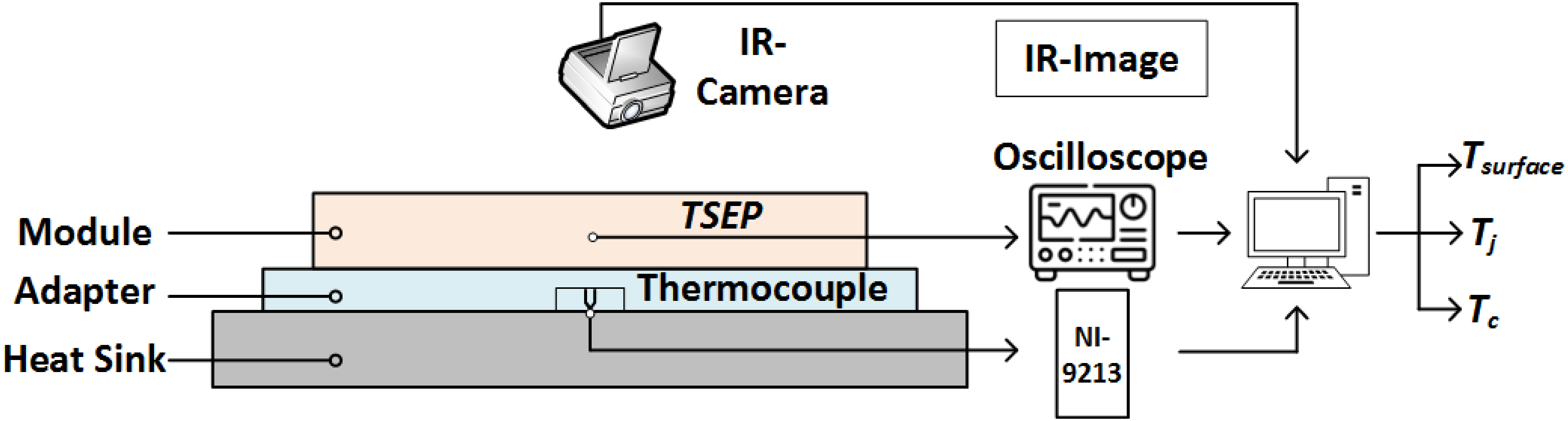
Outline

Overview

Note

- unsynchronisation of IR-camera & thermocouple with pulse pattern
  - ➢ T_c , $T_{surface}$ & T_j should be traded individually



T_j | TSEP | selection

Criteria

max. T_j within each cycle

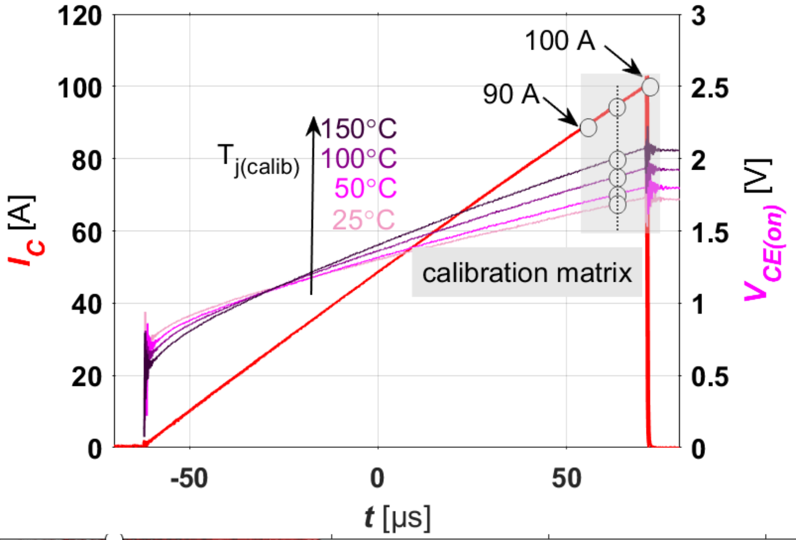
→TSEPs on conductive state or switching-off transition

TSEP	ageing state?	self-heating?	interruption during operation?	external circuit needed?	linearity	calibration effort
$V_{CE(on\text{-}sense)}$	no	no	yes	yes	good	medium
$V_{CE(on\text{-}load)}$	yes	yes	no	yes	good	medium
V_{Miller}	yes	yes	no	yes	medium	high
di/dt_max	no	yes	yes	no	low	high

T_j | determination

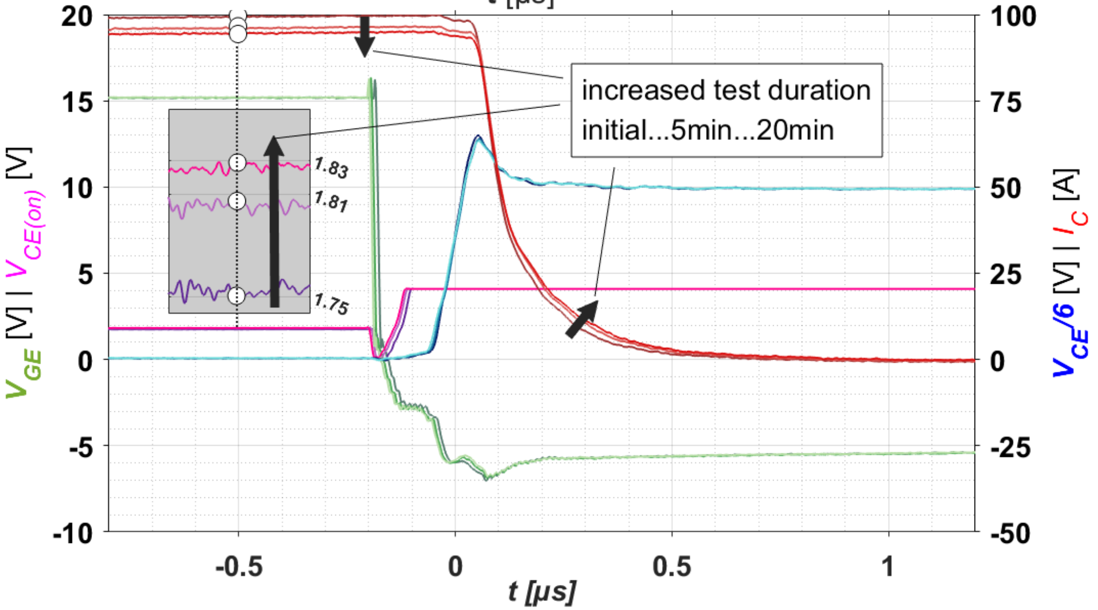
Calib.

Step 1



Rep.

Step 2



$I_{C(calib)}$ = [90 ··· 100]

with 0.1 A increment

Each scaled $I_{C(calib)}$

$V_{CE(on)} = A \cdot T_{j(calib)} + B$

uniform time point t = -0.5 µs

$\boldsymbol{I_{C(rep)}}$ | $\boldsymbol{V_{CE(on\text{-}rep)}}$

A* | *B

substitute into $\boldsymbol{V_{CE(on\text{-}rep)}}$

➢ $\boldsymbol{T_{j(rep)}}$

Bond-wire cut

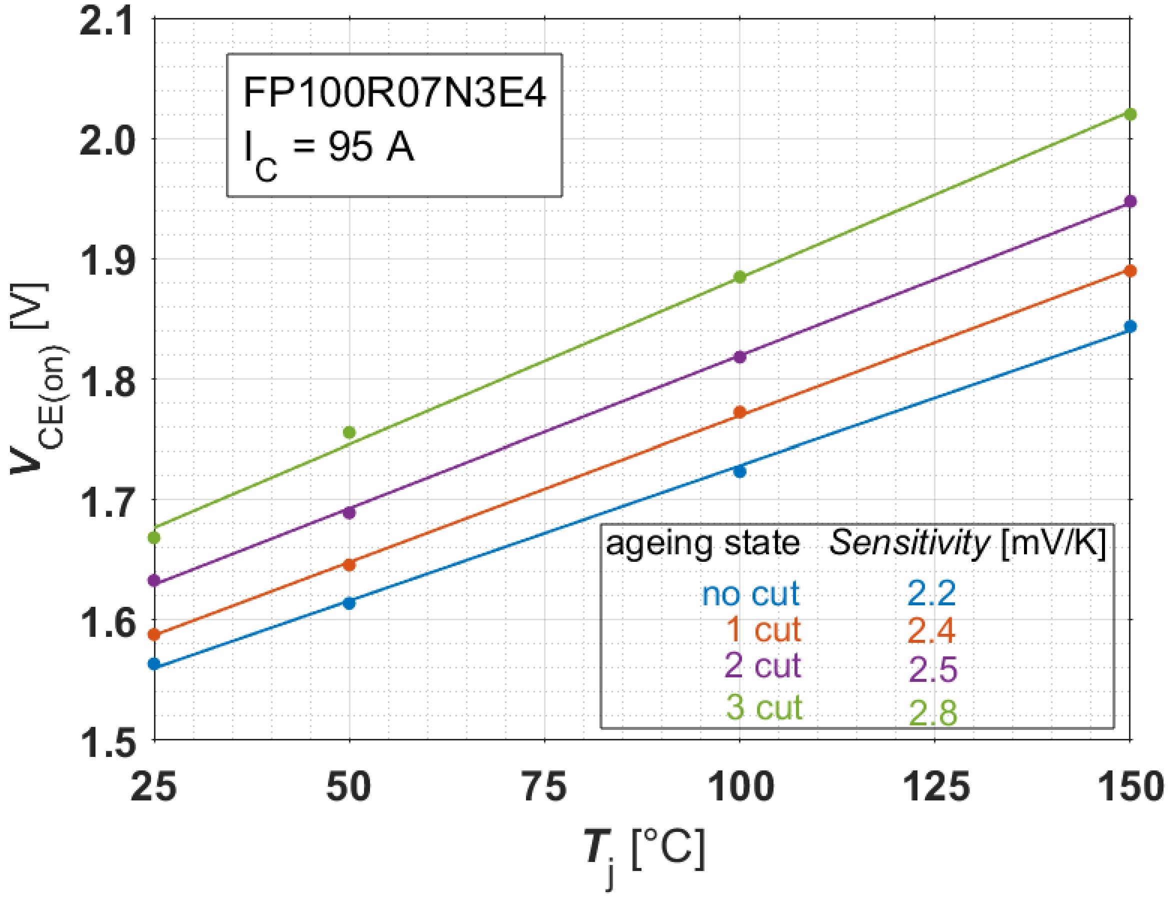
Step 3

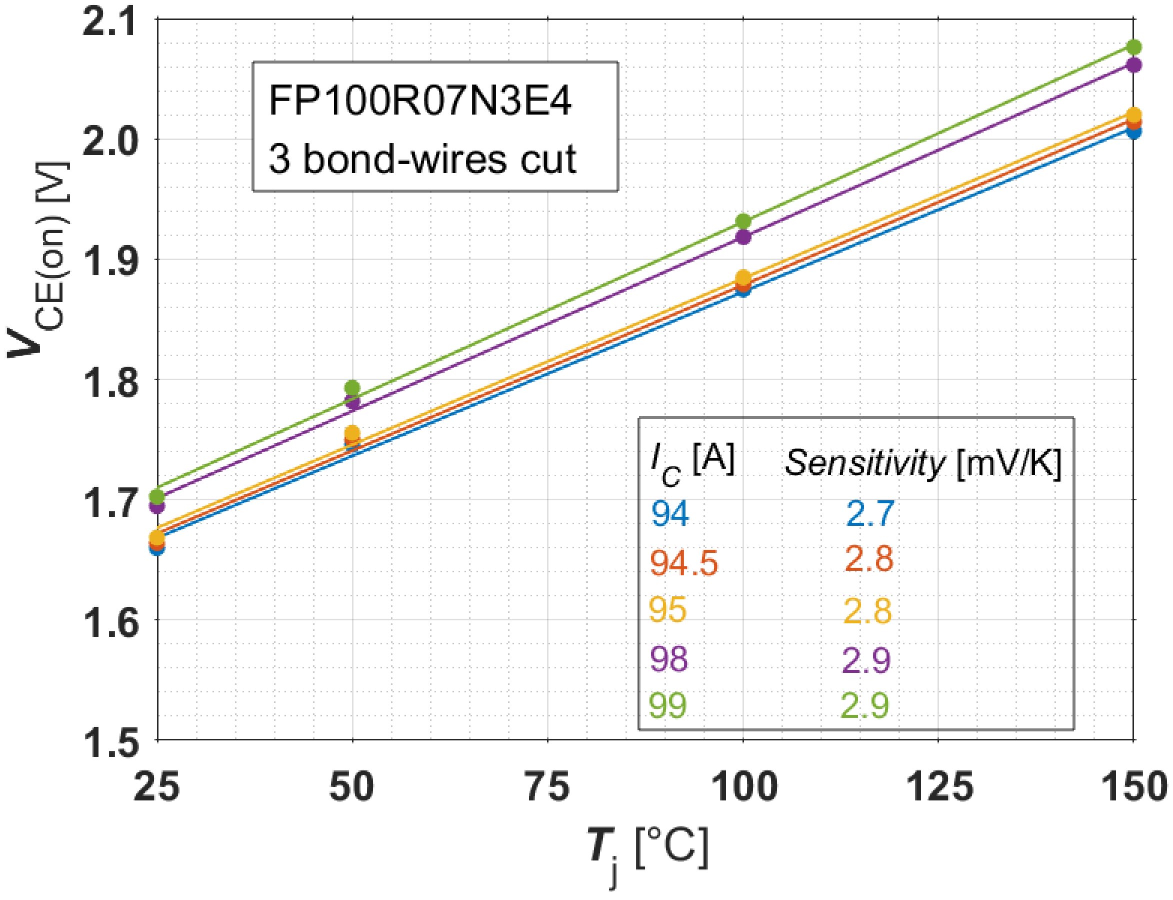
- repeat step 1 & 2

T_j | TSEP | dependency of $V_{CE(on)}$

Ageing ➢recalibration

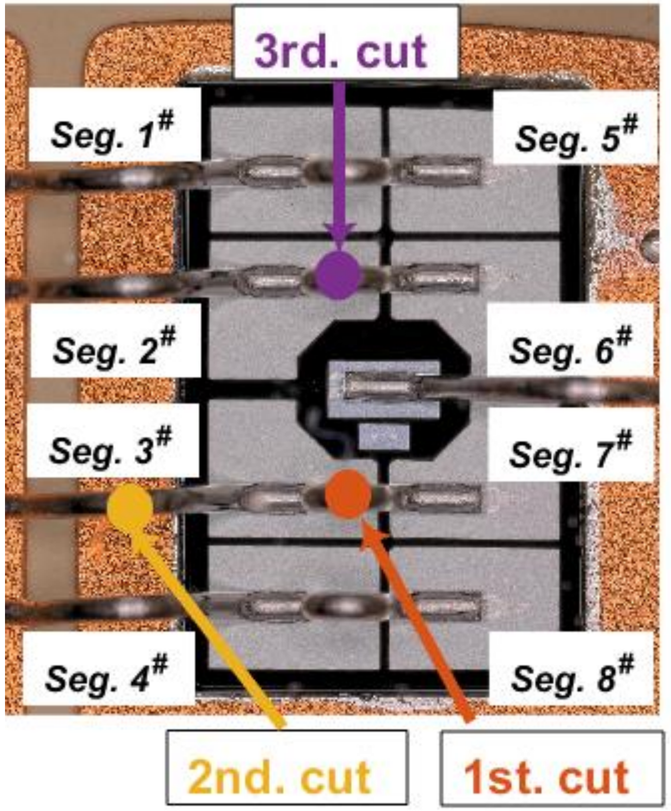
I_C ➢ calibration matrix



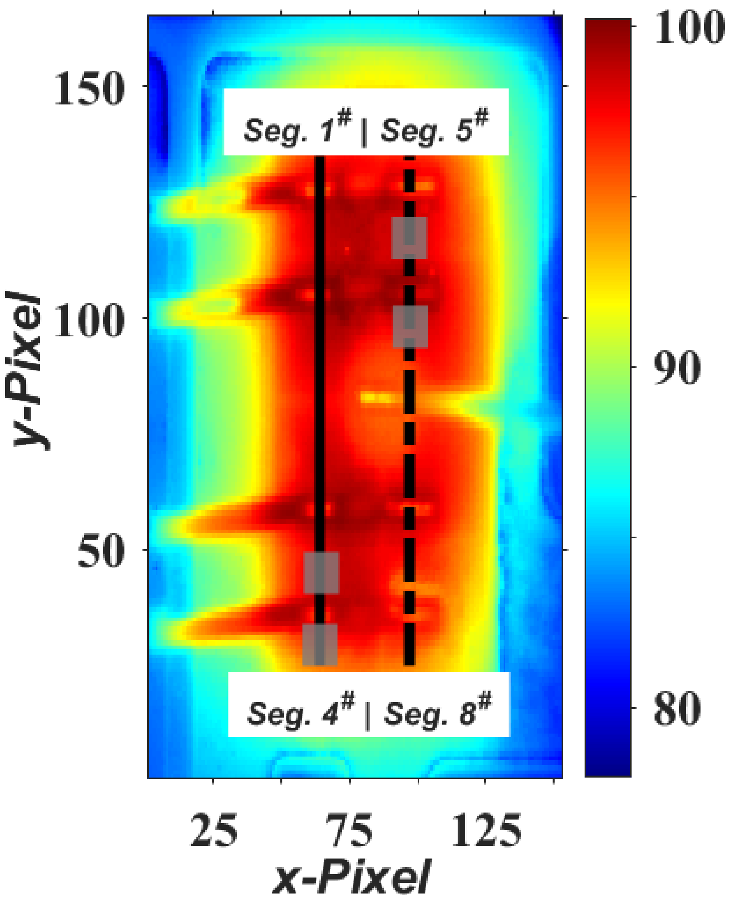


$T_{surface}$

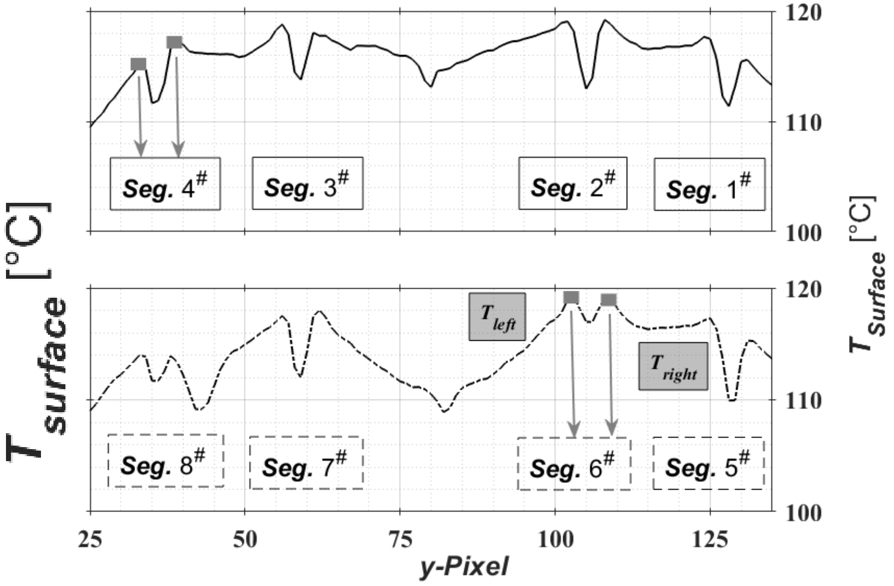
Segmentation | Cut chronology



IR-image (no cut | f = 500 Hz)



$T_{segment}$

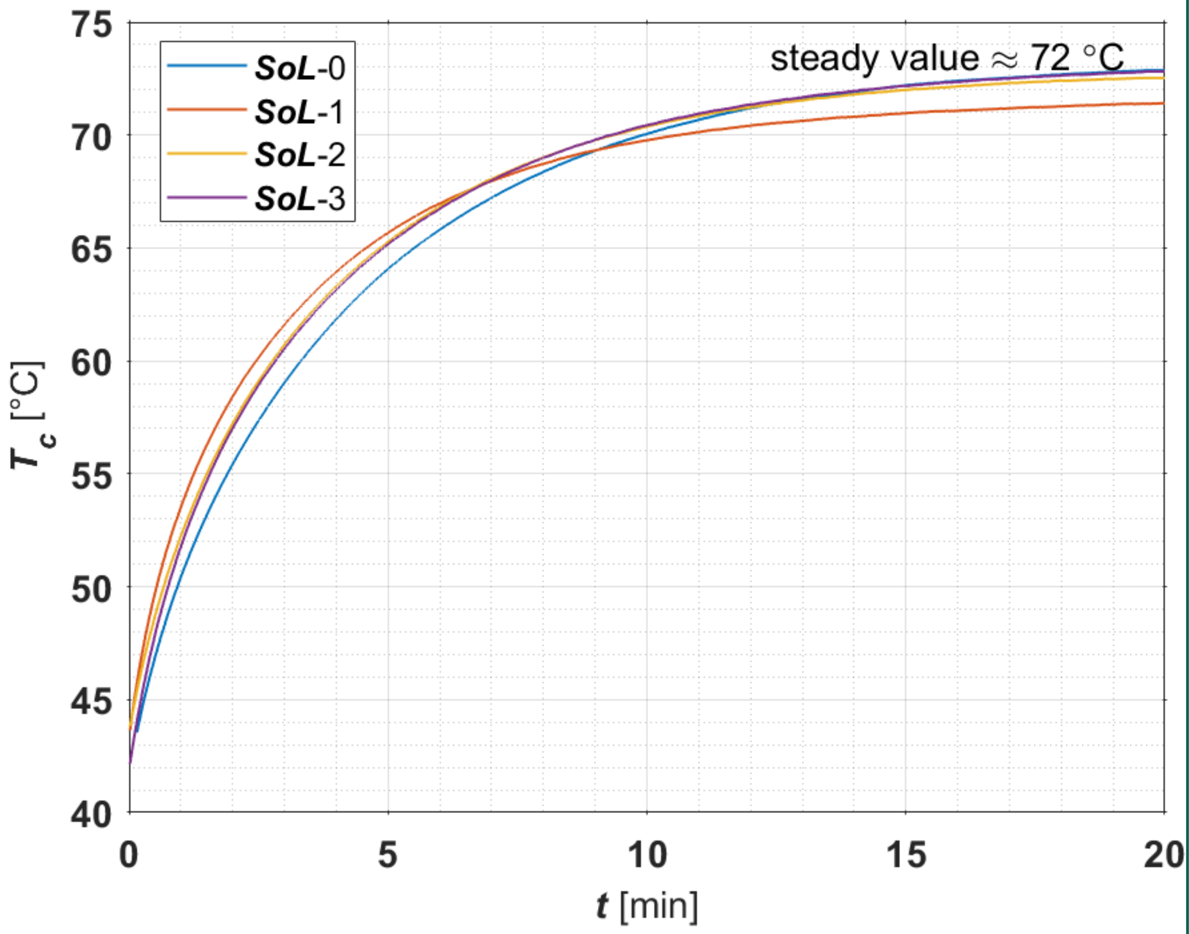


$$T_{segment} = (T_{left} + T_{right})/2$$

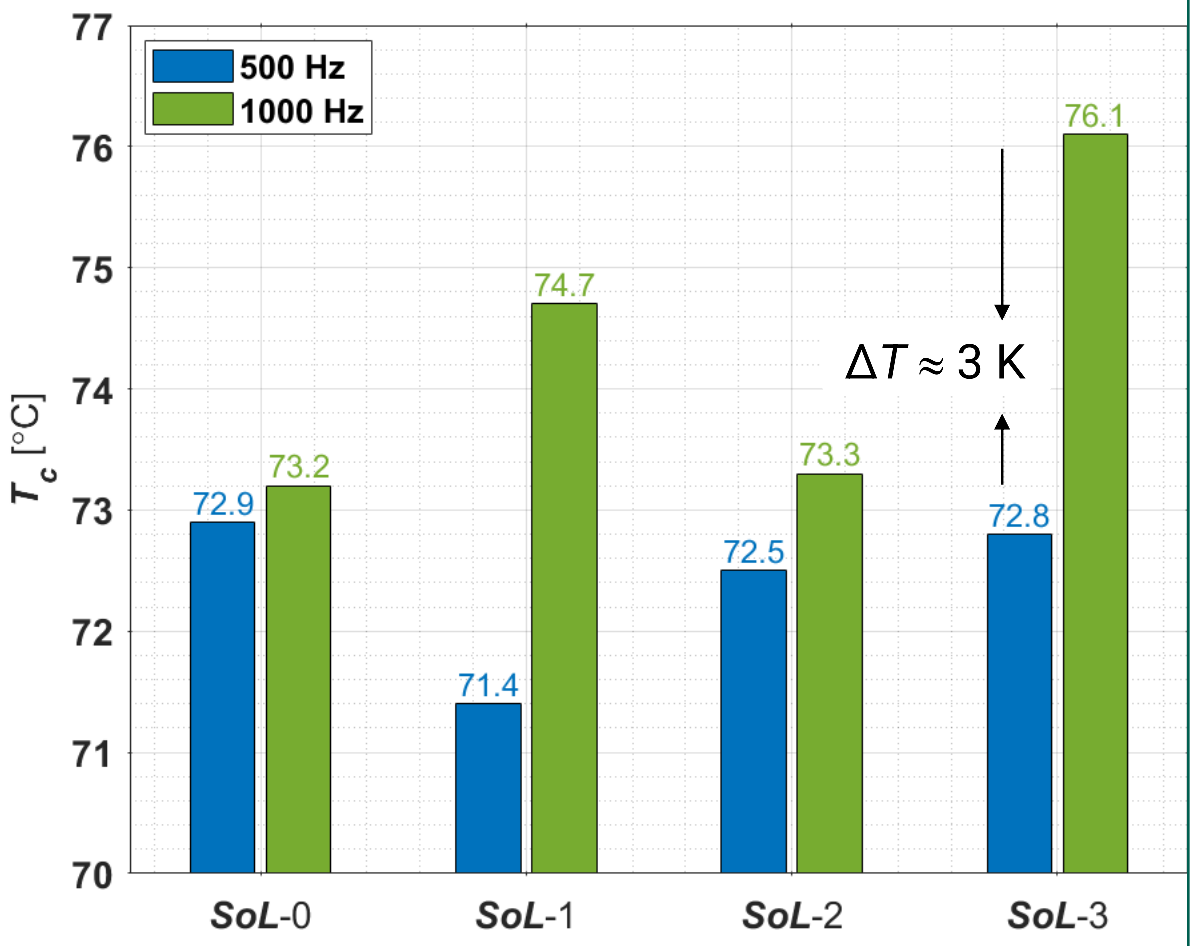
Outline

T_c

Development with f = 500 Hz

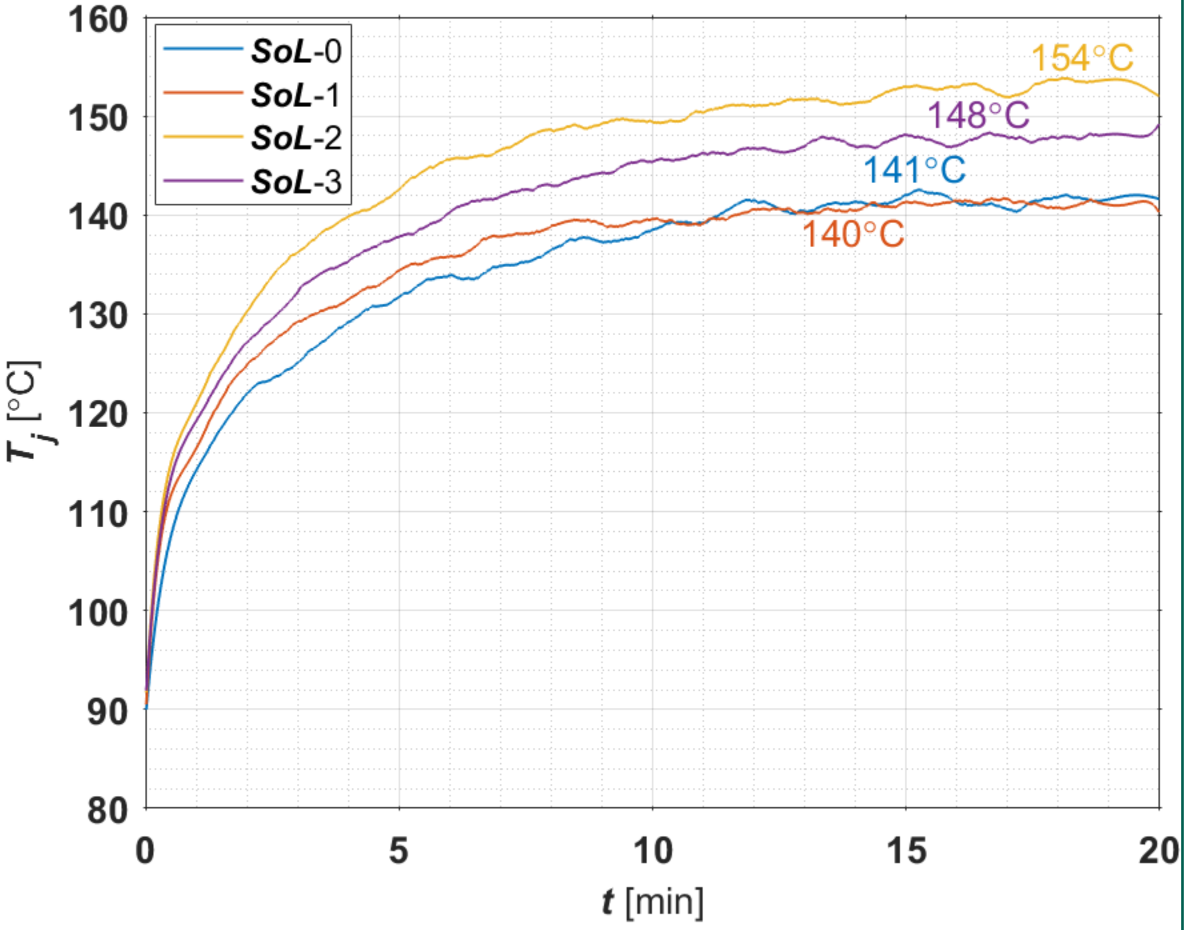


Comparison with 1000 Hz

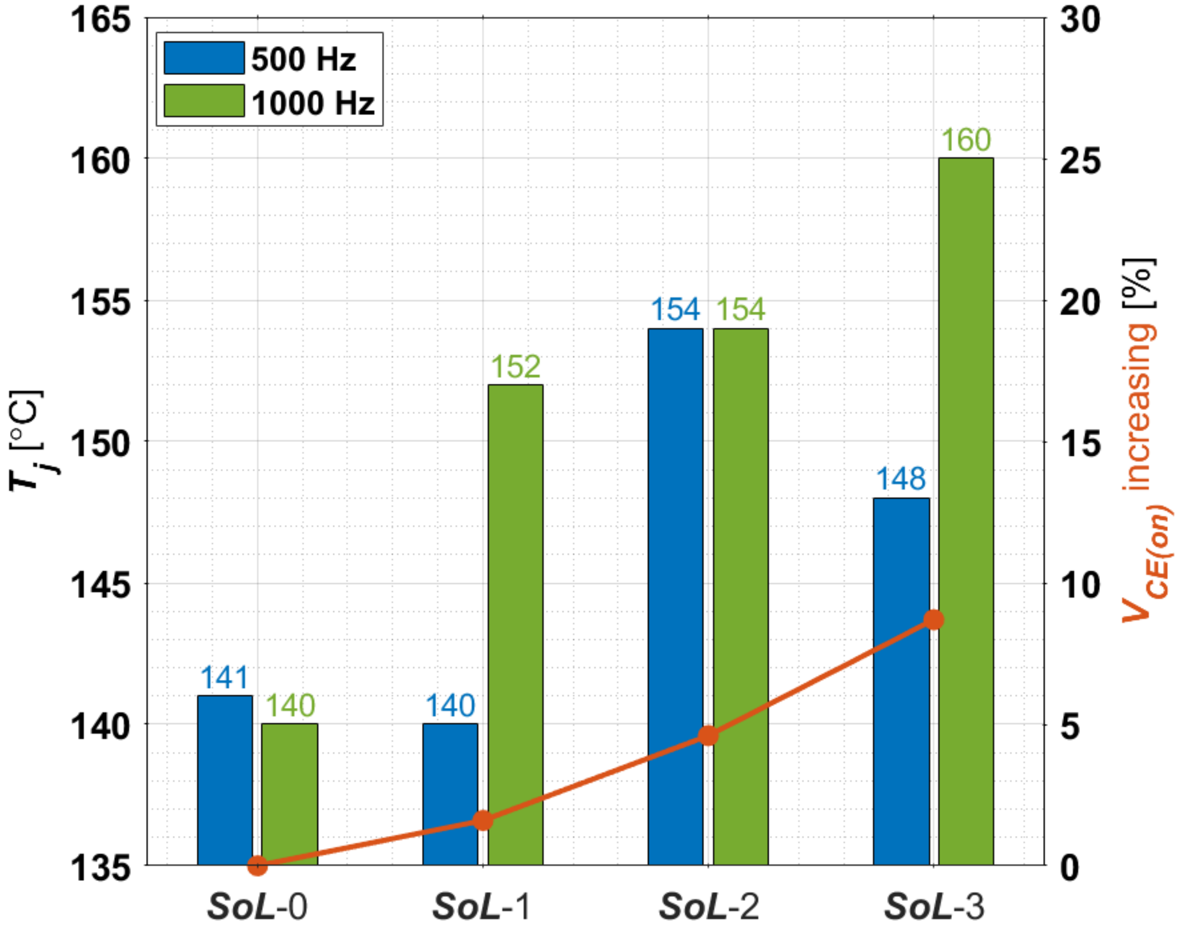


T_j

Development with f = 500 Hz

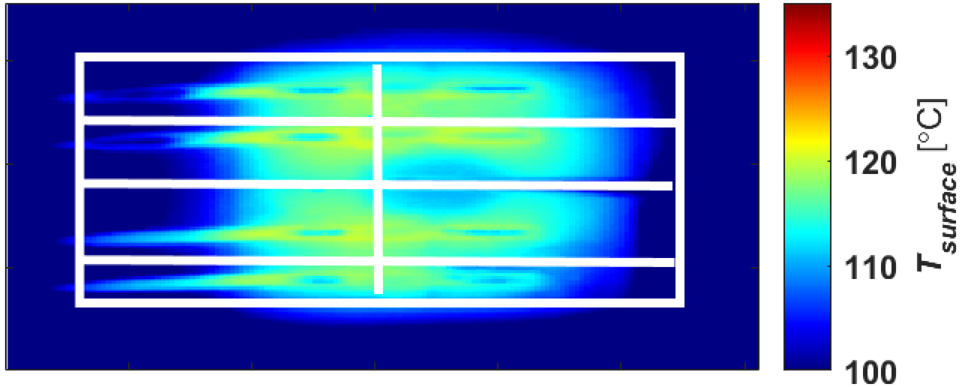


Comparison with 1000 Hz

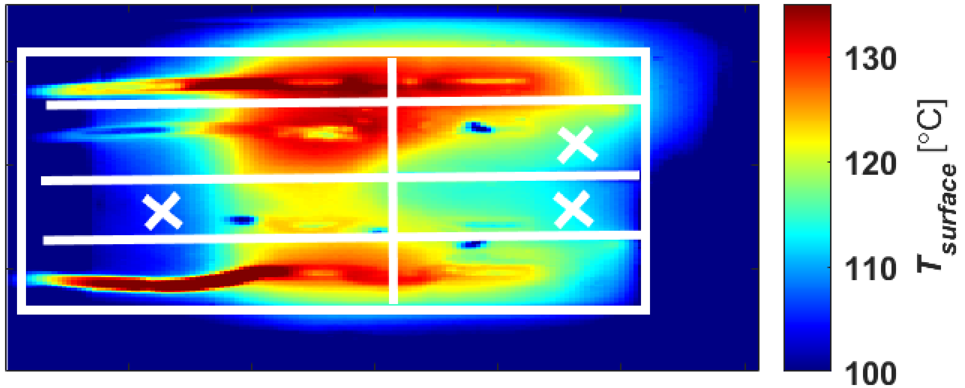


$T_{surface}$ | with f = 500 Hz

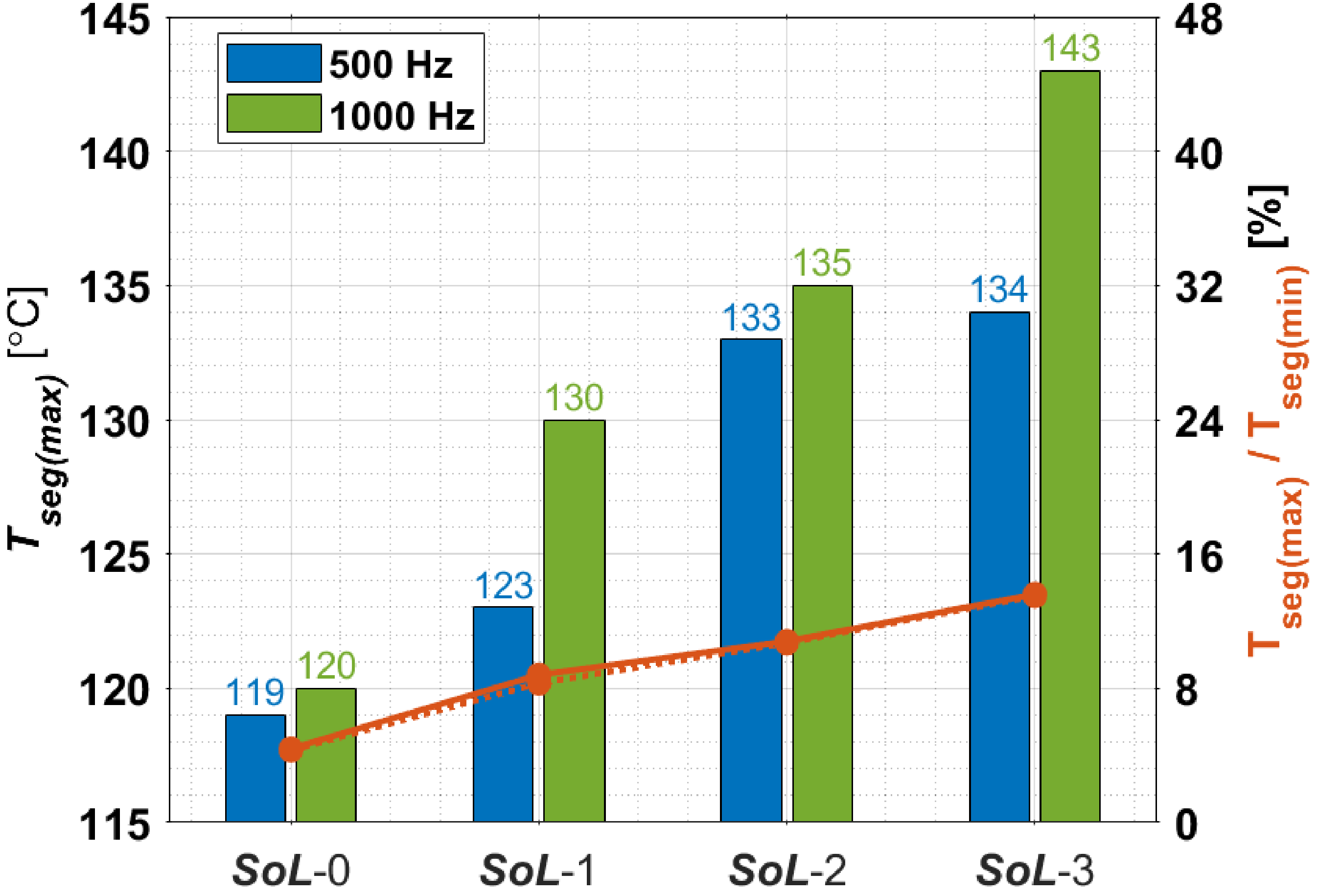
SoL-0



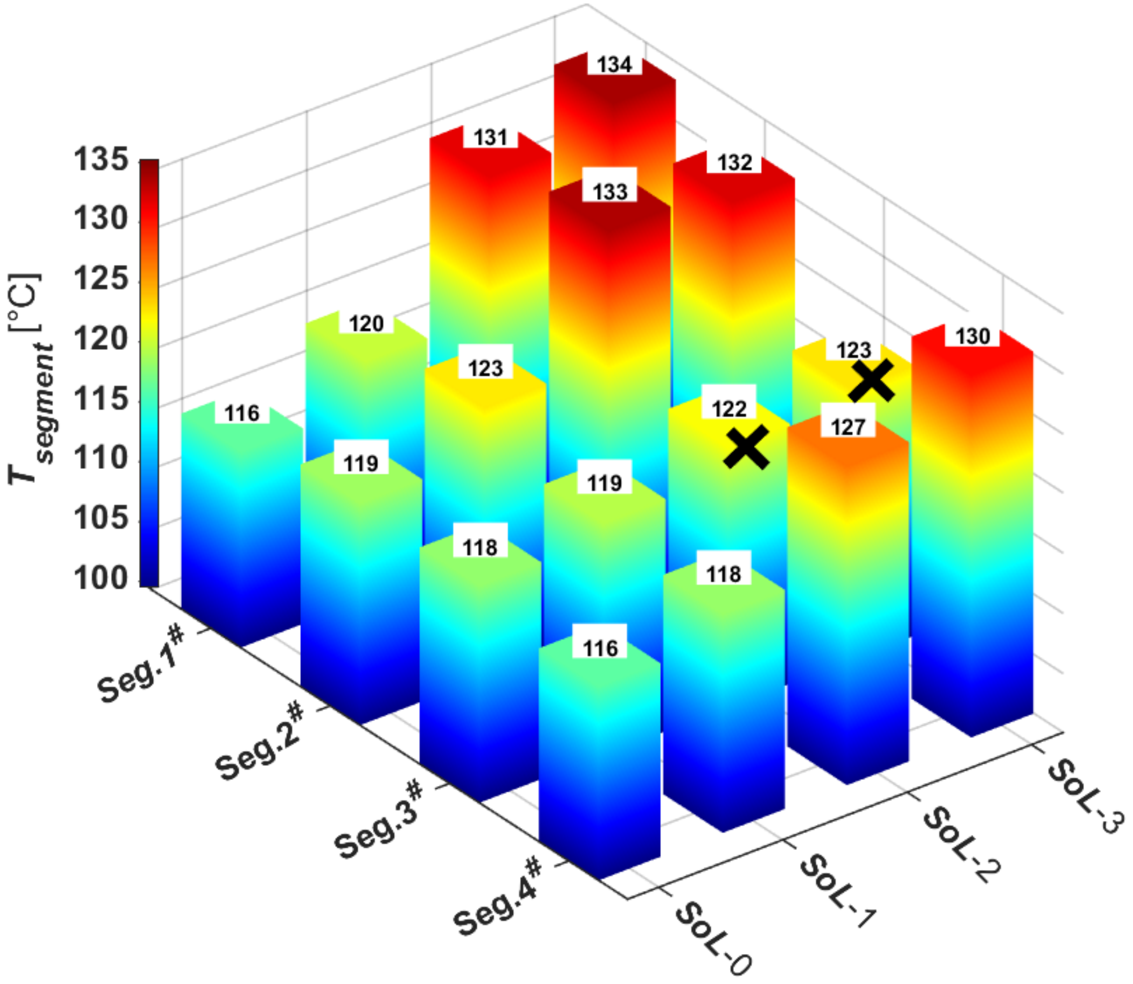
SoL-3

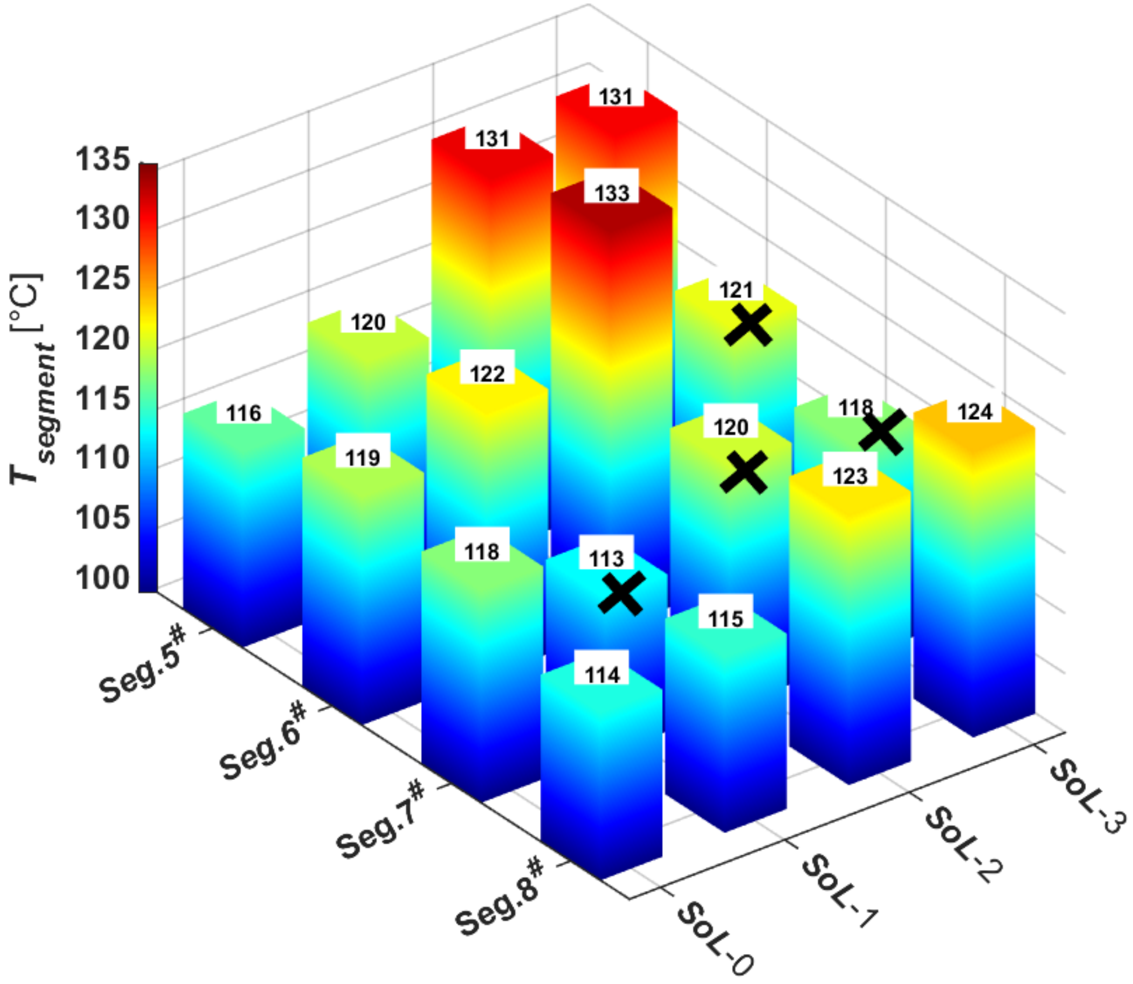


Comparison of $T_{seg(max)}$ with 1000 Hz & temperature inhomogeneity



$T_{segment}$ | overview with f = 500 Hz





Outline

Summary & Outlook

Summary

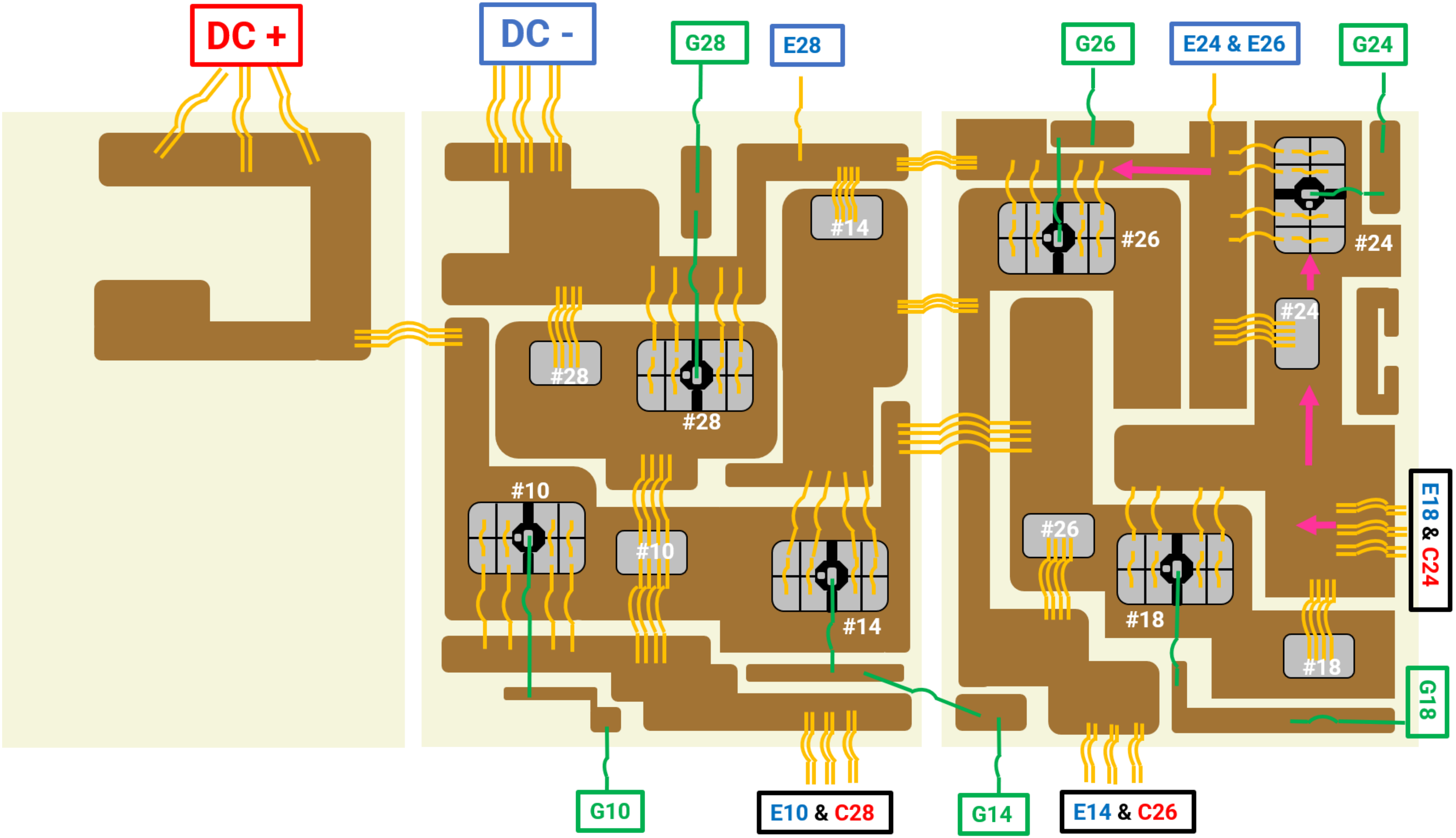
- Repetitive operation
  - ➢ a specified pulse pattern which is more like an inverter in the application approached
- Junction temperature determination
  - ➢ an investigation with respect to various TSEP
- T_c
  - ➢ no obvious variation could be extracted
- T_j & $T_{segment}$
  - ➢ significantly affected by ageing & f
  - ➢ ageing → inhomogeneity of temperature distribution ↑

Outlook

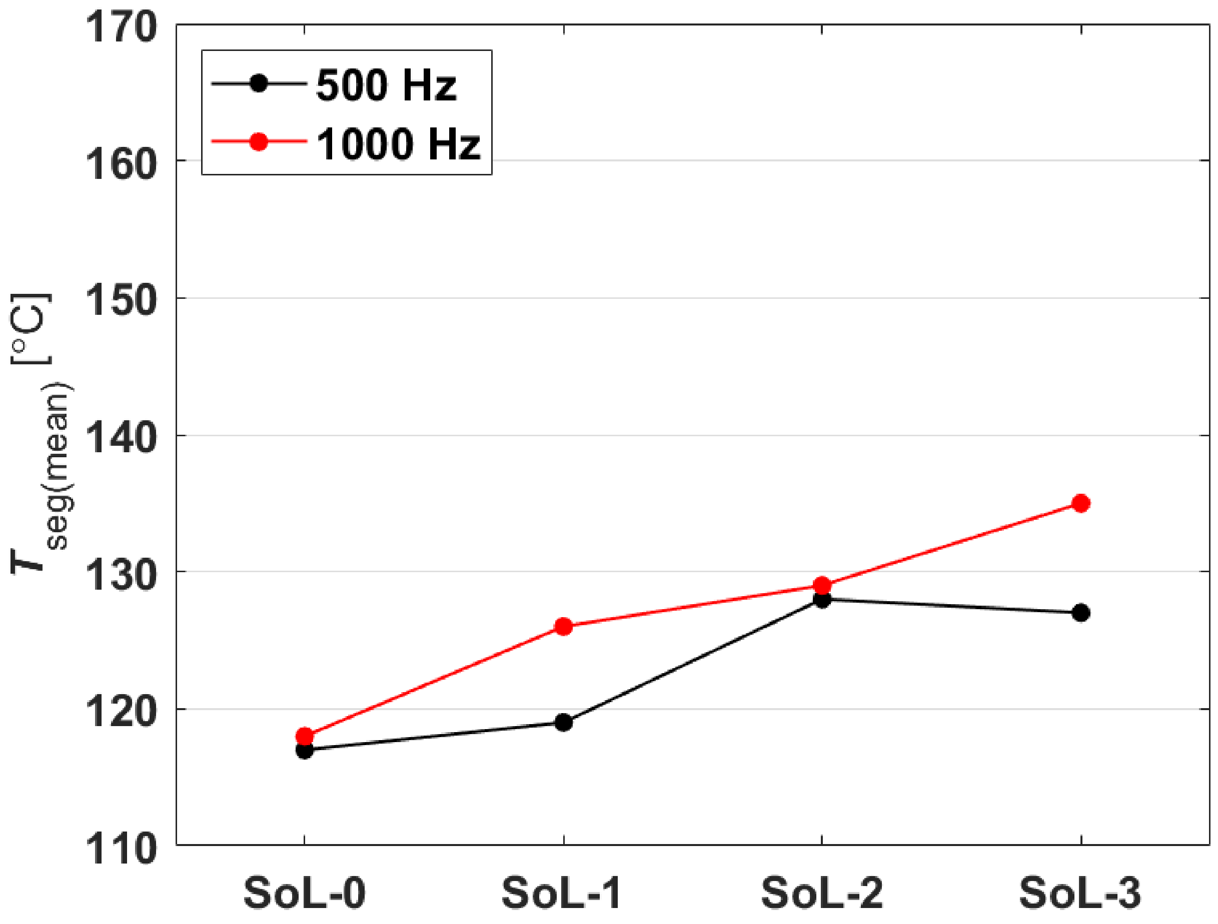
- DCB chip as DUT
  - ➢ Kelvin contact available
- dynamic pulse pattern
  - ➢ $I_{C(rep\text{-}mean)}$ ↑
- synchronization of thermocouple & IR-camera with pulse pattern
  - ➢ comparable T_j , T_c & $T_{segment}$
- $V_{CE(on\text{-}load)}$ → mean value of T_j?
  - ➢ FEM simulation
- bond-wire cut → power cycling
  - ➢ reconstruction of metallization

Thank you for your attention

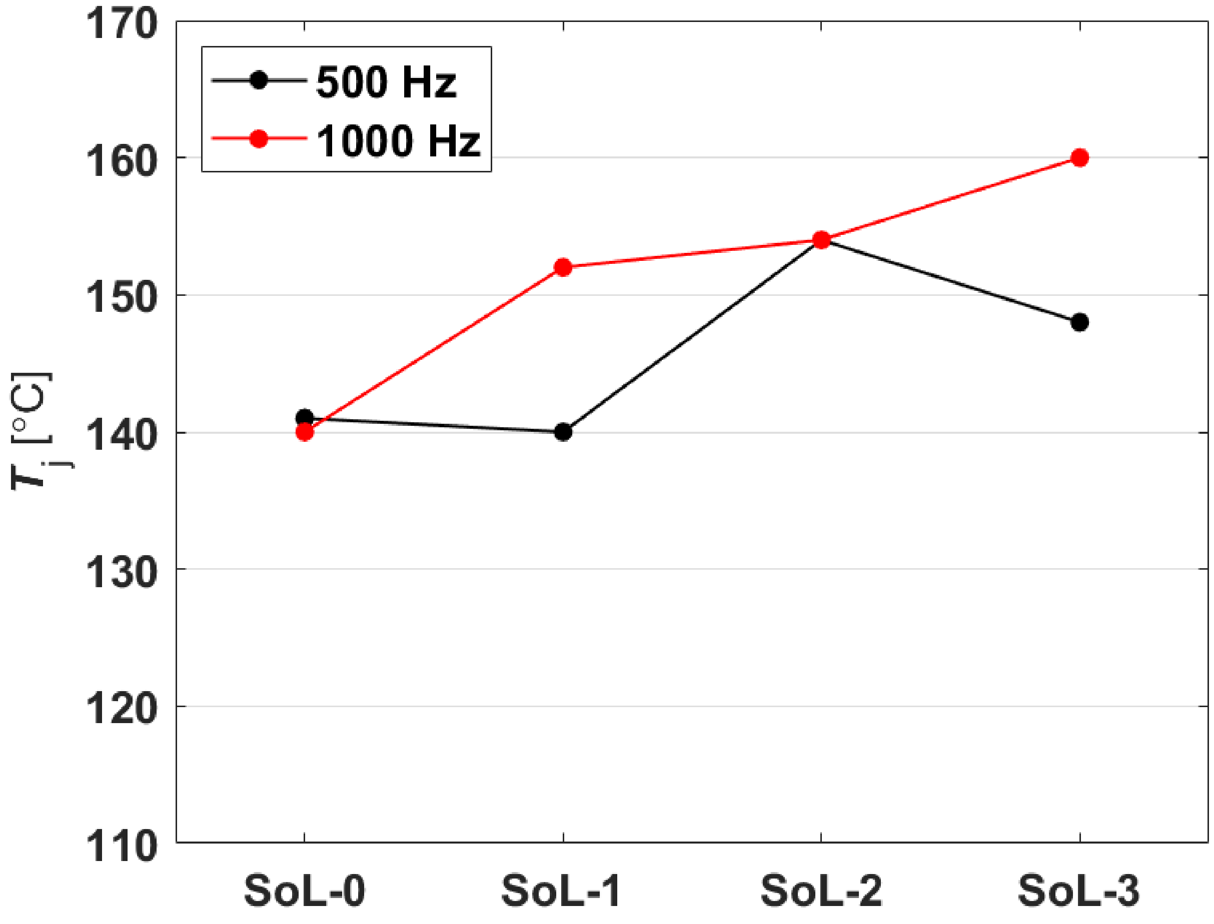
DUT | Layout


DC +
DC -
G28
E28
G26
E24 & E26
G24
#14
#26
#24
#24
#28
#28
#10
#10
#14
#26
#18
#18
E18 & C24
G18
G10
E10 & C28
G14
E14 & C26

$T_{seg(mean)}$ & T_j

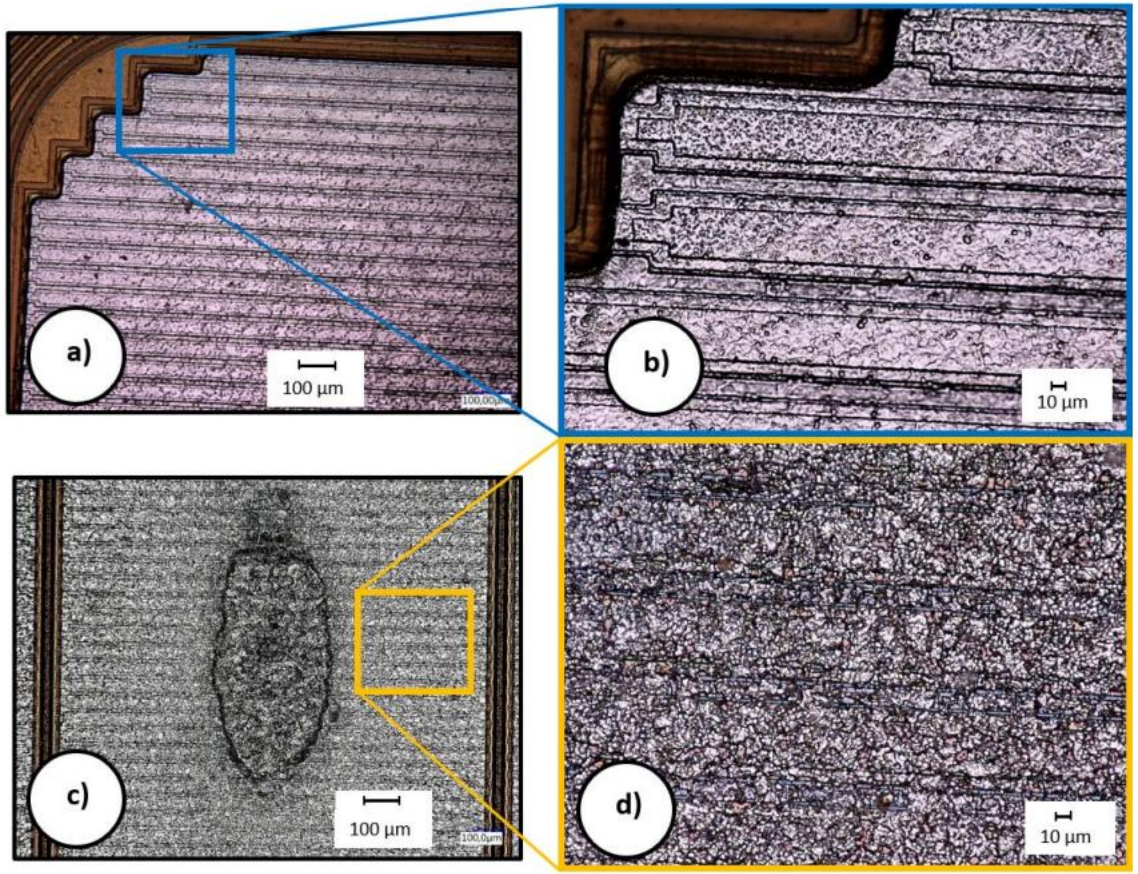


500 Hz
1000 Hz
170
160
150
140
130
120
110
T seg(mean) [°C]
SoL-0
SoL-1
SoL-2
SoL-3



500 Hz
1000 Hz
170
160
150
140
130
120
110
T j [°C]
SoL-0
SoL-1
SoL-2
SoL-3

Emitter surface of IGBT after power cycling test

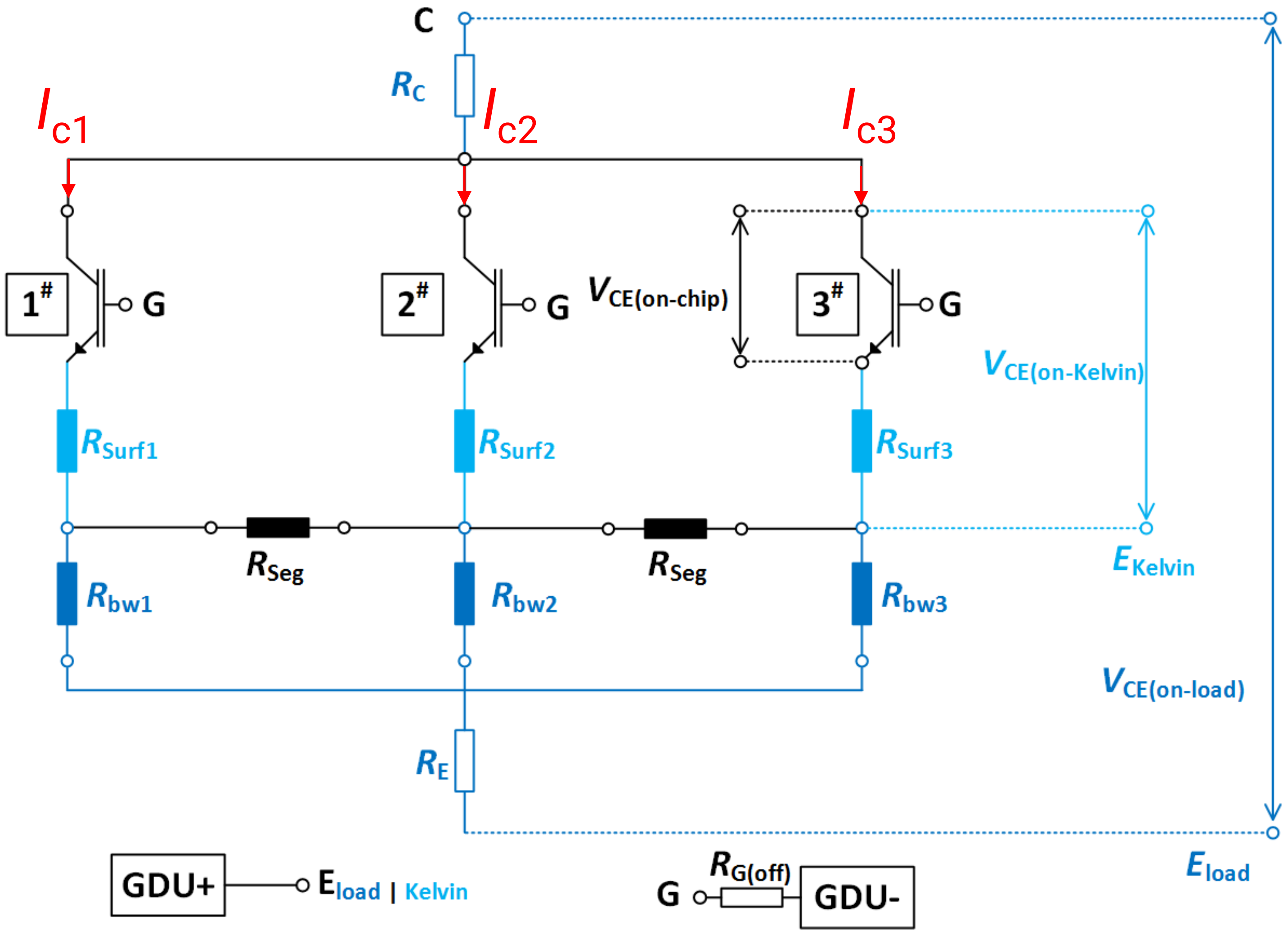


Aluminum reconstruction of the chip surface for different areas [1]:

a) edge area with 200 mm zoom
b) edge area with 1000 mm zoom
c) center area with 200 mm zoom
d) center area with1000 mm zoom

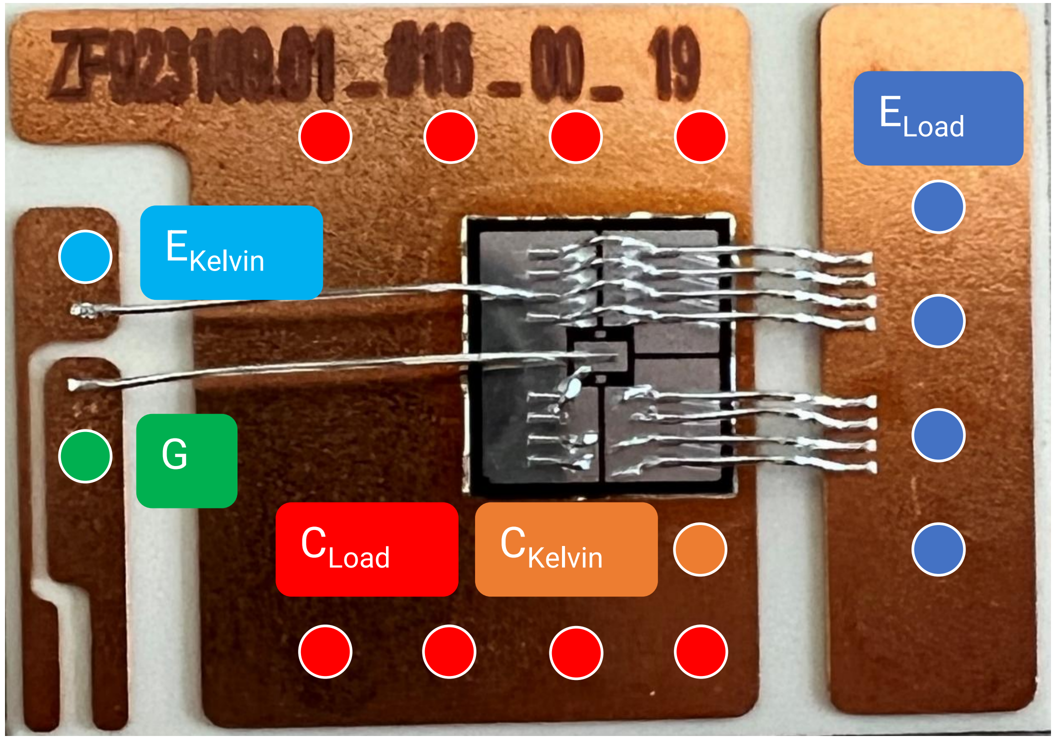
[1] Bäumler, C., Hernes, M., Kowalsky, J., & Lutz, J. Short Circuit Robustness of an Aged High Power IGBT-Module. *In 2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)* (pp. P-1). September 2019. IEEE.

Modelling of segment | all bond-wire intact

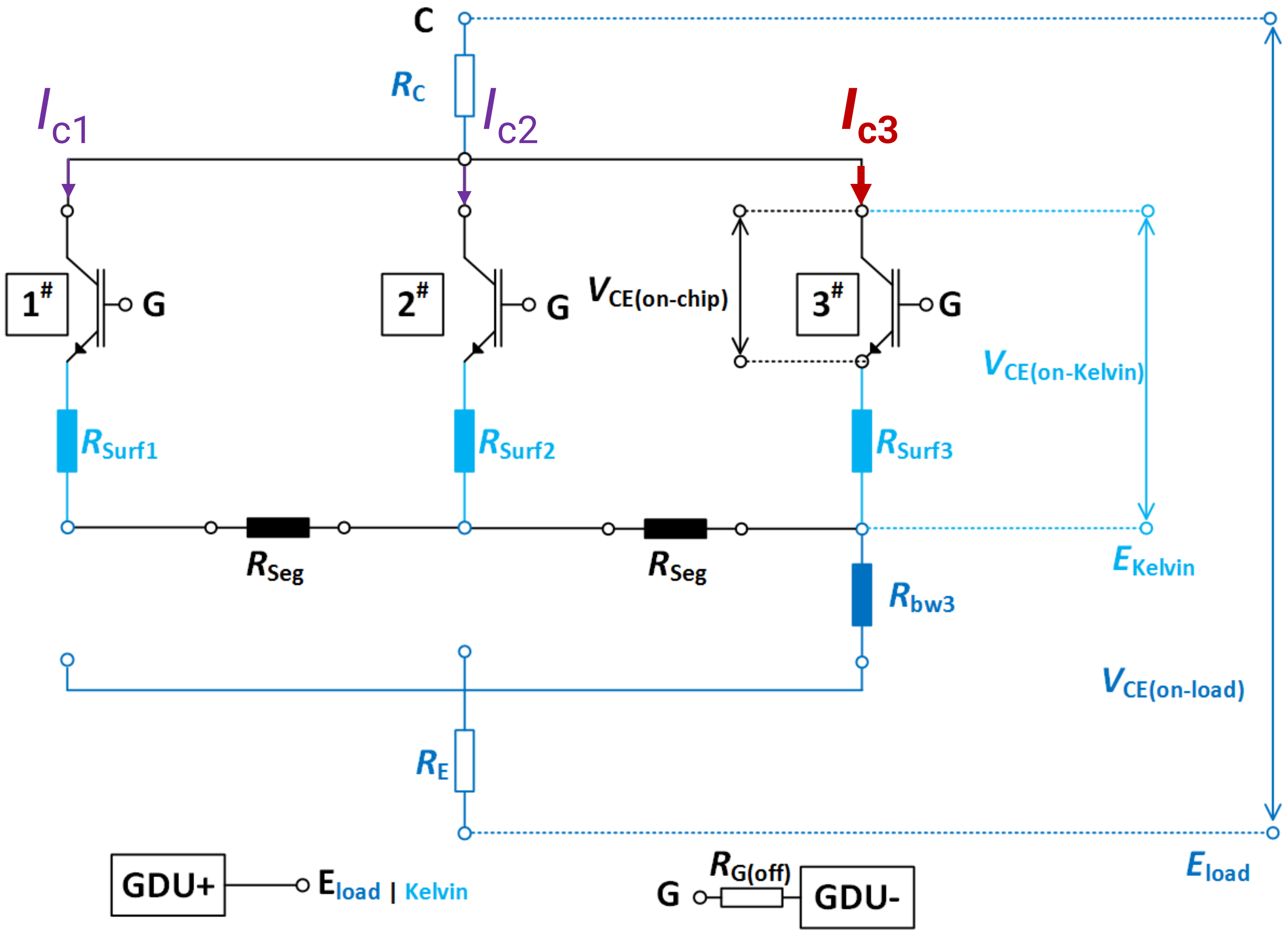


$$I_{c1} = I_{c2} = I_{c3}$$

$$I_{Load} = I_{c1} + I_{c2} + I_{c3} = \text{const.}$$

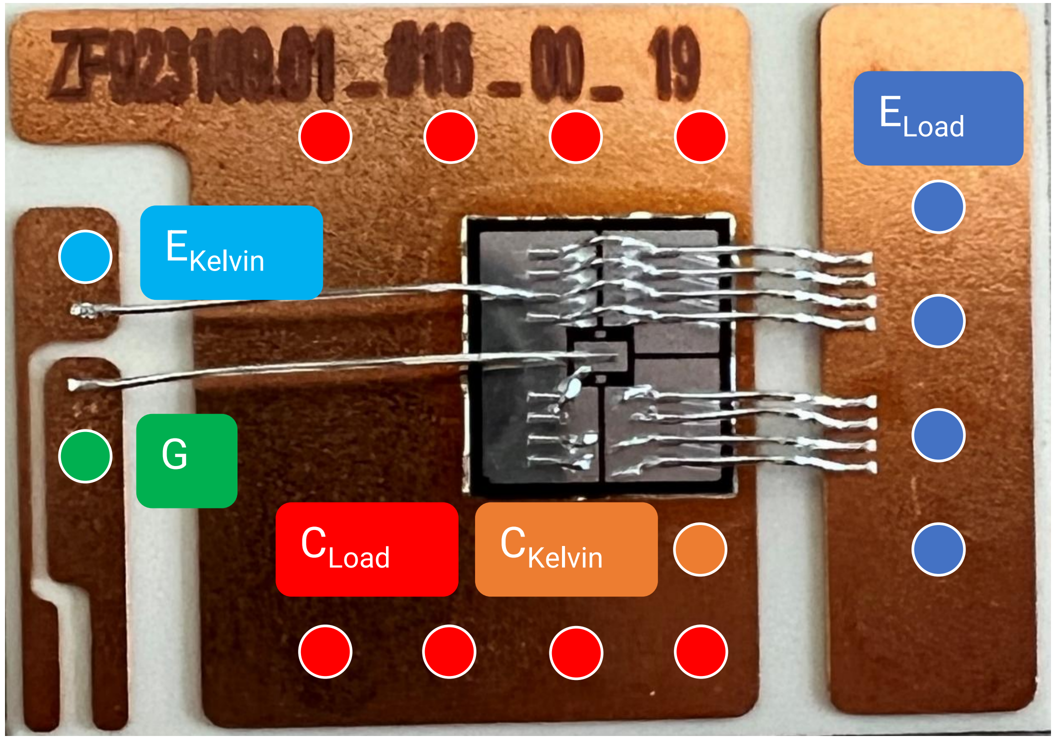


Modelling of segment | bond-wire 3 intact, 1 & 2 defect

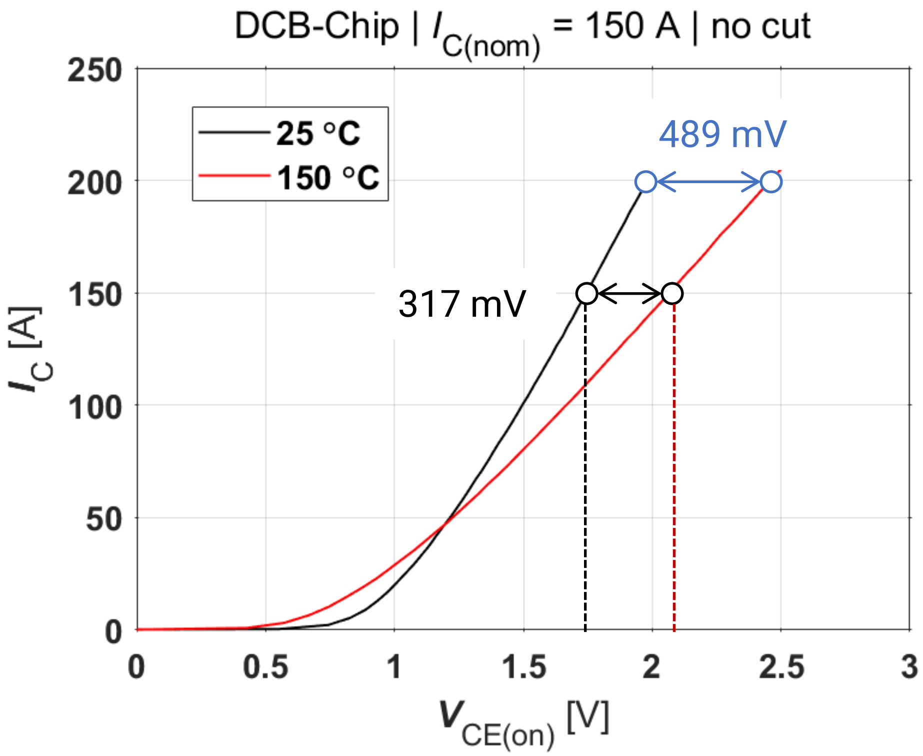


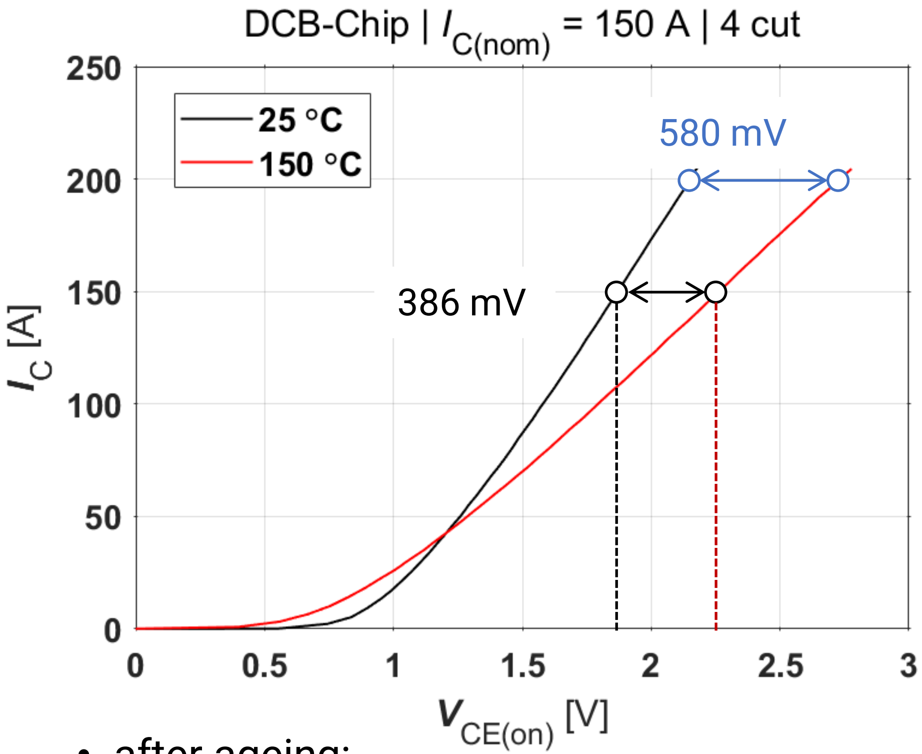
$I_{c3} > I_{c1}$ & I_{c2}

$I_{Load} = I_{c1} + I_{c2} + I_{c3} = \text{const.}$



Dependency of $V_{CE(on)}$ on ageing | DCB chip





Bond-wire state		no cut	2cut	4 cut
Sensitivty [mv/K]	Kelvin	2.5	2.6	2.9
	Load	2.8	3.0	3.2
Offset [V]	Kelvin	1.71	1.73	1.83
	Load	1.76	1.78	1.89

- after ageing:
  - ➢ fixed T & I_C → $V_{CE(on)}$↑ → offset↑
  - ➢ fixed ΔT & I_C → more $V_{CE(on)}$↑ → sensitivity↑
- offset @ Load > Kelvin
  - ➢ voltage drop over R_{bw}
- sensitivity @ Load > Kelvin
  - ➢ R_{bw} is also temperature dependent