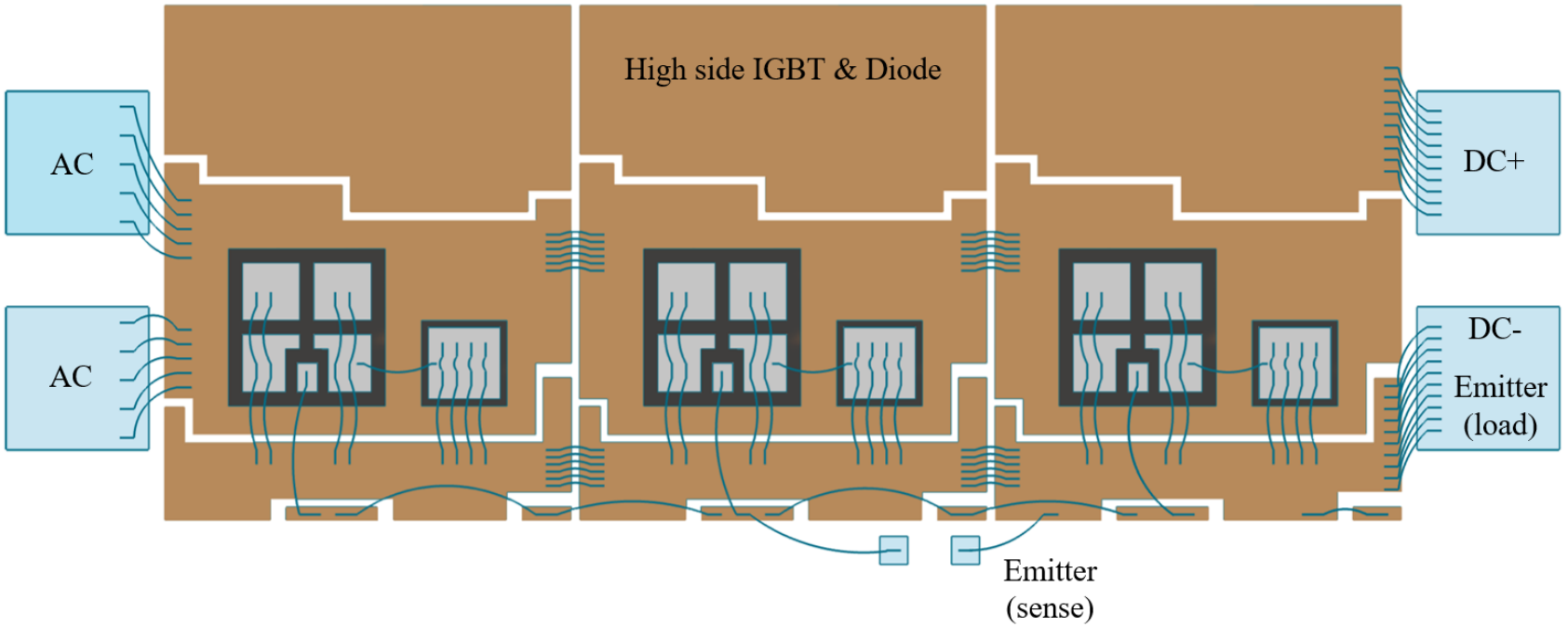
Investigation the influence of bond wire lift-off on the switching behavior of IGBT module

DUTs & Info.

- DUT FF225R17KE, 225A, 1.7kV
  3 IGBT chips parallel
  Each chip has 4 emitter segments
  Each segment 2 bonding foots

- Module layout shows following, only low side is tested

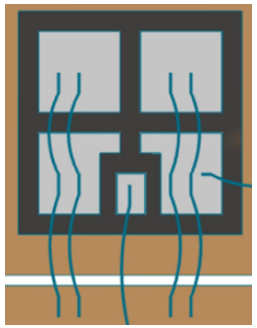


Test procedure

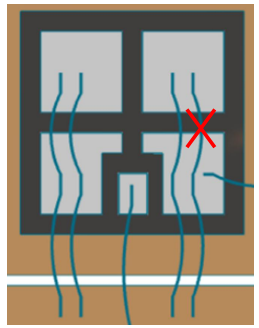
Double pluse test, $V_{ce,sat}$, $V_{G,th}$, C-V measurement up to 900 V

Cut bond wire to simulate the bond wire lift-off, 6 steps (S1 – S6)

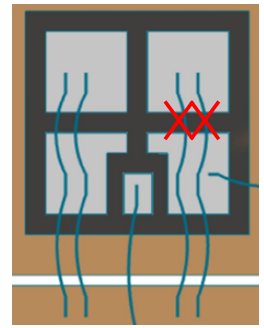
S1 (new module)



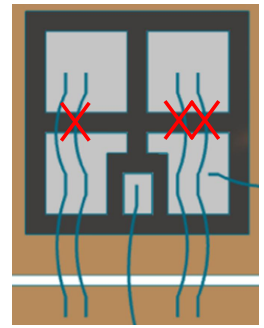
S2 cut 1 wire of each IGBT chip



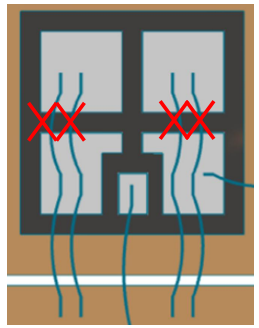
S3 cut 2 wires of each IGBT chip, ¼ area is „lossing“



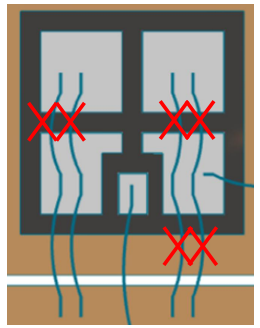
S4 cut 3 wires of each IGBT chip, ¼ area is „lossing“



S5 cut 4 wires of each IGBT chip, ½ area is „lossing“

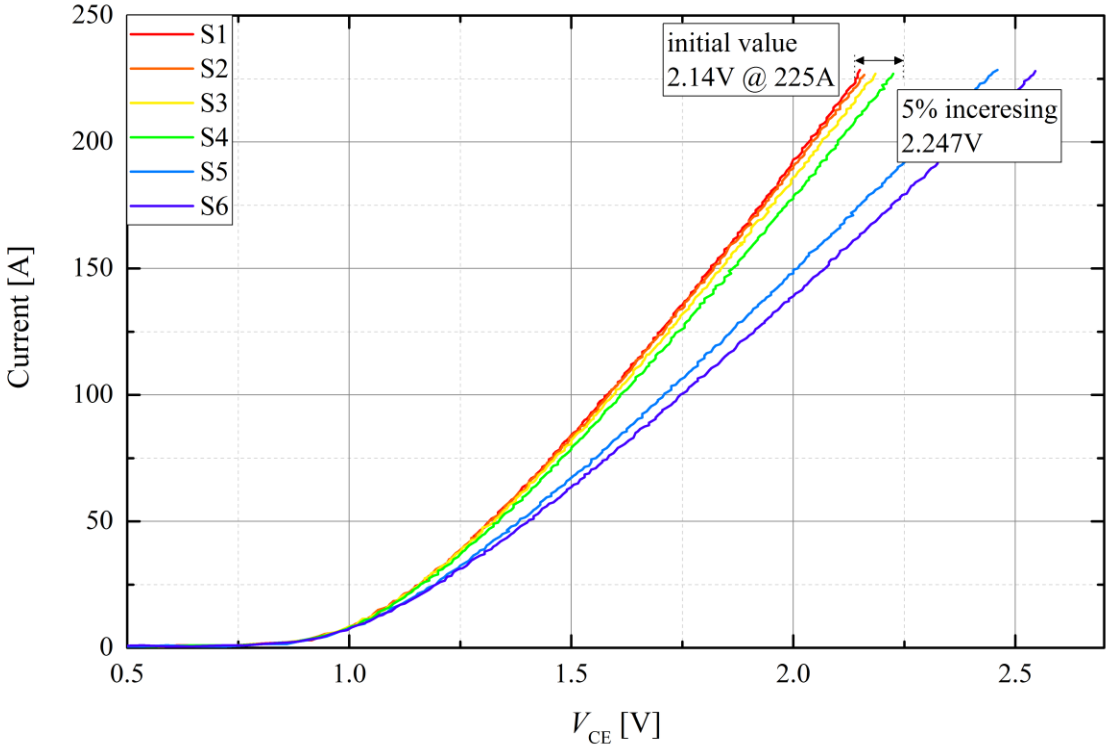


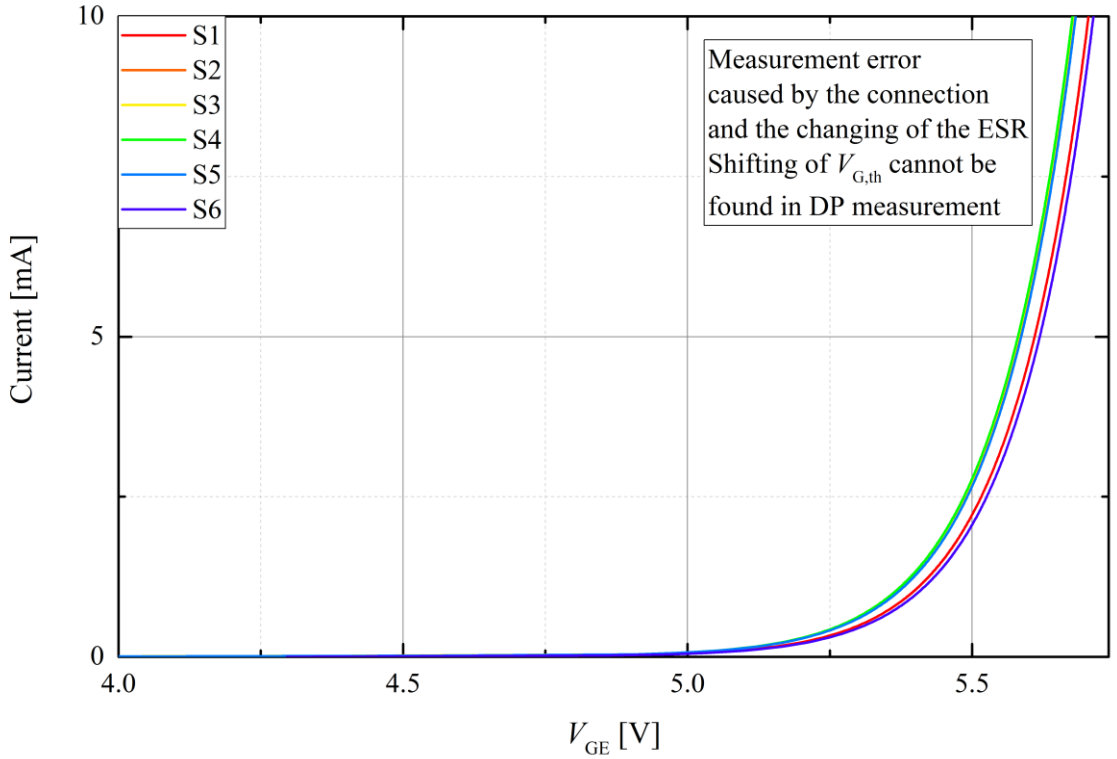
S6 cut 6 wires of each IGBT chip, ¾ area is „lossing“



Measurement results

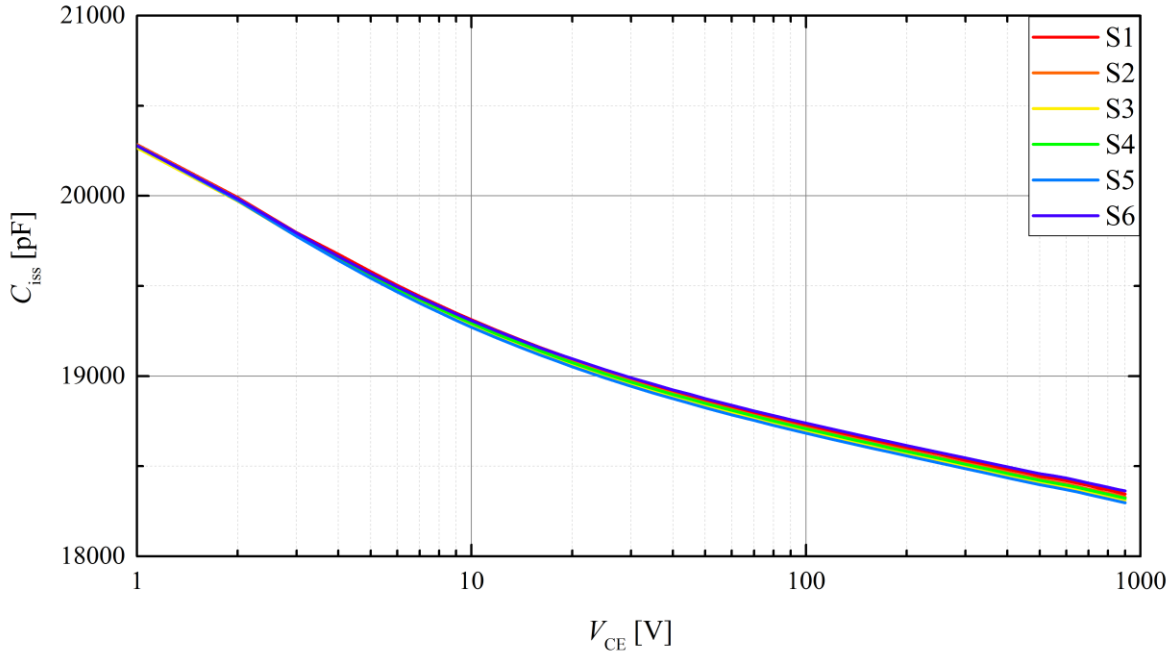
- $V_{CE,sat}$ and $V_{G,th}$

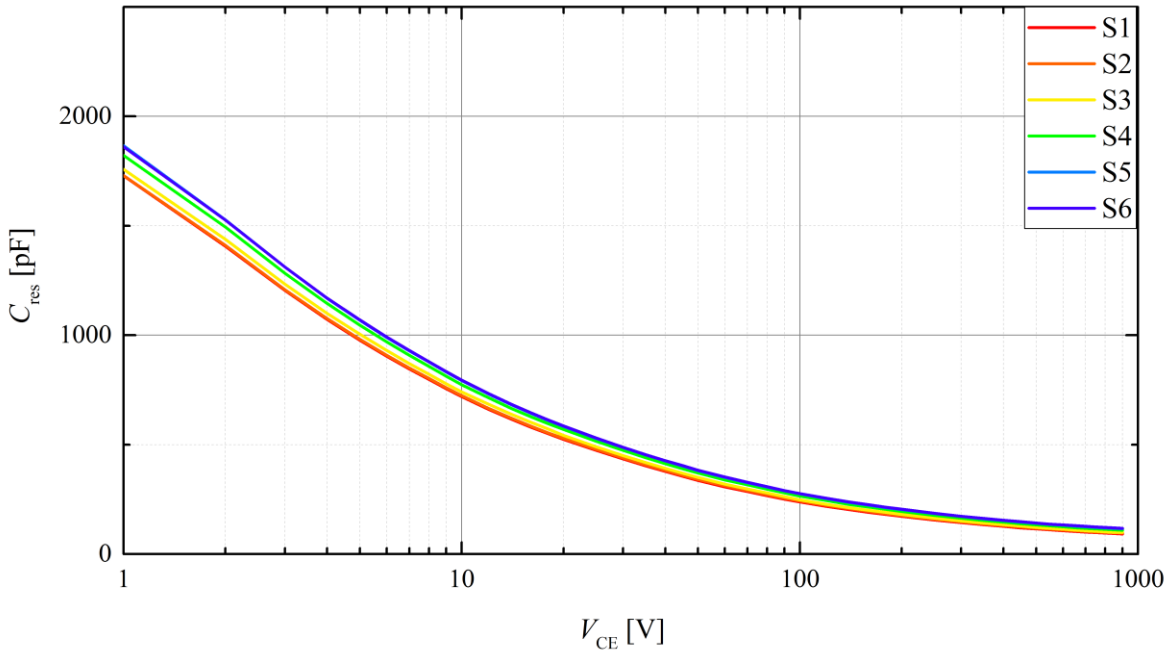




Measurement results

- C-V measurement

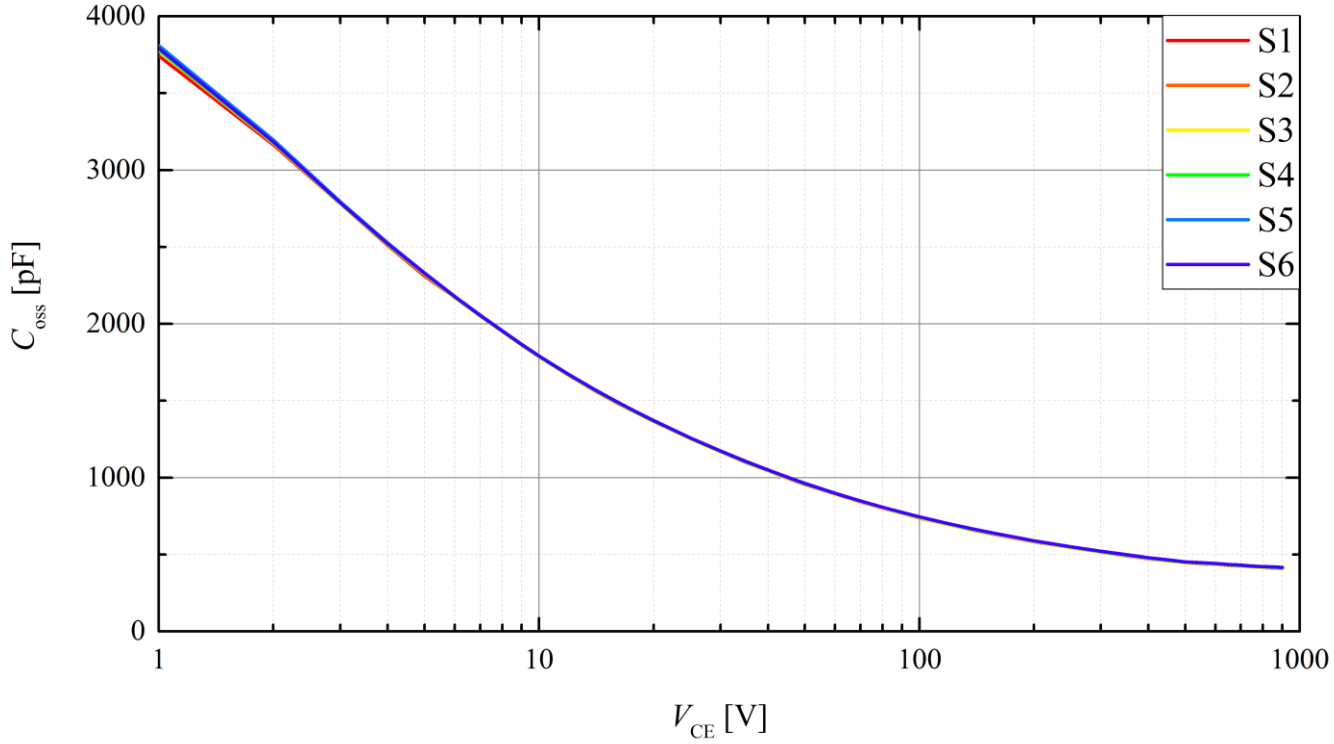




- The Ciss increases slightly at high voltage, which is due to the increased Miller capacitance. (the reason need to be discussed.. I don`t have it now in my mind… ☹)

Measurement results

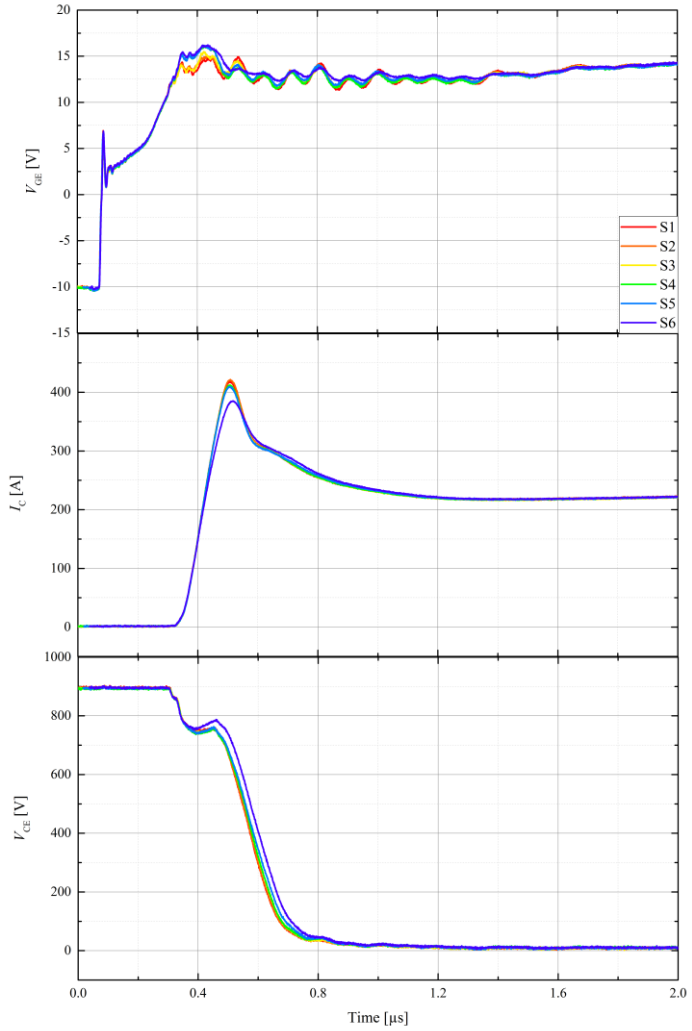
- C-V measurement

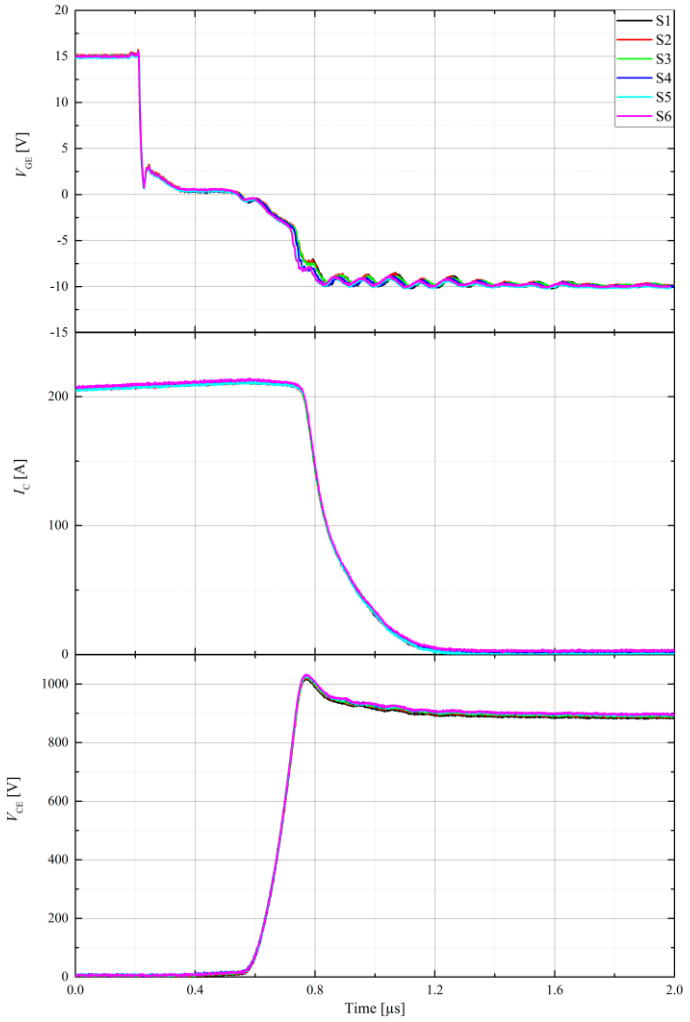


- No visiable change on the output capacitance

Measurement results

- Switching behavior (bigger figures are in word ☺)





For turn-ON:

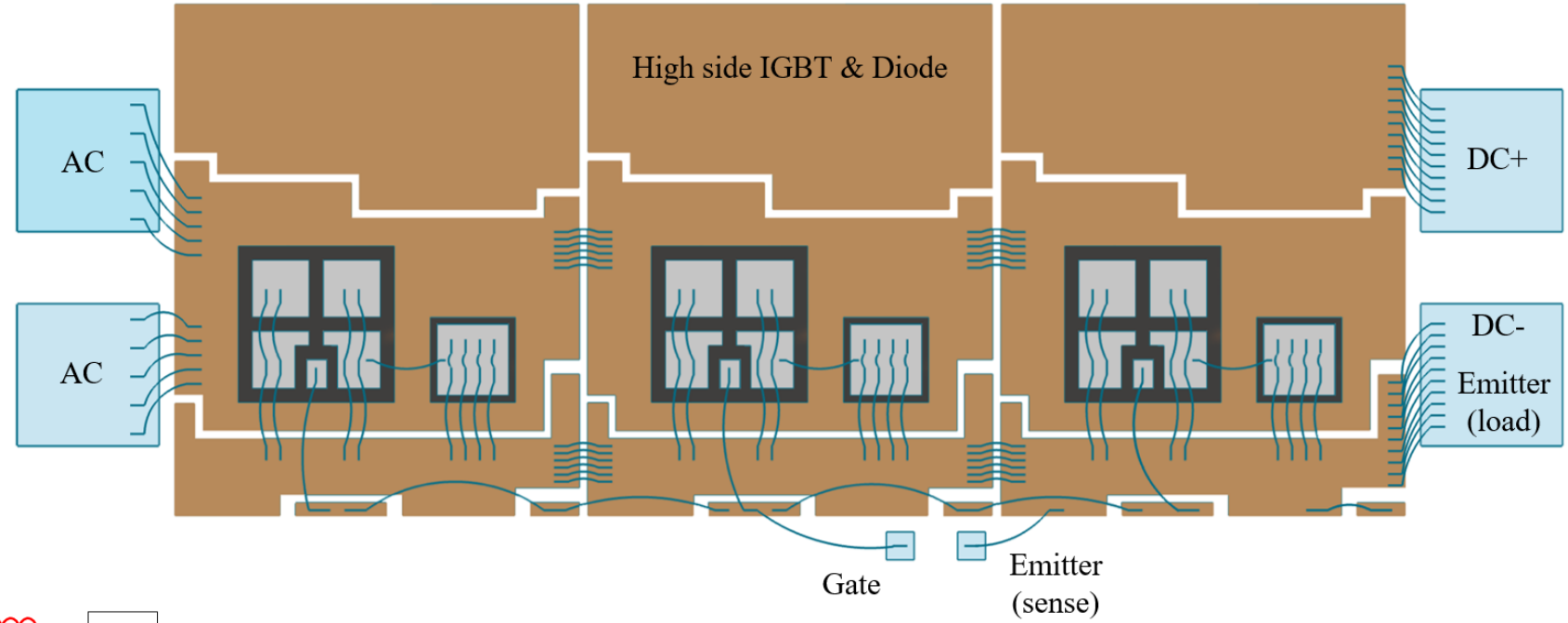
- A slightly increasing dv/dt can be found, however, very small.
- The obvious change of the turn-ON behavior is measurend, after cutting 6 bond wires for each chip

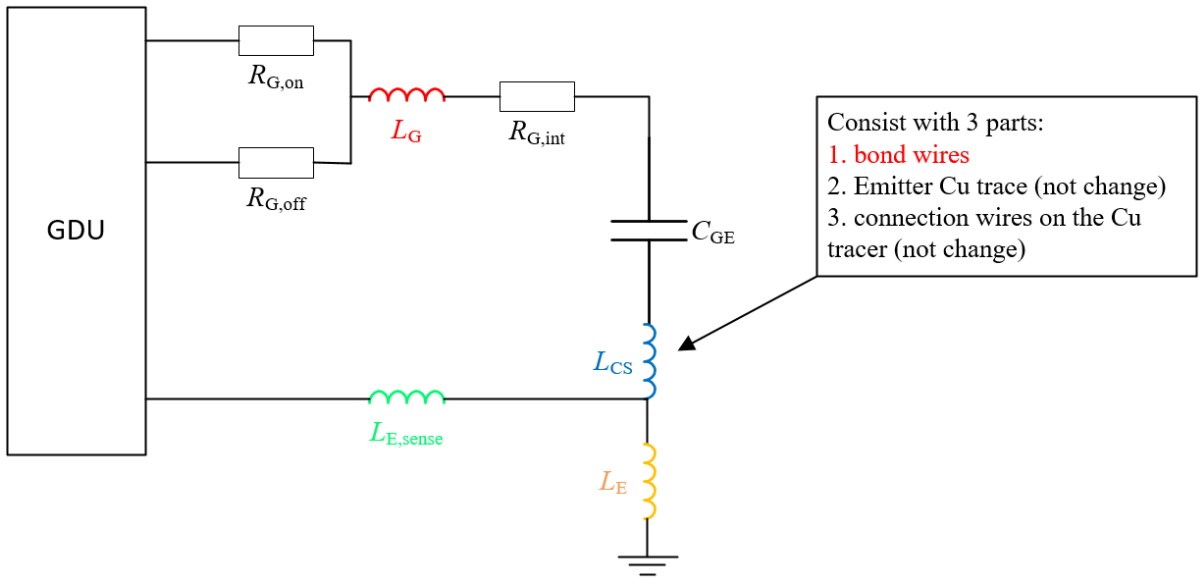
For turn-OFF:

- No visiable changing of the turn-OFF behavior (plasma controlled)

Testcondition: V_{CE} = 900V, I_C = 225A,
$R_{G,on}$ = $R_{G,off}$ = 3.3Ω, Room temperature

Analysis

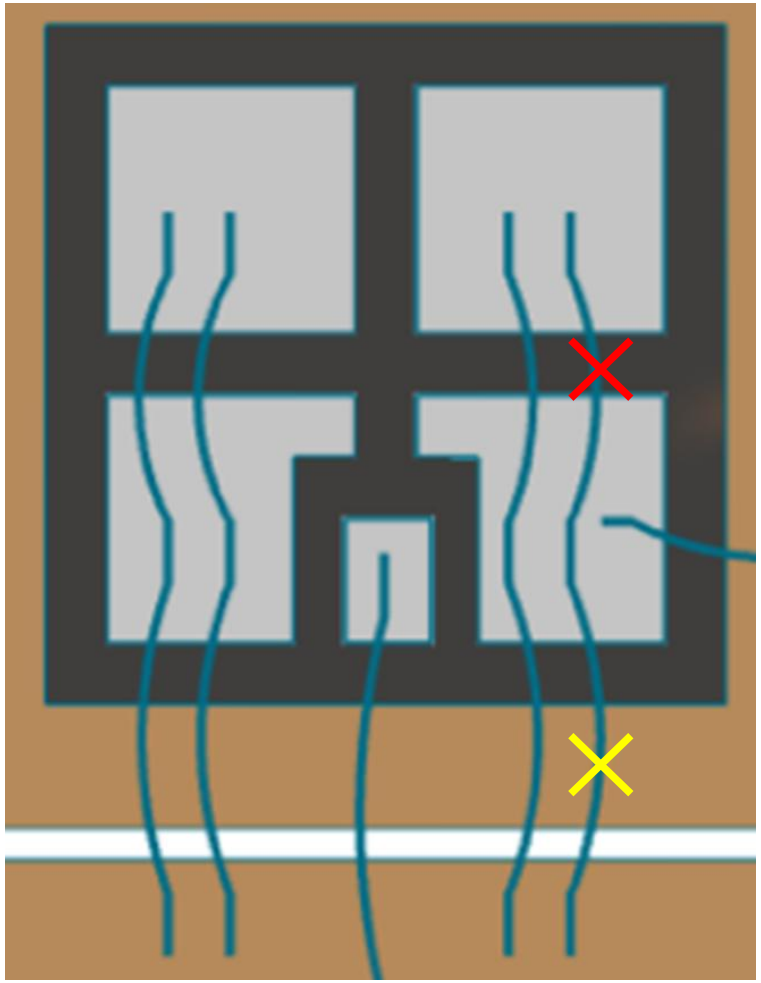




- L_G is high, due to the long gate wires
- Compare with the emitter Cu trace and strong unsymmetrical chip parallel, the portion of the bond wires on the common-source inductance is small. Therefore, cutting bond wire has only very small changing of the inductance in the gate-loop
- Wenn the load current flows through, the influence on the gate voltage can be reflected from the current waveform, but not from the gate. But the „real“ gate voltage can be seen from the simulation

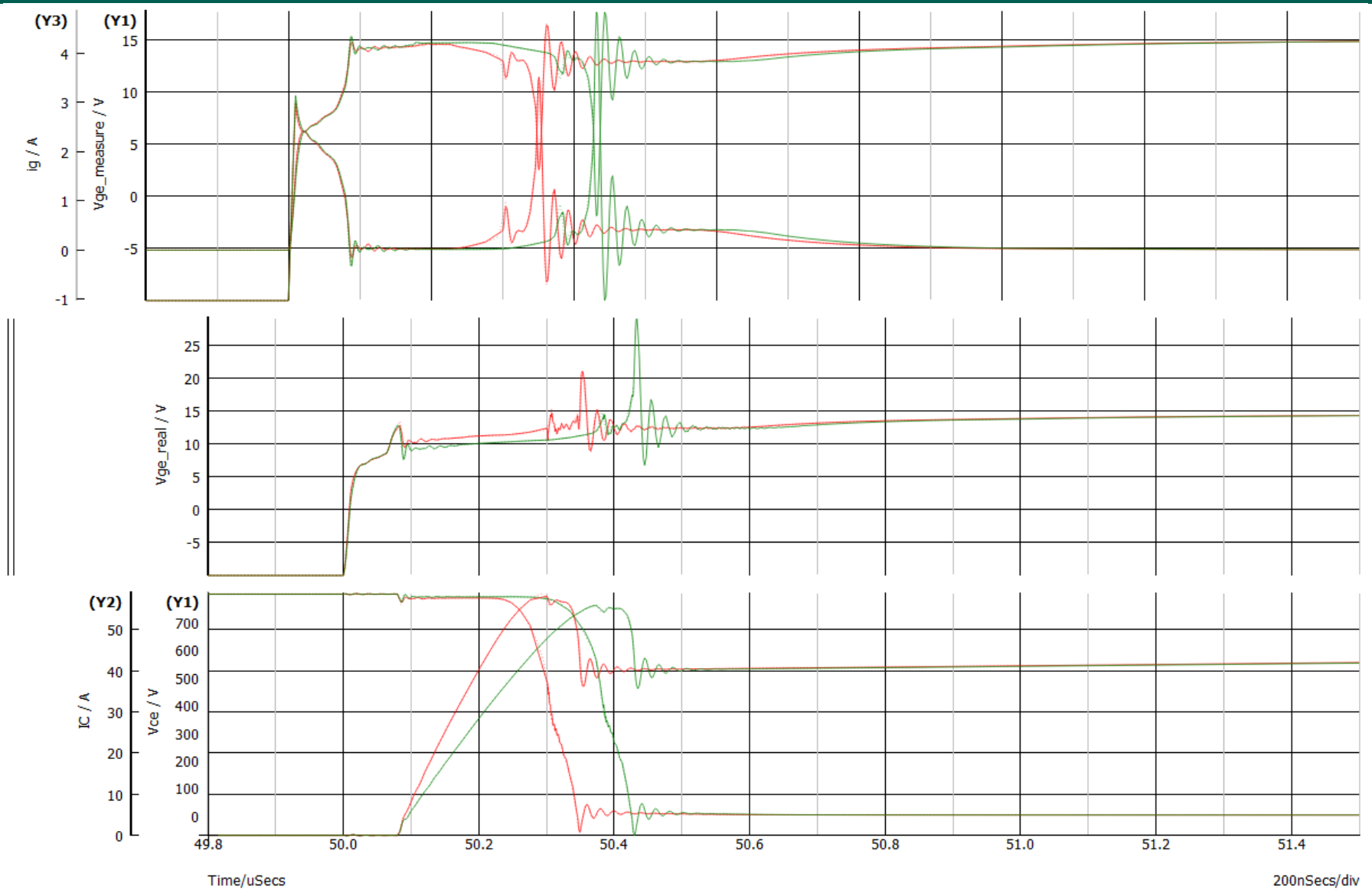
Analysis

- More carefully analysis / uncertainty analysis



- The cutting cannot 100% represent the bond wire lift-off, but only heel crack.
- If the lift-off happens on the bottom segments, the influence should be even higher. (inductance becomes higher, more current will flow through this long wire)
- The cutting position makes difference: the yellow position has more significant impact on the increasing of the inductance.
- Due to the real bond wire lift-off after power cycling, some early failure could happen, such as $V_{G,th}$ shifting and the decreasing of blocking capability.

Simulation



- The increased L_{CS} (10nH, red to 20nH, green) pulls the „real“ gate voltage down during the pos. di/dt. → lower di/dt
- This cannot be seen from the measured gate voltage, because the influence of the L_G , and another portions of L_{CS}. (Cu trace, etc.)
- Almost no change on the gate current, due to already high gate–loop inductance.
- Oszillation is caused by the snap diode RR, (not this case in the measurement)

Conclusion

- Loosing the connection of the segment on the IGBT active area will not change the capacitance.
- The changing of the turn-ON behavior is not significant, and related actually to the changing of the L_{CS}
- The results are packaging dependent, more tests are running

Complete DoE

- Here is my complete DoE:

1. PCT with two conditions on 34mm module, then DP (*50% done*).

Because the 34mm is normally failed due to V_{CE} and R_{th} increasing at the same time. This is used to confirm, that the PCT condition has no influence on our final conclusion. Further, confirm the aging of the solder layer has no influence on the capacitance. (other research groups have a different opinion)

2. PCT on 3-Pin and 4-Pin TO 247 DUT, then DP (*50% done*).

The TO device is normally failed with pure bond wire failure (again, change the L_{CS}) but due to the press effect of the mold compound, maybe the influence is not so significant as expected. 4-Pin device is just to confirm the results for 4-Pin, because of the connection of sense emitter, there should be no influence on the switching.

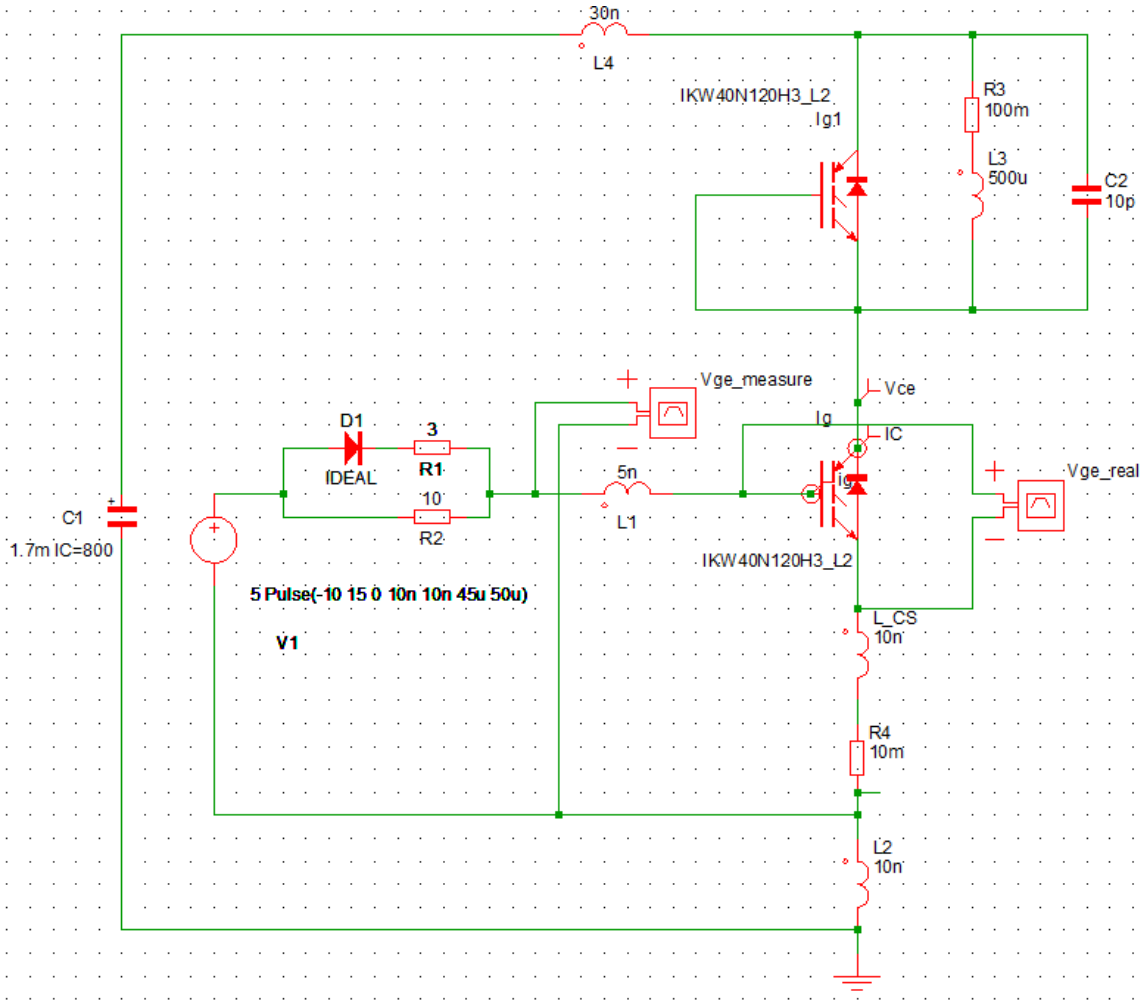
3. Module with more than one segment on the IGBT chip (*Done*)

What is your suggestion? Danke dir ^_^

Discussion the influence of the common-emitter resistance

- **Hypothesis: the common-emitter resistance has very significant impact on the turn-off behavior [only turn-OFF !]**

Simulation model:



Discussion the influence of the common-emitter resistance

- **Simulation results**

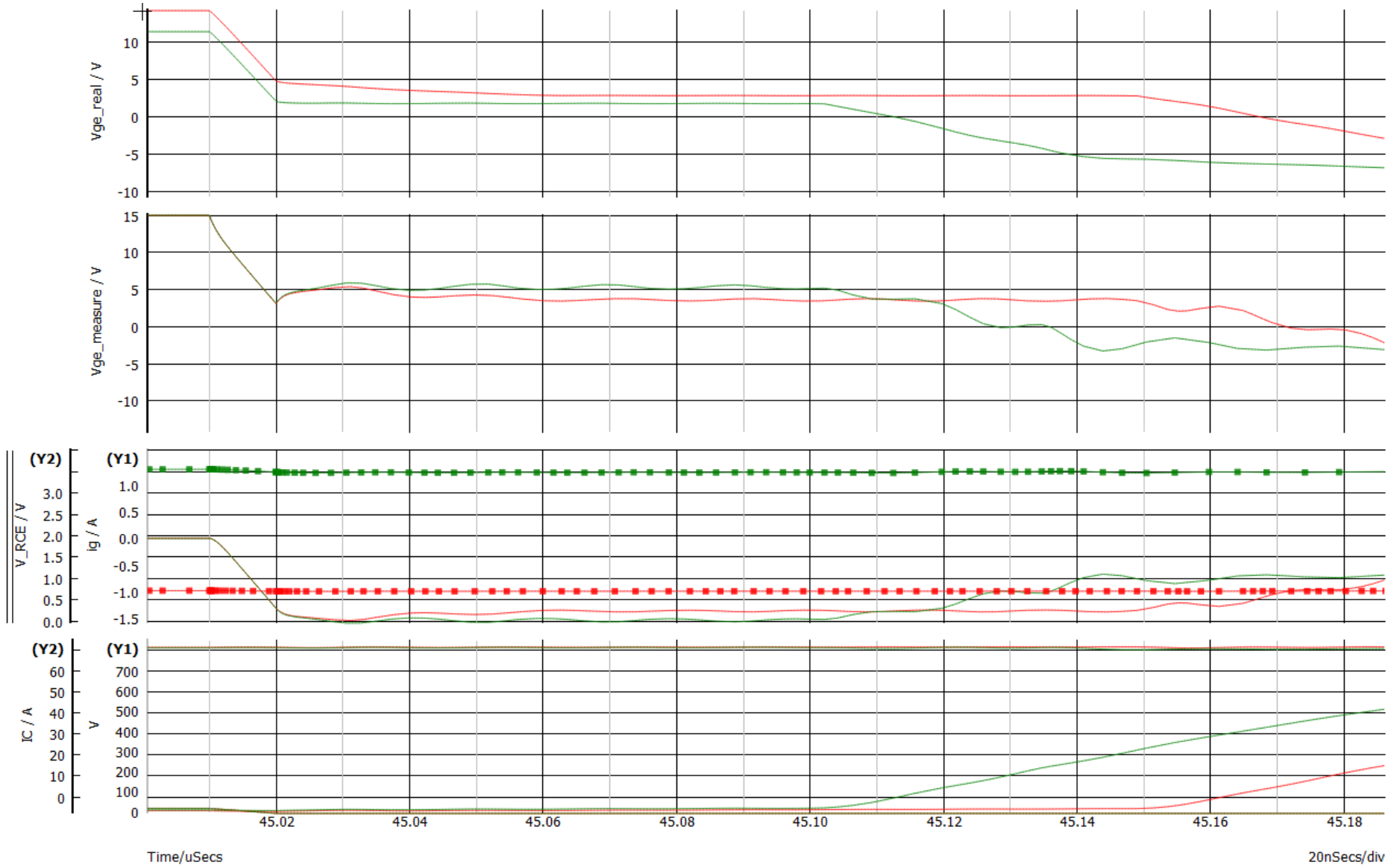
Green: R4 = 50mΩ

Red: R4 = 10mΩ

The measurement delivers a wrong and opposite voltage, if the increasing of R4 is significant

The real gate voltage is already lower, before the turn-OFF, because of the in creased R

The gate current for higher R is higher, the same as CB´s measurements

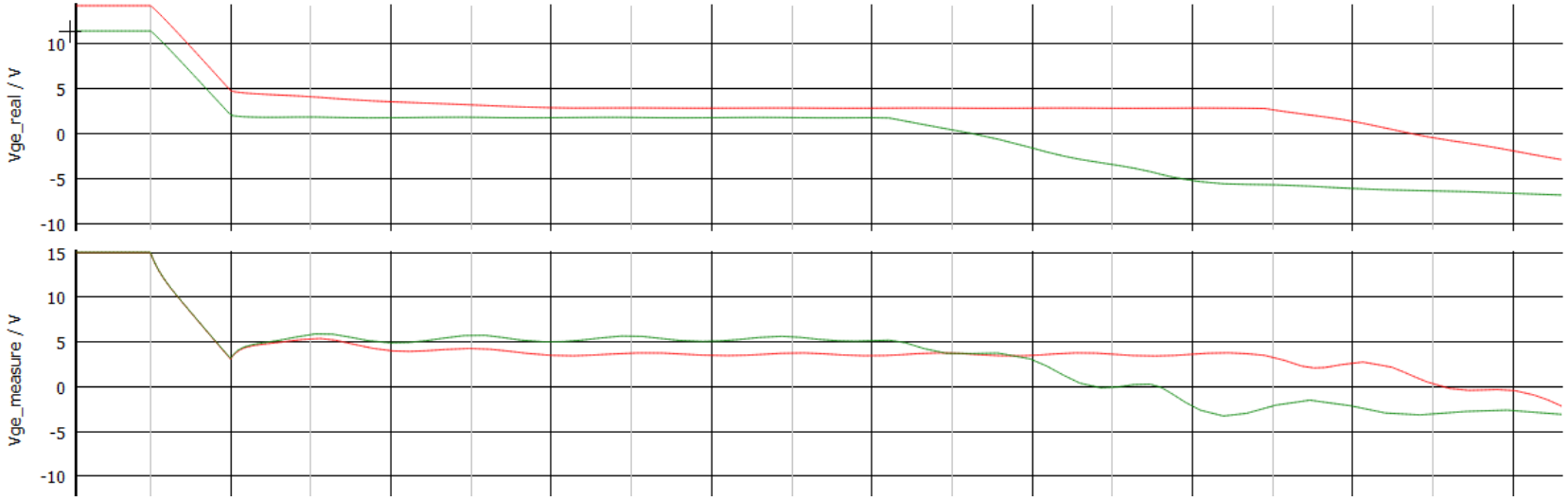


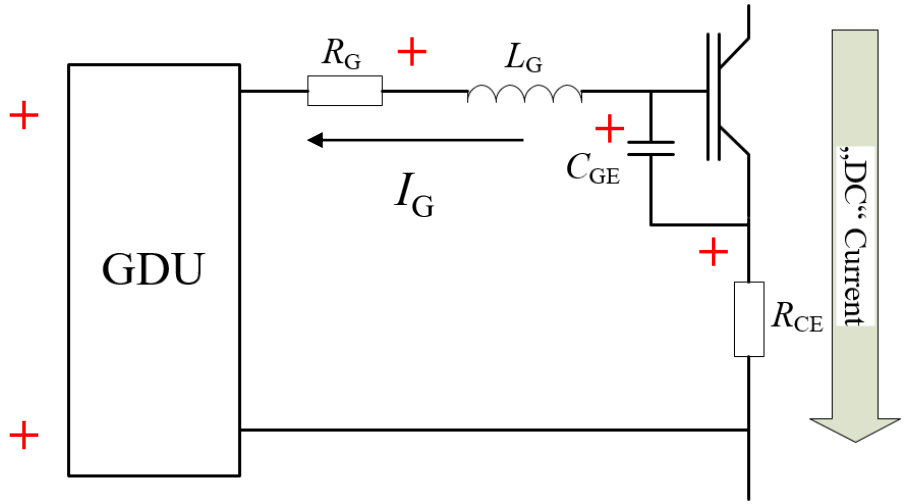
Discussion the influence of the common-emitter resistance

- **Analysis: Gate voltage**

Green: **R = 50mΩ**

Red: **R = 10mΩ**





$$Before\ turn-OFF\text{: } V_{CGE} = V_{GDU} - V_{RCE}$$

$$During\ the\ Platau\text{: } V_{CGE} = -V_{GDU} + V_{RG} - V_{RCE}$$

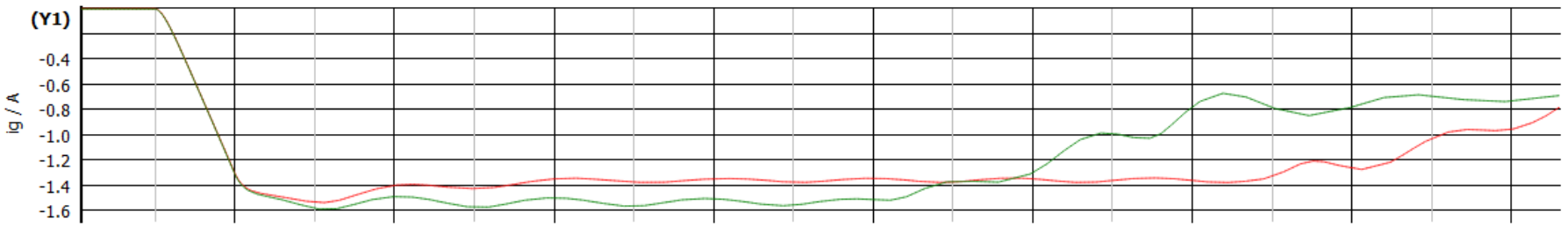
$$During\ the\ Platau\ [measure]\text{: } V_{CGE} + V_{RCE} = -V_{GDU} + V_{RG}$$

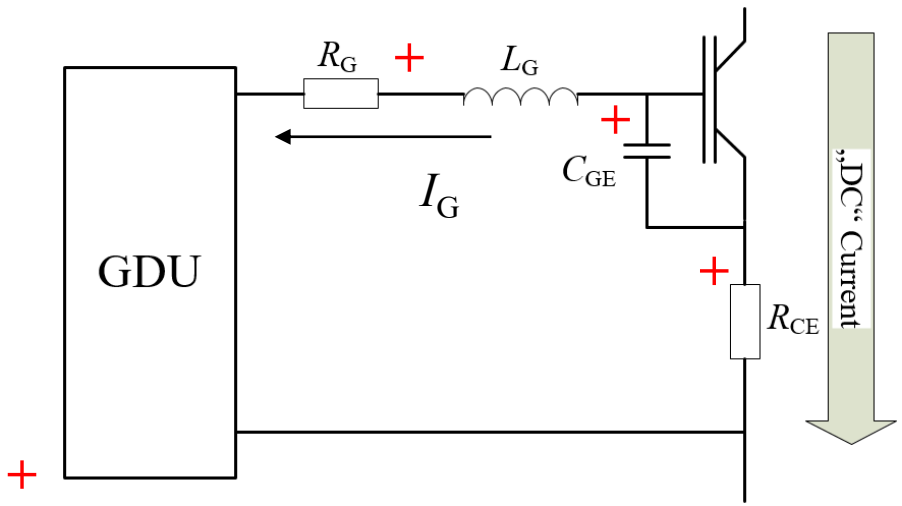
Discussion the influence of the common-emitter resistance

- **Analysis: Gate current**

Green: **R = 50mΩ**

Red: **R = 10mΩ**





- **The gate current is actually the current through the R_G**

$If\ the\ R_{CE}\ is\ small\ or\ even\ 0: V_{RG} = V_{GDU} + V_{CGE}$

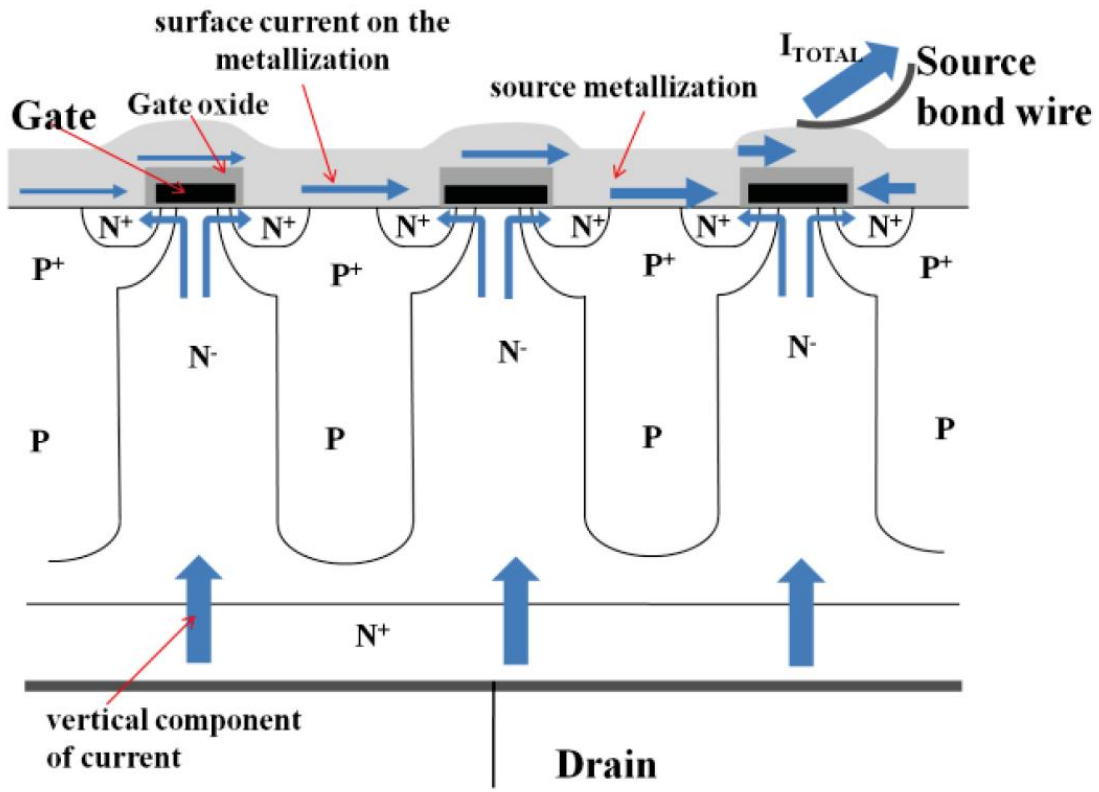
Current is the max. V_{RG} / R_G

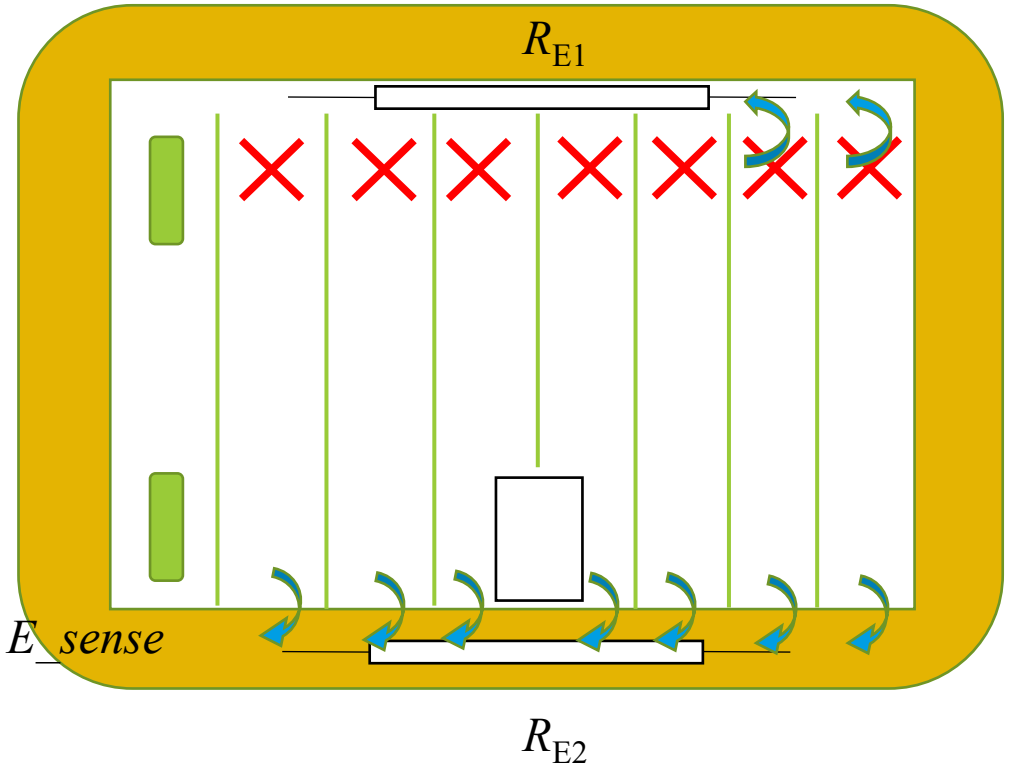
$If\ the\ R_{CE}\ becomes\ bigger: V_{RG} = V_{GDU} + V_{CGE} + V_{RCE}$

The real gate voltage V_{CGE} decreases during the turn-OFF, the voltage drop on the R_G becomes consequently smaller. However, the voltage drop on the R_{CE} helps to „hold“ the voltage difference; therefore, the current is higher.

Discussion emitter potential distribution

- **Analysis: current path**

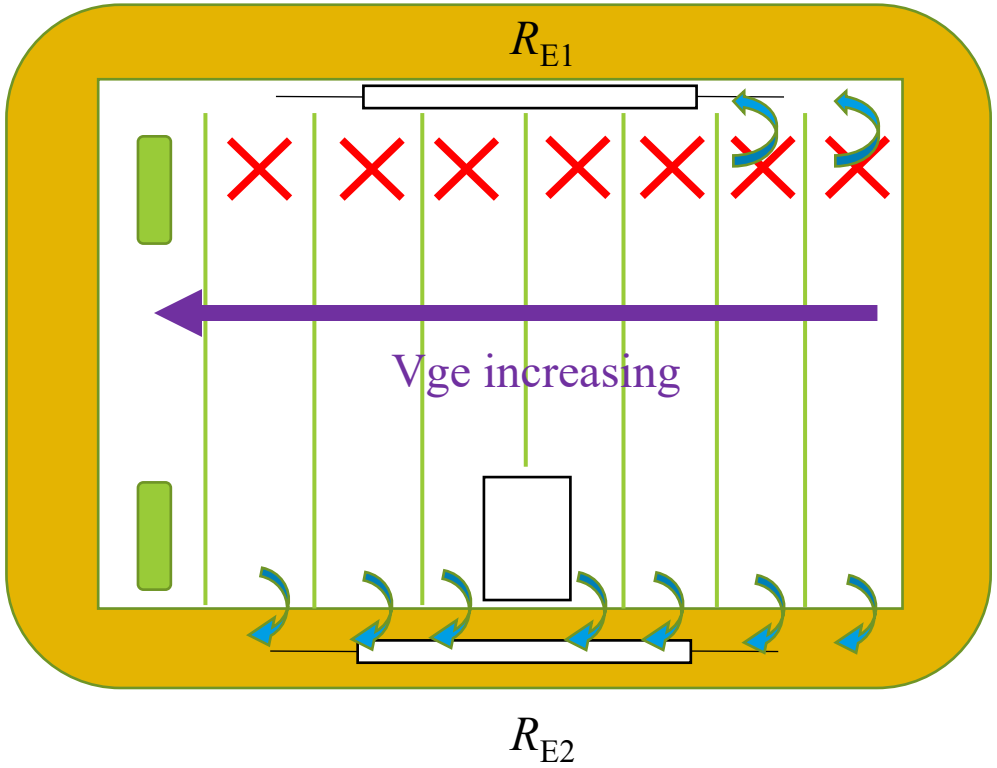




- **Besides the lateral current inside the device, also a portion of current through the metallization to the bond wire**

Discussion emitter potential distribution

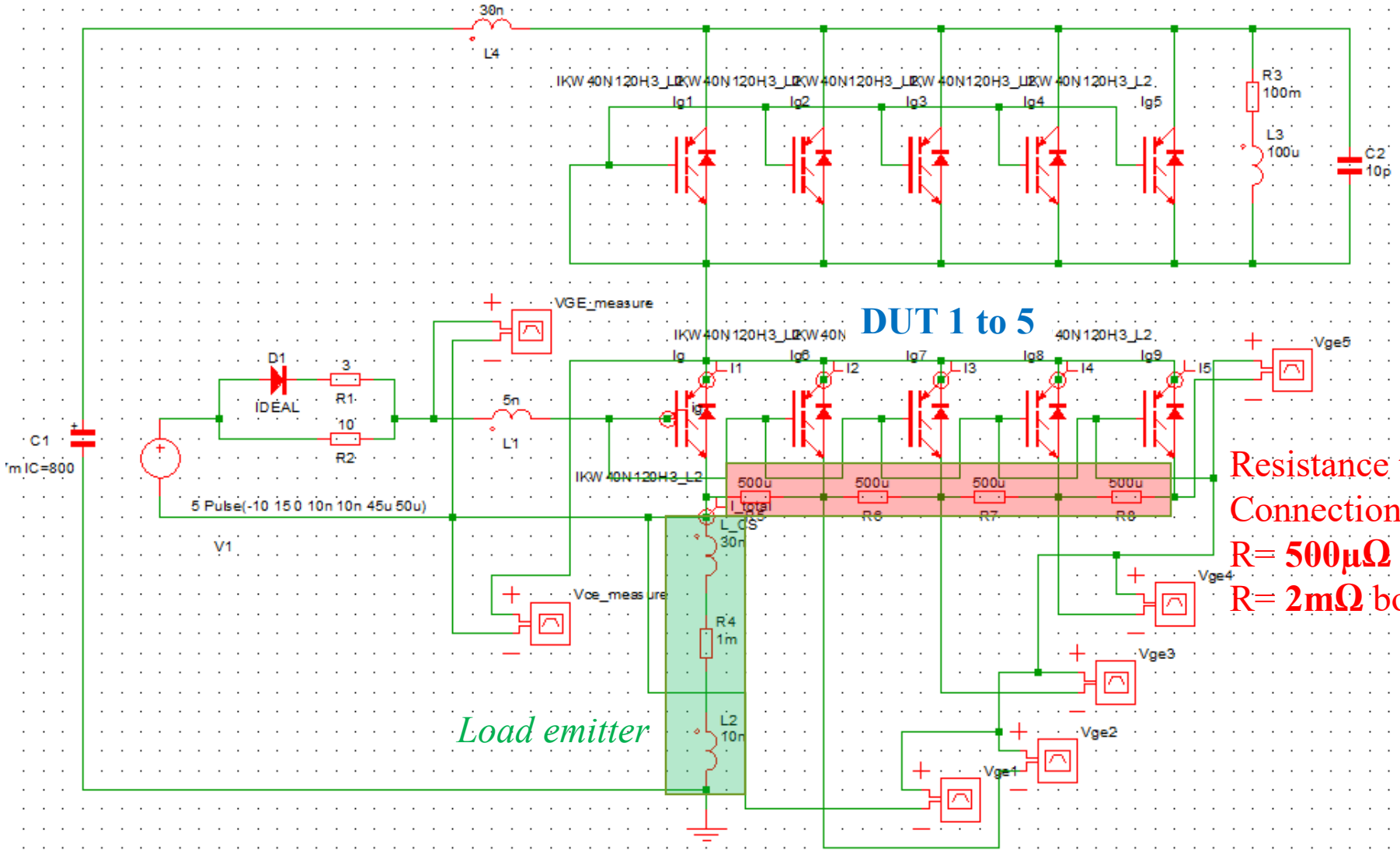
- **Analysis: current path**



- **If we assume that the resistance is constant, then the distribution of the emitter potential is current dependent**
- **The higher the current, the stronger the emitter potential unsymmetrical, more current flows through the left-hand side segment. (CB´s measurement: two times rated current into SCII)**
- **The right-hand side segment has the lowest gate voltage, the most left-hand side segment has the complete gate voltage**
- **Question: The lateral current is caused by the device itself or due to the lost bond wires caused unsymmetrical emitter potential ?**

Discussion emitter potential distribution

- **Simulation**



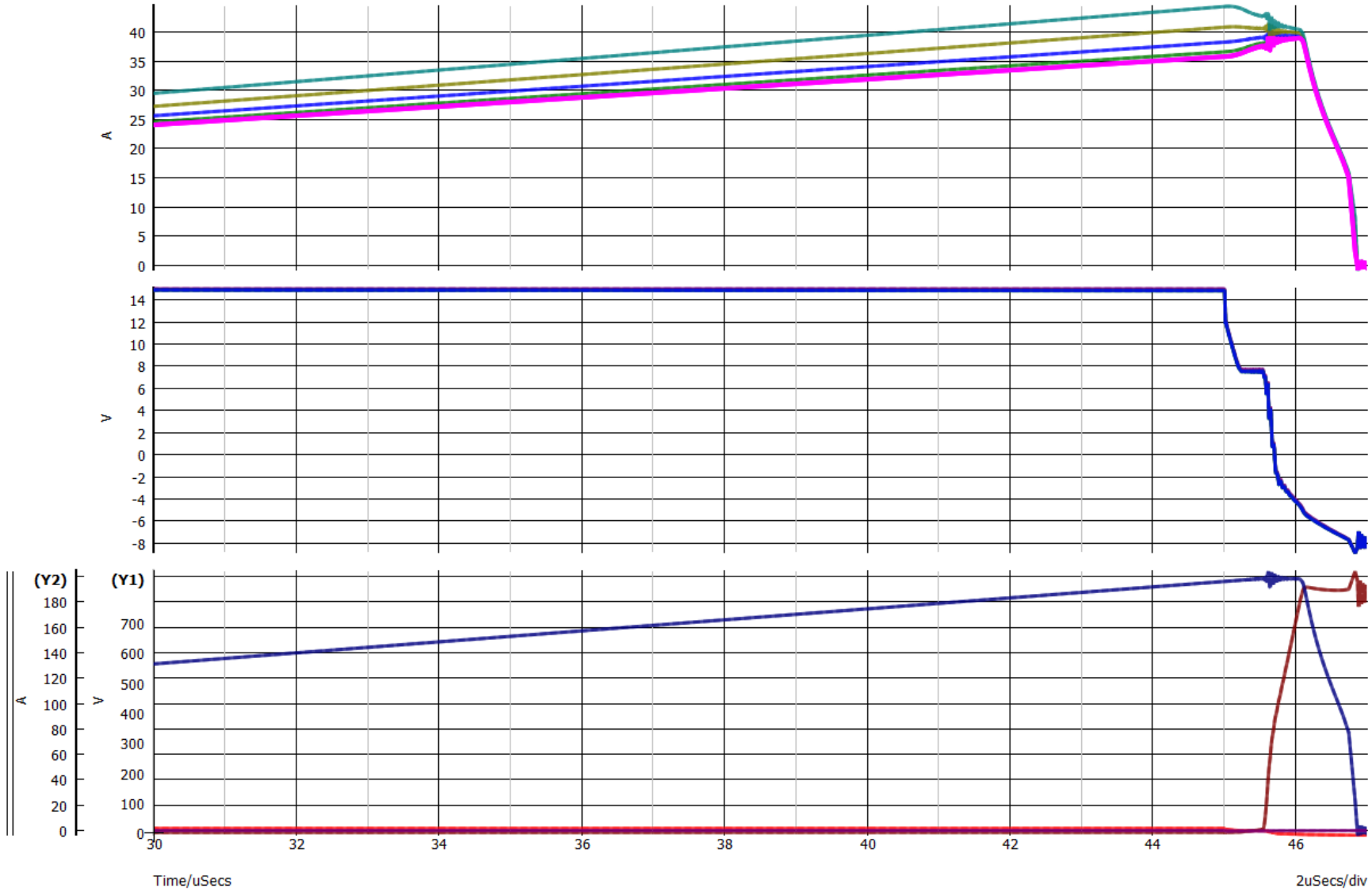
Resistance to simulate the Connection:

R= **500µΩ** good connection

R= **2mΩ** bond wires lift-off

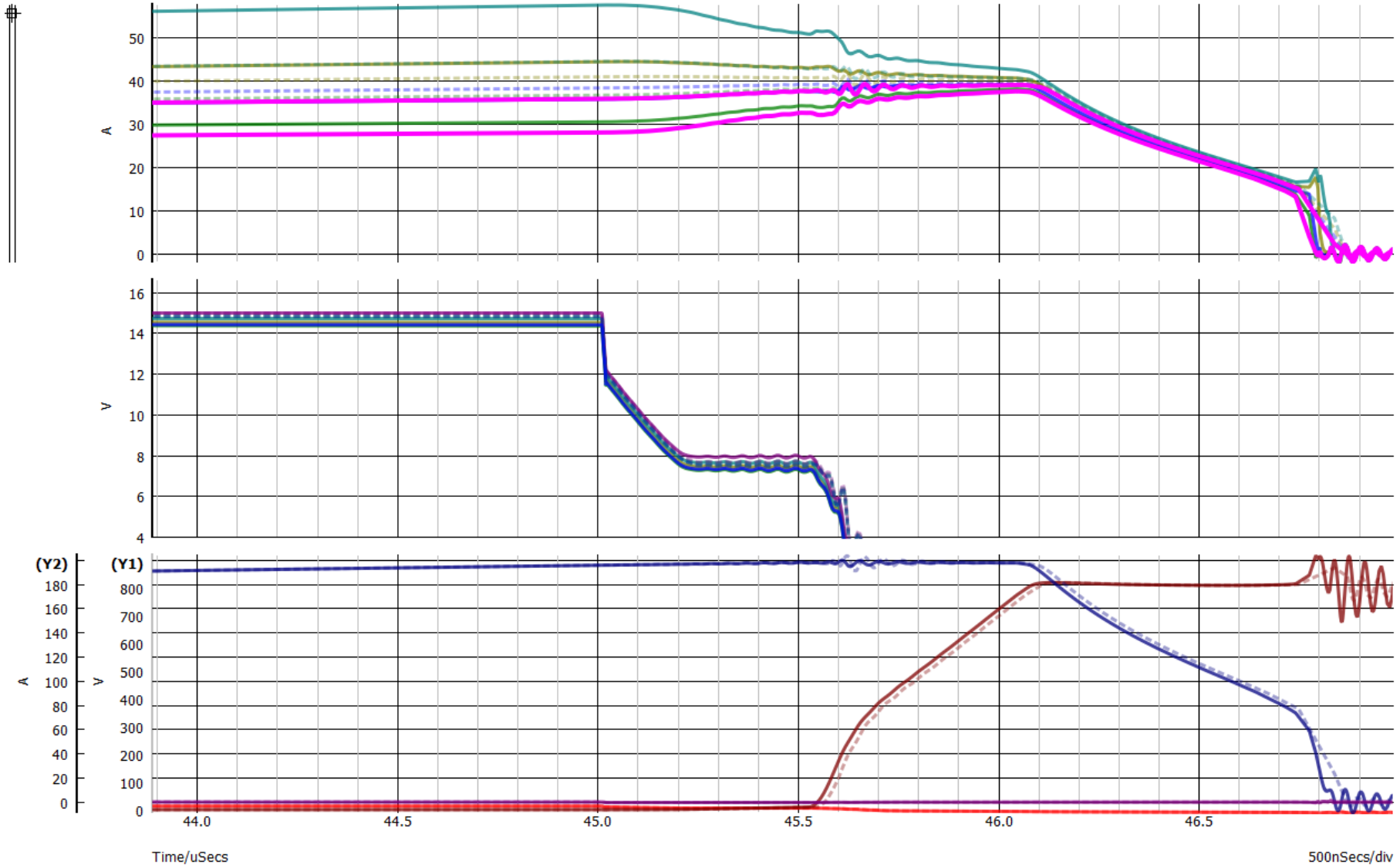
Discussion emitter potential distribution

- **500 µΩ**



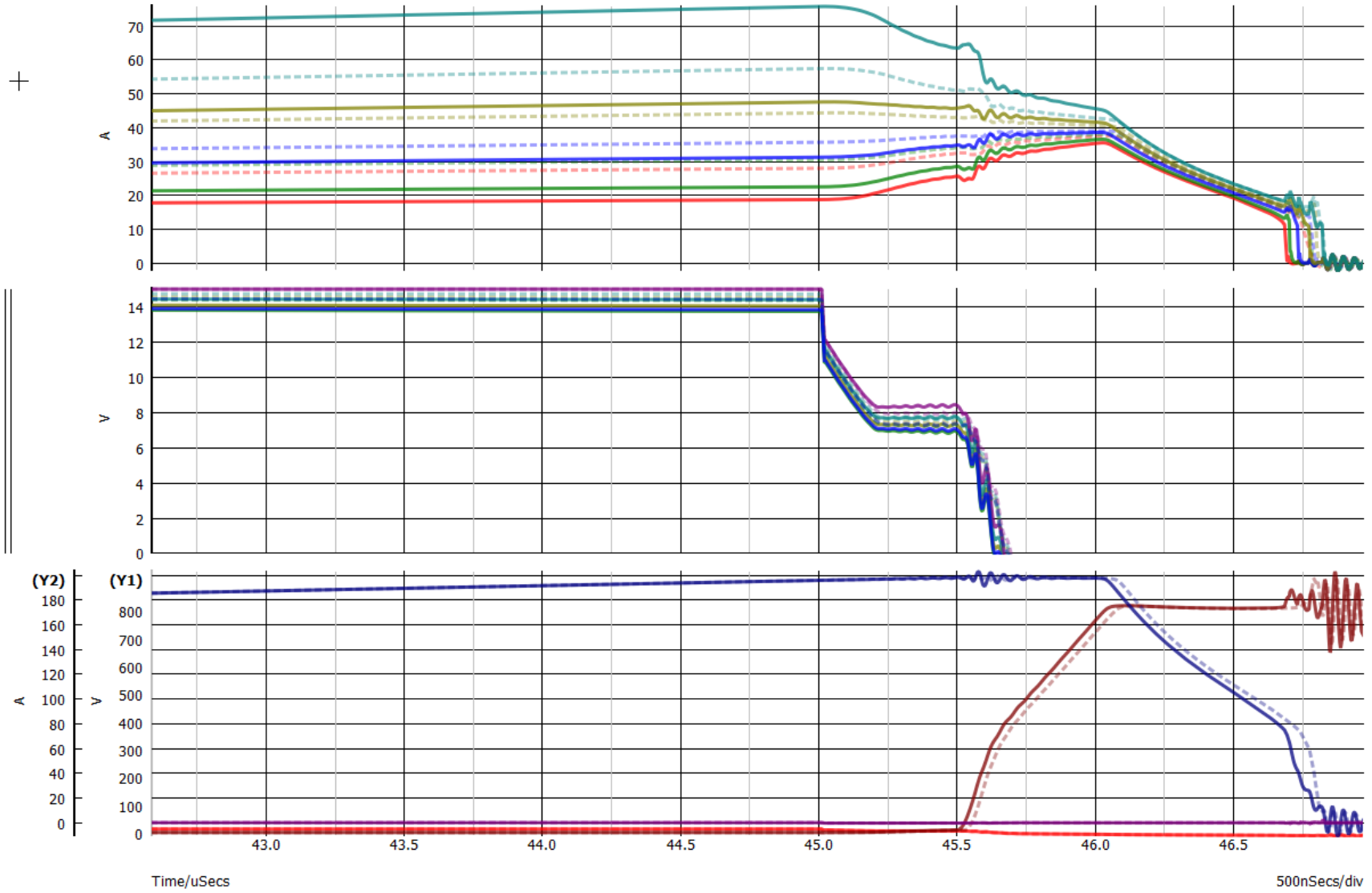
Discussion emitter potential distribution

- **2 mΩ**



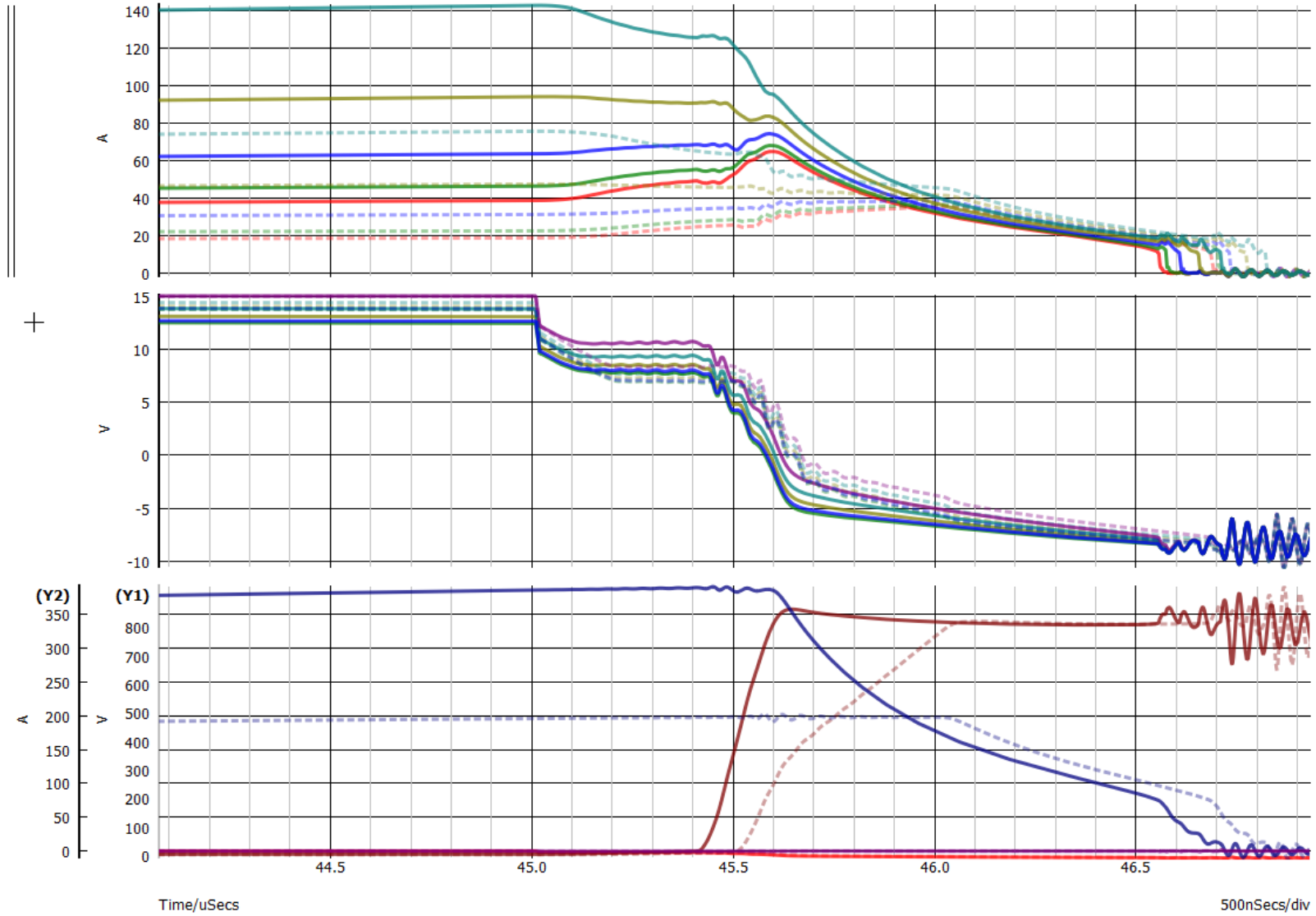
Discussion emitter potential distribution

- **5 mΩ**



Discussion emitter potential distribution

- **2 times current, 5mΩ**



Discussion emitter potential distribution

- **3 times current, 10mΩ**

SC II !!!

- **Gate voltage and load current play a major role for chip emitter layout without common-source Inductance after bond wire lift-off**