ASSIGNMENT 1 – CYCLIC REDUNDANCY CHECK

ARQUITETURA DE ALTO DESEMPENHO

WORK DONE BY:
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PARALLEL ENCODER

$$\left(\sum_{n=0}^{15} a_n \times x^{n+8}\right) mod\ (x^8 + x^7 + x^3 + x^2 + x + 1) =$$

$$= (a_0 \oplus a_1 \oplus a_3 \oplus a_5 \oplus a_7 \oplus a_{12} \oplus a_{13}) \times x^7 +$$
$$+ (a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7 \oplus a_{11} \oplus a_{13} \oplus a_{15}) \times x^6 +$$
$$+ (a_0 \oplus a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_{10} \oplus a_{12} \oplus a_{14}) \times x^5 +$$
$$+ (a_2 \oplus a_4 \oplus a_7 \oplus a_9 \oplus a_{11} \oplus a_{12} \oplus a_{15}) \times x^4 +$$
$$+ (a_1 \oplus a_3 \oplus a_6 \oplus a_8 \oplus a_{10} \oplus a_{11} \oplus a_{14}) \times x^3 +$$
$$+ (a_0 \oplus a_2 \oplus a_5 \oplus a_7 \oplus a_9 \oplus a_{10} \oplus a_{13}) \times x^2 +$$
$$+ (a_0 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7 \oplus a_8 \oplus a_9 \oplus a_{13} \oplus a_{15}) \times x +$$
$$+ (a_0 \oplus a_1 \oplus a_2 \oplus a_4 \oplus a_6 \oplus a_8 \oplus a_{13} \oplus a_{14})$$

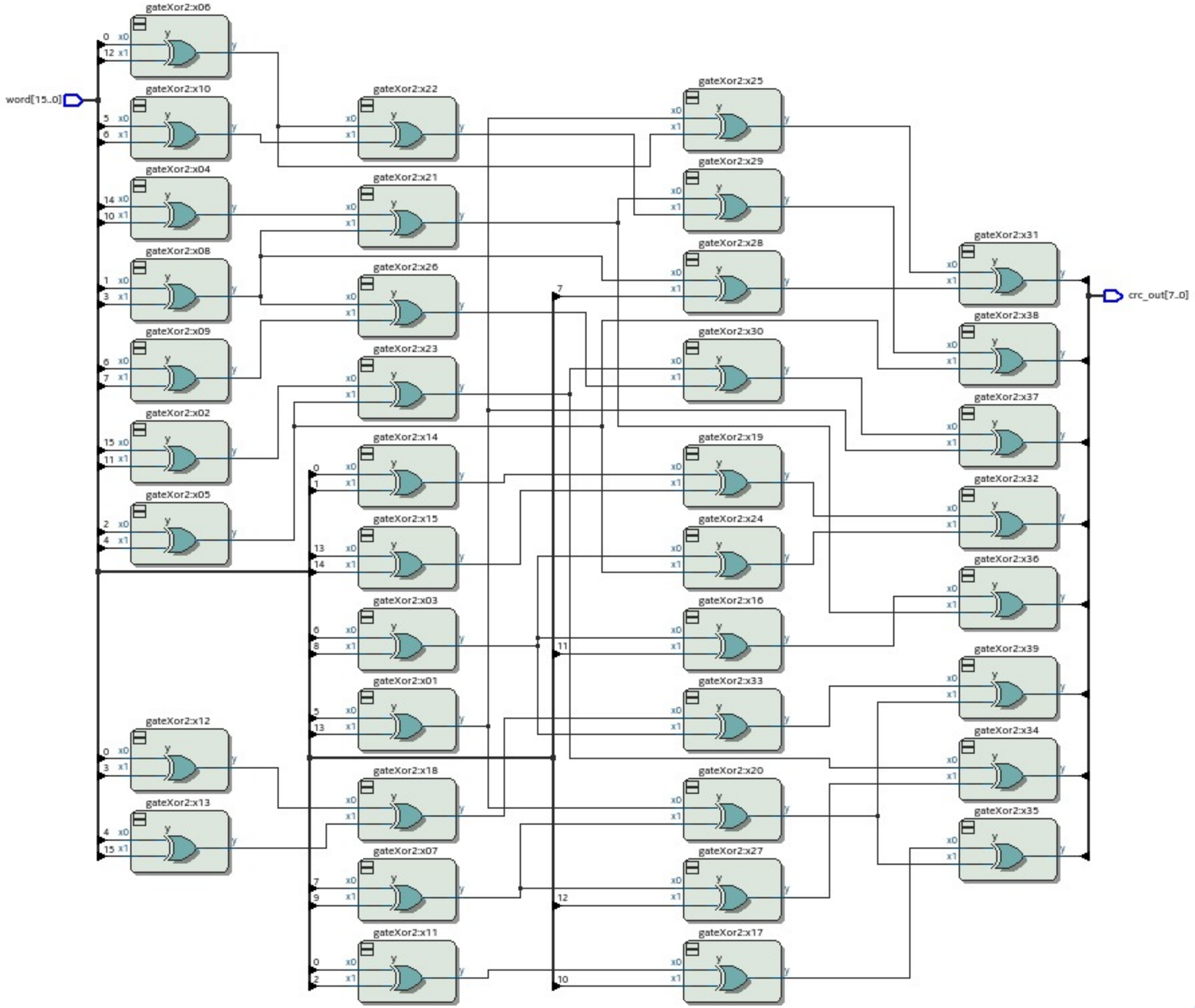
- 58 x-or gates are needed

To get the result we expected, we used the **Property of the Reminder**, and while doing this we tried to reduce the number of XORs the most we could so we reduce the time delays

	r7	r6	r5	r4	r3	r2	r1	r0
a0	X		X			X	X	X
a1	X	X	X		X			X
a2		X	X	X		X		X
a3	X	X	X		X		X	
a4		X	X	X			X	X
a5	X	X	X			X	X	
a6		X	X		X		X	X
a7	X	X		X		X	X	
a8					X		X	X
a9				X		X	X	
a10			X		X	X		
a11		X		X	X			
a12	X		X	X				
a13	X	X				X	X	X
a14			X		X			X
a15		X		X			X	

Xor1	a13,a5
Xor2	a15,a11
Xor3	a6,a8
Xor4	a14,a10
Xor5	a2,a4
Xor6	a0,a12
Xor7	a7,a9
Xor8	a1,a3
Xor9	a6,a7
Xor10	a5,a6
Xor11	a0,a2
Xor12	a0,a3
Xor13	a4,a15
Xor14	a0,a1
Xor15	a13,a14
a7	
a12	
a11	
a10	

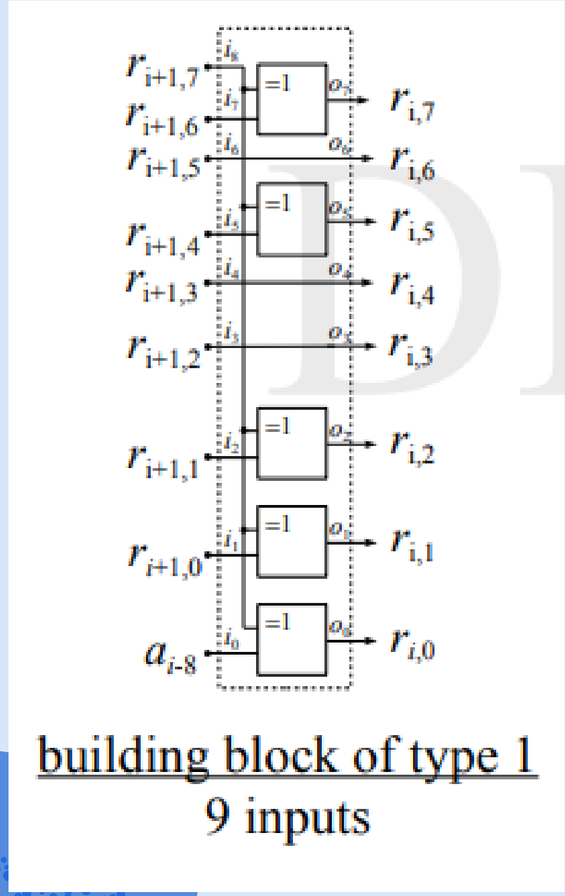
ENCODER ARCHITECTURE



39 Total XORs

4 Propagation Time Delay

BIT-SERIAL CHECKER



building block of type 1
9 inputs