Multiple issue processors

→ Exploiting ILP with multiple issue

3 multiple issue approaches:

- Dynamically sheduled super scalar processors
- VLIW (very long instruction word)
- statically scheduled superscalar processors

↳ Statically scheduled superscalar processor

This processor typically issues in order a variable number of instructions per clock cycle upto a limit that corresponds to the number of parallel pipelines which are implemented. It's variable for two reasons:

- the multiple pipelines are not exactly alike.
- it is not possible to prevent stalls due to data hazards among successive instructions.

↳ Dynamically Schedule Superscalar processors.

These need to fetch multiple instr./cycle which is highly complex due to branches.

Also, need to issue multiple instr. in the same cycle is very complex as instr. may depend on one another.

Two different approaches have been used:

- Run the step in a fraction of the whole clock cycle for each instruction (not easy for > 2 instr).
- Build the necessary logic to run simultaneously two or more instructions, including dependences among them.

Basic strategy to update the issue logic;

1. Assign a Reorder buffer and a reservation station for every instruction that might be issued in the next bundle.

2. Find all dependences among them (in the bundle)

3. If a dependence is found, the assigned ROB entry numbers should be used to update the reservation table for the dependent instruction.