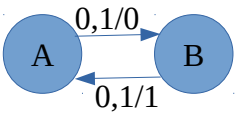
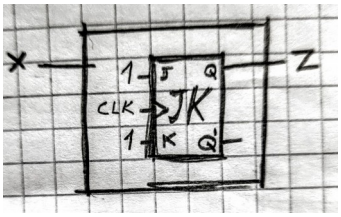
Digital Systems HW10

1. Design a sequential system with one input and one output. The output should show whether or not the number of previous inputs is even or odd. (if even output equals "1", if odd output equals "0"). Realize the system using J-K Flip-Flops.

   A - Even number of inputs
   B - Odd number of inputs



PS		NS		Z
		J	K	
A	0	1	Φ	0
B	1	Φ	1	1



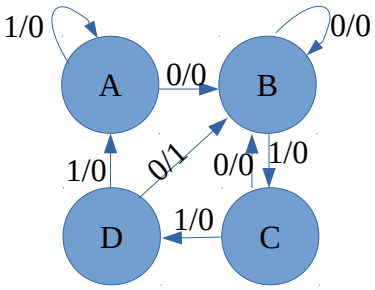
2. Design a sequential circuit meant to detect the sequence 0110. The output should equal "1" each time this sequence is detected. Draw the MEALY State-diagram. Realize the system using D Flip-Flops. Assume the initial state S0 is a state where the previous inputs have been a arbitrary sequence of at least three "1"s.

   A - Initial State

   B - Found a 0

   C - Found 01

   D - Found 011



PS			NS				Z	
			X=0		X=1		X=0	X=1
Y1	Y0		D1	D0	D1	D0		

0	0	A	0	1	0	0	0	0
0	1	B	0	1	1	0	0	0
1	0	C	0	1	1	1	0	0
1	1	D	0	1	0	0	1	0

D1 = X(Y1+Y0)(Y1’+Y0’)

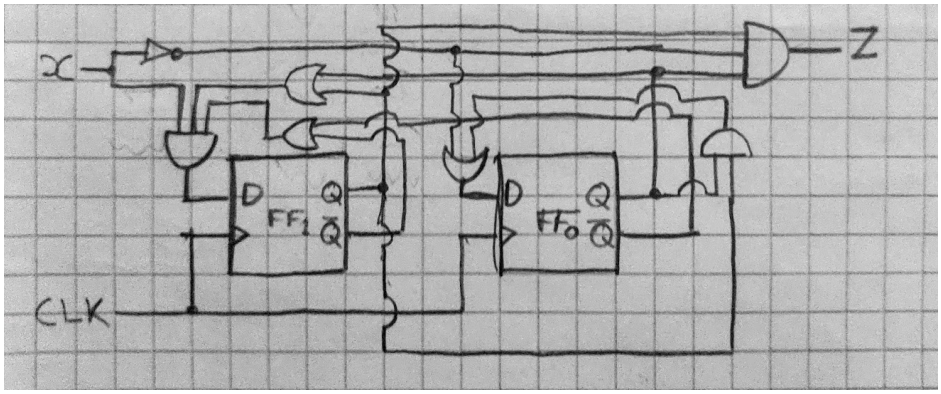
X\Y1Y0	00	01	11	10
0	0	0	0	0
1	0	1	0	1

D0 = x’+Y1Y0’

X\Y1Y0	00	01	11	10
0	1	1	1	1
1	0	0	0	1

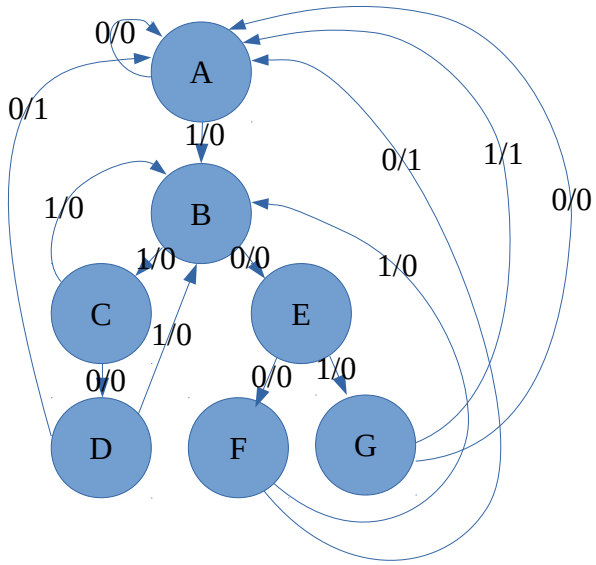
Z = X’Y1Y0

X\Y1Y0	00	01	11	10
0	0	0	1	0
1	0	0	0	0



3. Design a sequential circuit meant to detect the sequences: 1100, 1010, 1001. The output should equal "1" each time any one of these sequences is detected. Upon detecting any of these sequences, the system also reverts to its initial state. Realize the system using D Flip-Flops.

   A - Initial state
   B - Found 1
   C - Found 11
   D - Found 110
   E - Found 10
   F - Found 101
   G - Found 100


A
B
C
D
E
F
G
0/0
0/1
1/0
0/1
1/1
0/0
1/0
1/0
0/0
1/0
1/0
0/0
0/0
1/0

PS				NS						Z	
				X=0			X=1			X=0	X=1
	Y2	Y1	Y0	D2	D1	D0	D2	D1	D0		
A	0	0	0	0	0	0	0	0	1	0	0
B	0	0	1	1	0	0	0	1	0	0	0
C	0	1	0	0	1	1	0	0	1	0	0
D	0	1	1	0	0	0	0	0	1	1	0
E	1	0	0	1	0	1	1	1	0	0	0
F	1	0	1	0	0	0	0	0	1	1	0
G	1	1	0	0	0	0	0	0	0	0	1

Y0X\Y2Y1	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	0	0	Φ	0
10	1	0	Φ	0

D2 = Y2Y1’Y0’+Y2’Y1’

Y0X\Y2Y1	00	01	11	10
00	0	1	0	0
01	0	0	0	1
11	1	0	Φ	0
10	0	0	Φ	0

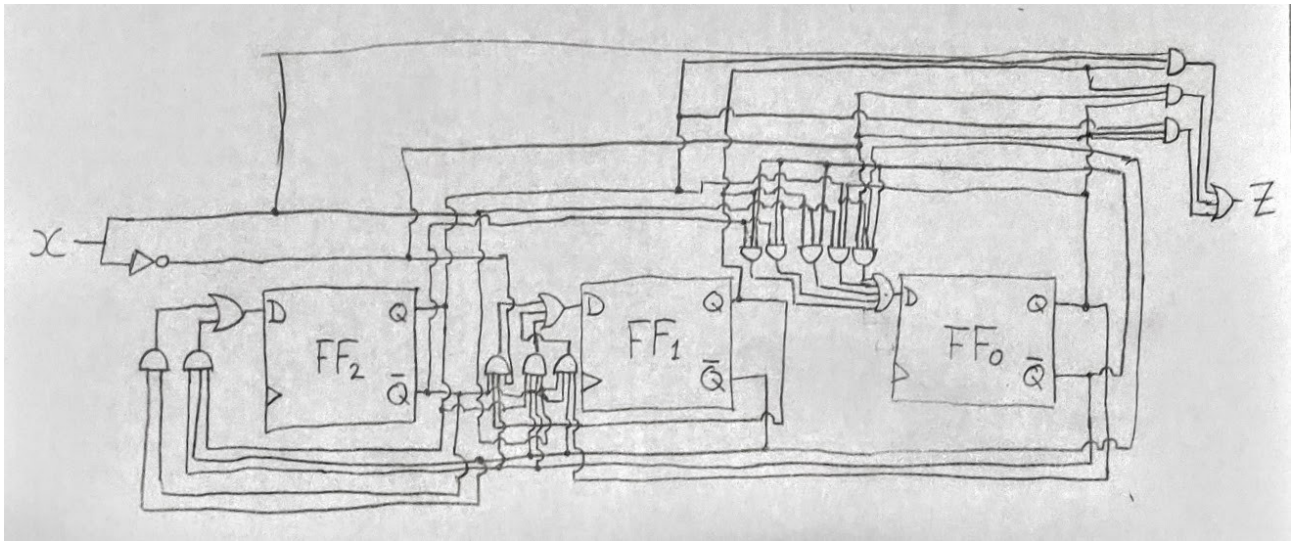
D1 = Y2’Y1Y0’X’ + Y2Y1’Y0’X + Y2’Y1’Y0X

Y0X\Y2Y1	00	01	11	10
00	0	1	0	1
01	1	1	1	0
11	0	0	Φ	1
10	0	0	Φ	0

D0 = Y2’Y1Y0’ + Y2’Y0’X + Y1Y0’X + Y2Y0X + Y2Y1’Y0’X’

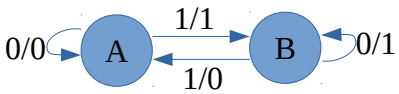
Y0X\Y2Y1	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	0	Φ	0
10	0	1	Φ	1

Z = Y2Y1X + Y1Y0X’ + Y2Y0X’



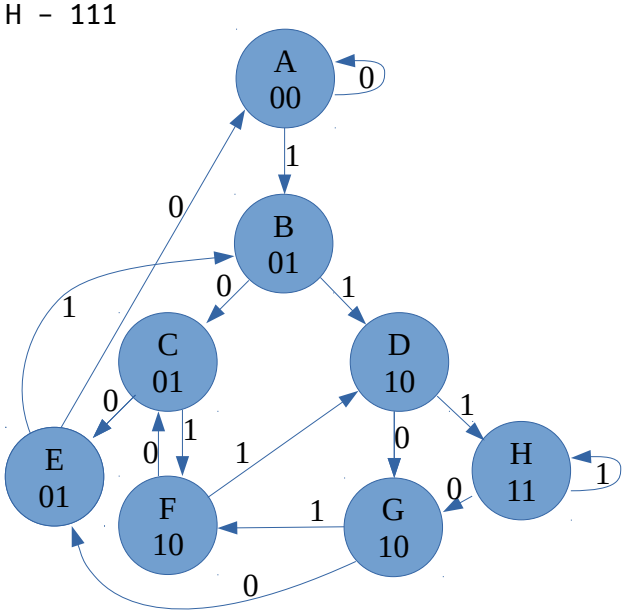
4. For the following two systems draw the state diagram (only)
   A) A system which outputs the XOR value of all the inputs received so far.

   A - Even number of 1s
   B - Odd number of 1s



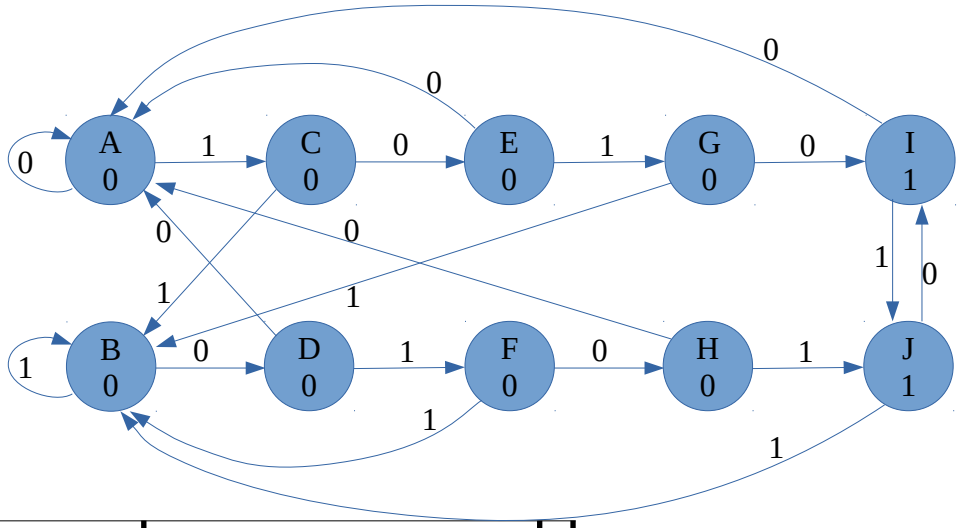
   B) A system that outputs the sum and carry of the previous three inputs.

   A - 000
   B - 001
   C - 010
   D - 011
   E - 100
   F - 101
   G - 110
   H - 111



5. Design a sequential circuit meant to detect the sequence 10101 or 01010. The output should equal "1" each time this sequence is detected. Upon detection the system does not revert to its initial state and there may be overlap between the previous sequence and the next one. Draw the MOORE State-diagram. Realize the system using T Flip-Flops.

A - 0
B - 1
C - 01
D - 10
E - 010
F - 101
G - 0101
H - 1010
I - 01010
J - 10101



ps					NS								Z
					X=0				X=1				
	Y3	Y2	Y1	Y0	y3	y2	y1	y0	y3	y2	y1	y0	
A	0	0	0	0	0	0	0	0	0	0	1	0	0
B	0	0	0	1	0	0	1	1	0	0	0	1	0
C	0	0	1	0	0	1	0	0	0	0	0	1	0
D	0	0	1	1	0	0	0	0	0	1	0	1	0
E	0	1	0	0	0	0	0	0	0	1	1	0	0
F	0	1	0	1	0	1	1	1	0	0	0	1	0
G	0	1	1	0	0	0	0	1	0	0	0	1	0
H	0	1	1	1	0	0	0	0	1	0	0	1	0
I	1	0	0	0	0	0	0	0	1	0	0	1	1
J	1	0	0	1	1	0	0	0	0	0	0	1	1

ps					NS								Z
					X=0				X=1				
	Y3	Y2	Y1	Y0	T3	T2	T1	T0	T3	T2	T1	T0	
A	0	0	0	0	0	0	0	0	0	0	1	0	0
B	0	0	0	1	0	0	1	0	0	0	0	0	0
C	0	0	1	0	0	1	1	0	0	0	1	1	0
D	0	0	1	1	0	0	1	1	0	1	1	0	0
E	0	1	0	0	0	1	0	0	0	0	1	0	0
F	0	1	0	1	0	0	1	0	0	1	0	0	0

G	0	1	1	0	0	1	1	1	0	1	1	1	0
H	0	1	1	1	0	1	1	1	1	1	1	0	0
I	1	0	0	0	1	0	0	0	0	0	0	1	1
J	1	0	0	1	0	0	0	1	1	0	0	0	1

X’	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’	X	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’
Y1’Y0’	0	0	ϕ	1	Y1’Y0’	0	0	ϕ	0
Y1’Y0	0	0	ϕ	0	Y1’Y0	0	0	ϕ	1
Y1Y0	0	0	ϕ	ϕ	Y1Y0	0	1	ϕ	ϕ
Y1Y0’	0	0	ϕ	ϕ	Y1Y0’	0	0	ϕ	ϕ

T3 = Y3Y0X + Y3Y0’X’ + Y2Y1Y0X

X’	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’	X	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’
Y1’Y0’	0	1	ϕ	0	Y1’Y0’	0	0	ϕ	0
Y1’Y0	0	0	ϕ	0	Y1’Y0	0	1	ϕ	0
Y1Y0	0	1	ϕ	ϕ	Y1Y0	1	1	ϕ	ϕ
Y1Y0’	1	1	ϕ	ϕ	Y1Y0’	0	1	ϕ	ϕ

T2 = Y2Y1’Y0’X’ + Y2Y1 + Y1Y0’X’ + Y2Y0X + Y1Y0X

X’	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’	X	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’
Y1’Y0’	0	0	ϕ	0	Y1’Y0’	1	1	ϕ	0
Y1’Y0	1	1	ϕ	0	Y1’Y0	0	0	ϕ	0
Y1Y0	1	1	ϕ	ϕ	Y1Y0	1	1	ϕ	ϕ
Y1Y0’	1	1	ϕ	ϕ	Y1Y0’	1	1	ϕ	ϕ

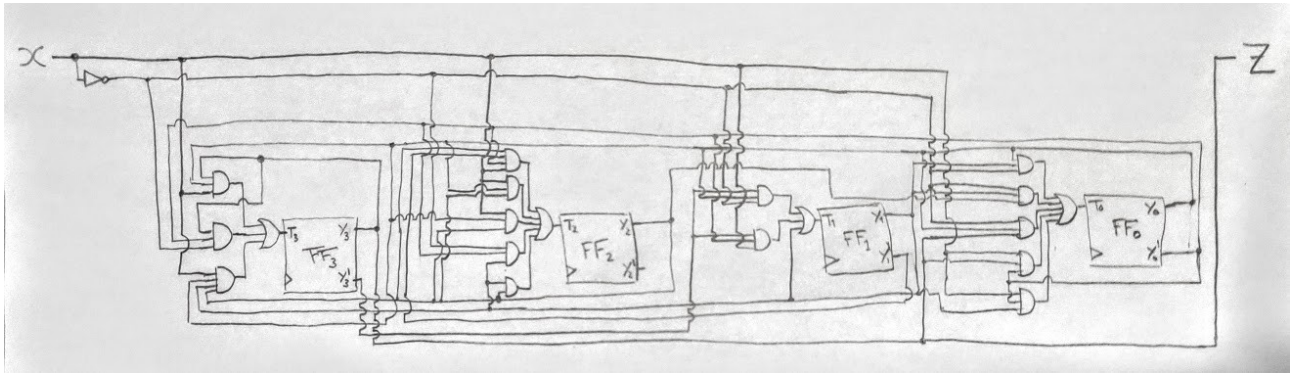
T1 = Y3’Y0X’ + Y1 + Y3’Y0’X

X’	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’	X	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’
Y1’Y0’	0	0	ϕ	0	Y1’Y0’	0	0	ϕ	1
Y1’Y0	0	0	ϕ	1	Y1’Y0	0	0	ϕ	0
Y1Y0	1	1	ϕ	ϕ	Y1Y0	0	0	ϕ	ϕ
Y1Y0’	0	1	ϕ	ϕ	Y1Y0’	1	1	ϕ	ϕ

T0 = Y1Y0X’ + Y2Y1X’ + Y3Y0X’ + Y3Y0’X + Y1Y0’X

	Y3’Y2’	Y3’Y2	Y3Y2	Y3Y2’
Y1’Y0’	0	0	ϕ	1
Y1’Y0	0	0	ϕ	1
Y1Y0	0	0	ϕ	ϕ
Y1Y0’	0	0	ϕ	ϕ

Z = Y3


x
z
T_3
FF_3
Y_3
Y_3'
T_2
FF_2
Y_2
Y_2'
T_1
FF_1
Y_1
Y_1'
T_0
FF_0
Y_0
Y_0'