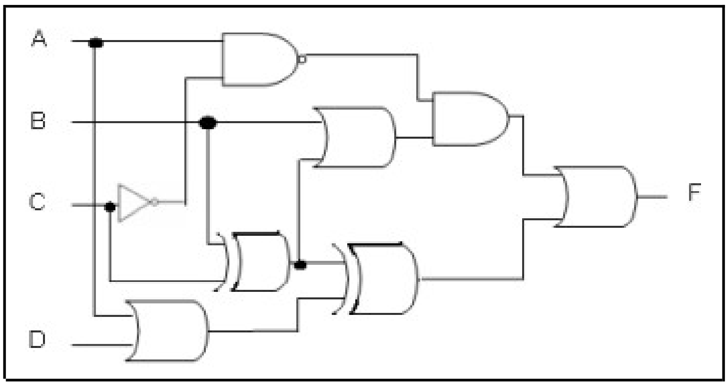
Digital Systems HW4

1. What function accurately describes the following circuit?



f(A,B,C,D)=(AC’)’(B+(B⊕C))+(B⊕C)⊕(A+D)

A	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
B	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
C	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
D	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
f	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1

	A’B’	A’B	AB	AB’
C’D’	0	1	0	1
C’D	1	1	0	1
CD	1	1	1	1
CD’	1	1	1	1

f(A,B,C,D) = C + AB’ + A’B + A’D

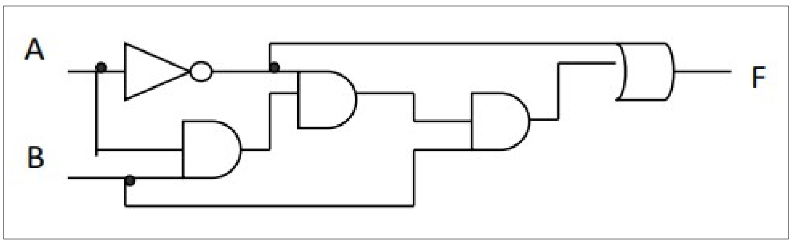
2. For each of the following logical circuits:

   a) Write out the corresponding function.

   b) Simplify as much as possible.

   c) Write out the corresponding truth table.

   d) Draw the simplified circuit.

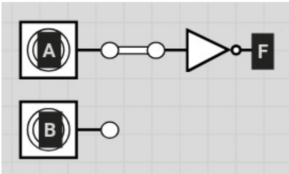


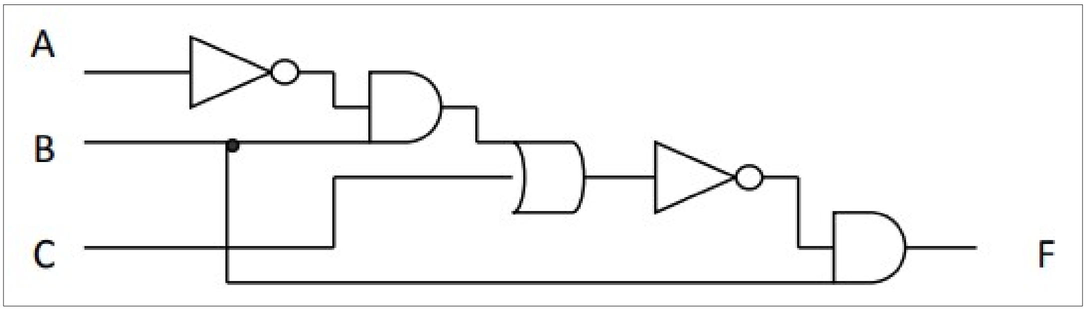
I. F(A,B) = A’ + (A’(AB))B

II. F(A,B) = A’

III.

A	0	0	1	1
B	0	1	0	1
F	1	1	0	0

IV. 



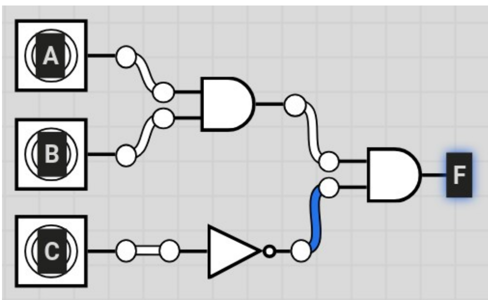
I. F(A,B,C) = B(C+BA’)’

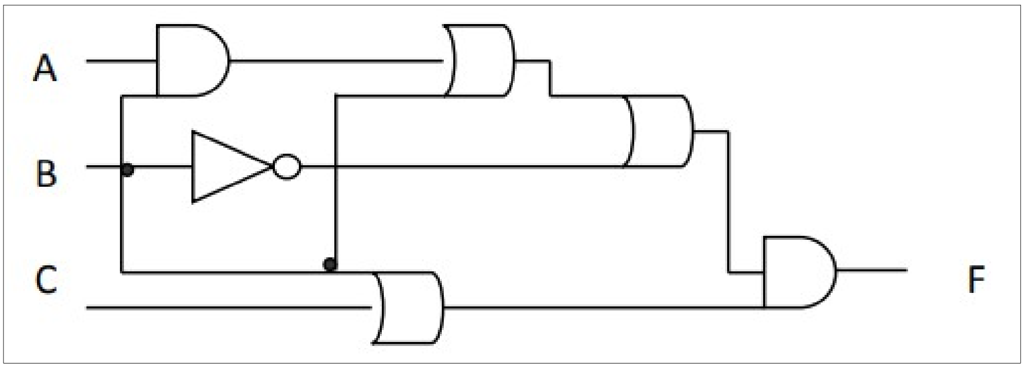
II.F(A,B,C) = B(C’(BA’)’) = BC’(B’+A) = BC’B’+BC’A = ABC’

III.

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
c	0	1	0	1	0	1	0	1
F	0	0	0	0	0	0	1	0

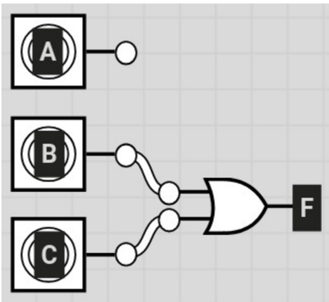
IV.

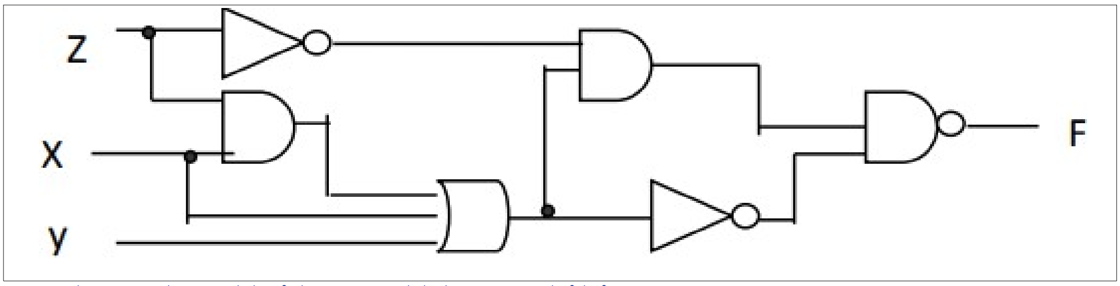




I. F(A,B,C) = (AB+B+B’)(B+C)
II. F(A,B,C) = B+C
III.

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
c	0	1	0	1	0	1	0	1
F	0	1	1	1	0	1	1	1

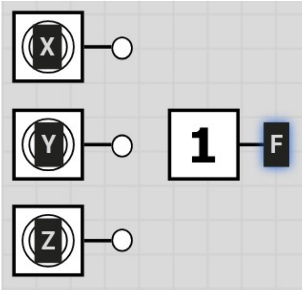
IV. 

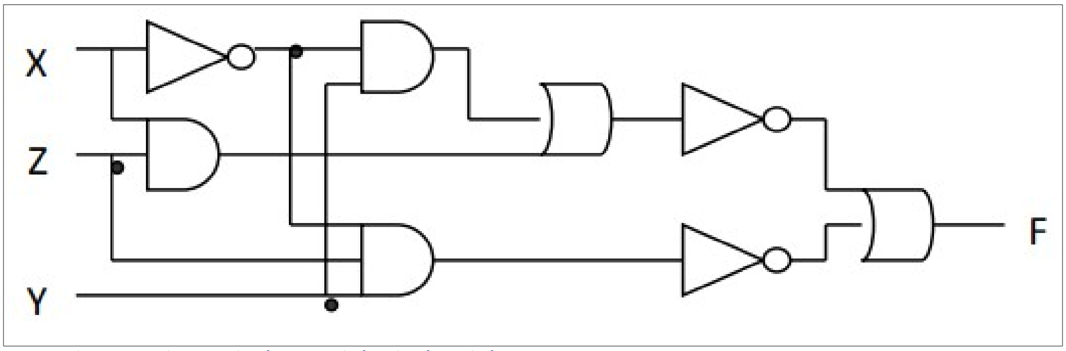


I. F(Z,X,Y) = ((Z’(ZX+X+Y))(ZX+X+Y)’)’
II. F(Z,X,Y) = (Z’(ZX+X+Y))’+(ZX+X+Y)
= Z+(ZX+X+Y)’+(ZX+X+Y)
= Z+(ZX)’X’Y’+ZX+X+Y
= Z+(Z’+X’)X’Y’+ZX+X+Y
= Z+Z’X’Y’+X’X’Y’+ZX+X+Y
= X+Y+Z+X’Y’+X’Y’
= X+Y+Z+Y’+X’
= 1
III.

Z	0	0	0	0	1	1	1	1
X	0	0	1	1	0	0	1	1
Y	0	1	0	1	0	1	0	1
F	0	1	1	1	1	1	1	1

IV.





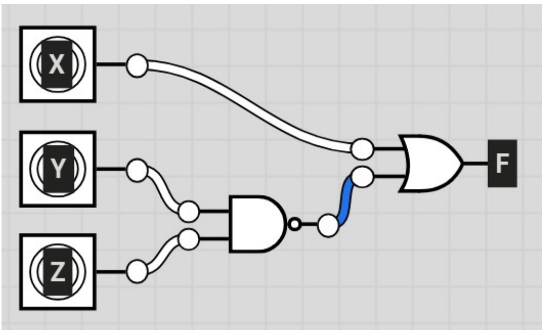
I. F(Z,X,Y) = (X’Y+XZ)’+(X’ZY)’

II. F(Z,X,Y) = (X’Y)’(XZ)’+X+Z’+Y’
    = (X+Y’)(X’+Z’)+X+Z’+Y’
    = XX’+XZ’+Y’X’+Y’Z’+X+Z’+Y’
    = X+Z’+Y’

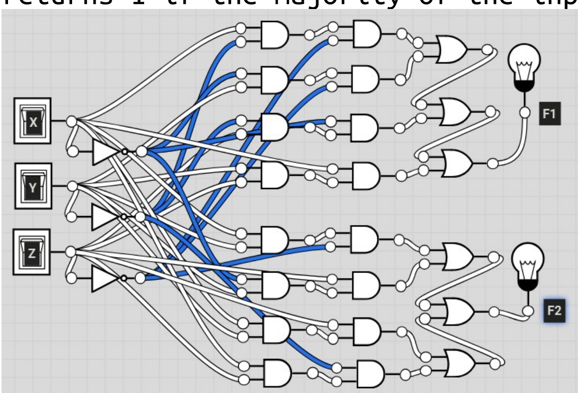
III.

X	0	0	0	0	1	1	1	1
Z	0	0	1	1	0	0	1	1
Y	0	1	0	1	0	1	0	1
F	1	1	1	0	1	1	1	1

IV.



3. Design a circuit with three inputs (x,y,z) and two outputs (F1 and F2). F1 returns the appropriate parity bit corresponding to the three inputs. F2 returns 1 if the majority of the inputs are on ("1"), and 0 otherwise.



a) Write out the truth table for functions F1 and F2.

X	0	0	0	0	1	1	1	1
Y	0	0	1	1	0	0	1	1
Z	0	1	0	1	0	1	0	1
F1	0	1	1	0	1	0	0	1
F2	0	0	0	1	0	1	1	1

b) Express F1 and F2 as standard SOP functions.

F1(X,Y,Z) = X'Y'Z+X'YZ'+XY'Z'+XYZ

F2(X,Y,Z) = X'YZ+XY'Z+XYZ'+XYZ

c) Simplify the expressions for the functions.

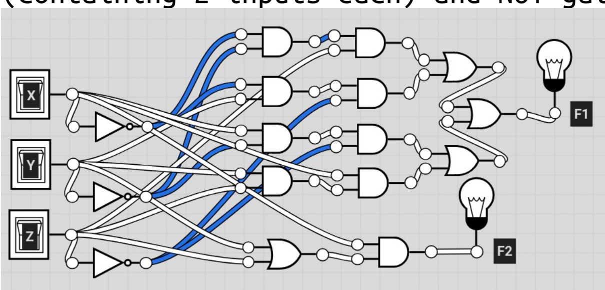
F1	**X'Y'**	**X'Y**	**XY**	**XY'**
Z'	**0**	**1**	**0**	**1**
Z	**1**	**0**	**1**	**0**

F1(X,Y,Z) = X'Y'Z+X'YZ'+XY'Z'+XYZ

F2	**X'Y'**	**X'Y**	**XY**	**XY'**
Z'	**0**	**0**	**1**	**0**
Z	**0**	**0**	**1**	**1**

F2(X,Y,Z) = XY+XZ = X(Y+Z)

d) Realize the functions (draw the logic circuit) using AND and OR gates (containing 2 inputs each) and NOT gates.



4. We wish to design a circuit capable of receiving a student's grade at the input and giving a 1 bit pass fail indicator at the output. Any grade 64 and above is considered passing, and would require an output of "1" any any grade lower an output of "0".

a) How many inputs are necessary?

7 because $2^7 = 128 > 100$, and $2^6 = 64 < 100$.

b) Write out the appropriate truth table.

A	B	C	D	E	F	G	f
0	0	0	0	0	0	0	0
0	..	..	..	..	..	..	0
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	..	..	..	..	..	..	1
1	1	0	0	1	0	0	1
1	1	0	0	1	0	0	Φ
1	1	..	..	..	..	..	Φ
1	1	1	1	1	1	1	Φ

c) Write the function in SOP form.

$f(A,B,C,D,E,F,G) = \Sigma(64, 65, \ldots, 99, 100) + \Sigma_\phi(101, 102, \ldots, 126, 127)$

$= A$

d) Realize the corresponding logic circuit.