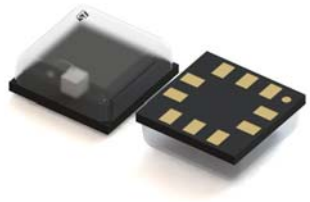
UVIS25

Digital UV Index sensor: 0 - 15 UV Index output range

Datasheet - preliminary data



LGA-10L
(2.5 x 2.5 x 0.76 mm)

Features

- 0 - 15 UV Index output range
- Resolution: UVI/16
- Active and power down modes
- Continuous reading at 1 Hz ODR / one shot mode
- Interrupt functions: Data Ready and UVI thresholds
- SPI and I²C interfaces
- Supply voltage: 1.7 to 3.6 V
- ECOPACK® lead-free compliant

Applications

- UV Index measurements
- Wearable devices
- Smartphone and tablet
- Weather stations

Description

The UVIS25 is a digital UV Index sensor able to provide an accurate measurement of the Ultraviolet radiation index (UVI) from the sunlight. It includes a sensing element and a mixed signal ASIC to provide the UV Index data trough I^2C and SPI interfaces.

A dedicated technology has been developed to achieve the best accuracy for UV Index measurements.

The UVIS25 allows the measurement of the UV Index, without the need of a dedicated algorithm to calculate the UV Index and without specific calibrations at customer manufacturing line.

The device can be configured to generate interrupt events based on a threshold crossing or when a new set of data is generated. The event is available in a register as well as in a dedicated pin.

The UVIS25 is available in a full-mold LGA package (LGA). It is guaranteed to operate over a temperature range extending from -20°C to +85°C. The package is transparent to allow external solar radiation to reach the sensing element.

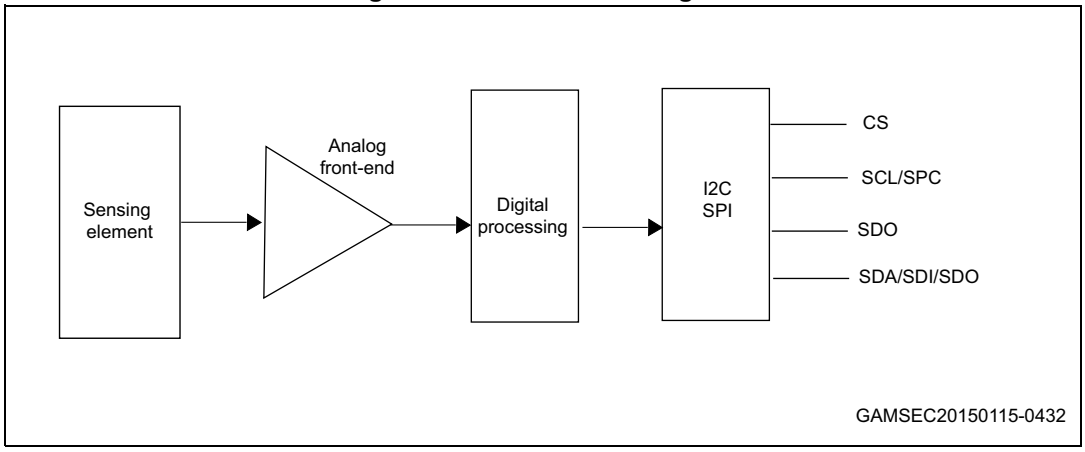
Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
UVIS25TR	-20 to +85	LGA-10L	Tape and reel

Contents

1 Block diagram and pin description

Figure 1. UVIS25 block diagram



1.1 Pin description

Figure 2. Pin layout (bottom view)

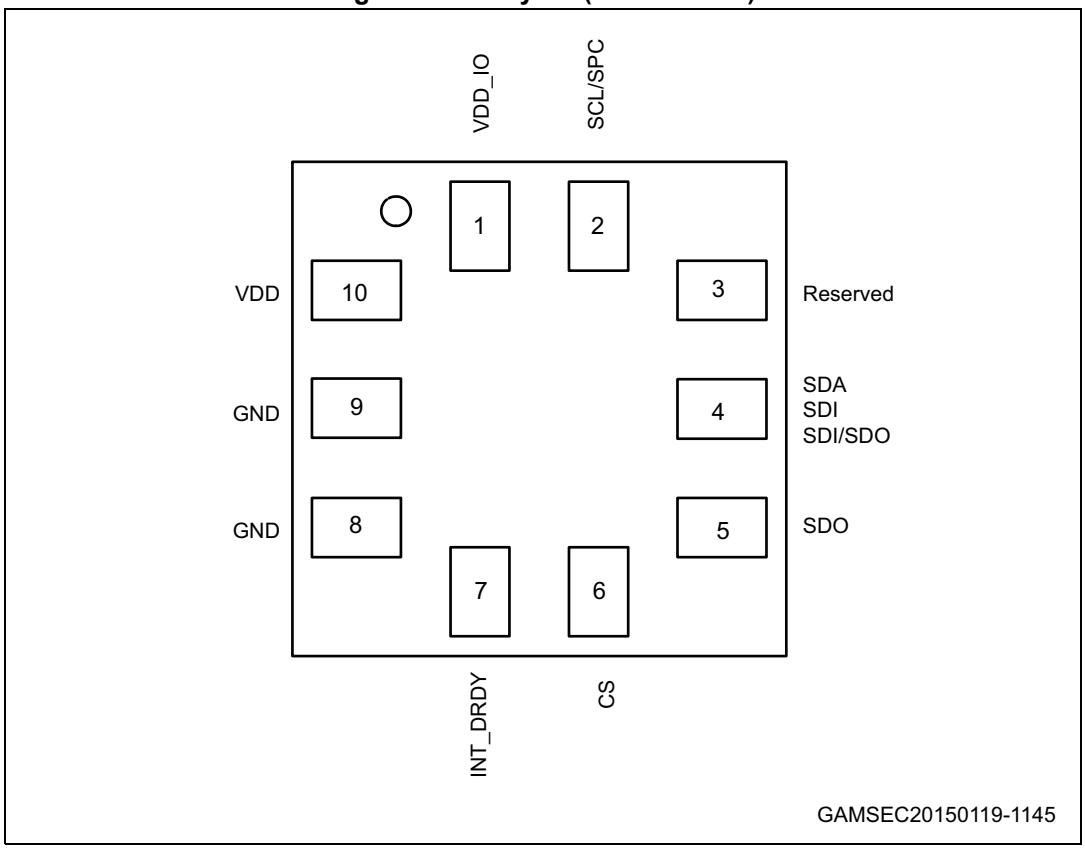


Table 2. Pin description

Pin number	Name	Function
1	VDD_IO	Power supply for I/O pins
2	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
3	Reserved	Connect to GND
4	SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
5	SDO	4-wire SPI serial data output (SDO)
6	CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
7	INT_DRDY	Interrupt or Data Ready
8	GND	0 V supply
9	GND	0 V supply
10	VDD	Power supply

2 Sensor parameters and electrical specifications

Conditions V_{DD} = 2.5 V, T = 25 °C, unless otherwise noted.

Table 3. Sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
UVIr	UV Index range		0		15	
UVIres	UV Index resolution			1/16		UV Index
ODR	Output data rate	Continuous reading		1		Hz
Top	Operating temperature range		-20		+85	°C

1. Typical specifications are not guaranteed.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.7		3.6	V
Vdd_IO	IO supply voltage		1.7		Vdd+0.1	V
Idd	Supply current @ ODR 1 Hz			10		µA
IddPdn	Supply current in power-down mode T = 25 °C			1.8		µA

1. Typical specifications are not guaranteed.

2.1 Absolute maximum ratings

Stress above those listed as "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

3 Functionality

The UVIS25 is a high resolution, digital output UVI sensor packaged in an LGA full-mold package. The device has been optimized for the UVI measurement to provide high level of accuracy: the UVIS25 allows the measurement of the UV Index, without the need of a dedicated algorithm to calculate the UV Index and without specific calibrations at customer manufacturing line.

3.1 I²C interface

The UV Index data may be accessed through an I²C or SPI interface, making the device particularly suitable for direct interfacing with a microcontroller.

The UVIS25 features a Data-Ready signal which indicates when a new UV Index is measured simplifying data synchronization or an interrupt generator that can identify if the UV Index crosses a threshold.

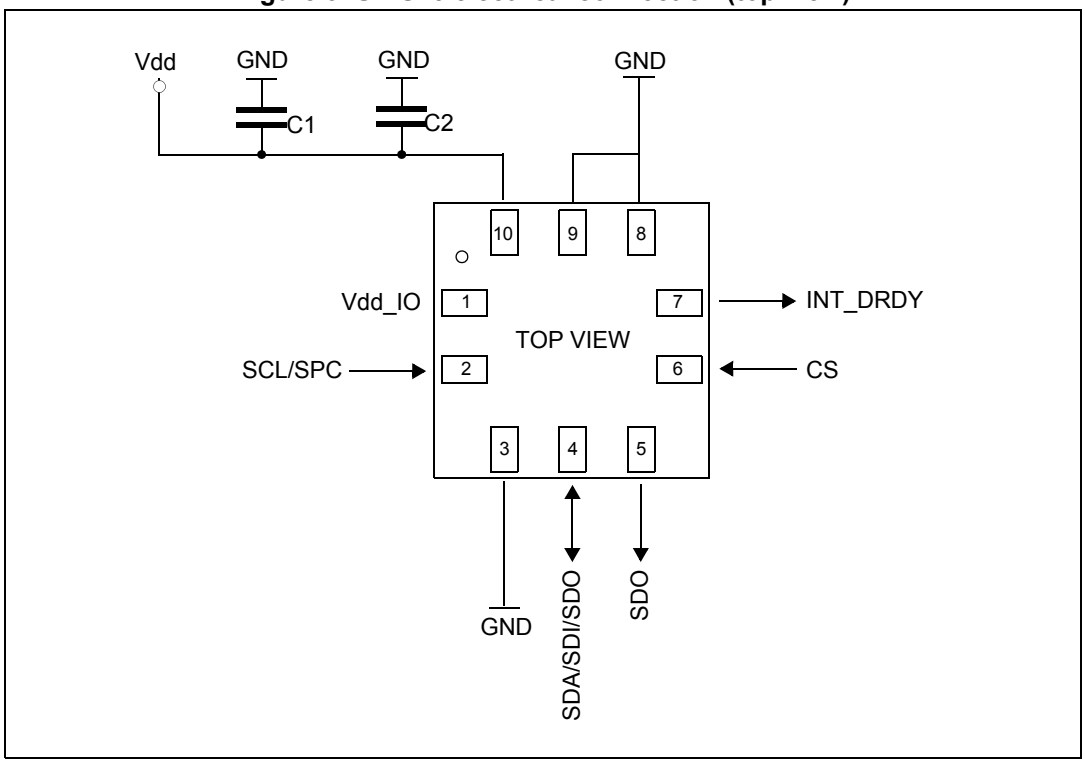
The two events are available on a register (*7.8: STATUS_REG (27h)*) or a dedicated pin (INT_DRDY) can be configured.

3.2 Factory calibration

The IC interface is factory calibrated to measure the sun radiation. The calibration data are stored inside the device in a non-volatile memory. Any time the device is turned on, the calibration data are downloaded into the registers to be used during the active operation. This allows to use the device without further calibration.

4 Application hints

Figure 3. UVIS25 electrical connection (top view)



The device core is supplied through the Vdd line. Power supply decoupling capacitors C_1 (100 nF) and C_2 (4.7 µF) should be placed as near as possible to the supply pad of the device (common design practice).

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I²C, CS must be tied to Vdd_IO.

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 3*). It is possible to remove VDD while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

4.1 Soldering information

The LGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

5 Digital interfaces

The registers embedded in the UVIS25 may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 6. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I2C communication enabled; 0: SPI communication mode / I2C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
SDO	4 - wire SPI serial data output (SDO)

5.1 I²C serial interface

The UVIS25 I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in *Table 7*.

Table 7. Serial interface pin description

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initiates a transfer generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the standard mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the UVIS25 is 1000111 (47h).

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the UVIS25 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address (SUB) will be transmitted: the 7 LSB represents the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is '1', the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit: 1000111b If the bit "b" is set to'1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit "b" is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 8* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 8. SAD+Read/Write patterns

Command	SAD[7:1]	R/W	SAD+R/W
Read	1000111	1	1000111 (8Fh)
Write	1000111	0	1000111 (8Eh)

Table 9. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 10. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 11. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 12. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB (7) must be equal to 1 while SUB (6-0) represents the address of the first register to be read.

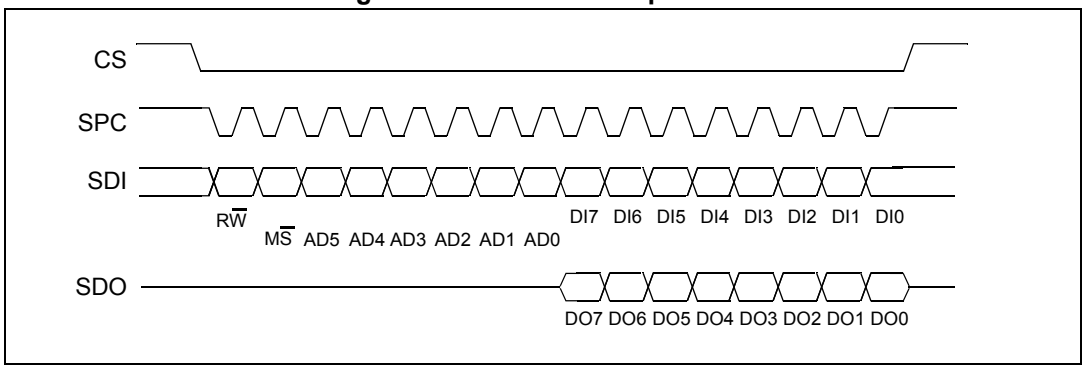
In the presented communication format MAK is Master acknowledge, and NMAK is no master acknowledge.

5.2 SPI bus interface

The UVIS25 SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 4. Read and write protocol



CS is the serial port enable, and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock, and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or multiples of 8 in the case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling

edge of **CS** while the last bit (bit 15, bit 23,...) begins at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: MS bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

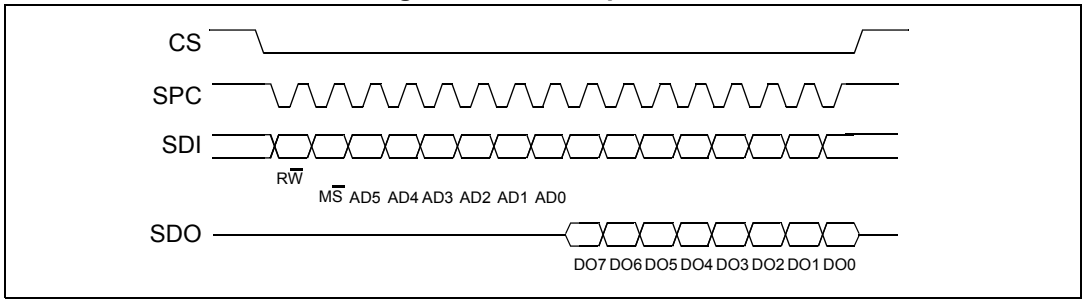
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the MS bit is 0 the address used to read/write data remains the same for every block. When MS bit is 1 the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 5. SPI read protocol



The SPI Read command is performed with 16 clock pulses. The multiple-byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

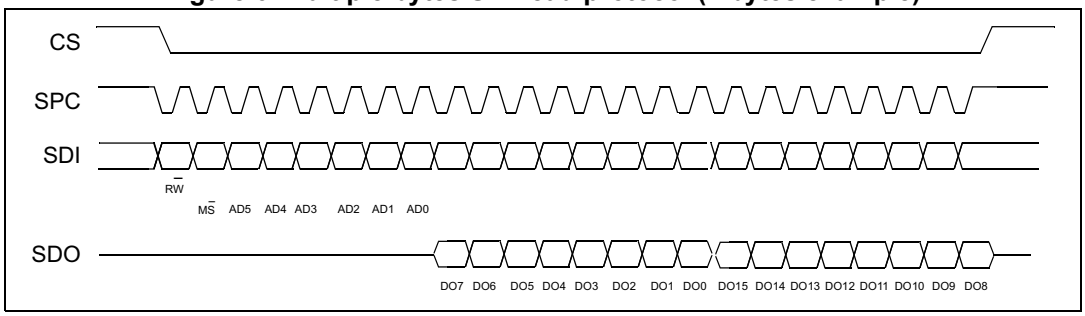
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

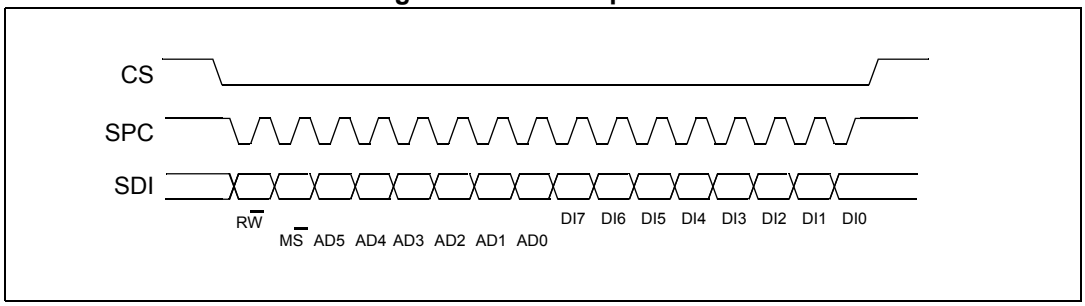
bit 16-...: data DO(...-8). Further data in multiple byte readings.

Figure 6. Multiple bytes SPI read protocol (2 bytes example)



5.2.2 SPI write

Figure 7. SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

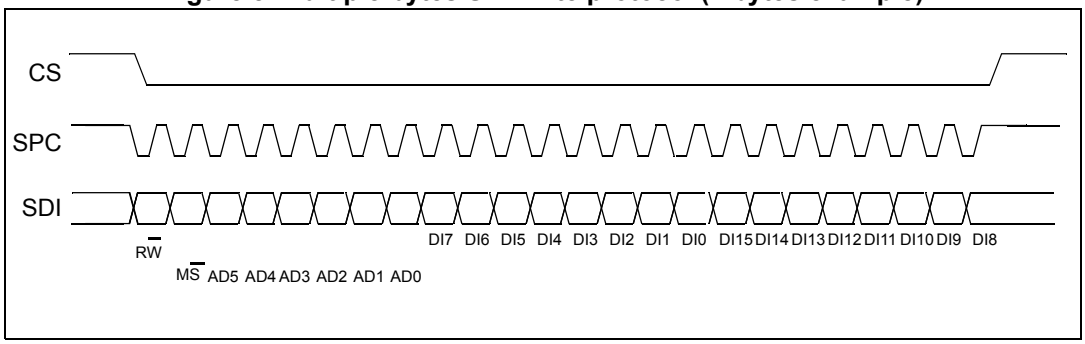
bit 1: $\overline{MS}$ bit. When 0 do not increment the address, when 1 increment the address in multiple writings.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

bit 16-...: data DI(...-8). Further data in multiple byte writings.

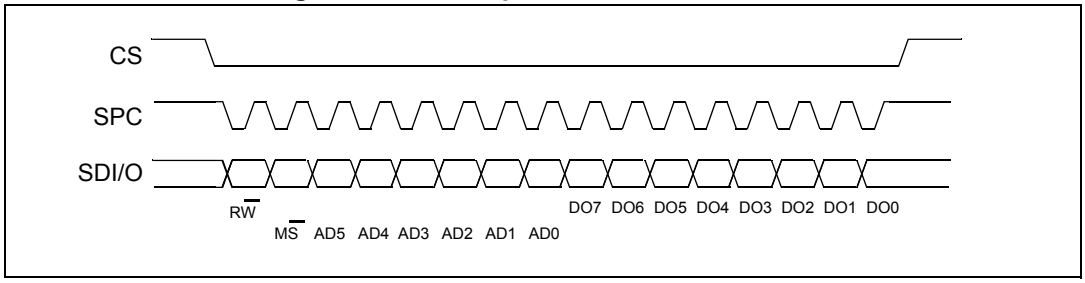
Figure 8. Multiple bytes SPI write protocol (2 bytes example)



5.2.3 SPI read in 3-wires mode

A 3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in *7.2: CTRL_REG1 (20h)*.

Figure 9. SPI read protocol in 3-wires mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: $\overline{MS}$ bit. When 0, do not increment the address, when 1, increment the address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Register mapping

Table 13 provides a quick overview of the 8-bit registers embedded in the device.

Table 13. Registers address map

Name	Type	Register address	Default	Function and comment
		Hex		
Reserved	-	00-0E	-	Reserved
WHO_AM_I	R	0F	11001010	ID register
Reserved	-	10-1F	-	Reserved
CTRL_REG1	R/W	20	00000000	
CTRL_REG2	R/W	21	00000000	
CTRL_REG3	R/W	22	00000000	
INT_CFG	R/W	23	00000000	
INT_SOURCE	R	24	00000000	
THS_UV	R/W	25	00000000	
Reserved	-	26	-	Reserved
STATUS_REG	R	27	00000000	
UV_OUT_REG	R	28	output	

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the previous table must not be accessed, and the content stored in those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve UV index data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

7.1 WHO_AM_I (0Fh)

Device who am I

7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	0

7.2 CTRL_REG1 (20h)

Control register 1

7	6	5	4	3	2	1	0
0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	BDU	ODR

1. These bits must be set to ‘0’ to ensure proper operation of the device

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
ODR	Enable continuous reading at 1 Hz. Default value: 0 (0: One-shot mode enabled; 1: ODR at 1 Hz)

ODR bit enables the continuous reading of the UV Index at 1 Hz.. When ODR is set to ‘0’ the device enables the one-shot mode. When ‘ONESHOT’ bit in *7.3: CTRL_REG2 (21h)* is set to ‘1’, a new UV Index value is acquired.

If ODR bit and 'ONESHOT’ bit in *7.3: CTRL_REG2 (21h)* are set to '0', the device is in power down mode. If ODR bit is set to '1', ‘ONESHOT’ bit in *7.3: CTRL_REG2 (21h)* must be '0'.

7.3 CTRL_REG2 (21h)

Control register 2

7	6	5	4	3	2	1	0
BOOT	0(1)	0(1)	I²C_DS	SIM	0(1)	0(1)	ONE_SHOT

1. These bits must be set to ‘0’ to ensure proper operation of the device

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content). The bit is self-cleared when the BOOT is completed.
I²C_DS	Disable I2C interface. Default value: 0 (0: I2C enable;1: I2C disable)
SIM	SPI Serial Interface Mode Selection.Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
ONE_SHOT	One shot enable. Default value: 0 (0: waiting for start of conversion; 1: start for a new dataset)

BOOT bit is used to refresh the content of the internal registers stored in the Flash memory block. At the device power-up, the content of the Flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason, the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When BOOT bit is set to ‘1’ the content of the internal Flash is copied into the corresponding internal registers and is used to calibrate the device. These values are factory trimmed, and they are different for every device. They permit good behavior of the device and generally they should not be changed. At the end of the boot process, the BOOT bit is set again to ‘0’ by hardware. BOOT bit takes effect after one ODR clock cycle.

ONE_SHOT bit is used to start a new conversion when the ODR bit in *7.2: CTRL_REG1 (20h)* is set to ‘0’. Writing a ‘1’ in ONE_SHOT triggers a single measurement of the UV Index. Once the measurement is done, the ONE_SHOT bit will self-clear, the new data is available in the output registers, and the *7.8: STATUS_REG (27h)* bits are updated. If ODR bit in *7.2: CTRL_REG1 (20h)* is set to '1', ‘ONESHOT’ bit in must be '0'.

7.4 CTRL_REG3 (22h)

Interrupt control

7	6	5	4	3	2	1	0
INT_H_L	PP_OD	0(1)	0(1)	0(1)	0(1)	INT_S2	INT_S1

1. These bits must be set to ‘0’ to ensure proper operation of the device

NT_H_L	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
PP_OD:	Push-pull/open drain selection on interrupt pads. Default value: 0 (0: push-pull; 1: open drain)
INT_S[2:1]	Data signal on INT_DRDY pin control bits. Default value: 00. Refer to *Table 14*.

Table 14. Interrupt configurations

INT1_S2	INT1_S1	INT1 pin
0	0	Data ready
0	1	UV Index High
1	0	UV Index Low
1	1	UV Index High or Low

The device features one fully-programmable interrupt source (INT) that can be configured to trigger different events.

The device may also be configured to generate, a Data Ready signal (DRDY) which indicates when a new measured UV Index is available, thus simplifying data synchronization in digital systems or to optimize the system power consumption.

7.5 INT_CFG (23h)

Interrupt configuration

7	6	5	4	3	2	1	0
0(1)	0(1)	0(1)	0(1)	DIFF_EN	LIR	UVLE	UVHE

1. These bits must be set to '0' to ensure proper operation of the device

DIFF_EN	Interrupt generation enable. Default value: 0 (0: interrupt circuit disable;1: interrupt circuit enabled)
LIR	Latch interrupt request to the *INT_SOURCE (24h)* register. Default value:0 (0: interrupt request not latched; 1: interrupt request latched)
UVLE	Enable interrupt generation on differential UV low event. Default value:0 (0: disable interrupt request;1: enable interrupt request on measured differential UV values lower than preset threshold)
UVHE	:Enable interrupt generation on differential UV high event .Default value:0 (0: disable interrupt request;1: enable interrupt request on measured differential UV values higher than preset threshold)

7.6 INT_SOURCE (24h)

Interrupt source configuration

7	6	5	4	3	2	1	0
-	-	-	-	-	IA	UVL	UVH

IA	Interrupt Active. Default value:0. (0: no interrupt has been generated; 1: one or more interrupt events have been generated).
UVL	Differential UV low. Default value:0. (0: no interrupt has been generated; 1: UV low event has occurred)
UVH	Differential UV high. Default value:0. (0: no interrupt has been generated; 1: UV high event has occurred)

7.7 THS_UV (25h)

Threshold register

7	6	5	4	3	2	1	0
THS_UV7	THS_UV6	THS_UV5	THS_UV4	THS_UV3	THS_UV2	THS_UV1	THS_UV0

THS_UV[7:0]	This register contains the differential UV Interrupt threshold value for the interrupt generation.

7.8 STATUS_REG (27h)

Status register

7	6	5	4	3	2	1	0
0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	UV_DA

1. These bits must be set to ‘0’ to ensure proper operation of the device

UV_DA	UV data available.Default value:0. (0: UVI data not available; 1: UVI data available). UV_DA is set to 1 whenever a new UVI sample is available. UV_DA is cleared when the *UV_OUT_REG (28h)* is read.

7.9 UV_OUT_REG (28h)

UV Index output register

7	6	5	4	3	2	1	0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

OUT[7:0]	UVI data output value.

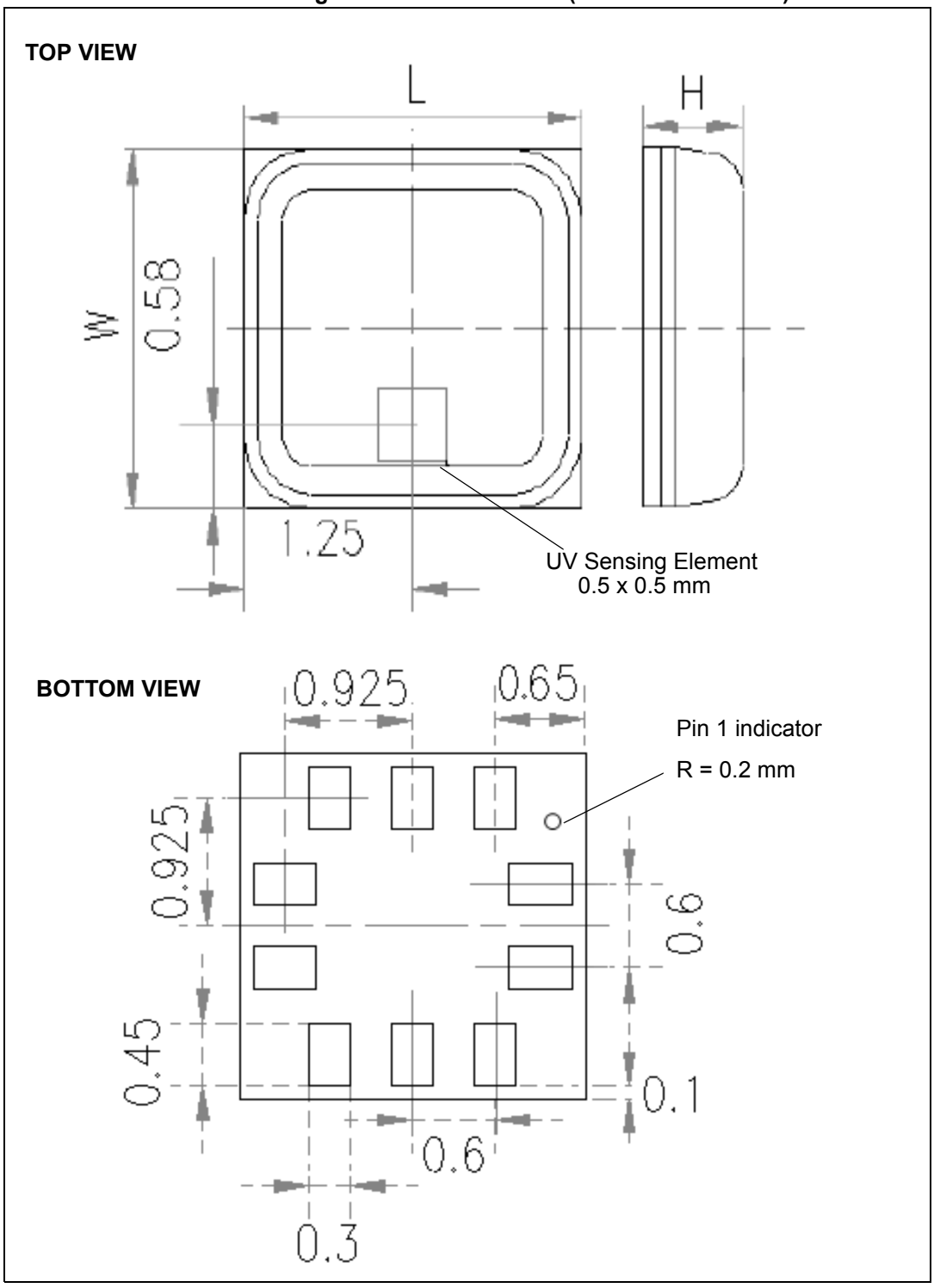
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 15. LGA - 10L (2.5 x 2.5 x 0.76 mm typ) outline and mechanical data

Item	Dimensions (mm)	Tolerance (mm)
Length [L]	2.5	± 0.1
Width [W]	2.5	± 0.1
Height [H]	0.8 MAX	
Pad size	0.30 x 0.45	± 0.05

Table 16. Package outline for LGA-10L (2.5 x 2.5 x 0.76 mm)



9 Revision history

Table 17. Document revision history

Date	Revision	Changes
06-Feb-2015	1	Initial release.