RuuviTag

Pretty Capable Bluetooth Smart Sensor Beacon :P

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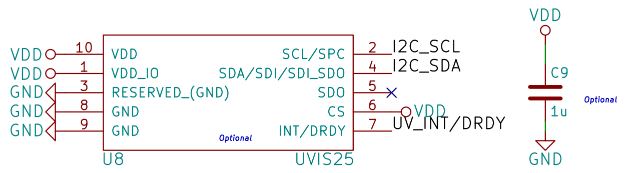
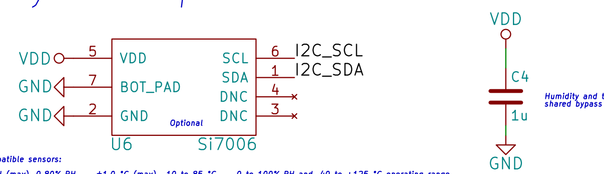
UV Sensor



The slave address (SAD) associated to the UVIS25 is 0b1000111 (47h).

Power-down mode 1.8uA, 1Hz output 10uA

Humidity + Temperature Sensor



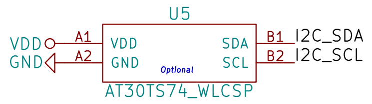
Pin and SW compatible sensors:

Si7006: ± 5% RH (max), 0-80% RH ±1.0 °C (max), -10 to 85 °C 0 to 100% RH and -40 to +125 °C operating range
Si7020: ± 4% RH (max), 0-80% RH ±0.4 °C (max), -10 to 85 °C 0 to 100% RH and -40 to +125 °C operating range
Si7021: ± 3% RH (max), 0-80% RH ±0.4 °C (max), -10 to 85 °C 0 to 100% RH and -40 to +125 °C operating range

150 µA active current 60 nA standby current

I2C 7-bit slave address: 0x40 / 0b100000

Temperature Sensor



Measures temperatures from -55C to 125C.
Standby current consumption 400-600nA.

Manufacturer offers chips with different 7-bit I2C slave addresses. For example:
AT30TS74-UFM10-T's 7-bit address is 0b1001000 and
AT30TS74-UFM17-T's 7-bit address is 0b1001111.

NOTES ABOUT GPIOs:

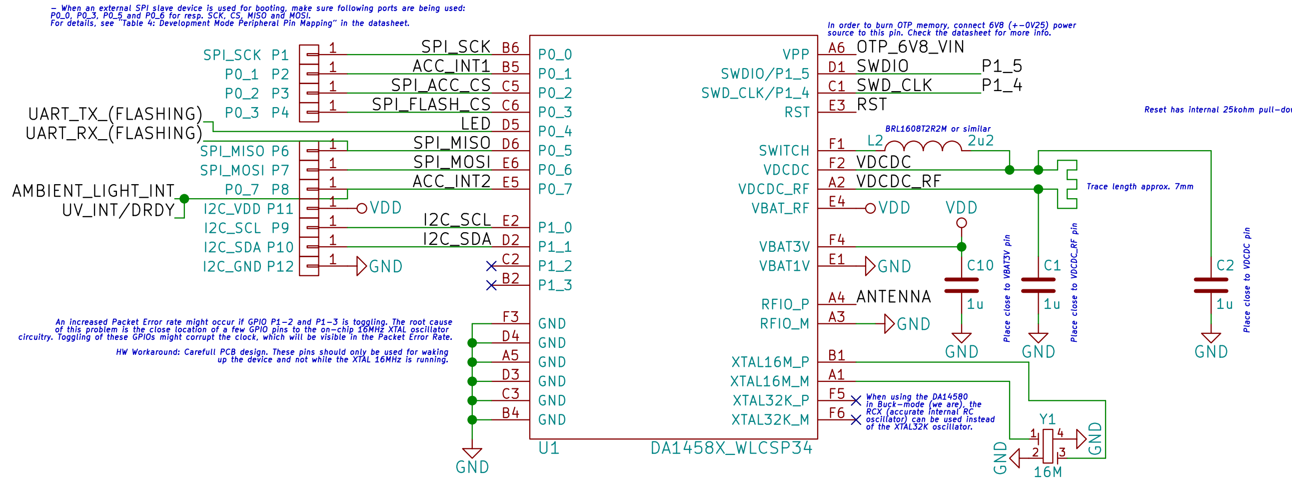
- For UART communication, check that preferably the UART ports P0_4 and P0_5 are used. These are the default ports for the DA14580_01, and these are part of the Boot-Sequence. If not possible, use either one of the other UART pairs: i.e. P0_0/P0_1 or P0_2/P0_3.

- When not using the ADC, make sure the voltage levels at the ports P0_0 thru P0_3 are not higher than Vbat3V in order to prevent that these signals are interfering with internal ADC measurements.

- In case the ADC is being used, check that the voltages at the ADC input ports, P0_0 thru P0_3, are not higher than Vbat3V + 0.2V and never exceeding the maximum level of 3.45 V.

- When an external SPI slave device is used for booting, make sure following ports are being used: P0_0, P0_3, P0_5 and P0_6 for resp. SCK, CS, MISO and MOSI. For details, see "Table 4: Development Mode Peripheral Pin Mapping" in the datasheet.

Bluetooth Smart SoC



In order to burn OTP memory, connect 6V8 (+-0V25) power source to this pin. Check the datasheet for more info.

Reset has internal 25kohm pull-down resistor.

When using the DA14580 in Buck-mode (we are), the RCX (accurate internal RC oscillator) can be used instead of the XTAL32K oscillator.

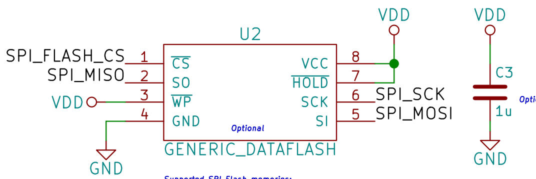
For example: TSX-3225 - 16MHz - 60ohm - 7pF - +-10ppm

! *An increased Packet Error rate might occur if GPIO P1-2 and P1-3 is toggling. The root cause of this problem is the close location of a few GPIO pins to the on-chip 16MHz XTAL oscillator circuitry. Toggling of these GPIOs might corrupt the clock, which will be visible in the Packet Error Rate.*

HW Workaround: Carefull PCB design. These pins should only be used for waking up the device and not while the XTAL 16MHz is running.

The WLCSP casing device is sensitive to sunlight, halogen lamp light and infrared light. Device must be protected against light by a coating or mold compound. Care must be taken that the sides of the WLCSP package are well covered. The proposed process flow is to build a test batch and test the light sensitivity of the application with a halogen lamp before going into production.

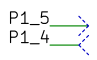
DataFlash



Supported SPI Flash memories:

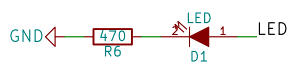
Name	Memory	Page size	
W25X20CL	256 kB	256B	<- the one we're using (W25X20CLZPIG, USON casing)
AT25XE011	128 kB	256B	
W25X10CL	128 kB	256B	
MX25V1006E	128 kB	256B	

Piezo Element



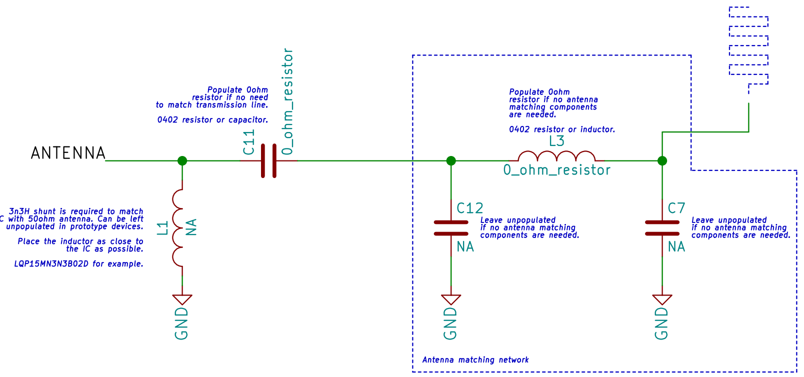
Piezo element can driven using SWD pins (P1_4 and P1_5).

LED



Low forward voltage version 0402 LED, VLMO1500-GS08 for example.

Optional



Populate 0ohm resistor if no need to match transmission line.

0402 resistor or capacitor.

3n3H shunt is required to match SoC with 50ohm antenna. Can be left unpopulated in prototype devices.

Place the inductor as close to the IC as possible.

LQP15MN3N3B02D for example.

Populate 0ohm resistor if no antenna matching components are needed.

0402 resistor or inductor.

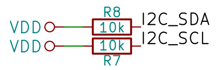
Leave unpopulated if no antenna matching components are needed.

Leave unpopulated if no antenna matching components are needed.

Nordic Semiconductor's 1/4 wavelength monopole antenna design guide states:
When implementing the monopole as a trace on the PCB, the length of the trace should be extended somewhat to allow for some fine-tuning of the antenna to resonance at 2.45GHz. If the size of available ground plane is approaching the ideal size and the antenna trace is uniformly surrounded by the FR4 substrate, then the length of the trace should be extended by about 20%. If the ground plane size is considerably smaller than the ideal size and/or much of the antenna trace is routed close to the edge of the PCB, then the length of the antenna trace should be extended by about 30%.

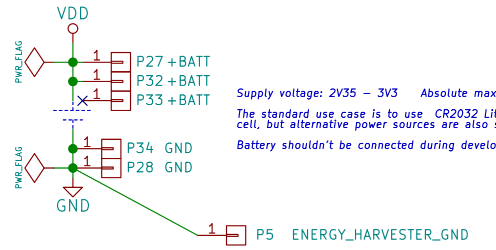
*Theoretical length: L = 92mm / 4 = 23mm -> 23mm * 1.3 = 30mm.*

I2C Pull-ups



Ports has SW configurable 25kohm pull-up resistor, so these resistors aren't probably needed (in low speeds).

Power Source

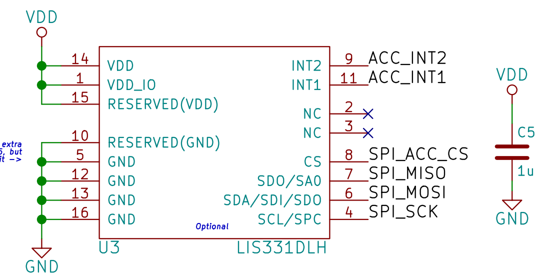


Supply voltage: 2V35 - 3V3 Absolute maximum: 3V6

The standard use case is to use CR2032 Lithium coin cell, but alternative power sources are also supported.

Battery shouldn't be connected during developing/flashing.

Accelerometer

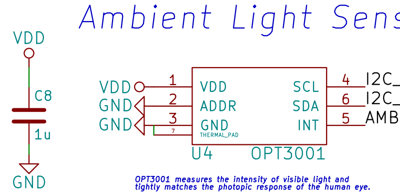


ADXL363 has extra ADC input in pin 5, but we're not supporting it ->

Accelerometer choices:

STM LIS331DLH (+-8G, 16-bit, 1uA shutdown, 10uA low-current mode)
STM H3LIS331DL (+-400G, 16-bit, 1uA shutdown, 10uA low-current mode)
Analog Devices ADXL363 (+-8G, 12-bit, 10nA standby, 270nA low-current mode)

Ambient Light Sensor

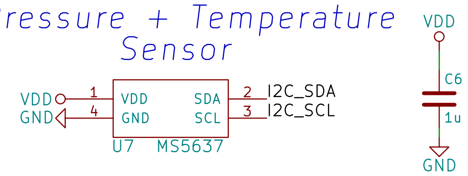


The OPT3001 is fully self-contained to measure the ambient light and report the result in lux digitally over the I2C bus. The result can also be used to alert a system and interrupt a processor with the INT pin. The result can also be summarized with a programmable window comparison and communicated with the INT pin. INT is active low -> pull-up the INT pin from SW.

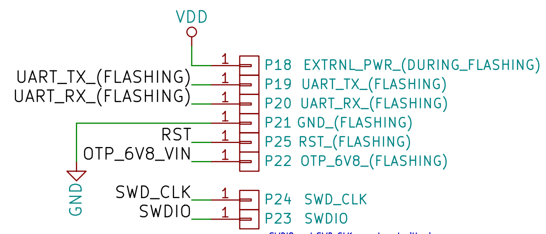
OPT3001 measures the intensity of visible light and tightly matches the photopic response of the human eye.

1.8 µA active current, 300 nA shutdown current
I2C 7-bit slave address (when ADDR pin is tied to GND): 0x44 / 0b1000100

Pressure + Temperature Sensor



Flashing/Debug



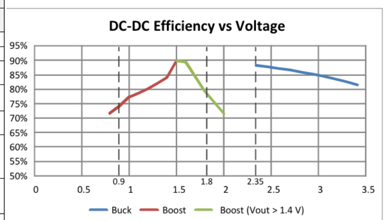
SWDIO and SWD_CLK are shared with piezo.

The DA1458x can boot from external serial devices when the OTP memory is not programmed, to enable development of the application code. At power-up the system enters Development Mode, where the boot code decides which interface to boot from. Application note AN-B-001 describes the booting sequence for all supported serial interfaces and provides the developer with the necessary information for realising the protocol required for establishing communication between an external device and the DA1458x.

To allow for maximum flexibility, a predefined number of pins are examined and utilised at boot time to communicate with external devices using the three serial interfaces available on chip: UART, SPI and I2C. SPI and I2C can be masters on the DA1458x side expecting to communicate with an external slave device and SPI can also be slave expecting to communicate with an external master.

Table 2: Comparison between external memory and OTP

	DA14580 with OTP usage	DA14580 without OTP usage	
	OTP	SPI Flash (W25X10CL)	I2C EEPROM (M24M01-RMN)
Supply voltage	0.9V – 3.3V	2.3 – 3.6V	1.8 – 5.5V
Memory size	32 kB	128 kB	128 kB
Peak read current (@ 1 MHz)	0.6 mA	2 mA	1.5 mA
Programming / Erase current	1.5 mA (only once during production)	15 mA	2 mA
Time to mirror to SRAM (with 32 kB of data)	1.2 ms *(1)*	202.2 ms *(2)*	3.18 sec *(3)*
Energy consumption during mirroring to SRAM	2.3 µC	385 µC (using default 2 MHz clock speed for SPI bus)	5655 µC (using default 100 kbit/s speed for I2C bus)
Deep power down current	0µA (switched off during the sleep time)	1µA	3µA
Operating range	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C



The DA14581 is optimized for deeply embedded applications such as health monitoring, sports measuring, human interaction devices etc. Customers are able to develop and test their own applications. Upon completion of the development, the application code can be programmed into the OTP. In general, the system has three functional modes of operation:

A. Development mode: During this phase application code is developed using the ARM Cortex-M0 SW environment. The compiled code is then downloaded into the System RAM or any Retention RAMs by means of SWD (JTAG) or any serial interface (e.g. UART). Address 0x00 is remapped to the physical memory that contains the code and the CPU is configured to reset and execute code from the remapped device. This mode is enabling application development, debugging and on-the-fly testing.

B. Normal mode: After the application is ready and verified, the code can be burned into the OTP. When the system boots/wakes up, the DMA of the OTP controller will automatically copy the program code from the OTP into the system RAM. Next, a SW reset or a jump to the System RAM occurs and code execution is started. Hence, in this mode, the system is autono- mous, contains the required SW in OTP and is ready for integration into the final product.

C. Calibration mode: Between Development and Normal mode, there is an intermediate stage where the chip needs to be calibrated with respect to two important features:
- *Programming of the Bluetooth device address*
- *Programming of the trimming value for the external 16 MHz crystal.*

This mode of operation applies to the final product and is performed by the customer. During this phase, certain fields in the OTP should be programmed.

There are four different power modes in the DA14580:

- *Active mode: System is active and operates at full speed.*
- *Sleep mode: No power gating has been pro- grammed, the ARM CPU is idle, waiting for an inter- rupt. PD_SYS is on. PD_PER and PED_RAD depending on the programmed enabled value.*
- *Extended Sleep mode: All power domains are off except for the PD_AON, the programmed PD_RRx and the PD_SR. Since the SysRAM retains its data, no OTP mirroring is required upon waking up the system.*
- *Deep Sleep mode: All power domains are off except for the PD_AON and the programmed PD_RRx. This mode dissipates the minimum leakage power. However, since the SysRAM has not retained its data, an OTP mirror action is required upon waking up the system.*

The DA14581 has software-configurable I/O pin assignment, organized into ports Port 0, Port 1 and Port 2. Port 2 is only available in the QFN40 package.

Features:
- *Port 0: 8 pins, Port 1: 6 pins (including SW_CLK and SWDIO), Port 2: 10 pins*
- *Fully programmable pin assignment (!)*
- *Selectable 25 kohm pull-up, pull-down resistors per pin*
- *Pull-up voltage either VBAT3V (BUCK mode) or VBAT1V (BOOST mode) configurable per pin*
- *Fixed assignment for analog pin ADC[3:0]*
- *Pins retain their last state when system enters the Extended or Deep Sleep mode.*

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Title: RuuviTag

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