HUJI'S ENGINEERS

סדנה מעשית אלקטרוניקה 1

סדנה מעשית באלקטרוניקה , שמטרתה להקנות בסיס של עבודה עם רכיבים אלקטרוניים.
הסדנה תועבר על ידי אלדד הלרמן, סטודנט שנה ב' להנדסת חשמל ומדעי המחשב.

מה בתכנון?

- נבנה מחלק מתח.
- נבנה מעגל של נורה וכפתור, ואז נשלב לד צבעוני.
- נציג פעימות לב באמצעות נורה.
- נבנה מעגלי RC ו-RLC ונראה את התנודות.
- נבנה מעגל של נורה וכפתור עם שבב של שער לוגי.
- למתקדמים – עבודה עם שבבים והיכרות עם ה-555.

13.02.2024

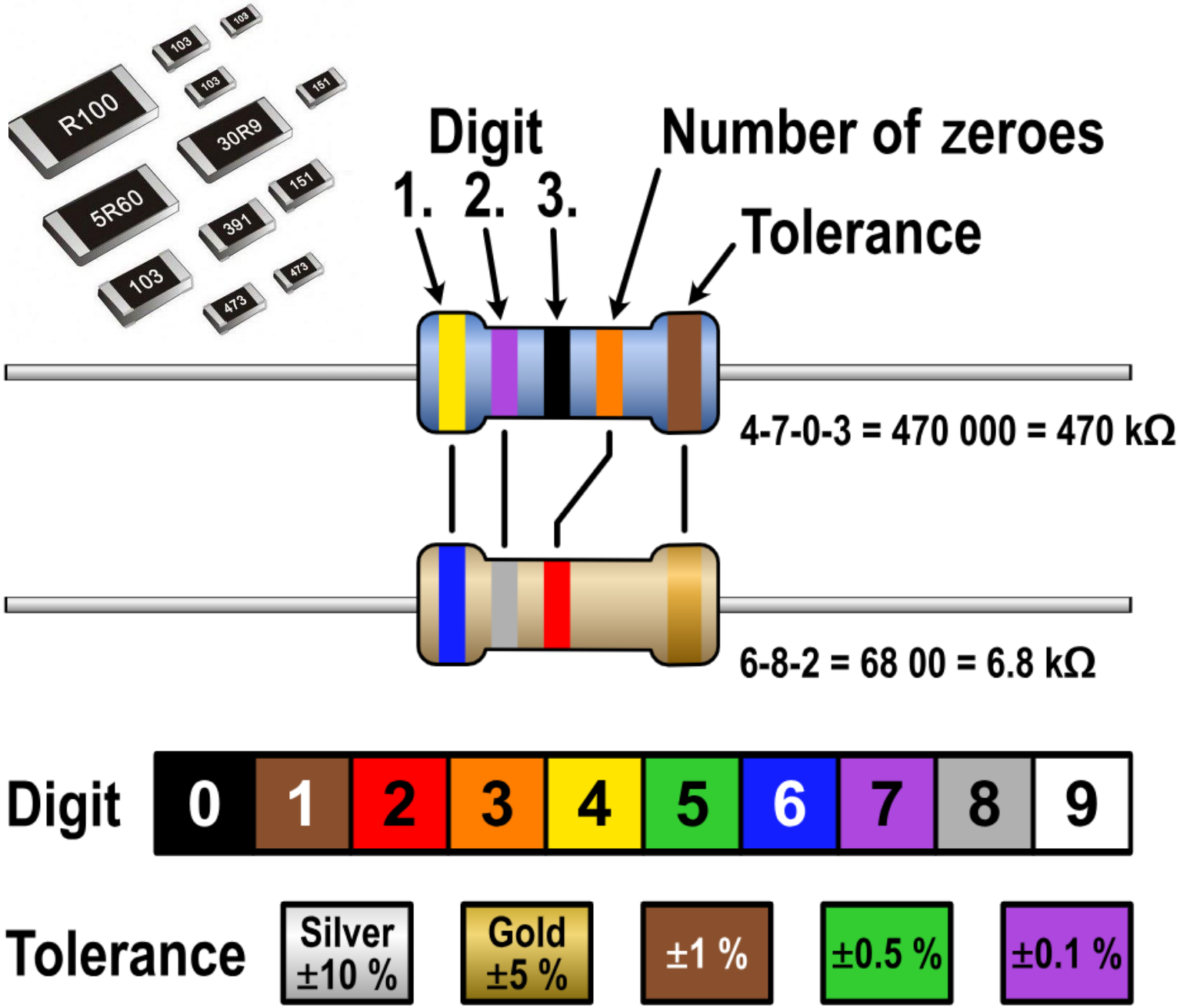
16:00 – 19:00

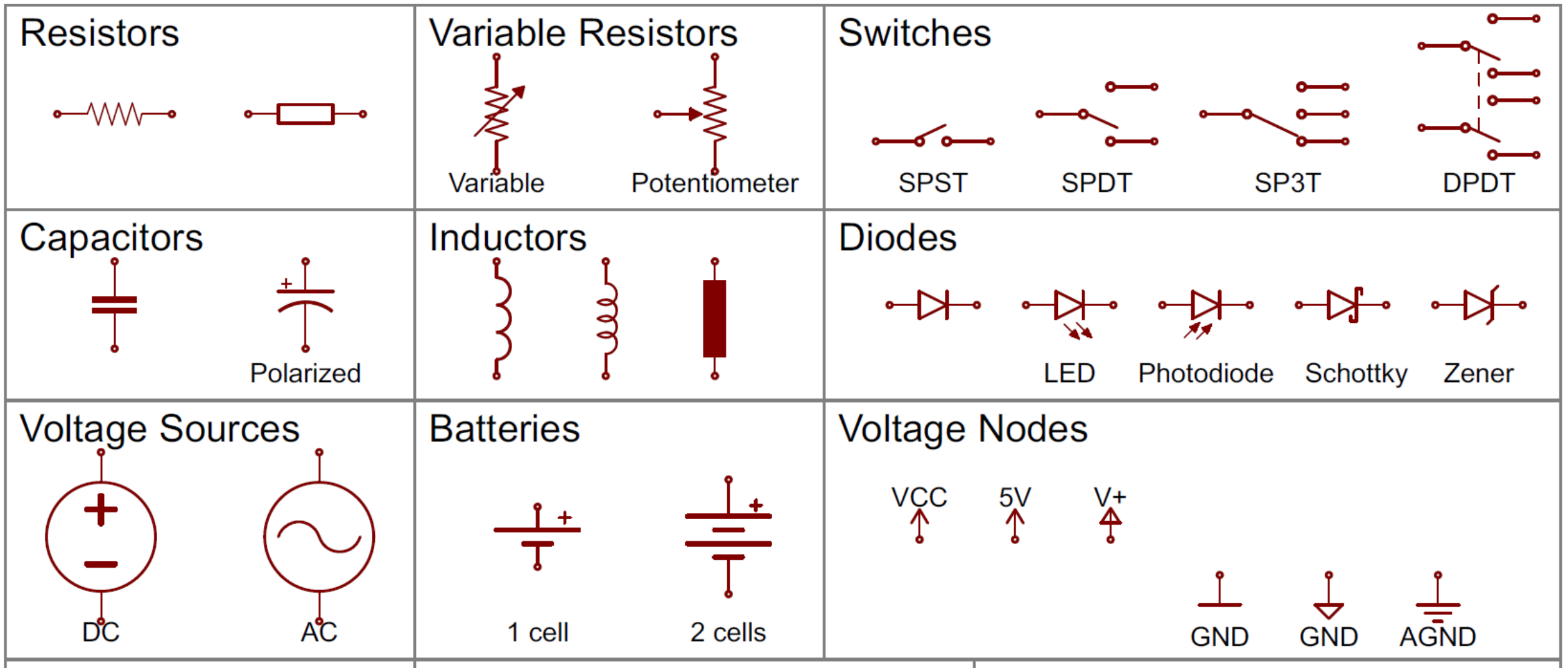
מעבדת הנדסה
קומה מתחת לאודיטוריום

SI prefixes

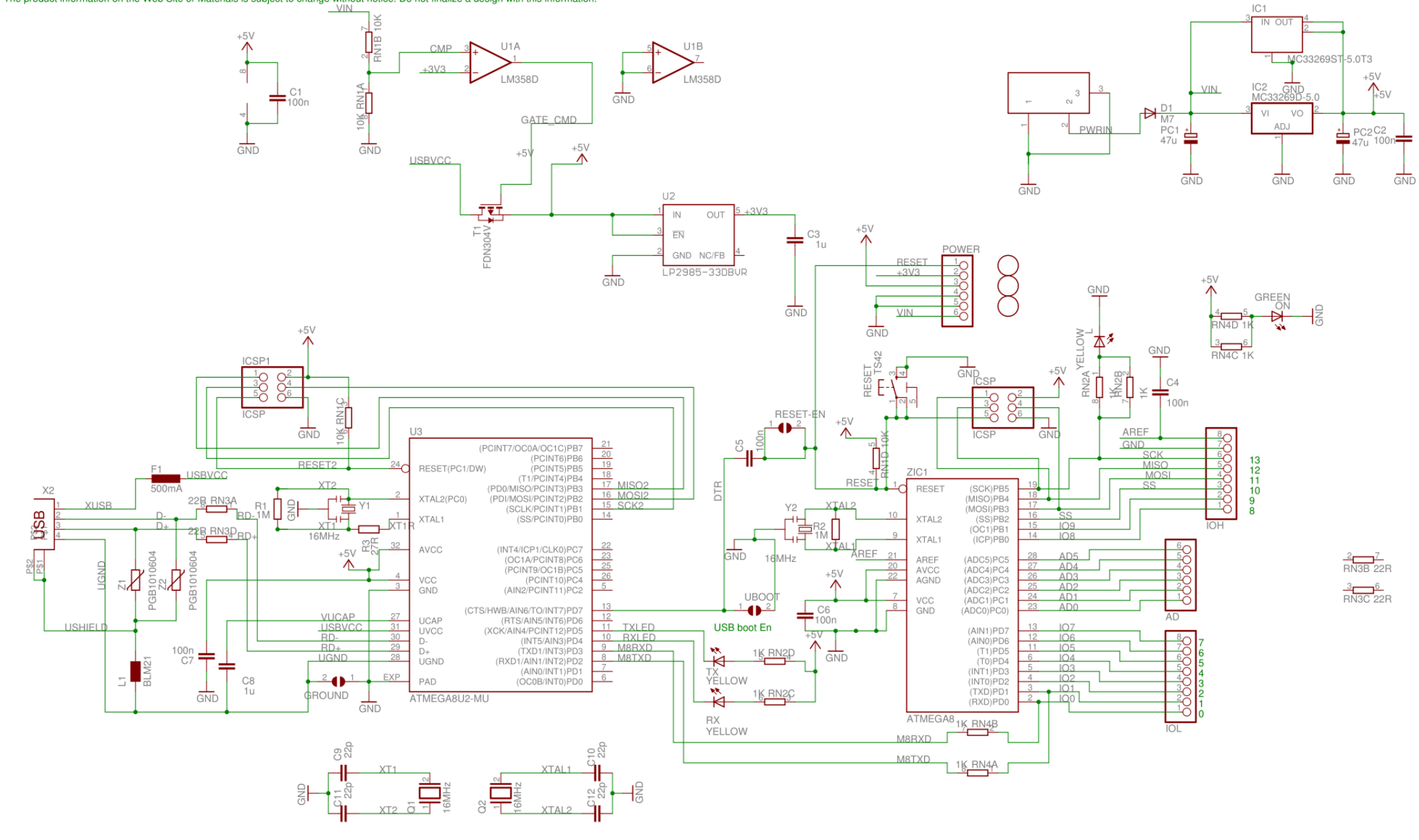
v · t · e

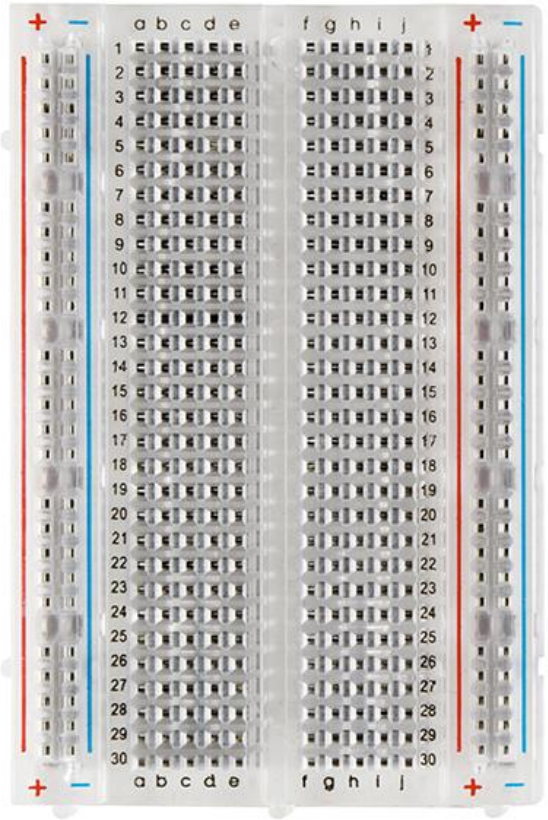
Prefix		Base 10	Decimal	Adoption [nb 1]
Name	Symbol			
quetta	Q	10^{30}	1 000 000 000 000 000 000 000 000 000 000	2022[1]
ronna	R	10^{27}	1 000 000 000 000 000 000 000 000 000	
yotta	Y	10^{24}	1 000 000 000 000 000 000 000 000	1991
zetta	Z	10^{21}	1 000 000 000 000 000 000 000	
exa	E	10^{18}	1 000 000 000 000 000 000	1975[2]
peta	P	10^{15}	1 000 000 000 000 000	
tera	T	10^{12}	1 000 000 000 000	1960
giga	G	10^{9}	1 000 000 000	
mega	M	10^{6}	1 000 000	1873
kilo	k	10^{3}	1 000	1795
hecto	h	10^{2}	100	
deca	da	10^{1}	10	
—	—	10^{0}	1	—
deci	d	10^{-1}	0.1	1795
centi	c	10^{-2}	0.01	
milli	m	10^{-3}	0.001	
micro	μ	10^{-6}	0.000 001	1873
nano	n	10^{-9}	0.000 000 001	1960
pico	p	10^{-12}	0.000 000 000 001	
femto	f	10^{-15}	0.000 000 000 000 001	1964
atto	a	10^{-18}	0.000 000 000 000 000 001	
zepto	z	10^{-21}	0.000 000 000 000 000 000 001	1991
yocto	y	10^{-24}	0.000 000 000 000 000 000 000 001	
ronto	r	10^{-27}	0.000 000 000 000 000 000 000 000 001	2022[1]
quecto	q	10^{-30}	0.000 000 000 000 000 000 000 000 000 001	

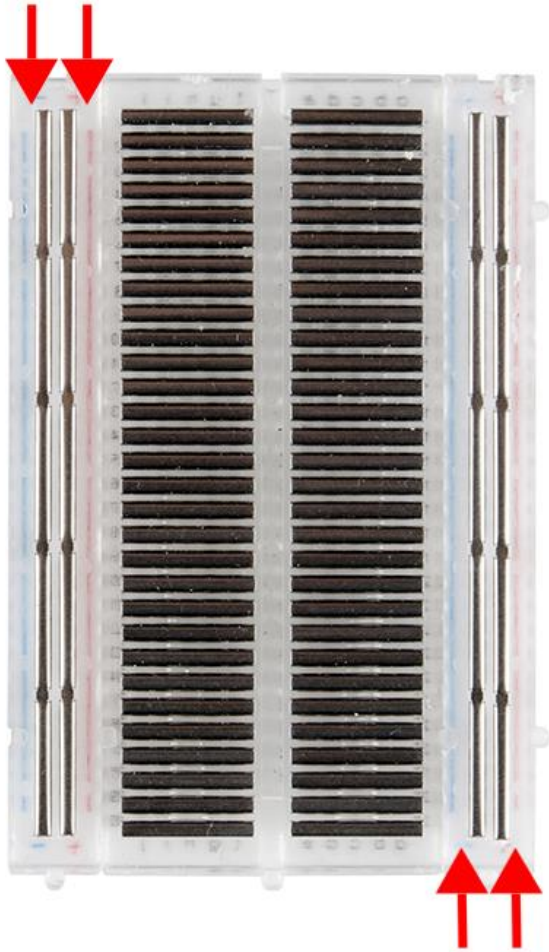


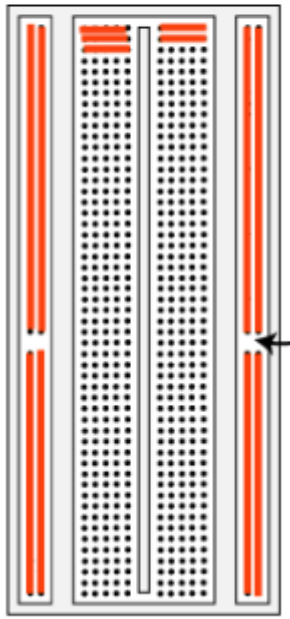

Resistors
Variable Resistors
Variable
Potentiometer
Switches
SPST
SPDT
SP3T
DPDT
Capacitors
Polarized
Inductors
Diodes
LED
Photodiode
Schottky
Zener
Voltage Sources
DC
AC
Batteries
1 cell
2 cells
Voltage Nodes
VCC
5V
V+
GND
GND
AGND

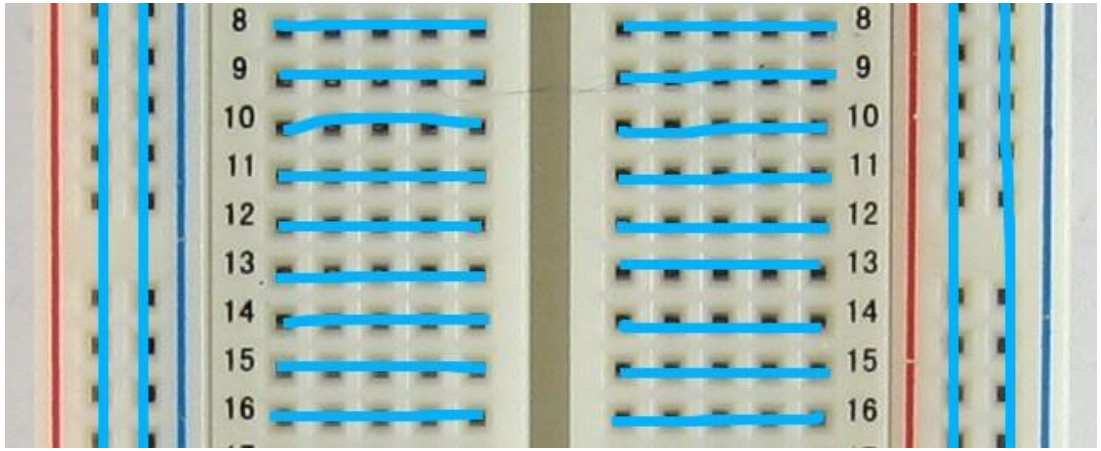
Arduino™ UNO Reference Design

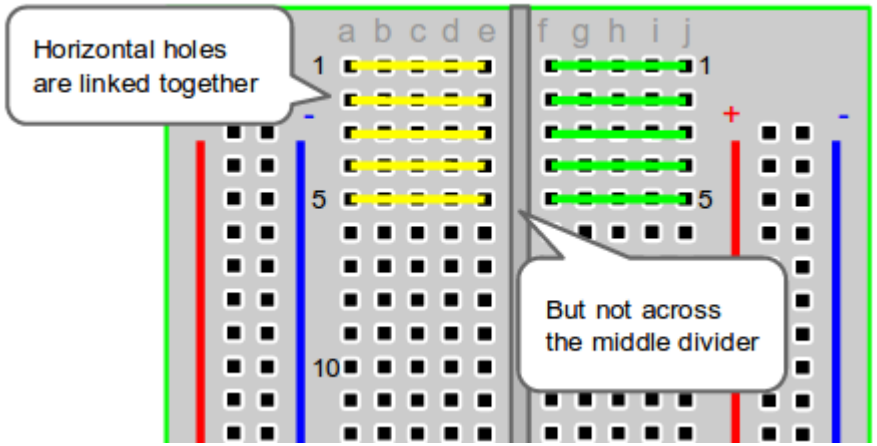


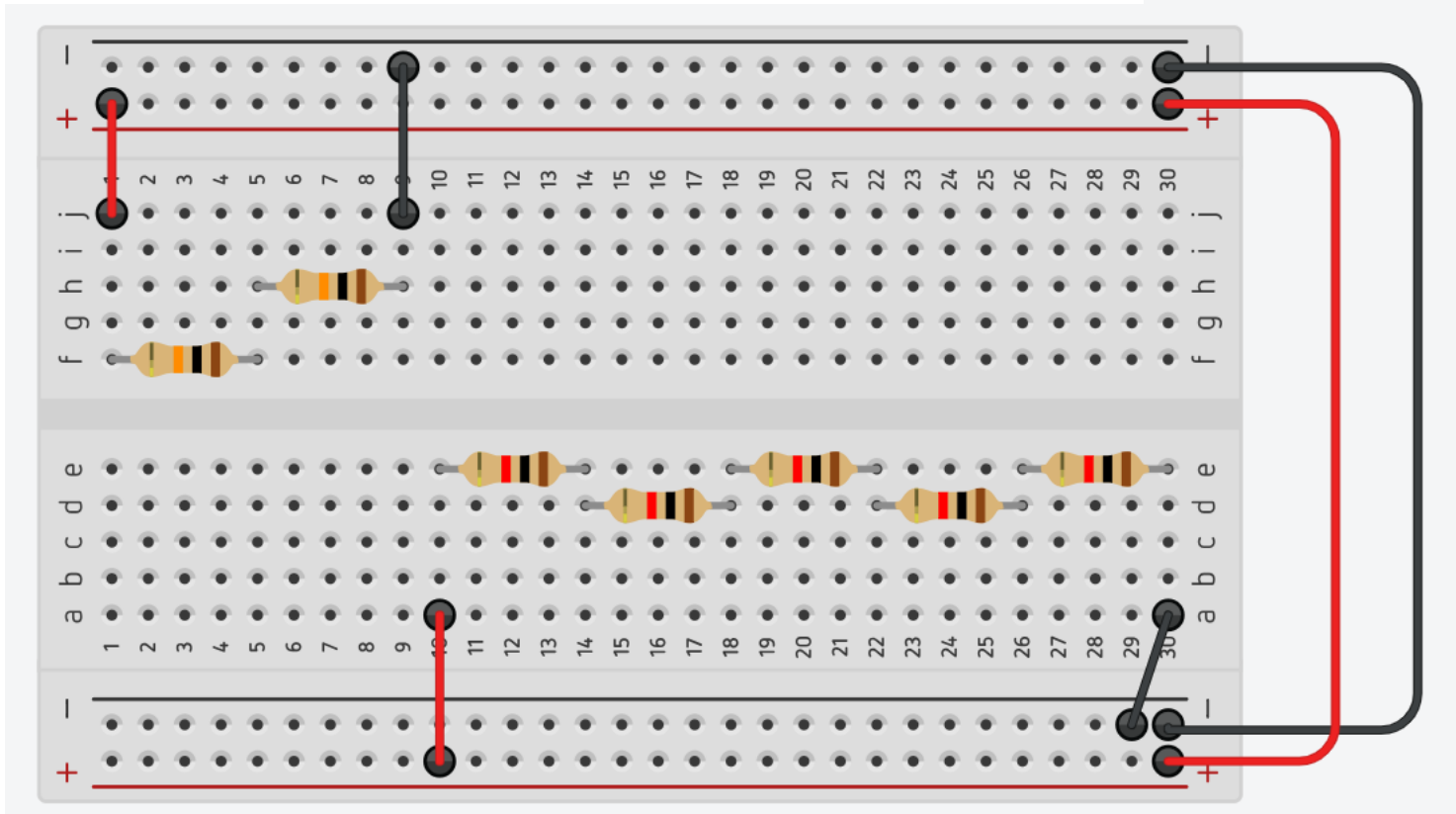

a b c d e
f g h i j
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

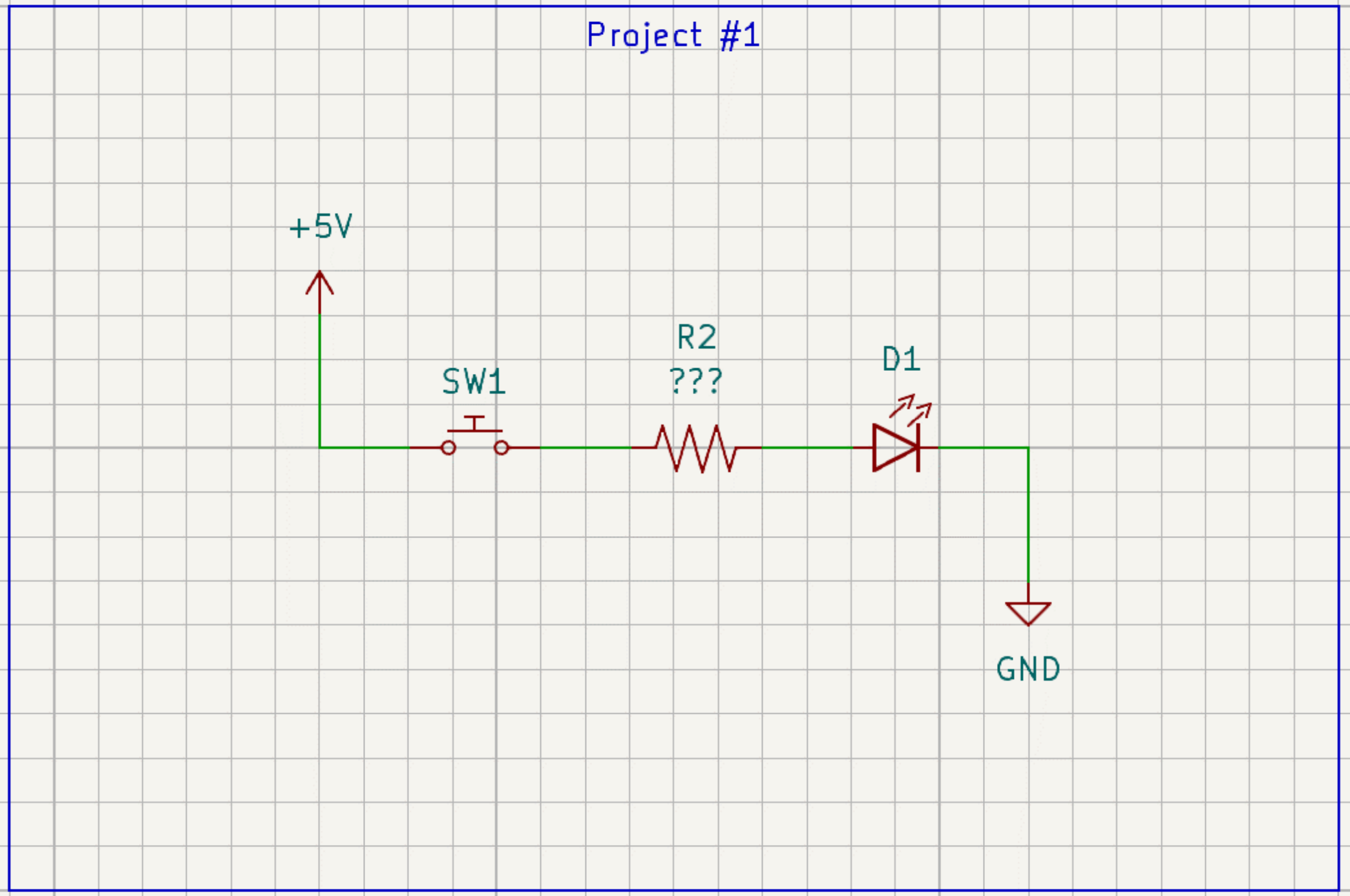


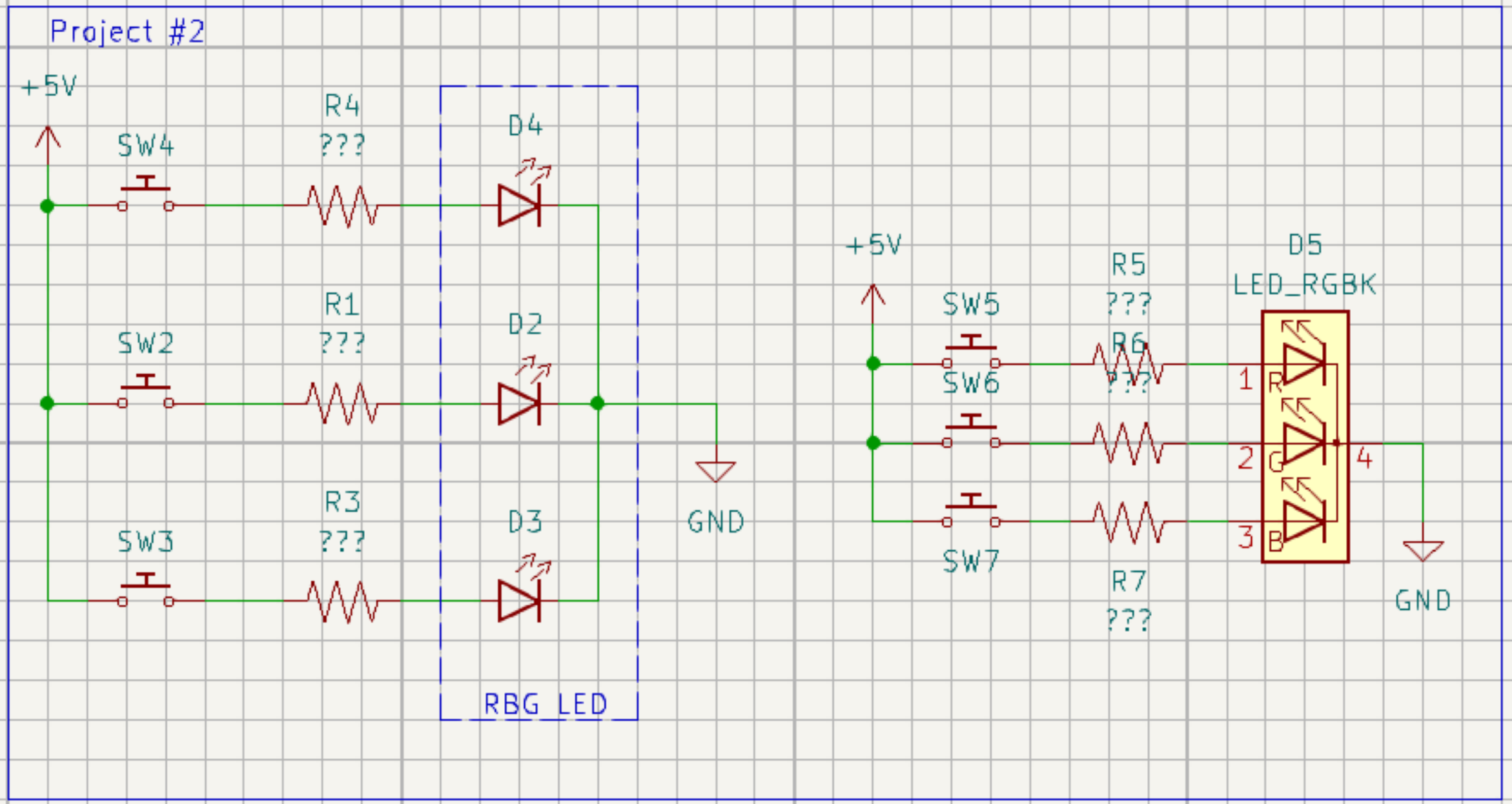

lines indicate
connected holes
Often gap here

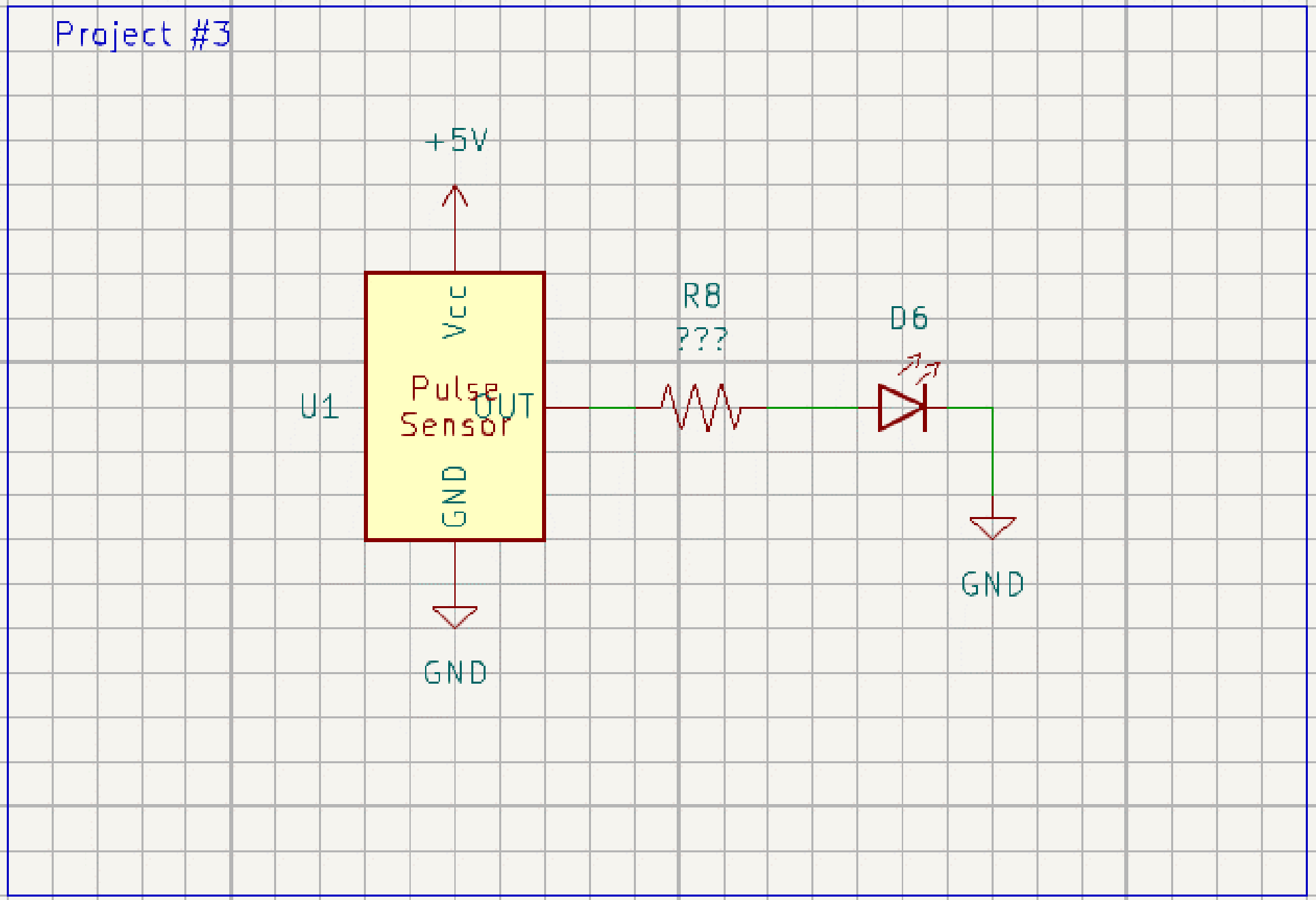

8 9 10 11 12 13 14 15 16

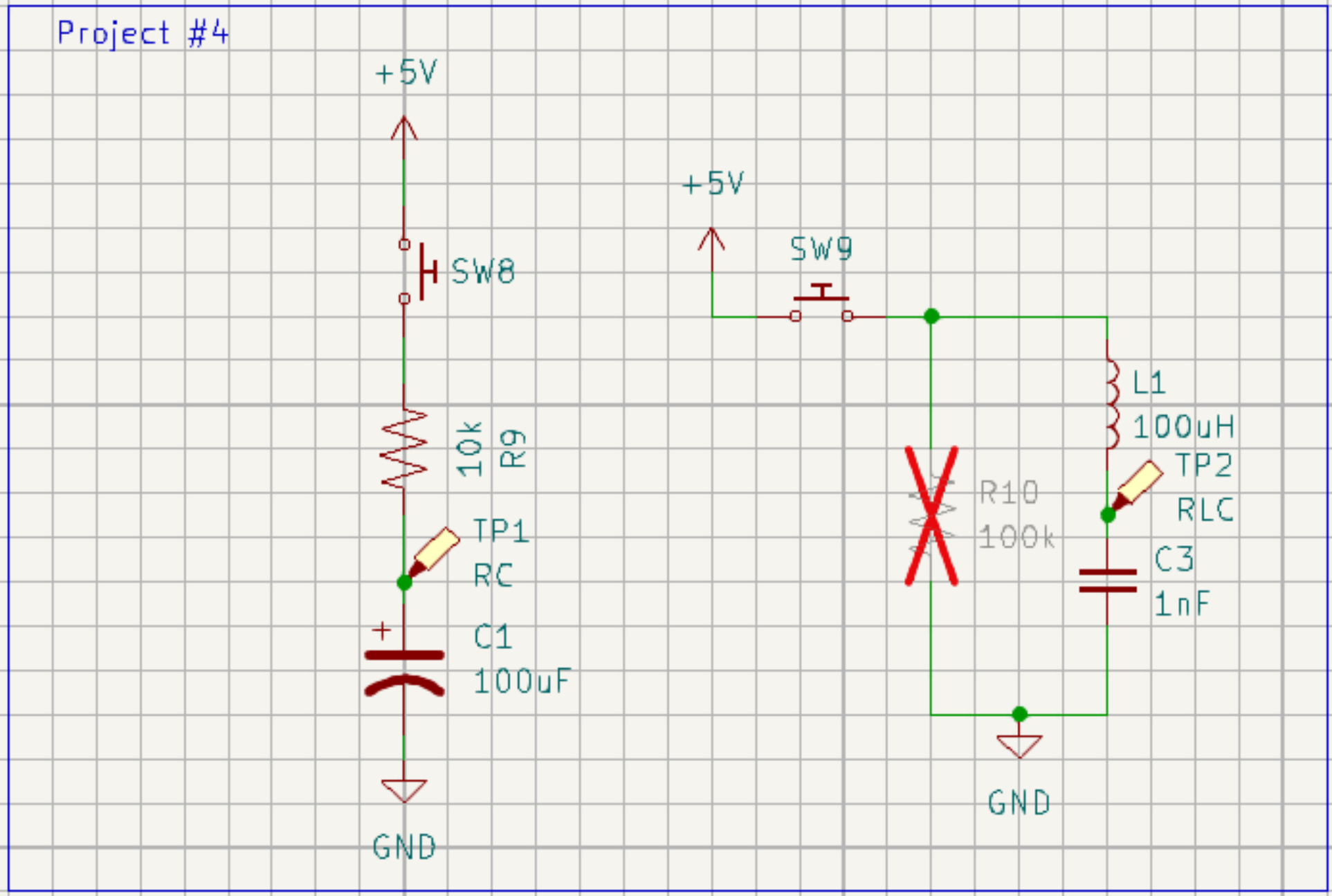

Horizontal holes
are linked together
a b c d e
f g h i j
1
5
10
But not across
the middle divider

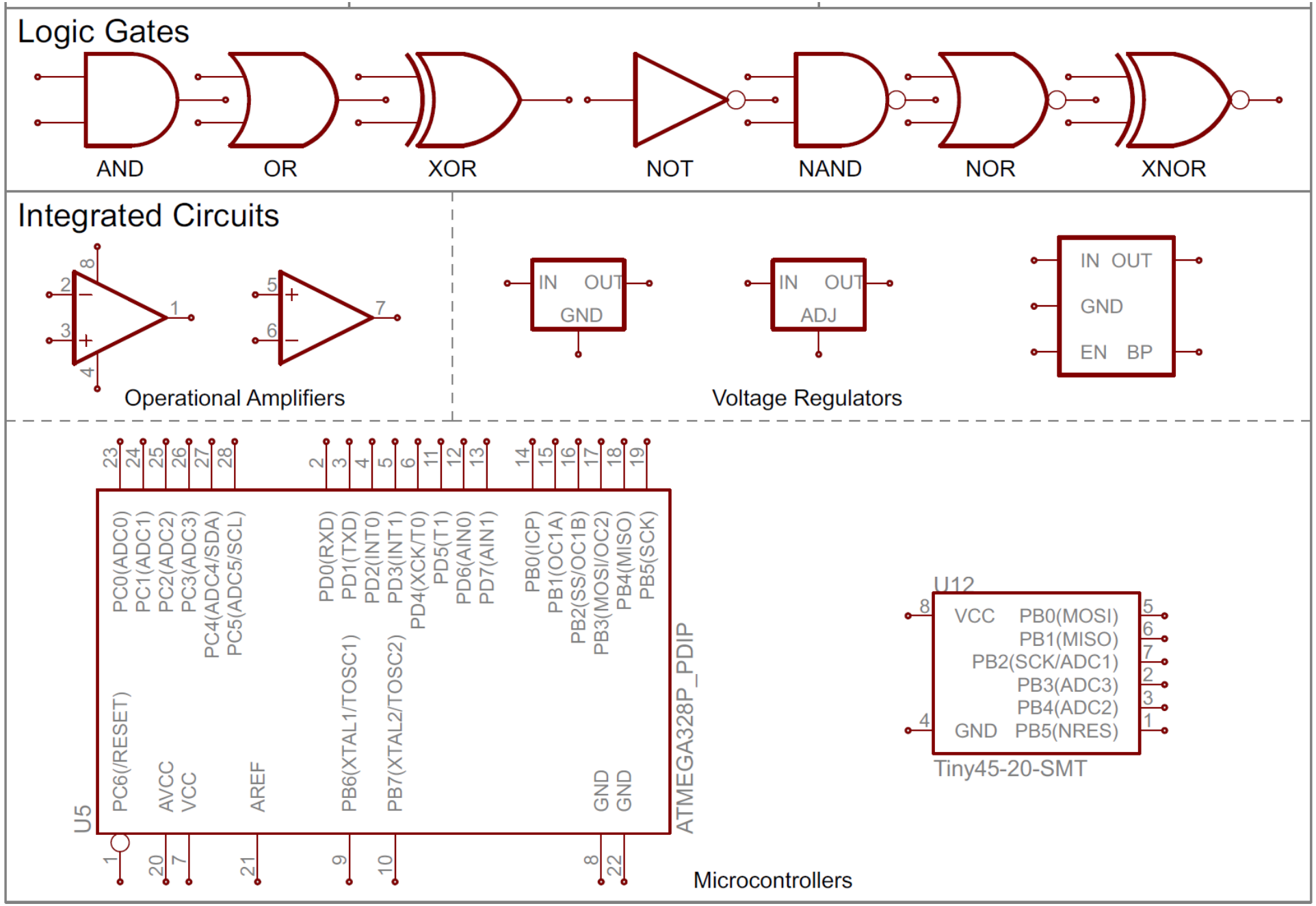

DIGITAL (PWM~)
UNO
ARDUINO
POWER
ANALOG IN


Project #1
+5V
SW1
R2
???
D1
GND

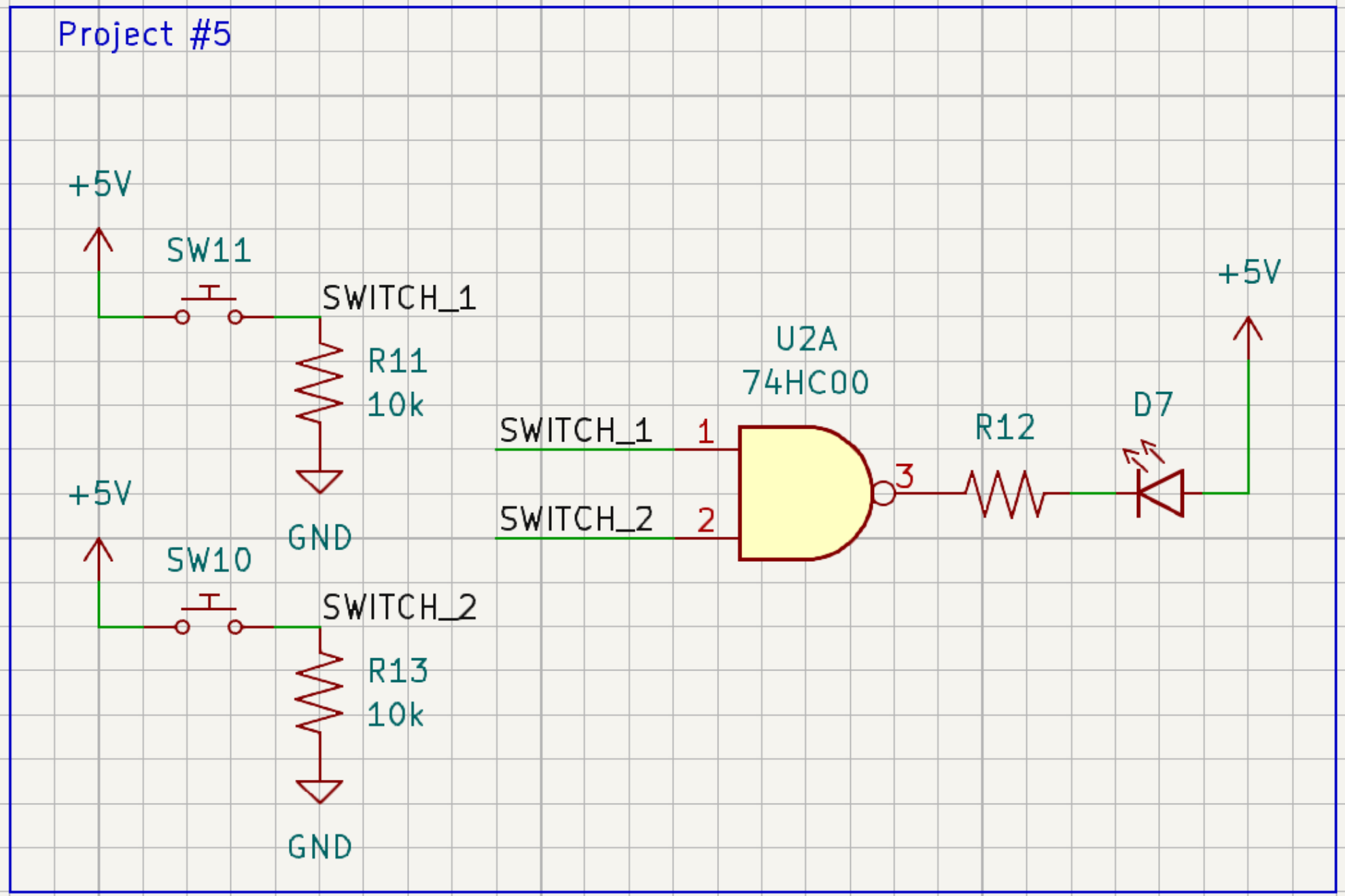

Project #2
+5V
SW4
R4
???
D4
SW2
R1
???
D2
SW3
R3
???
D3
RBG LED
GND
+5V
SW5
R5
???
D5
LED_RGBK
SW6
R6
???
SW7
R7
???
1
2
3
4
R
G
B
GND


Project #3
+5V
Vcc
U1
Pulse
Sensor
OUT
GND
GND
R8
???
D6
GND


Project #4
+5V
SW8
10k
R9
TP1
RC
C1
100uF
GND
+5V
SW9
L1
100uH
TP2
RLC
R10
100k
C3
1nF
GND


Logic Gates
AND
OR
XOR
NOT
NAND
NOR
XNOR
Integrated Circuits
Operational Amplifiers
IN OUT
GND
IN OUT
ADJ
IN OUT
GND
EN BP
Voltage Regulators
U5
PC6(/RESET)
AVCC
VCC
AREF
PB6(XTAL1/TOSC1)
PB7(XTAL2/TOSC2)
GND
GND
PC0(ADC0)
PC1(ADC1)
PC2(ADC2)
PC3(ADC3)
PC4(ADC4/SDA)
PC5(ADC5/SCL)
PD0(RXD)
PD1(TXD)
PD2(INT0)
PD3(INT1)
PD4(XCK/T0)
PD5(T1)
PD6(AIN0)
PD7(AIN1)
PB0(ICP)
PB1(OC1A)
PB2(SS/OC1B)
PB3(MOSI/OC2)
PB4(MISO)
PB5(SCK)
ATMEGA328P_PDIP
U12
VCC
GND
PB0(MOSI)
PB1(MISO)
PB2(SCK/ADC1)
PB3(ADC3)
PB4(ADC2)
PB5(NRES)
Tiny45-20-SMT
Microcontrollers

Input		Output (Q)						
								
A	B	AND	OR	INH	XOR	NAND	NOR	XNOR
0	0	0	0	0	0	1	1	1
0	1	0	1	0	1	1	0	0
1	0	0	1	1	1	1	0	0
1	1	1	1	0	0	0	0	1


Project #5
+5V
SW11
SWITCH_1
R11
10k
GND
+5V
SW10
SWITCH_2
R13
10k
GND
U2A
74HC00
SWITCH_1
1
SWITCH_2
2
3
R12
D7
+5V

Data taken from 74LS00 datasheet:

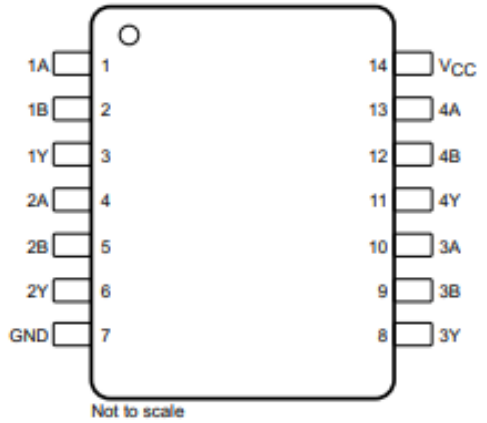
5 Pin Configuration and Functions

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN54xx00	4.5	5	5.5	V
		SN74xx00	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage	SNx400, SN7LS400, and SNx4S00			0.8	V
		SN54LS00			0.7	
I_{OH}	High-level output current	SN5400, SN54LS00, and SN74LS00			–0.4	mA
		SNx4S00			–1	
I_{OL}	Low-level output current	SNx400			16	mA
		SN5LS400			4	
		SN7LS400			8	
		SNx4S00			20	

0 J, SN54xx00 J and W, SN74x00 D, N, and N
SN74LS00 D, DB, N, and NS Packages
14-Pin CDIP, CFP, SOIC, PDIP, SO, or SSOP
Top View



Not to scale

Logic Diagram, Each Gate (Positive Logic)