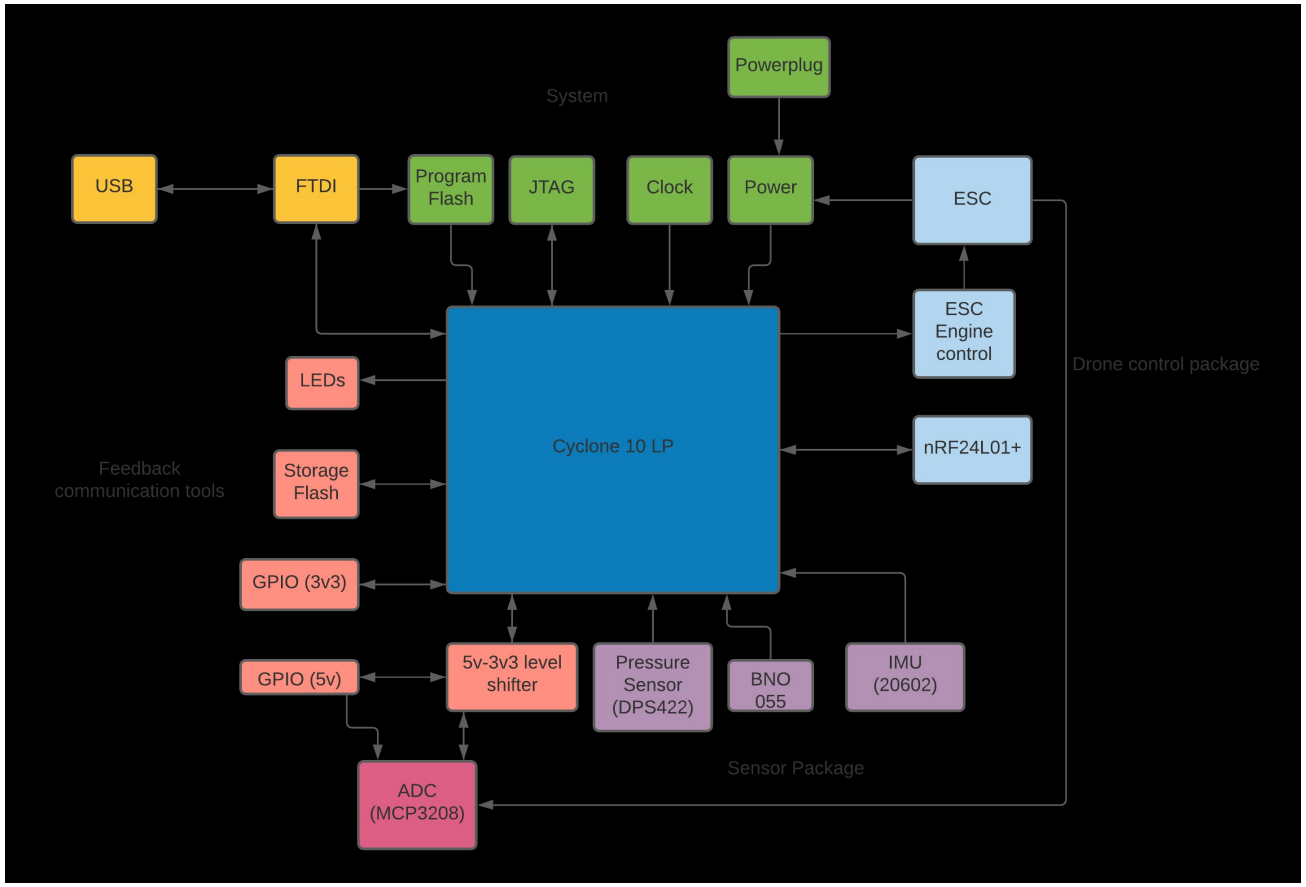
Functional diagram and index



Index

H101 MountingHole
H102 MountingHole
H103 MountingHole
H104 MountingHole
H105 MountingHole
H106 MountingHole

Drone flight controller PCB with FPGA on the board

Eldalote.Electronics

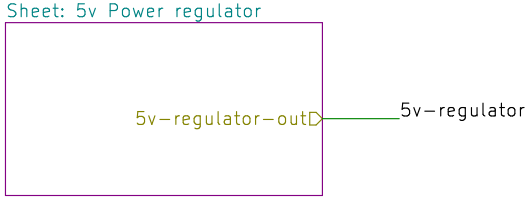
Sheet: /

File: PCB-Drone-With-FPGA.sch

Title: Drone PCB with FPGA

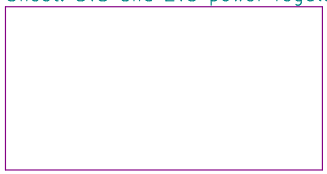
Size: A4	Date: 2020-08-24	Rev: 1
KiCad E.D.A. kicad (5.1.6)-1		Id: 1/15

Sheet: 5v Power regulator



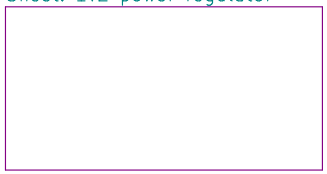
File: 5v-power-regulator.sch

Sheet: 3v3 and 2v5 power regulators



File: 3v3-2v5-regulator.sch

Sheet: 1v2 power regulator



File: 1v2-power-regulator.sch

Power requirements:
1v2 (FPGA core): 1.5A estimated. Supply 2A to have margin. Derived from 5v rail.
-- 1v2 at 2A is 2.4 watt. 90% regulator efficiency: 2.7 watt input. Around 540mA drain on 5v rail.
-- Regulator: AP63200WU-7

2v5 (FPGA PLL): 40mA estimated. Use small LDO, derived from 3v3. 40mA drain on 3v3 rail.
-- Regulator: NCP115ASN250T2G

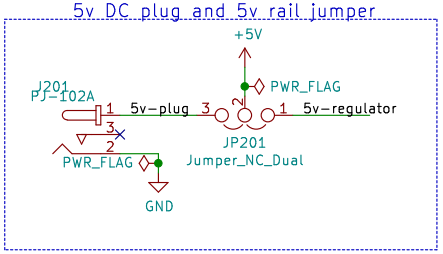
3v3 (FPGA IO, sensors, radio, flash, LEDs, GPIO): Radio combined max 110mA, LEDs max 150mA,
-- Sensors: combined less than 20mA, FPGA-IO: 100mA, 2v5LDO: 40mA. Total combined: 380mA.
-- With a 1.5A regulator that leaves more and 1amps for the GPIOs. Should be good enough.
-- 3v3 at 1.5A is 4.95 watts, 90% efficency: 5.5 watts. 1.1Amps drain on 5v rail.
-- Regulator: SC189ZSKTRT

5v (Other power rails, ADC, GPIO): 1v2: 540mA, 3v3: 1.1A, ADC <1mA. Total: 1.65 A. Powered by either
-- 2A regulator or DC power plug, even with everything on full power, that leaves 350mA for GPIO.
-- Regulator: AP63205WU-7

5v USB (FTDI): Self powered through USB.

Power in: 10v 2A From 4-in-1 ESC
Alternate: 5v from DC plug. Added jumper to enable switching between supplies

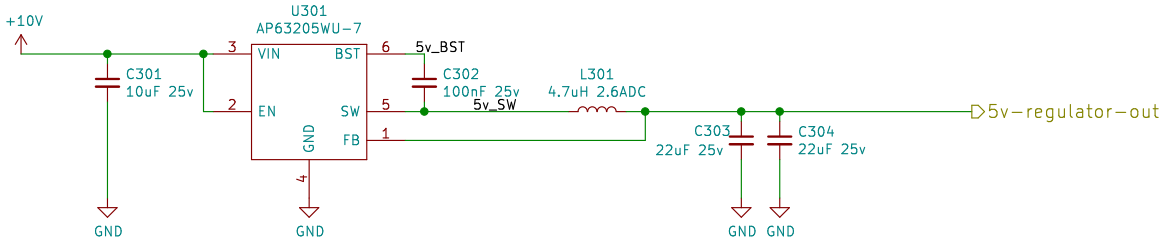
5v DC plug and 5v rail jumper



Sheet: /Power Distribution and Estimation/
File: Power-Distribution-Estimation.sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.6)-1		Id: 2/15

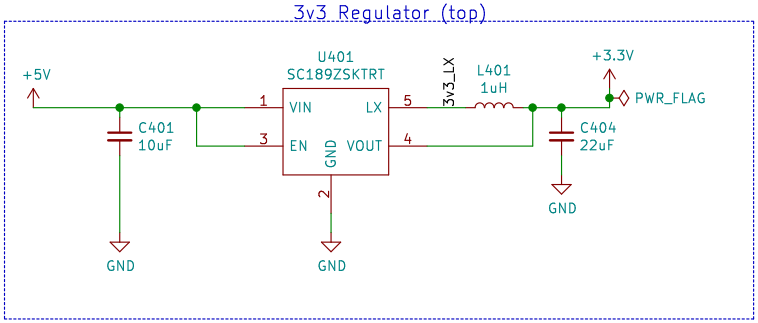


Sheet: /Power Distribution and Estimation/5v Power regulator/
File: 5v-power-regulator.sch

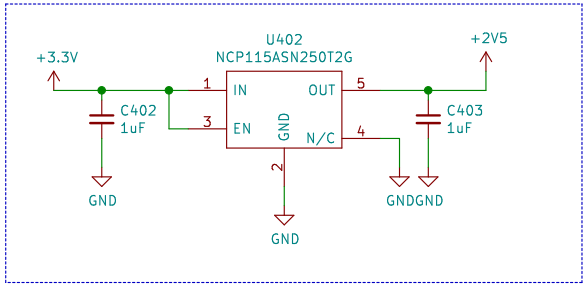
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6)-1		Id: 3/15

3v3 Regulator (top)



2v5 LDO (top)



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File: 3v3-2v5-regulator.sch

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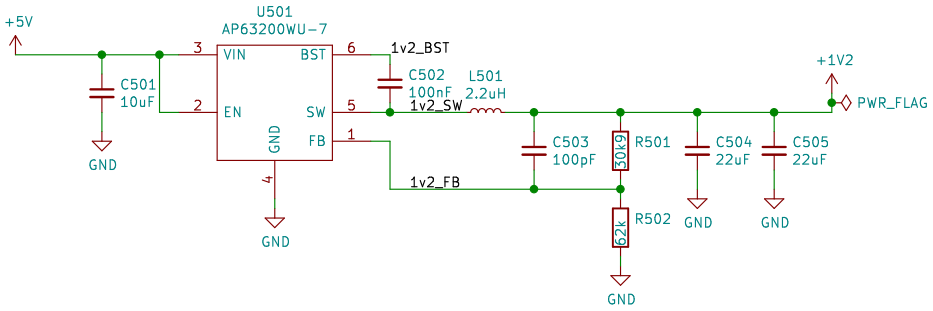

Sheet: /Power Distribution and Estimation/1v2 power regulator/
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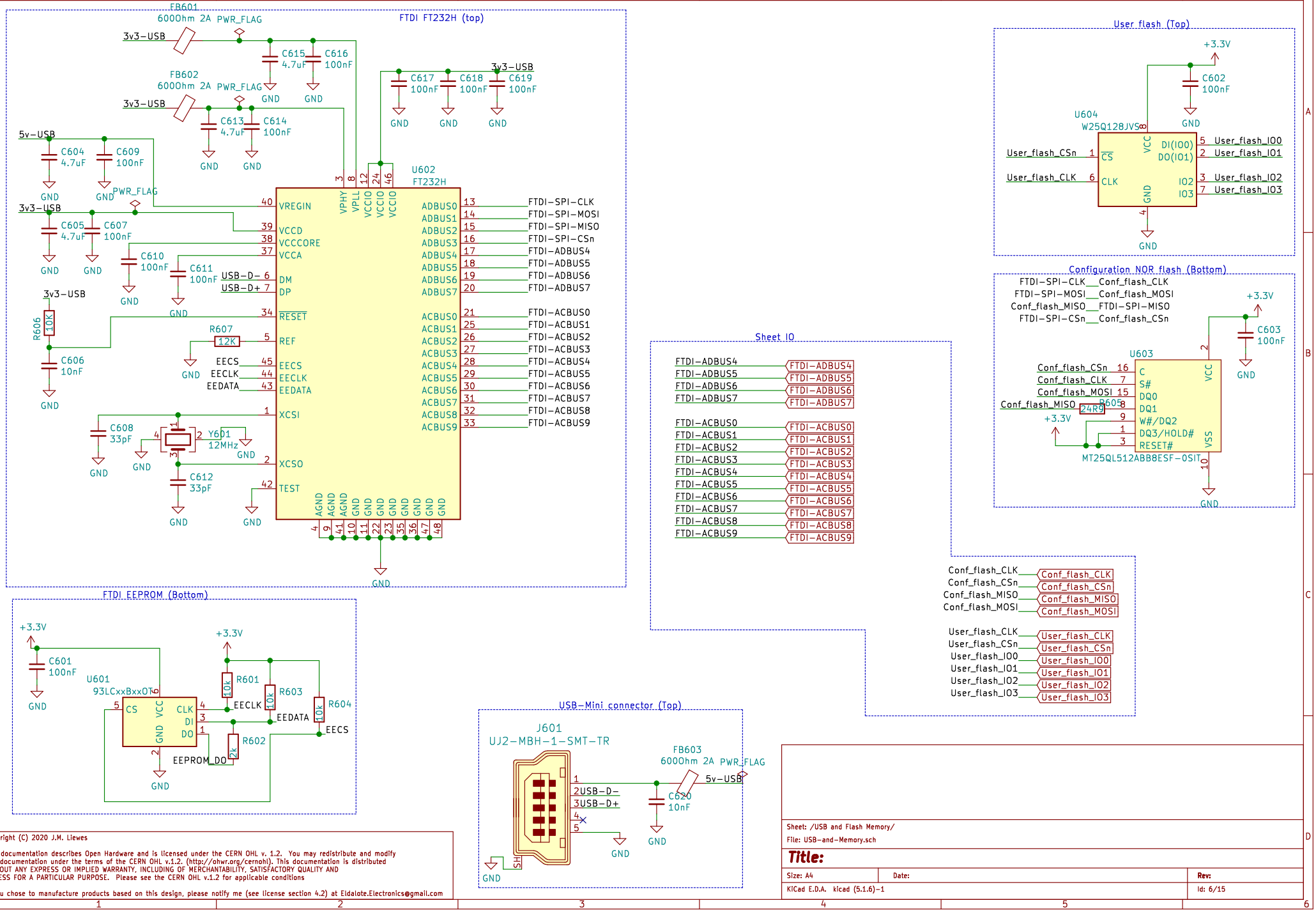
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6)-1		Id: 5/15



Sheet: /USB and Flash Memory/
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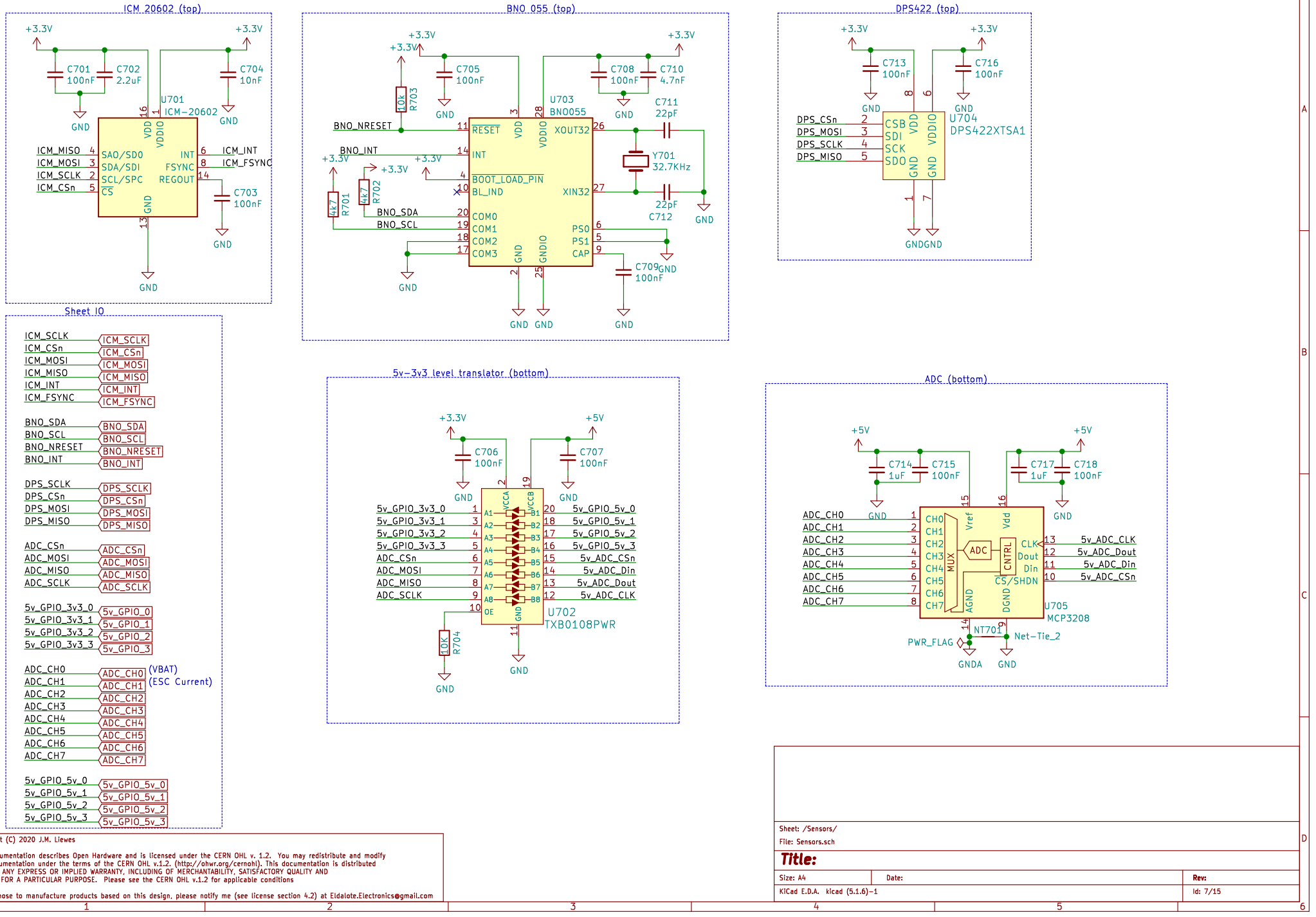
Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.6)-1		Id: 6/15



Sheet: /Sensors/
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Title:

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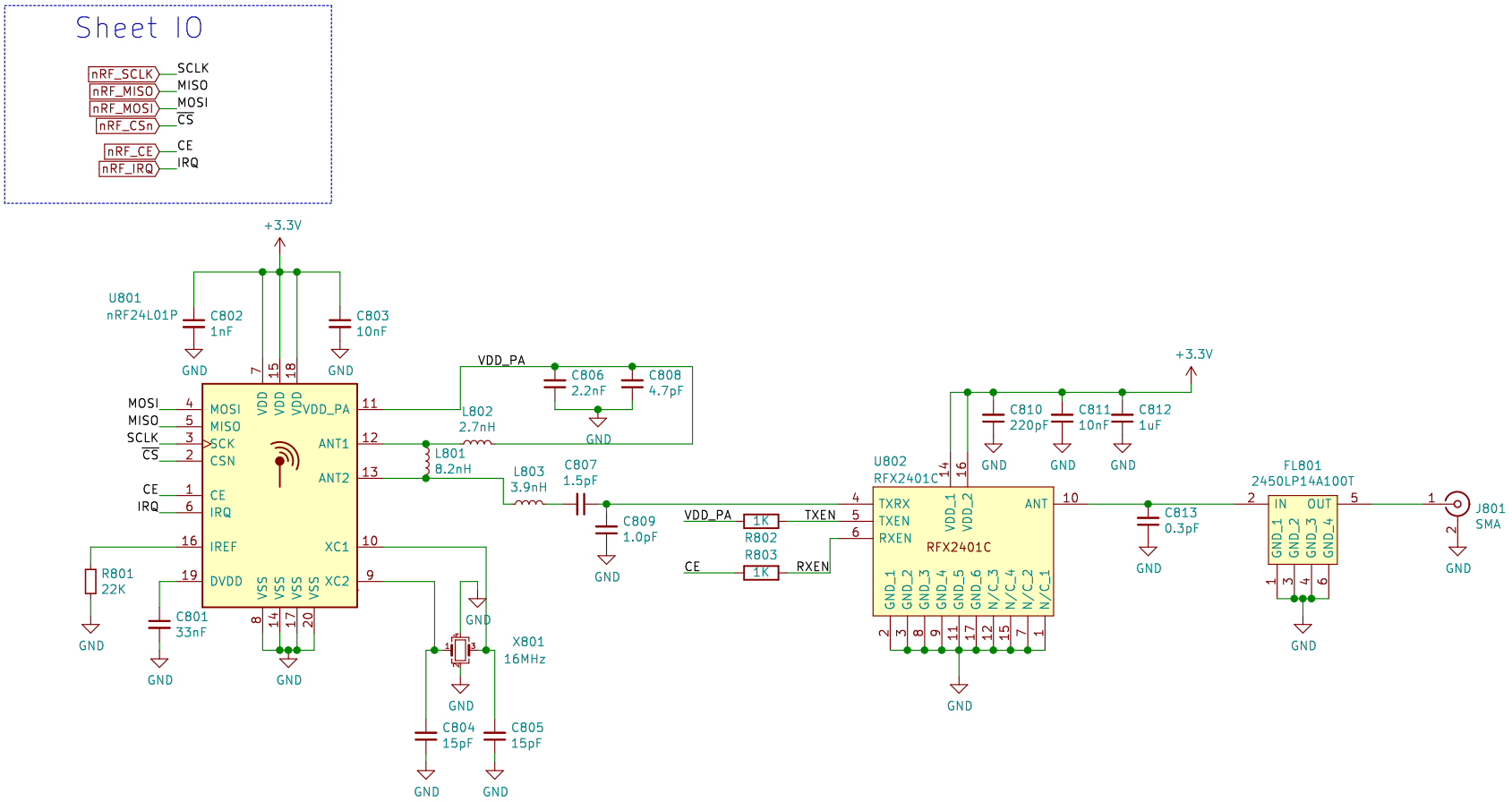
KiCad E.D.A. kicad (5.1.6)-1		Id: 7/15



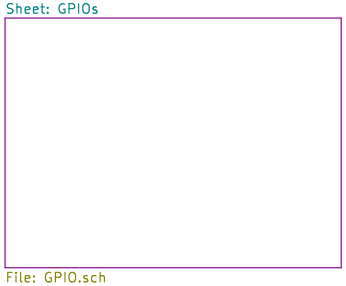
Sheet: /nRF24L01+ Radio module/
File: nRF24L01p-radio.sch

Title:

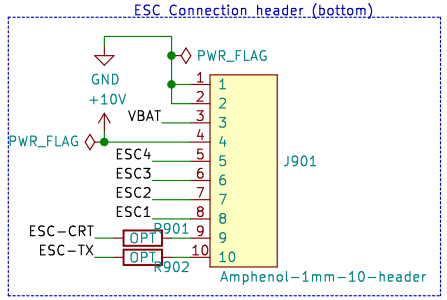
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6)-1		Id: 8/15

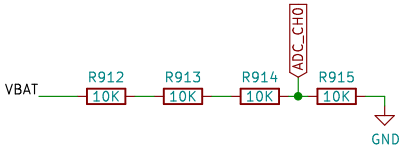
Sheet: GPIOs

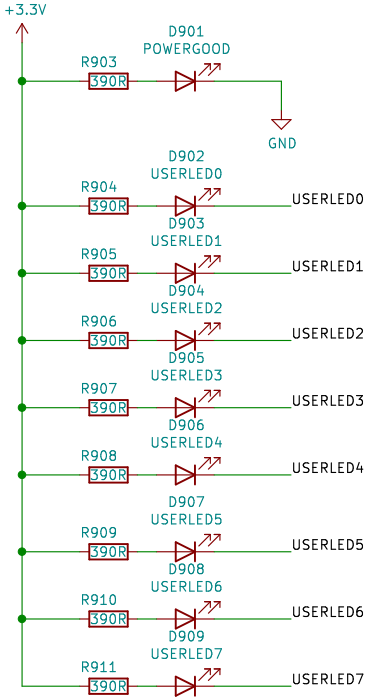
File: GPIO.sch



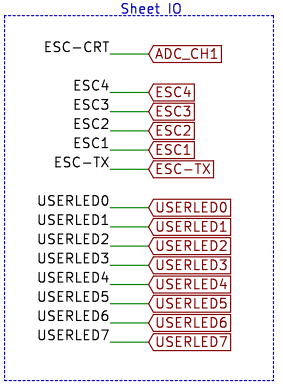
ESC Connection header (bottom)







Sheet IO



Sheet: /Engine signals, LEDs, and GPIO/

File: Outside-com.sch

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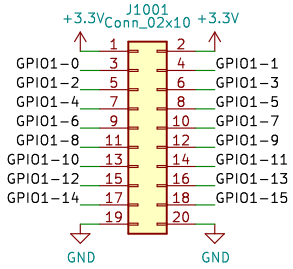

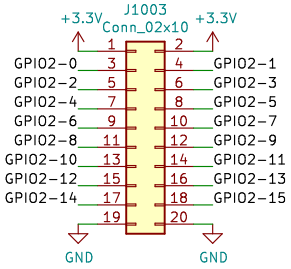

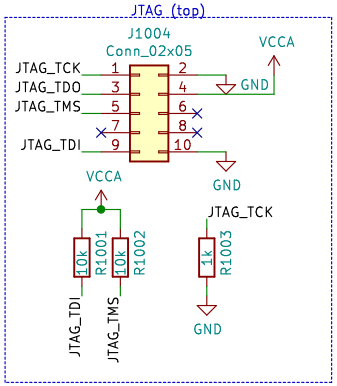

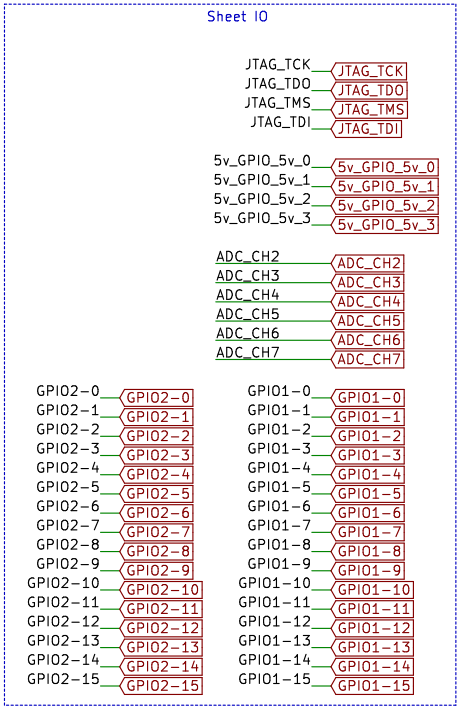

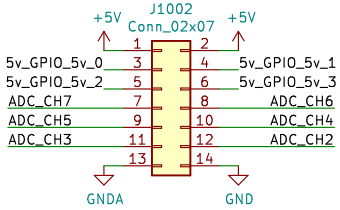

Sheet: /Engine signals, LEDs, and GPIO/GPIOs/
File: GPIO.sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.6)-1		Id: 10/15

Functional Block	Pin Name	Pin Number	Bank
50 MHz Clock	Clock	T1	Clocks
FTDI	ADBUS4	AB3	3
	ADBUS5	AA3	3
	ADBUS6	AB4	3
	ADBUS7	AA4	3
	ACBUS0	AB5	3
	ACBUS1	AA5	3
	ACBUS2	AB7	3
	ACBUS3	AA7	3
	ACBUS4	AA13	4
	ACBUS5	AB13	4
	ACBUS6	AA14	4
	ACBUS7	AB14	4
	ACBUS8	AA15	4
	ACBUS9	AB15	4
User Flash	CLK	F1	1
	Csn	J1	1
	IO0	F2	1
	IO1	J2	1
	IO2	H1	1
	IO3	H2	1
User LED	LED0	Y1	2
	LED1	Y2	2
	LED2	W1	2
	LED3	W2	2
	LED4	V1	2
	LED5	V2	2
	LED6	U1	2
	LED7	U2	2

Functional Block	Pin Name	Pin Number	Bank
DPS422	Csn	AA22	5
	MOSI	AA21	5
	SCLK	Y22	5
	MISO	Y21	5
BNO055	SDA	E1	1
	SCL	D2	1
	INT	B1	1
	NRESET	B2	1
ICM-20602	SCLK	AB8	3
	MOSI	AA8	3
	MISO	AB9	3
	Csn	AA9	3
	INT	AA10	3
	FSYNC	AB10	3
ADC	Csn	AB18	4
	MOSI	AA18	4
	MISO	AB16	4
	SCLK	AA16	4
Radio	CE	C22	6
	Csn	C21	6
	SCLK	B22	6
	MOSI	A20	7
	MISO	A19	7
	IRQ	B20	7
ESC	ESC1	N2	2
	ESC2	N1	2
	ESC3	M2	2
	ESC4	M1	2
	ESC-TX	P1	2

Functional Block	Pin Name	Pin Number	Bank
GPIO 1	GPIO 0	V21	5
	GPIO 1	V22	5
	GPIO 2	U21	5
	GPIO 3	U22	5
	GPIO 4	D22	6
	GPIO 5	D21	6
	GPIO 6	E22	6
	GPIO 7	E21	6
	GPIO 8	F22	6
	GPIO 9	F21	6
	GPIO 10	H22	6
	GPIO 11	H21	6
	GPIO 12	J22	6
	GPIO 13	J21	6
	GPIO 14	M21	5
	GPIO 15	M22	5
GPIO 2	GPIO 0	B6	8
	GPIO 1	A6	8
	GPIO 2	B7	8/CONF
	GPIO 3	A7	8
	GPIO 4	B18	7
	GPIO 5	A18	7
	GPIO 6	B17	7
	GPIO 7	A17	7
	GPIO 8	B16	7
	GPIO 9	A16	7
	GPIO 10	B15	7
	GPIO 11	A15	7
	GPIO 12	B14	7
	GPIO 13	A14	7
	GPIO 14	B13	7
	GPIO 15	A13	7
5volt GPIO	5vGPIO-0	AB20	4
	5vGPIO-1	AA20	4
	5vGPIO-2	AB19	4
	5vGPIO-3	AA19	4

Sheet: /FPGA Pin Listings/
File: FPGA-Pinning.sch

Title:

Size: A4	Date:	Rev:
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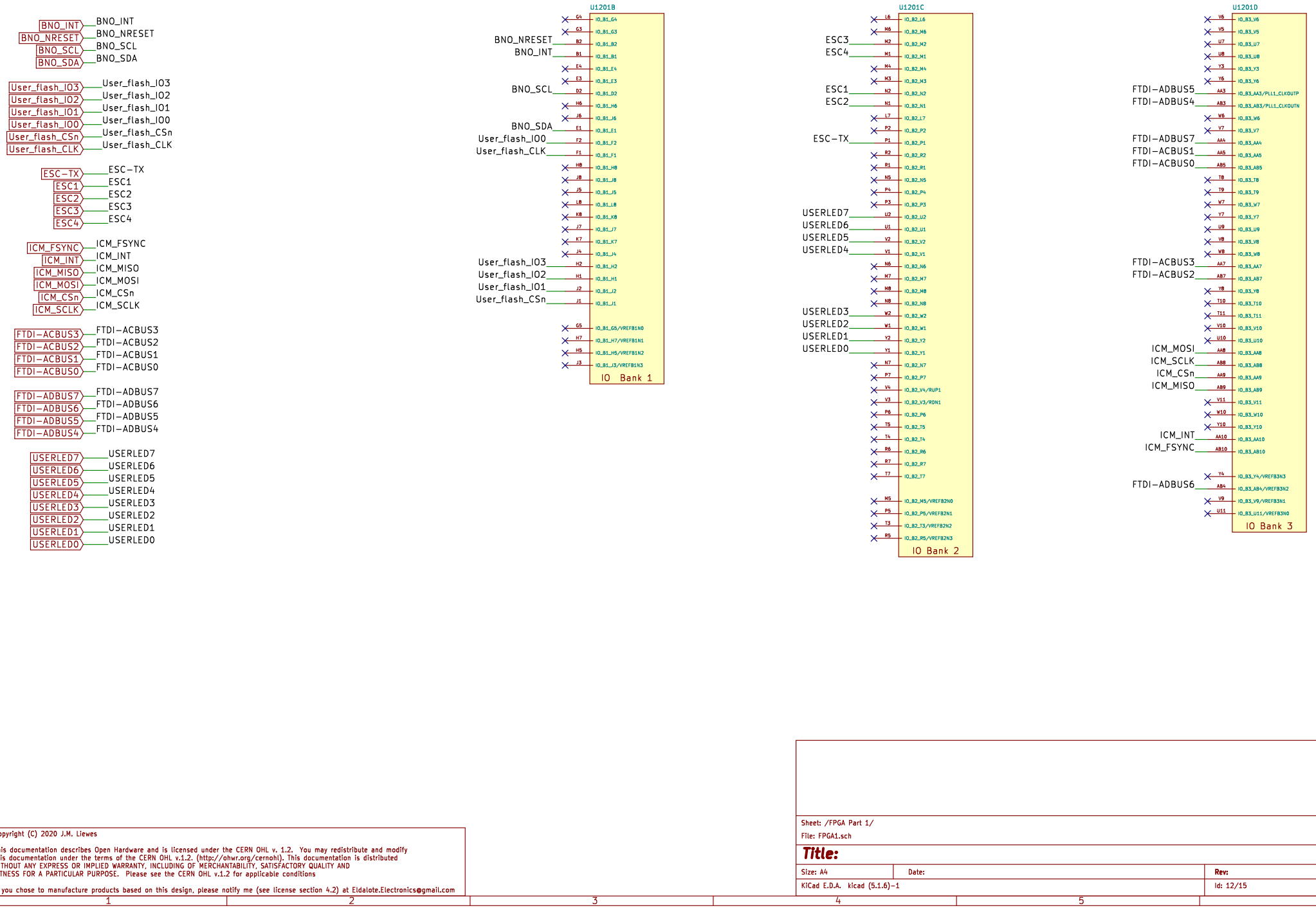

Sheet: /FPGA Part 1/
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Title:

Size: A4	Date:	**Rev:**
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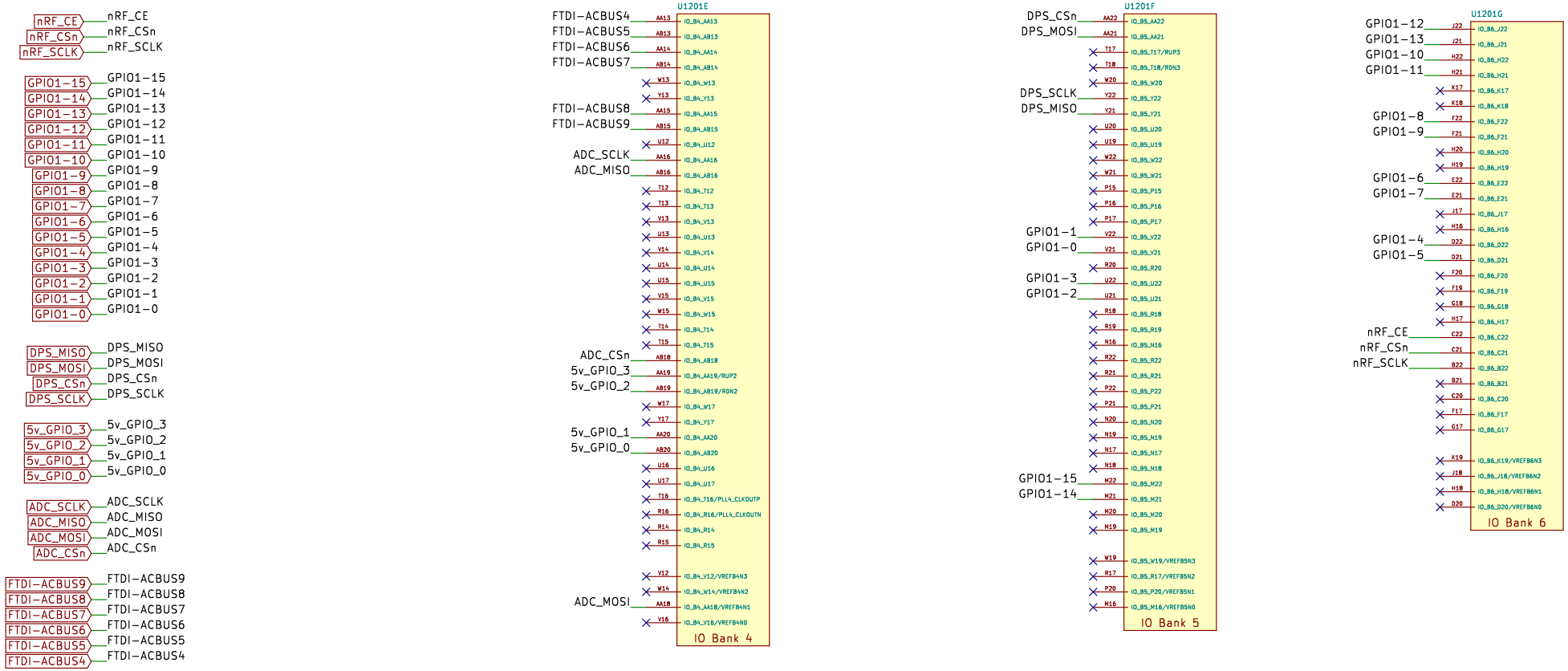

Sheet: /FPGA Part 2/
File: FPGA2.sch

Title:

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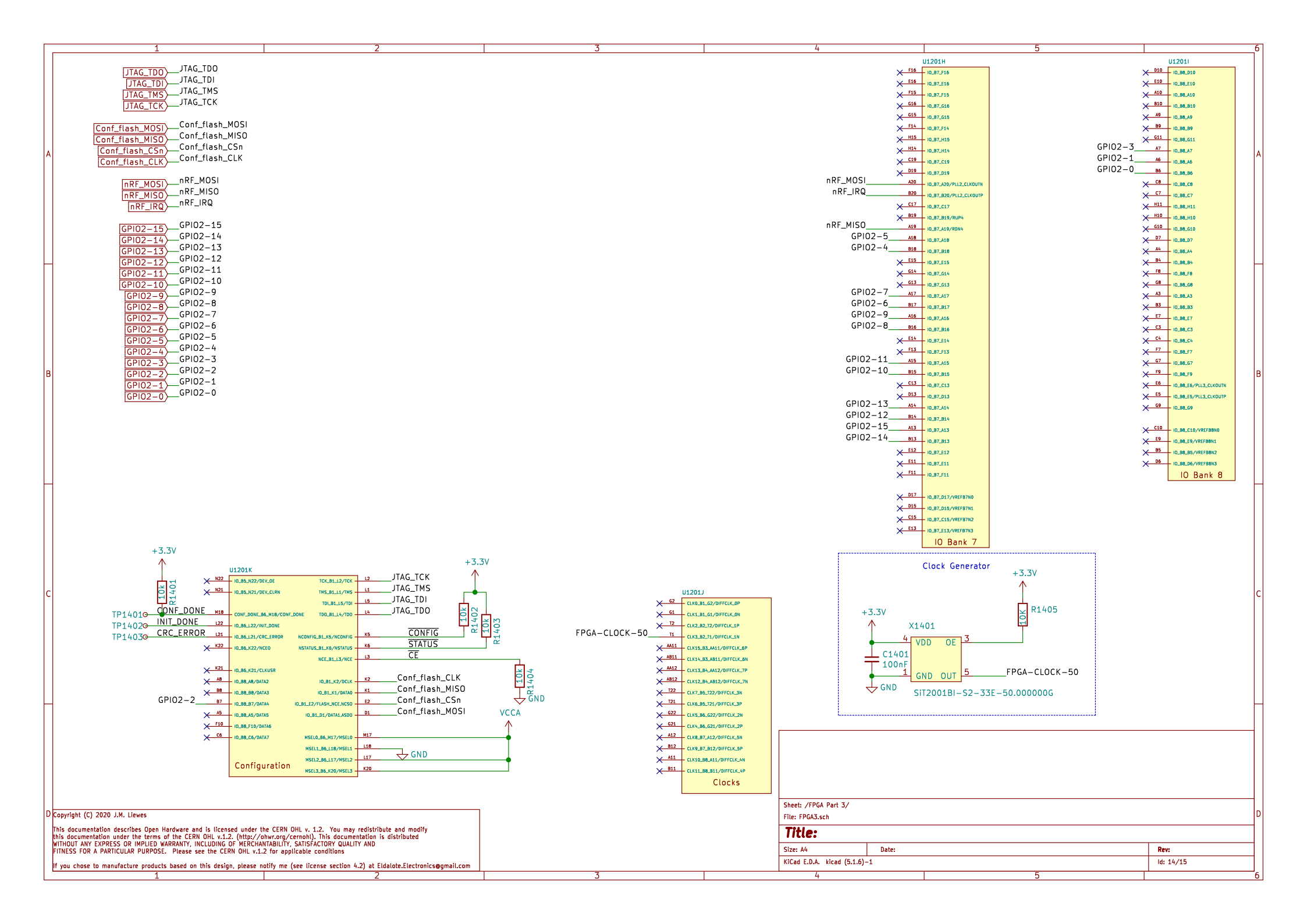
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TCK
Conf_flash_MOSI
Conf_flash_MISO
Conf_flash_CSn
Conf_flash_CLK
nRF_MOSI
nRF_MISO
nRF_IRQ
GPIO2-15
GPIO2-14
GPIO2-13
GPIO2-12
GPIO2-11
GPIO2-10
GPIO2-9
GPIO2-8
GPIO2-7
GPIO2-6
GPIO2-5
GPIO2-4
GPIO2-3
GPIO2-2
GPIO2-1
GPIO2-0
U1201H
IO_B7_F16
IO_B7_E16
IO_B7_F15
IO_B7_G16
IO_B7_G15
IO_B7_F14
IO_B7_H15
IO_B7_H14
IO_B7_C19
IO_B7_D19
IO_B7_A20/PLL2_CLKOUTN
IO_B7_B20/PLL2_CLKOUTP
IO_B7_C17
IO_B7_B19/RUP4
IO_B7_A19/RDN4
IO_B7_A18
IO_B7_B18
IO_B7_E15
IO_B7_G14
IO_B7_G13
IO_B7_A17
IO_B7_B17
IO_B7_A16
IO_B7_B16
IO_B7_E14
IO_B7_F13
IO_B7_A15
IO_B7_B15
IO_B7_C13
IO_B7_D13
IO_B7_A14
IO_B7_B14
IO_B7_A13
IO_B7_B13
IO_B7_E12
IO_B7_E11
IO_B7_F11
IO_B7_D17/VREFB7N0
IO_B7_D15/VREFB7N1
IO_B7_C15/VREFB7N2
IO_B7_E13/VREFB7N3
IO Bank 7
U1201I
IO_B8_D10
IO_B8_E10
IO_B8_A10
IO_B8_B10
IO_B8_A9
IO_B8_B9
IO_B8_G11
IO_B8_A7
IO_B8_A6
IO_B8_B6
IO_B8_C8
IO_B8_C7
IO_B8_H11
IO_B8_H10
IO_B8_G10
IO_B8_D7
IO_B8_A4
IO_B8_B4
IO_B8_F8
IO_B8_G8
IO_B8_A3
IO_B8_B3
IO_B8_E7
IO_B8_C3
IO_B8_C4
IO_B8_F7
IO_B8_G7
IO_B8_F9
IO_B8_E6/PLL3_CLKOUTN
IO_B8_E5/PLL3_CLKOUTP
IO_B8_G9
IO_B8_C10/VREFB8N0
IO_B8_E9/VREFB8N1
IO_B8_B5/VREFB8N2
IO_B8_D6/VREFB8N3
IO Bank 8
+3.3V
R1401
10k
TP1401
TP1402
TP1403
CONF_DONE
INIT_DONE
CRC_ERROR
U1201K
CONF_DONE_B6_M18/CONF_DONE
IO_B6_L22/INIT_DONE
IO_B6_L21/CRC_ERROR
IO_B6_K22/NCEO
IO_B6_K21/CLKUSR
IO_B8_A8/DATA2
IO_B8_B8/DATA3
IO_B8_B7/DATA4
IO_B8_A5/DATA5
IO_B8_F10/DATA6
IO_B8_C6/DATA7
TCK_B1_L2/TCK
TMS_B1_L1/TMS
TDI_B1_L5/TDI
TDO_B1_L4/TDO
NCONFIG_B1_K5/NCONFIG
NSTATUS_B1_K6/NSTATUS
NCE_B1_L3/NCE
IO_B1_K2/DCLK
IO_B1_K1/DATA0
IO_B1_E2/FLASH_NCE_NCSO
IO_B1_D1/DATA1_ASDO
MSEL0_B6_M17/MSEL0
MSEL1_B6_L18/MSEL1
MSEL2_B6_L17/MSEL2
MSEL3_B6_K20/MSEL3
Configuration
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
CONFIG
STATUS
CE
Conf_flash_CLK
Conf_flash_MISO
Conf_flash_CSn
Conf_flash_MOSI
GPIO2-2
+3.3V
R1402
10k
R1403
10k
R1404
10k
GND
VCCA
GND
U1201J
CLK0_B1_G2/DIFFCLK_0P
CLK1_B1_G1/DIFFCLK_0N
CLK2_B2_T2/DIFFCLK_1P
CLK3_B2_T1/DIFFCLK_1N
CLK15_B3_AA11/DIFFCLK_6P
CLK14_B3_AB11/DIFFCLK_6N
CLK13_B4_AA12/DIFFCLK_7P
CLK12_B4_AB12/DIFFCLK_7N
CLK7_B5_T22/DIFFCLK_3N
CLK6_B5_T21/DIFFCLK_3P
CLK5_B6_G22/DIFFCLK_2N
CLK4_B6_G21/DIFFCLK_2P
CLK8_B7_A12/DIFFCLK_5N
CLK9_B7_B12/DIFFCLK_5P
CLK10_B8_A11/DIFFCLK_4N
CLK11_B8_B11/DIFFCLK_4P
Clocks
FPGA-CLOCK-50
Clock Generator
+3.3V
R1405
10K
+3.3V
X1401
C1401
100nF
VDD
OE
GND
OUT
FPGA-CLOCK-50
GND
SiT2001BI-S2-33E-50.000000G
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If you chose to manufacture products based on this design, please notify me (see license section 4.2) at Eldalote.Electronics@gmail.com
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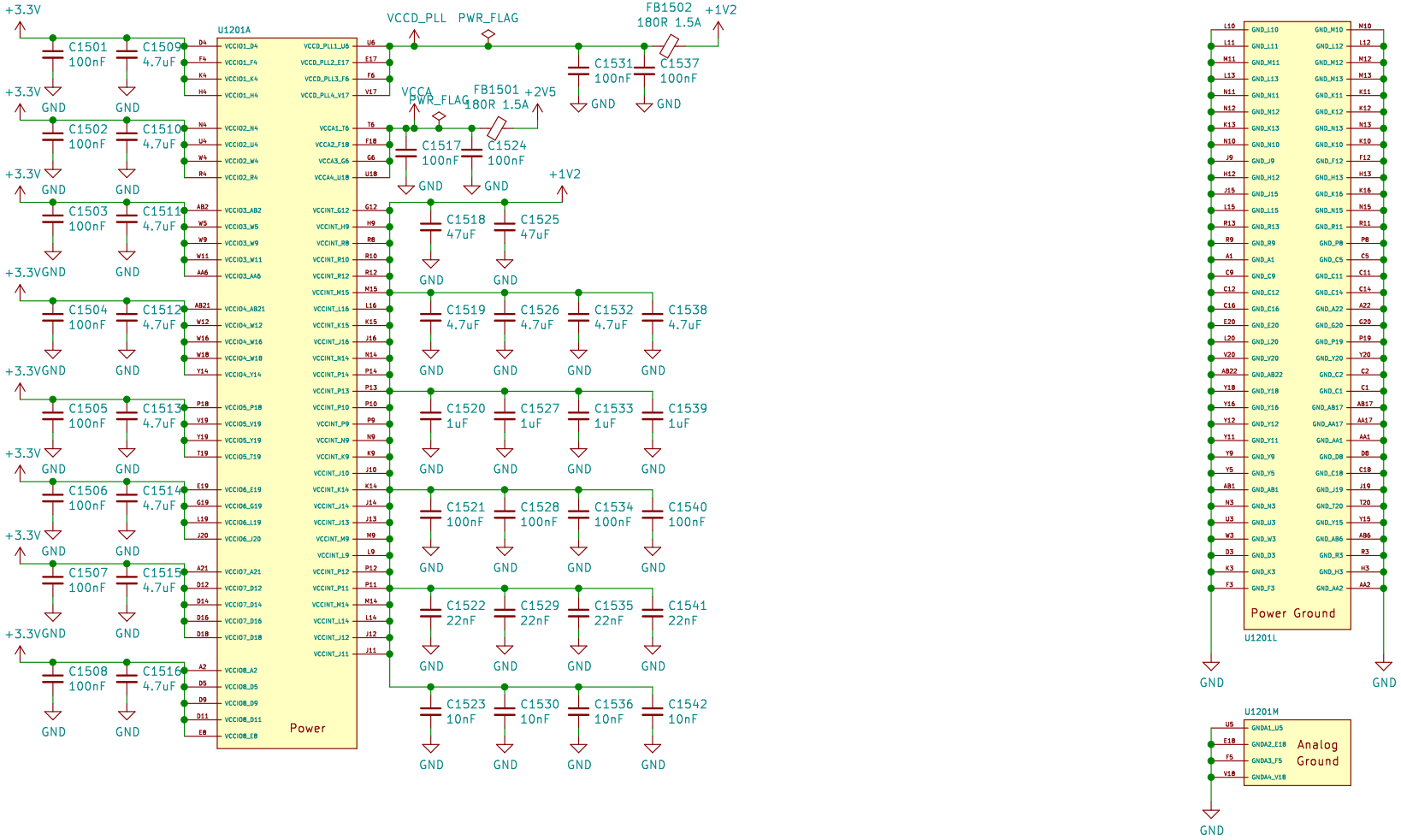
Id: 14/15



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