

Implementation of FPGA accelerators for Traffic Signal Classification using CNN

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Abstract—The improvement of traffic management and road safety depends on effective and real-time traffic signal classification. Although Convolutional Neural Networks (CNNs) have showed potential in this field, challenges arise from their high computing requirements. We provide an FPGA-based CNN accelerator designed specifically for traffic signal classification to address this issue. This accelerator achieves a compelling mix between performance and energy economy by parallelizing CNN layer processing and designing unique hardware. Our FPGA architecture makes use of the inherent CNN parallelism, which significantly accelerates performance compared to solutions using a standard CPU.

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I. INTRODUCTION

The projected goal is to demonstrate the FPGA accelerator's capabilities by preliminary analysis of well-established traffic signal classification datasets, emphasizing competitive classification accuracy and enhanced inference time compared to software-based alternatives. A preliminary investigation of the FPGA solution's energy efficiency is also planned, with an eye towards its usefulness in situations when power is limited.

This study presents a CNN accelerator design for real-time traffic signal categorization built on an FPGA. Our goal is to show how FPGA accelerators can effectively handle the computing demands of current computer vision applications in intelligent transportation systems. As transportation systems advance towards more intelligence and autonomy, the continuous development and assessment of an FPGA accelerator show promise for helping to provide effective and timely traffic signal classification.

II. FPGA AND CNN

A. Field Programmable Gate Array (FPGA)

Field-Programmable Gate Arrays (FPGAs) are hardware devices that may be reconfigured to carry out certain digital logic operations. FPGAs are ideal for speeding computationally demanding CNN procedures like convolutions and

pooling because they provide parallel processing and may be customised in terms of hardware architecture.

When compared to conventional processors, FPGAs can perform these processes in parallel, which increases throughput and decreases latency. FPGAs are powerful tools for boosting CNN performance, especially in scenarios demanding quick and effective image processing.

B. Convolutional Neural Network(CNN)

An advanced form of artificial neural network called convolutional neural network (CNN) is created specifically to process and analyze visual input, such as pictures and videos.

They are made up of layers with linked neurons, such as convolutional layers that use filters to identify different characteristics like edges or textures, pooling layers that reduce the sample size and fully connected layers that carry out classification. Due to its capacity to automatically learn and represent complicated visual patterns, CNNs are widely employed in computer vision tasks including picture identification, object detection, and image segmentation.

C. Integrated Development Environment(IDE)

Comprehensive IDEs for FPGA development, including design entry, synthesis, implementation, and debugging, are offered by tools like Xilinx Vivado or Intel Quartus Prime.

III. CONCLUSION

The study has two results: first, the use of FPGA accelerators designed for traffic signal categorization shows that real-time processing is feasible in contexts with limited resources. Second, the effort adds to the body of knowledge about CNN model deployment optimisation for FPGAs by revealing the trade-offs between accuracy, speed, and resource usage.

In conclusion, our study tries to close the gap between the real-time requirements of traffic signal categorization and the computing demands of CNNs. The project aims to provide the foundation for effective and responsive traffic management systems, with implications for improving traffic safety and urban mobility.

IV. REFERENCES

- 1) Y. Wu, "Review on FPGA-Based Accelerators in Deep learning," 2023 IEEE 6th Information Technology, Networking, Electronic and Automation Control Conference (ITNEC), Chongqing, China, 2023, pp. 452-456, doi: 10.1109/ITNEC56291.2023.10082175.
- 2) J. Kim, J. -K. Kang and Y. Kim, "A Low-Cost Fully Integer-Based CNN Accelerator on FPGA for Real-Time Traffic Sign Recognition," in IEEE Access, vol. 10, pp. 84626-84634, 2022, doi: 10.1109/ACCESS.2022.3197906.