[Documentation Index | Device index]

Configuration-Bit Settings for PIC32MZ2048EFM144

(Data Sheet # DS-60001320)

Usage:
#pragma config *SETTING = VALUE*
#pragma config_alt *SETTING = VALUE*
#pragma config_bf1 *SETTING = VALUE*
#pragma config_abf1 *SETTING = VALUE*
#pragma config_bf2 *SETTING = VALUE*
#pragma config_abf2 *SETTING = VALUE*

USERID	
USERID = 00000000	Range is from 0 to 0xffff

FMIIEN	Ethernet RMII/MII Enable
FMIIEN = OFF	RMII Enabled
FMIIEN = ON	MII Enabled

FETHIO	Ethernet I/O Pin Select
FETHIO = OFF	Alternate Ethernet I/O
FETHIO = ON	Default Ethernet I/O

PGL1WAY	Permission Group Lock One Way Configuration
PGL1WAY = ON	Allow only one reconfiguration
PGL1WAY = OFF	Allow multiple reconfigurations

PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration
PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USBID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FPLLIDIV	System PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
FPLLIDIV = DIV_2	2x Divider
FPLLIDIV = DIV_3	3x Divider
FPLLIDIV = DIV_4	4x Divider
FPLLIDIV = DIV_5	5x Divider
FPLLIDIV = DIV_6	6x Divider
FPLLIDIV = DIV_7	7x Divider
FPLLIDIV = DIV_8	8x Divider

FPLLRNG	System PLL Input Range
FPLLRNG = RANGE_BYPASS	Bypass
FPLLRNG = RANGE_5_10_MHZ	5-10 MHz Input
FPLLRNG = RANGE_8_16_MHZ	8-16 MHz Input
FPLLRNG = RANGE_13_26_MHZ	13-26 MHz Input
FPLLRNG = RANGE_21_42_MHZ	21-42 MHz Input
FPLLRNG = RANGE_34_68_MHZ	34-68 MHz Input

FPLLICLK	System PLL Input Clock Selection
FPLLICLK = PLL_FRC	FRC is input to the System PLL
FPLLICLK = PLL_POSC	POSC is input to the System PLL

FPLLMULT	System PLL Multiplier

FPLLMULT = MUL_1	PLL Multiply by 1
FPLLMULT = MUL_2	PLL Multiply by 2
FPLLMULT = MUL_3	PLL Multiply by 3
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FPLLMULT = MUL_116	PLL Multiply by 116

FPLLMULT = MUL_117	PLL Multiply by 117
FPLLMULT = MUL_118	PLL Multiply by 118
FPLLMULT = MUL_119	PLL Multiply by 119
FPLLMULT = MUL_120	PLL Multiply by 120
FPLLMULT = MUL_121	PLL Multiply by 121
FPLLMULT = MUL_122	PLL Multiply by 122
FPLLMULT = MUL_123	PLL Multiply by 123
FPLLMULT = MUL_124	PLL Multiply by 124
FPLLMULT = MUL_125	PLL Multiply by 125
FPLLMULT = MUL_126	PLL Multiply by 126
FPLLMULT = MUL_127	PLL Multiply by 127
FPLLMULT = MUL_128	PLL Multiply by 128

FPLLODIV	System PLL Output Clock Divider
FPLLODIV = DIV_2	2x Divider
FPLLODIV = DIV_4	4x Divider
FPLLODIV = DIV_8	8x Divider
FPLLODIV = DIV_16	16x Divider
FPLLODIV = DIV_32	32x Divider

UPLLFSEL	USB PLL Input Frequency Selection
UPLLFSEL = FREQ_24MHZ	USB PLL input is 24 MHz
UPLLFSEL = FREQ_12MHZ	USB PLL input is 12 MHz

FNOSC	Oscillator Selection Bits
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)
FNOSC = SPLL	System PLL
FNOSC = POSC	Primary Osc (HS,EC)
FNOSC = SOSC	Low Power Secondary Osc (SOSC)
FNOSC = LPRC	Low Power RC Osc (LPRC)

DMTINTV	DMT Count Window Interval
DMTINTV = WIN_0	Window/Interval value is zero
DMTINTV = WIN_1_2	Window/Interval value is 1/2 counter value
DMTINTV = WIN_3_4	Window/Interval value is 3/4 counter value
DMTINTV = WIN_7_8	Window/Interval value is 7/8 counter value
DMTINTV = WIN_15_16	Window/Interval value is 15/16 counter value
DMTINTV = WIN_31_32	Window/Interval value is 31/32 counter value
DMTINTV = WIN_63_64	Window/Interval value is 63/64 counter value
DMTINTV = WIN_127_128	Window/Interval value is 127/128 counter value

FSOSCEN	Secondary Oscillator Enable
FSOSCEN = OFF	Disable SOSC
FSOSCEN = ON	Enable SOSC

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = HS	HS osc mode
POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled
OSCIOFNC = ON	Enabled

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSDCMD	Clock Switch Disabled, FSCM Disabled
FCKSM = CSECMD	Clock Switch Enabled, FSCM Disabled

FCKSM = CSDCME	Clock Switch Disabled, FSCM Enabled
FCKSM = CSECME	Clock Switch Enabled, FSCM Enabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1
WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64
WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512
WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192
WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WDTSPGM	Watchdog Timer Stop During Flash Programming
WDTSPGM = RUN	WDT runs during Flash programming
WDTSPGM = STOP	WDT stops during Flash programming

WINDIS	Watchdog Timer Window Mode
WINDIS = NORMAL	Watchdog Timer is in non-Window mode
WINDIS = WINDOW	Watchdog Timer is in Window mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_25	Window size is 25%
FWDTWINSZ = WINSZ_37	Window size is 37.5%
FWDTWINSZ = WINSZ_50	Window size is 50%
FWDTWINSZ = WINSZ_75	Window size is 75%

DMTCNT	Deadman Timer Count Selection
DMTCNT = DMT8	2^8 (256)
DMTCNT = DMT9	2^9 (512)
DMTCNT = DMT10	2^10 (1024)
DMTCNT = DMT11	2^11 (2048)
DMTCNT = DMT12	2^12 (4096)
DMTCNT = DMT13	2^13 (8192)
DMTCNT = DMT14	2^14 (16384)
DMTCNT = DMT15	2^15 (32768)
DMTCNT = DMT16	2^16 (65536)
DMTCNT = DMT17	2^17 (131072)
DMTCNT = DMT18	2^18 (262144)
DMTCNT = DMT19	2^19 (524288)
DMTCNT = DMT20	2^20 (1048576)
DMTCNT = DMT21	2^21 (2097152)
DMTCNT = DMT22	2^22 (4194304)

DMTCNT = DMT23	2^23 (8388608)
DMTCNT = DMT24	2^24 (16777216)
DMTCNT = DMT25	2^25 (33554432)
DMTCNT = DMT26	2^26 (67108864)
DMTCNT = DMT27	2^27 (134217728)
DMTCNT = DMT28	2^28 (268435456)
DMTCNT = DMT29	2^29 (536870912)
DMTCNT = DMT30	2^30 (1073741824)
DMTCNT = DMT31	2^31 (2147483648)

FDMTEN	Deadman Timer Enable
FDMTEN = ON	Deadman Timer is enabled
FDMTEN = OFF	Deadman Timer is disabled

DEBUG	Background Debugger Enable
DEBUG = ON	Debugger is enabled
DEBUG = OFF	Debugger is disabled

JTAGEN	JTAG Enable
JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

TRCEN	Trace Enable
TRCEN = ON	Trace features in the CPU are enabled
TRCEN = OFF	Trace features in the CPU are disabled

BOOTISA	Boot ISA Selection
BOOTISA = MIPS32	Boot code and Exception code is MIPS32
BOOTISA = MICROMIPS	Boot code and Exception code is microMIPS

FECCCON	Dynamic Flash ECC Configuration
FECCCON = ON	Flash ECC is enabled (ECCCON bits are locked)
FECCCON = DYNAMIC	Dynamic Flash ECC is enabled (ECCCON bits are locked)
FECCCON = OFF_LOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are locked)
FECCCON = OFF_UNLOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are writable)

FSLEEP	Flash Sleep Mode
FSLEEP = OFF	Flash is powered down when the device is in Sleep mode
FSLEEP = VREGS	Flash power down is controlled by the VREGS bit

DBGPER	Debug Mode CPU Access Permission
DBGPER = ALLOW_PG2	Allow CPU access to Permission Group 2 permission regions
DBGPER = ALLOW_PG1	Allow CPU access to Permission Group 1 permission regions
DBGPER = ALLOW_PG0	Allow CPU access to Permission Group 0 permission regions
DBGPER = PG_1_0	PG0: Allow PG1: Allow PG2: Deny
DBGPER = PG_2_0	PG0: Allow PG1: Deny PG2: Allow
DBGPER = PG_2_1	PG0: Deny PG1: Allow PG2: Allow
DBGPER = PG_ALL	Allow CPU access to all permission regions
DBGPER = PG_NONE	Deny CPU access to all permission regions

SMCLR	Soft Master Clear Enable bit
SMCLR = MCLR_NORM	MCLR pin generates a normal system Reset
SMCLR = MCLR_POR	MCLR pin generates an emulated POR Reset

SOSCGAIN	Secondary Oscillator Gain Control bits
SOSCGAIN = GAIN_2X	2x gain setting
SOSCGAIN = GAIN_1_5X	1.5x gain setting
SOSCGAIN = GAIN_0_5X	0.5x gain setting

SOSCGAIN = GAIN_1X	1x gain setting
SOSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
SOSCGAIN = GAIN_LEVEL_2	Gain level 2
SOSCGAIN = GAIN_LEVEL_1	Gain level 1
SOSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

SOSCBOOST	Secondary Oscillator Boost Kick Start Enable bit
SOSCBOOST = ON	Boost the kick start of the oscillator
SOSCBOOST = OFF	Normal start of the oscillator

POSCGAIN	Primary Oscillator Gain Control bits
POSCGAIN = GAIN_2X	2x gain setting
POSCGAIN = GAIN_1_5X	1.5x gain setting
POSCGAIN = GAIN_0_5X	0.5x gain setting
POSCGAIN = GAIN_1X	1x gain setting
POSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
POSCGAIN = GAIN_LEVEL_2	Gain level 2
POSCGAIN = GAIN_LEVEL_1	Gain level 1
POSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

POSCBOOST	Primary Oscillator Boost Kick Start Enable bit
POSCBOOST = ON	Boost the kick start of the oscillator
POSCBOOST = OFF	Normal start of the oscillator

EJTAGBEN	EJTAG Boot
EJTAGBEN = NORMAL	Normal EJTAG functionality
EJTAGBEN = REDUCED	Reduced EJTAG functionality

CP	Code Protect
CP = ON	Protection Enabled
CP = OFF	Protection Disabled

TSEQ	Boot Flash True Sequence Number
TSEQ = 00000000	Range is from 0 to 0xffff

CSEQ	Boot Flash Complement Sequence Number
CSEQ = 00000000	Range is from 0 to 0xffff

ADCFG	
ADCFG = 00000000	Range is from 0 to 0xffffffff

ADCFG	
ADCFG = 00000000	Range is from 0 to 0xffffffff

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ADCFG = 00000000	Range is from 0 to 0xffffffff

ADCFG	
ADCFG = 00000000	Range is from 0 to 0xffffffff

SN	
SN = 00000000	Range is from 0 to 0xffffffff

SN	
SN = 00000000	Range is from 0 to 0xffffffff

USERID	
USERID = 00000000	Range is from 0 to 0xffff

FMIIEN	Ethernet RMII/MII Enable
FMIIEN = OFF	RMII Enabled
FMIIEN = ON	MII Enabled

FETHIO	Ethernet I/O Pin Select
FETHIO = OFF	Alternate Ethernet I/O
FETHIO = ON	Default Ethernet I/O

PGL1WAY	Permission Group Lock One Way Configuration
PGL1WAY = ON	Allow only one reconfiguration
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PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration
PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USBID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FPLLIDIV	System PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
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FPLLMULT = MUL_113	PLL Multiply by 113
FPLLMULT = MUL_114	PLL Multiply by 114
FPLLMULT = MUL_115	PLL Multiply by 115
FPLLMULT = MUL_116	PLL Multiply by 116
FPLLMULT = MUL_117	PLL Multiply by 117
FPLLMULT = MUL_118	PLL Multiply by 118
FPLLMULT = MUL_119	PLL Multiply by 119
FPLLMULT = MUL_120	PLL Multiply by 120
FPLLMULT = MUL_121	PLL Multiply by 121
FPLLMULT = MUL_122	PLL Multiply by 122
FPLLMULT = MUL_123	PLL Multiply by 123
FPLLMULT = MUL_124	PLL Multiply by 124
FPLLMULT = MUL_125	PLL Multiply by 125
FPLLMULT = MUL_126	PLL Multiply by 126
FPLLMULT = MUL_127	PLL Multiply by 127
FPLLMULT = MUL_128	PLL Multiply by 128

FPLLODIV	System PLL Output Clock Divider

FPLLODIV = DIV_2	2x Divider
FPLLODIV = DIV_4	4x Divider
FPLLODIV = DIV_8	8x Divider
FPLLODIV = DIV_16	16x Divider
FPLLODIV = DIV_32	32x Divider

UPLLFSEL	USB PLL Input Frequency Selection
UPLLFSEL = FREQ_24MHZ	USB PLL input is 24 MHz
UPLLFSEL = FREQ_12MHZ	USB PLL input is 12 MHz

FNOSC	Oscillator Selection Bits
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)
FNOSC = SPLL	System PLL
FNOSC = POSC	Primary Osc (HS,EC)
FNOSC = SOSC	Low Power Secondary Osc (SOSC)
FNOSC = LPRC	Low Power RC Osc (LPRC)

DMTINTV	DMT Count Window Interval
DMTINTV = WIN_0	Window/Interval value is zero
DMTINTV = WIN_1_2	Window/Interval value is 1/2 counter value
DMTINTV = WIN_3_4	Window/Interval value is 3/4 counter value
DMTINTV = WIN_7_8	Window/Interval value is 7/8 counter value
DMTINTV = WIN_15_16	Window/Interval value is 15/16 counter value
DMTINTV = WIN_31_32	Window/Interval value is 31/32 counter value
DMTINTV = WIN_63_64	Window/Interval value is 63/64 counter value
DMTINTV = WIN_127_128	Window/Interval value is 127/128 counter value

FSOSCEN	Secondary Oscillator Enable
FSOSCEN = OFF	Disable SOSC
FSOSCEN = ON	Enable SOSC

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = HS	HS osc mode
POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled
OSCIOFNC = ON	Enabled

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSDCMD	Clock Switch Disabled, FSCM Disabled
FCKSM = CSECMD	Clock Switch Enabled, FSCM Disabled
FCKSM = CSDCME	Clock Switch Disabled, FSCM Enabled
FCKSM = CSECME	Clock Switch Enabled, FSCM Enabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1
WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64
WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512

WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192
WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WDTSPGM	Watchdog Timer Stop During Flash Programming
WDTSPGM = RUN	WDT runs during Flash programming
WDTSPGM = STOP	WDT stops during Flash programming

WINDIS	Watchdog Timer Window Mode
WINDIS = NORMAL	Watchdog Timer is in non-Window mode
WINDIS = WINDOW	Watchdog Timer is in Window mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_25	Window size is 25%
FWDTWINSZ = WINSZ_37	Window size is 37.5%
FWDTWINSZ = WINSZ_50	Window size is 50%
FWDTWINSZ = WINSZ_75	Window size is 75%

DMTCNT	Deadman Timer Count Selection
DMTCNT = DMT8	2^8 (256)
DMTCNT = DMT9	2^9 (512)
DMTCNT = DMT10	2^10 (1024)
DMTCNT = DMT11	2^11 (2048)
DMTCNT = DMT12	2^12 (4096)
DMTCNT = DMT13	2^13 (8192)
DMTCNT = DMT14	2^14 (16384)
DMTCNT = DMT15	2^15 (32768)
DMTCNT = DMT16	2^16 (65536)
DMTCNT = DMT17	2^17 (131072)
DMTCNT = DMT18	2^18 (262144)
DMTCNT = DMT19	2^19 (524288)
DMTCNT = DMT20	2^20 (1048576)
DMTCNT = DMT21	2^21 (2097152)
DMTCNT = DMT22	2^22 (4194304)
DMTCNT = DMT23	2^23 (8388608)
DMTCNT = DMT24	2^24 (16777216)
DMTCNT = DMT25	2^25 (33554432)
DMTCNT = DMT26	2^26 (67108864)
DMTCNT = DMT27	2^27 (134217728)
DMTCNT = DMT28	2^28 (268435456)
DMTCNT = DMT29	2^29 (536870912)
DMTCNT = DMT30	2^30 (1073741824)
DMTCNT = DMT31	2^31 (2147483648)

FDMTEN	Deadman Timer Enable
FDMTEN = ON	Deadman Timer is enabled
FDMTEN = OFF	Deadman Timer is disabled

DEBUG	Background Debugger Enable

DEBUG = ON	Debugger is enabled
DEBUG = OFF	Debugger is disabled

JTAGEN	JTAG Enable
JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

TRCEN	Trace Enable
TRCEN = ON	Trace features in the CPU are enabled
TRCEN = OFF	Trace features in the CPU are disabled

BOOTISA	Boot ISA Selection
BOOTISA = MIPS32	Boot code and Exception code is MIPS32
BOOTISA = MICROMIPS	Boot code and Exception code is microMIPS

FECCCON	Dynamic Flash ECC Configuration
FECCCON = ON	Flash ECC is enabled (ECCCON bits are locked)
FECCCON = DYNAMIC	Dynamic Flash ECC is enabled (ECCCON bits are locked)
FECCCON = OFF_LOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are locked)
FECCCON = OFF_UNLOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are writable)

FSLEEP	Flash Sleep Mode
FSLEEP = OFF	Flash is powered down when the device is in Sleep mode
FSLEEP = VREGS	Flash power down is controlled by the VREGS bit

DBGPER	Debug Mode CPU Access Permission
DBGPER = ALLOW_PG2	Allow CPU access to Permission Group 2 permission regions
DBGPER = ALLOW_PG1	Allow CPU access to Permission Group 1 permission regions
DBGPER = ALLOW_PG0	Allow CPU access to Permission Group 0 permission regions
DBGPER = PG_1_0	PG0: Allow PG1: Allow PG2: Deny
DBGPER = PG_2_0	PG0: Allow PG1: Deny PG2: Allow
DBGPER = PG_2_1	PG0: Deny PG1: Allow PG2: Allow
DBGPER = PG_ALL	Allow CPU access to all permission regions
DBGPER = PG_NONE	Deny CPU access to all permission regions

SMCLR	Soft Master Clear Enable bit
SMCLR = MCLR_NORM	MCLR pin generates a normal system Reset
SMCLR = MCLR_POR	MCLR pin generates an emulated POR Reset

SOSCGAIN	Secondary Oscillator Gain Control bits
SOSCGAIN = GAIN_2X	2x gain setting
SOSCGAIN = GAIN_1_5X	1.5x gain setting
SOSCGAIN = GAIN_0_5X	0.5x gain setting
SOSCGAIN = GAIN_1X	1x gain setting
SOSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
SOSCGAIN = GAIN_LEVEL_2	Gain level 2
SOSCGAIN = GAIN_LEVEL_1	Gain level 1
SOSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

SOSCBOOST	Secondary Oscillator Boost Kick Start Enable bit
SOSCBOOST = ON	Boost the kick start of the oscillator
SOSCBOOST = OFF	Normal start of the oscillator

POSCGAIN	Primary Oscillator Gain Control bits
POSCGAIN = GAIN_2X	2x gain setting
POSCGAIN = GAIN_1_5X	1.5x gain setting
POSCGAIN = GAIN_0_5X	0.5x gain setting
POSCGAIN = GAIN_1X	1x gain setting

POSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
POSCGAIN = GAIN_LEVEL_2	Gain level 2
POSCGAIN = GAIN_LEVEL_1	Gain level 1
POSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

POSCBOOST	Primary Oscillator Boost Kick Start Enable bit
POSCBOOST = ON	Boost the kick start of the oscillator
POSCBOOST = OFF	Normal start of the oscillator

EJTAGBEN	EJTAG Boot
EJTAGBEN = NORMAL	Normal EJTAG functionality
EJTAGBEN = REDUCED	Reduced EJTAG functionality

CP	Code Protect
CP = ON	Protection Enabled
CP = OFF	Protection Disabled

TSEQ	Boot Flash True Sequence Number
TSEQ = 00000000	Range is from 0 to 0xffff

CSEQ	Boot Flash Complement Sequence Number
CSEQ = 00000000	Range is from 0 to 0xffff

USERID	
USERID = 00000000	Range is from 0 to 0xffff

FMIIEN	Ethernet RMII/MII Enable
FMIIEN = OFF	RMII Enabled
FMIIEN = ON	MII Enabled

FETHIO	Ethernet I/O Pin Select
FETHIO = OFF	Alternate Ethernet I/O
FETHIO = ON	Default Ethernet I/O

PGL1WAY	Permission Group Lock One Way Configuration
PGL1WAY = ON	Allow only one reconfiguration
PGL1WAY = OFF	Allow multiple reconfigurations

PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration
PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USBID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FPLLIDIV	System PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
FPLLIDIV = DIV_2	2x Divider
FPLLIDIV = DIV_3	3x Divider
FPLLIDIV = DIV_4	4x Divider
FPLLIDIV = DIV_5	5x Divider
FPLLIDIV = DIV_6	6x Divider
FPLLIDIV = DIV_7	7x Divider
FPLLIDIV = DIV_8	8x Divider

FPLLRNG	System PLL Input Range
FPLLRNG = RANGE_BYPASS	Bypass
FPLLRNG = RANGE_5_10_MHZ	5-10 MHz Input

FPLLRNG = RANGE_8_16_MHZ	8-16 MHz Input
FPLLRNG = RANGE_13_26_MHZ	13-26 MHz Input
FPLLRNG = RANGE_21_42_MHZ	21-42 MHz Input
FPLLRNG = RANGE_34_68_MHZ	34-68 MHz Input

FPLLICLK	System PLL Input Clock Selection
FPLLICLK = PLL_FRC	FRC is input to the System PLL
FPLLICLK = PLL_POSC	POSC is input to the System PLL

FPLLMULT	System PLL Multiplier
FPLLMULT = MUL_1	PLL Multiply by 1
FPLLMULT = MUL_2	PLL Multiply by 2
FPLLMULT = MUL_3	PLL Multiply by 3
FPLLMULT = MUL_4	PLL Multiply by 4
FPLLMULT = MUL_5	PLL Multiply by 5
FPLLMULT = MUL_6	PLL Multiply by 6
FPLLMULT = MUL_7	PLL Multiply by 7
FPLLMULT = MUL_8	PLL Multiply by 8
FPLLMULT = MUL_9	PLL Multiply by 9
FPLLMULT = MUL_10	PLL Multiply by 10
FPLLMULT = MUL_11	PLL Multiply by 11
FPLLMULT = MUL_12	PLL Multiply by 12
FPLLMULT = MUL_13	PLL Multiply by 13
FPLLMULT = MUL_14	PLL Multiply by 14
FPLLMULT = MUL_15	PLL Multiply by 15
FPLLMULT = MUL_16	PLL Multiply by 16
FPLLMULT = MUL_17	PLL Multiply by 17
FPLLMULT = MUL_18	PLL Multiply by 18
FPLLMULT = MUL_19	PLL Multiply by 19
FPLLMULT = MUL_20	PLL Multiply by 20
FPLLMULT = MUL_21	PLL Multiply by 21
FPLLMULT = MUL_22	PLL Multiply by 22
FPLLMULT = MUL_23	PLL Multiply by 23
FPLLMULT = MUL_24	PLL Multiply by 24
FPLLMULT = MUL_25	PLL Multiply by 25
FPLLMULT = MUL_26	PLL Multiply by 26
FPLLMULT = MUL_27	PLL Multiply by 27
FPLLMULT = MUL_28	PLL Multiply by 28
FPLLMULT = MUL_29	PLL Multiply by 29
FPLLMULT = MUL_30	PLL Multiply by 30
FPLLMULT = MUL_31	PLL Multiply by 31
FPLLMULT = MUL_32	PLL Multiply by 32
FPLLMULT = MUL_33	PLL Multiply by 33
FPLLMULT = MUL_34	PLL Multiply by 34
FPLLMULT = MUL_35	PLL Multiply by 35
FPLLMULT = MUL_36	PLL Multiply by 36
FPLLMULT = MUL_37	PLL Multiply by 37
FPLLMULT = MUL_38	PLL Multiply by 38
FPLLMULT = MUL_39	PLL Multiply by 39
FPLLMULT = MUL_40	PLL Multiply by 40
FPLLMULT = MUL_41	PLL Multiply by 41
FPLLMULT = MUL_42	PLL Multiply by 42
FPLLMULT = MUL_43	PLL Multiply by 43
FPLLMULT = MUL_44	PLL Multiply by 44
FPLLMULT = MUL_45	PLL Multiply by 45
FPLLMULT = MUL_46	PLL Multiply by 46
FPLLMULT = MUL_47	PLL Multiply by 47
FPLLMULT = MUL_48	PLL Multiply by 48
FPLLMULT = MUL_49	PLL Multiply by 49

FPLLMULT = MUL_50	PLL Multiply by 50
FPLLMULT = MUL_51	PLL Multiply by 51
FPLLMULT = MUL_52	PLL Multiply by 52
FPLLMULT = MUL_53	PLL Multiply by 53
FPLLMULT = MUL_54	PLL Multiply by 54
FPLLMULT = MUL_55	PLL Multiply by 55
FPLLMULT = MUL_56	PLL Multiply by 56
FPLLMULT = MUL_57	PLL Multiply by 57
FPLLMULT = MUL_58	PLL Multiply by 58
FPLLMULT = MUL_59	PLL Multiply by 59
FPLLMULT = MUL_60	PLL Multiply by 60
FPLLMULT = MUL_61	PLL Multiply by 61
FPLLMULT = MUL_62	PLL Multiply by 62
FPLLMULT = MUL_63	PLL Multiply by 63
FPLLMULT = MUL_64	PLL Multiply by 64
FPLLMULT = MUL_65	PLL Multiply by 65
FPLLMULT = MUL_66	PLL Multiply by 66
FPLLMULT = MUL_67	PLL Multiply by 67
FPLLMULT = MUL_68	PLL Multiply by 68
FPLLMULT = MUL_69	PLL Multiply by 69
FPLLMULT = MUL_70	PLL Multiply by 70
FPLLMULT = MUL_71	PLL Multiply by 71
FPLLMULT = MUL_72	PLL Multiply by 72
FPLLMULT = MUL_73	PLL Multiply by 73
FPLLMULT = MUL_74	PLL Multiply by 74
FPLLMULT = MUL_75	PLL Multiply by 75
FPLLMULT = MUL_76	PLL Multiply by 76
FPLLMULT = MUL_77	PLL Multiply by 77
FPLLMULT = MUL_78	PLL Multiply by 78
FPLLMULT = MUL_79	PLL Multiply by 79
FPLLMULT = MUL_80	PLL Multiply by 80
FPLLMULT = MUL_81	PLL Multiply by 81
FPLLMULT = MUL_82	PLL Multiply by 82
FPLLMULT = MUL_83	PLL Multiply by 83
FPLLMULT = MUL_84	PLL Multiply by 84
FPLLMULT = MUL_85	PLL Multiply by 85
FPLLMULT = MUL_86	PLL Multiply by 86
FPLLMULT = MUL_87	PLL Multiply by 87
FPLLMULT = MUL_88	PLL Multiply by 88
FPLLMULT = MUL_89	PLL Multiply by 89
FPLLMULT = MUL_90	PLL Multiply by 90
FPLLMULT = MUL_91	PLL Multiply by 91
FPLLMULT = MUL_92	PLL Multiply by 92
FPLLMULT = MUL_93	PLL Multiply by 93
FPLLMULT = MUL_94	PLL Multiply by 94
FPLLMULT = MUL_95	PLL Multiply by 95
FPLLMULT = MUL_96	PLL Multiply by 96
FPLLMULT = MUL_97	PLL Multiply by 97
FPLLMULT = MUL_98	PLL Multiply by 98
FPLLMULT = MUL_99	PLL Multiply by 99
FPLLMULT = MUL_100	PLL Multiply by 100
FPLLMULT = MUL_101	PLL Multiply by 101
FPLLMULT = MUL_102	PLL Multiply by 102
FPLLMULT = MUL_103	PLL Multiply by 103
FPLLMULT = MUL_104	PLL Multiply by 104
FPLLMULT = MUL_105	PLL Multiply by 105
FPLLMULT = MUL_106	PLL Multiply by 106
FPLLMULT = MUL_107	PLL Multiply by 107

FPLLMULT = MUL_108	PLL Multiply by 108
FPLLMULT = MUL_109	PLL Multiply by 109
FPLLMULT = MUL_110	PLL Multiply by 110
FPLLMULT = MUL_111	PLL Multiply by 111
FPLLMULT = MUL_112	PLL Multiply by 112
FPLLMULT = MUL_113	PLL Multiply by 113
FPLLMULT = MUL_114	PLL Multiply by 114
FPLLMULT = MUL_115	PLL Multiply by 115
FPLLMULT = MUL_116	PLL Multiply by 116
FPLLMULT = MUL_117	PLL Multiply by 117
FPLLMULT = MUL_118	PLL Multiply by 118
FPLLMULT = MUL_119	PLL Multiply by 119
FPLLMULT = MUL_120	PLL Multiply by 120
FPLLMULT = MUL_121	PLL Multiply by 121
FPLLMULT = MUL_122	PLL Multiply by 122
FPLLMULT = MUL_123	PLL Multiply by 123
FPLLMULT = MUL_124	PLL Multiply by 124
FPLLMULT = MUL_125	PLL Multiply by 125
FPLLMULT = MUL_126	PLL Multiply by 126
FPLLMULT = MUL_127	PLL Multiply by 127
FPLLMULT = MUL_128	PLL Multiply by 128

FPLLODIV	System PLL Output Clock Divider
FPLLODIV = DIV_2	2x Divider
FPLLODIV = DIV_4	4x Divider
FPLLODIV = DIV_8	8x Divider
FPLLODIV = DIV_16	16x Divider
FPLLODIV = DIV_32	32x Divider

UPLLFSEL	USB PLL Input Frequency Selection
UPLLFSEL = FREQ_24MHZ	USB PLL input is 24 MHz
UPLLFSEL = FREQ_12MHZ	USB PLL input is 12 MHz

FNOSC	Oscillator Selection Bits
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)
FNOSC = SPLL	System PLL
FNOSC = POSC	Primary Osc (HS,EC)
FNOSC = SOSC	Low Power Secondary Osc (SOSC)
FNOSC = LPRC	Low Power RC Osc (LPRC)

DMTINTV	DMT Count Window Interval
DMTINTV = WIN_0	Window/Interval value is zero
DMTINTV = WIN_1_2	Window/Interval value is 1/2 counter value
DMTINTV = WIN_3_4	Window/Interval value is 3/4 counter value
DMTINTV = WIN_7_8	Window/Interval value is 7/8 counter value
DMTINTV = WIN_15_16	Window/Interval value is 15/16 counter value
DMTINTV = WIN_31_32	Window/Interval value is 31/32 counter value
DMTINTV = WIN_63_64	Window/Interval value is 63/64 counter value
DMTINTV = WIN_127_128	Window/Interval value is 127/128 counter value

FSOSCEN	Secondary Oscillator Enable
FSOSCEN = OFF	Disable SOSC
FSOSCEN = ON	Enable SOSC

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = HS	HS osc mode

POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled
OSCIOFNC = ON	Enabled

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSDCMD	Clock Switch Disabled, FSCM Disabled
FCKSM = CSECMD	Clock Switch Enabled, FSCM Disabled
FCKSM = CSDCME	Clock Switch Disabled, FSCM Enabled
FCKSM = CSECME	Clock Switch Enabled, FSCM Enabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1
WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64
WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512
WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192
WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WDTSPGM	Watchdog Timer Stop During Flash Programming
WDTSPGM = RUN	WDT runs during Flash programming
WDTSPGM = STOP	WDT stops during Flash programming

WINDIS	Watchdog Timer Window Mode
WINDIS = NORMAL	Watchdog Timer is in non-Window mode
WINDIS = WINDOW	Watchdog Timer is in Window mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_25	Window size is 25%
FWDTWINSZ = WINSZ_37	Window size is 37.5%
FWDTWINSZ = WINSZ_50	Window size is 50%
FWDTWINSZ = WINSZ_75	Window size is 75%

DMTCNT	Deadman Timer Count Selection
DMTCNT = DMT8	2^8 (256)
DMTCNT = DMT9	2^9 (512)
DMTCNT = DMT10	2^10 (1024)
DMTCNT = DMT11	2^11 (2048)
DMTCNT = DMT12	2^12 (4096)
DMTCNT = DMT13	2^13 (8192)
DMTCNT = DMT14	2^14 (16384)

DMTCNT = DMT15	2^15 (32768)
DMTCNT = DMT16	2^16 (65536)
DMTCNT = DMT17	2^17 (131072)
DMTCNT = DMT18	2^18 (262144)
DMTCNT = DMT19	2^19 (524288)
DMTCNT = DMT20	2^20 (1048576)
DMTCNT = DMT21	2^21 (2097152)
DMTCNT = DMT22	2^22 (4194304)
DMTCNT = DMT23	2^23 (8388608)
DMTCNT = DMT24	2^24 (16777216)
DMTCNT = DMT25	2^25 (33554432)
DMTCNT = DMT26	2^26 (67108864)
DMTCNT = DMT27	2^27 (134217728)
DMTCNT = DMT28	2^28 (268435456)
DMTCNT = DMT29	2^29 (536870912)
DMTCNT = DMT30	2^30 (1073741824)
DMTCNT = DMT31	2^31 (2147483648)

FDMTEN	Deadman Timer Enable
FDMTEN = ON	Deadman Timer is enabled
FDMTEN = OFF	Deadman Timer is disabled

DEBUG	Background Debugger Enable
DEBUG = ON	Debugger is enabled
DEBUG = OFF	Debugger is disabled

JTAGEN	JTAG Enable
JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

TRCEN	Trace Enable
TRCEN = ON	Trace features in the CPU are enabled
TRCEN = OFF	Trace features in the CPU are disabled

BOOTISA	Boot ISA Selection
BOOTISA = MIPS32	Boot code and Exception code is MIPS32
BOOTISA = MICROMIPS	Boot code and Exception code is microMIPS

FECCCON	Dynamic Flash ECC Configuration
FECCCON = ON	Flash ECC is enabled (ECCCON bits are locked)
FECCCON = DYNAMIC	Dynamic Flash ECC is enabled (ECCCON bits are locked)
FECCCON = OFF_LOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are locked)
FECCCON = OFF_UNLOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are writable)

FSLEEP	Flash Sleep Mode
FSLEEP = OFF	Flash is powered down when the device is in Sleep mode
FSLEEP = VREGS	Flash power down is controlled by the VREGS bit

DBGPER	Debug Mode CPU Access Permission
DBGPER = ALLOW_PG2	Allow CPU access to Permission Group 2 permission regions
DBGPER = ALLOW_PG1	Allow CPU access to Permission Group 1 permission regions
DBGPER = ALLOW_PG0	Allow CPU access to Permission Group 0 permission regions
DBGPER = PG_1_0	PG0: Allow PG1: Allow PG2: Deny
DBGPER = PG_2_0	PG0: Allow PG1: Deny PG2: Allow
DBGPER = PG_2_1	PG0: Deny PG1: Allow PG2: Allow
DBGPER = PG_ALL	Allow CPU access to all permission regions
DBGPER = PG_NONE	Deny CPU access to all permission regions

SMCLR	Soft Master Clear Enable bit
SMCLR = MCLR_NORM	MCLR pin generates a normal system Reset
SMCLR = MCLR_POR	MCLR pin generates an emulated POR Reset

SOSCGAIN	Secondary Oscillator Gain Control bits
SOSCGAIN = GAIN_2X	2x gain setting
SOSCGAIN = GAIN_1_5X	1.5x gain setting
SOSCGAIN = GAIN_0_5X	0.5x gain setting
SOSCGAIN = GAIN_1X	1x gain setting
SOSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
SOSCGAIN = GAIN_LEVEL_2	Gain level 2
SOSCGAIN = GAIN_LEVEL_1	Gain level 1
SOSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

SOSCBOOST	Secondary Oscillator Boost Kick Start Enable bit
SOSCBOOST = ON	Boost the kick start of the oscillator
SOSCBOOST = OFF	Normal start of the oscillator

POSCGAIN	Primary Oscillator Gain Control bits
POSCGAIN = GAIN_2X	2x gain setting
POSCGAIN = GAIN_1_5X	1.5x gain setting
POSCGAIN = GAIN_0_5X	0.5x gain setting
POSCGAIN = GAIN_1X	1x gain setting
POSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
POSCGAIN = GAIN_LEVEL_2	Gain level 2
POSCGAIN = GAIN_LEVEL_1	Gain level 1
POSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

POSCBOOST	Primary Oscillator Boost Kick Start Enable bit
POSCBOOST = ON	Boost the kick start of the oscillator
POSCBOOST = OFF	Normal start of the oscillator

EJTAGBEN	EJTAG Boot
EJTAGBEN = NORMAL	Normal EJTAG functionality
EJTAGBEN = REDUCED	Reduced EJTAG functionality

CP	Code Protect
CP = ON	Protection Enabled
CP = OFF	Protection Disabled

TSEQ	Boot Flash True Sequence Number
TSEQ = 00000000	Range is from 0 to 0xffff

CSEQ	Boot Flash Complement Sequence Number
CSEQ = 00000000	Range is from 0 to 0xffff

USERID	
USERID = 00000000	Range is from 0 to 0xffff

FMIIEN	Ethernet RMII/MII Enable
FMIIEN = OFF	RMII Enabled
FMIIEN = ON	MII Enabled

FETHIO	Ethernet I/O Pin Select
FETHIO = OFF	Alternate Ethernet I/O
FETHIO = ON	Default Ethernet I/O

PGL1WAY	Permission Group Lock One Way Configuration
PGL1WAY = ON	Allow only one reconfiguration
PGL1WAY = OFF	Allow multiple reconfigurations

PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration

PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USBID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FPLLIDIV	System PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
FPLLIDIV = DIV_2	2x Divider
FPLLIDIV = DIV_3	3x Divider
FPLLIDIV = DIV_4	4x Divider
FPLLIDIV = DIV_5	5x Divider
FPLLIDIV = DIV_6	6x Divider
FPLLIDIV = DIV_7	7x Divider
FPLLIDIV = DIV_8	8x Divider

FPLLRNG	System PLL Input Range
FPLLRNG = RANGE_BYPASS	Bypass
FPLLRNG = RANGE_5_10_MHZ	5-10 MHz Input
FPLLRNG = RANGE_8_16_MHZ	8-16 MHz Input
FPLLRNG = RANGE_13_26_MHZ	13-26 MHz Input
FPLLRNG = RANGE_21_42_MHZ	21-42 MHz Input
FPLLRNG = RANGE_34_68_MHZ	34-68 MHz Input

FPLLICLK	System PLL Input Clock Selection
FPLLICLK = PLL_FRC	FRC is input to the System PLL
FPLLICLK = PLL_POSC	POSC is input to the System PLL

FPLLMULT	System PLL Multiplier
FPLLMULT = MUL_1	PLL Multiply by 1
FPLLMULT = MUL_2	PLL Multiply by 2
FPLLMULT = MUL_3	PLL Multiply by 3
FPLLMULT = MUL_4	PLL Multiply by 4
FPLLMULT = MUL_5	PLL Multiply by 5
FPLLMULT = MUL_6	PLL Multiply by 6
FPLLMULT = MUL_7	PLL Multiply by 7
FPLLMULT = MUL_8	PLL Multiply by 8
FPLLMULT = MUL_9	PLL Multiply by 9
FPLLMULT = MUL_10	PLL Multiply by 10
FPLLMULT = MUL_11	PLL Multiply by 11
FPLLMULT = MUL_12	PLL Multiply by 12
FPLLMULT = MUL_13	PLL Multiply by 13
FPLLMULT = MUL_14	PLL Multiply by 14
FPLLMULT = MUL_15	PLL Multiply by 15
FPLLMULT = MUL_16	PLL Multiply by 16
FPLLMULT = MUL_17	PLL Multiply by 17
FPLLMULT = MUL_18	PLL Multiply by 18
FPLLMULT = MUL_19	PLL Multiply by 19
FPLLMULT = MUL_20	PLL Multiply by 20
FPLLMULT = MUL_21	PLL Multiply by 21
FPLLMULT = MUL_22	PLL Multiply by 22
FPLLMULT = MUL_23	PLL Multiply by 23
FPLLMULT = MUL_24	PLL Multiply by 24
FPLLMULT = MUL_25	PLL Multiply by 25
FPLLMULT = MUL_26	PLL Multiply by 26
FPLLMULT = MUL_27	PLL Multiply by 27

FPLLMULT = MUL_28	PLL Multiply by 28
FPLLMULT = MUL_29	PLL Multiply by 29
FPLLMULT = MUL_30	PLL Multiply by 30
FPLLMULT = MUL_31	PLL Multiply by 31
FPLLMULT = MUL_32	PLL Multiply by 32
FPLLMULT = MUL_33	PLL Multiply by 33
FPLLMULT = MUL_34	PLL Multiply by 34
FPLLMULT = MUL_35	PLL Multiply by 35
FPLLMULT = MUL_36	PLL Multiply by 36
FPLLMULT = MUL_37	PLL Multiply by 37
FPLLMULT = MUL_38	PLL Multiply by 38
FPLLMULT = MUL_39	PLL Multiply by 39
FPLLMULT = MUL_40	PLL Multiply by 40
FPLLMULT = MUL_41	PLL Multiply by 41
FPLLMULT = MUL_42	PLL Multiply by 42
FPLLMULT = MUL_43	PLL Multiply by 43
FPLLMULT = MUL_44	PLL Multiply by 44
FPLLMULT = MUL_45	PLL Multiply by 45
FPLLMULT = MUL_46	PLL Multiply by 46
FPLLMULT = MUL_47	PLL Multiply by 47
FPLLMULT = MUL_48	PLL Multiply by 48
FPLLMULT = MUL_49	PLL Multiply by 49
FPLLMULT = MUL_50	PLL Multiply by 50
FPLLMULT = MUL_51	PLL Multiply by 51
FPLLMULT = MUL_52	PLL Multiply by 52
FPLLMULT = MUL_53	PLL Multiply by 53
FPLLMULT = MUL_54	PLL Multiply by 54
FPLLMULT = MUL_55	PLL Multiply by 55
FPLLMULT = MUL_56	PLL Multiply by 56
FPLLMULT = MUL_57	PLL Multiply by 57
FPLLMULT = MUL_58	PLL Multiply by 58
FPLLMULT = MUL_59	PLL Multiply by 59
FPLLMULT = MUL_60	PLL Multiply by 60
FPLLMULT = MUL_61	PLL Multiply by 61
FPLLMULT = MUL_62	PLL Multiply by 62
FPLLMULT = MUL_63	PLL Multiply by 63
FPLLMULT = MUL_64	PLL Multiply by 64
FPLLMULT = MUL_65	PLL Multiply by 65
FPLLMULT = MUL_66	PLL Multiply by 66
FPLLMULT = MUL_67	PLL Multiply by 67
FPLLMULT = MUL_68	PLL Multiply by 68
FPLLMULT = MUL_69	PLL Multiply by 69
FPLLMULT = MUL_70	PLL Multiply by 70
FPLLMULT = MUL_71	PLL Multiply by 71
FPLLMULT = MUL_72	PLL Multiply by 72
FPLLMULT = MUL_73	PLL Multiply by 73
FPLLMULT = MUL_74	PLL Multiply by 74
FPLLMULT = MUL_75	PLL Multiply by 75
FPLLMULT = MUL_76	PLL Multiply by 76
FPLLMULT = MUL_77	PLL Multiply by 77
FPLLMULT = MUL_78	PLL Multiply by 78
FPLLMULT = MUL_79	PLL Multiply by 79
FPLLMULT = MUL_80	PLL Multiply by 80
FPLLMULT = MUL_81	PLL Multiply by 81
FPLLMULT = MUL_82	PLL Multiply by 82
FPLLMULT = MUL_83	PLL Multiply by 83
FPLLMULT = MUL_84	PLL Multiply by 84
FPLLMULT = MUL_85	PLL Multiply by 85

FPLLMULT = MUL_86	PLL Multiply by 86
FPLLMULT = MUL_87	PLL Multiply by 87
FPLLMULT = MUL_88	PLL Multiply by 88
FPLLMULT = MUL_89	PLL Multiply by 89
FPLLMULT = MUL_90	PLL Multiply by 90
FPLLMULT = MUL_91	PLL Multiply by 91
FPLLMULT = MUL_92	PLL Multiply by 92
FPLLMULT = MUL_93	PLL Multiply by 93
FPLLMULT = MUL_94	PLL Multiply by 94
FPLLMULT = MUL_95	PLL Multiply by 95
FPLLMULT = MUL_96	PLL Multiply by 96
FPLLMULT = MUL_97	PLL Multiply by 97
FPLLMULT = MUL_98	PLL Multiply by 98
FPLLMULT = MUL_99	PLL Multiply by 99
FPLLMULT = MUL_100	PLL Multiply by 100
FPLLMULT = MUL_101	PLL Multiply by 101
FPLLMULT = MUL_102	PLL Multiply by 102
FPLLMULT = MUL_103	PLL Multiply by 103
FPLLMULT = MUL_104	PLL Multiply by 104
FPLLMULT = MUL_105	PLL Multiply by 105
FPLLMULT = MUL_106	PLL Multiply by 106
FPLLMULT = MUL_107	PLL Multiply by 107
FPLLMULT = MUL_108	PLL Multiply by 108
FPLLMULT = MUL_109	PLL Multiply by 109
FPLLMULT = MUL_110	PLL Multiply by 110
FPLLMULT = MUL_111	PLL Multiply by 111
FPLLMULT = MUL_112	PLL Multiply by 112
FPLLMULT = MUL_113	PLL Multiply by 113
FPLLMULT = MUL_114	PLL Multiply by 114
FPLLMULT = MUL_115	PLL Multiply by 115
FPLLMULT = MUL_116	PLL Multiply by 116
FPLLMULT = MUL_117	PLL Multiply by 117
FPLLMULT = MUL_118	PLL Multiply by 118
FPLLMULT = MUL_119	PLL Multiply by 119
FPLLMULT = MUL_120	PLL Multiply by 120
FPLLMULT = MUL_121	PLL Multiply by 121
FPLLMULT = MUL_122	PLL Multiply by 122
FPLLMULT = MUL_123	PLL Multiply by 123
FPLLMULT = MUL_124	PLL Multiply by 124
FPLLMULT = MUL_125	PLL Multiply by 125
FPLLMULT = MUL_126	PLL Multiply by 126
FPLLMULT = MUL_127	PLL Multiply by 127
FPLLMULT = MUL_128	PLL Multiply by 128

FPLLODIV	System PLL Output Clock Divider
FPLLODIV = DIV_2	2x Divider
FPLLODIV = DIV_4	4x Divider
FPLLODIV = DIV_8	8x Divider
FPLLODIV = DIV_16	16x Divider
FPLLODIV = DIV_32	32x Divider

UPLLFSEL	USB PLL Input Frequency Selection
UPLLFSEL = FREQ_24MHZ	USB PLL input is 24 MHz
UPLLFSEL = FREQ_12MHZ	USB PLL input is 12 MHz

FNOSC	Oscillator Selection Bits
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)
FNOSC = SPLL	System PLL
FNOSC = POSC	Primary Osc (HS,EC)

FNOSC = SOSC	Low Power Secondary Osc (SOSC)
FNOSC = LPRC	Low Power RC Osc (LPRC)

DMTINTV	DMT Count Window Interval
DMTINTV = WIN_0	Window/Interval value is zero
DMTINTV = WIN_1_2	Window/Interval value is 1/2 counter value
DMTINTV = WIN_3_4	Window/Interval value is 3/4 counter value
DMTINTV = WIN_7_8	Window/Interval value is 7/8 counter value
DMTINTV = WIN_15_16	Window/Interval value is 15/16 counter value
DMTINTV = WIN_31_32	Window/Interval value is 31/32 counter value
DMTINTV = WIN_63_64	Window/Interval value is 63/64 counter value
DMTINTV = WIN_127_128	Window/Interval value is 127/128 counter value

FSOSCEN	Secondary Oscillator Enable
FSOSCEN = OFF	Disable SOSC
FSOSCEN = ON	Enable SOSC

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = HS	HS osc mode
POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled
OSCIOFNC = ON	Enabled

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSDCMD	Clock Switch Disabled, FSCM Disabled
FCKSM = CSECMD	Clock Switch Enabled, FSCM Disabled
FCKSM = CSDCME	Clock Switch Disabled, FSCM Enabled
FCKSM = CSECME	Clock Switch Enabled, FSCM Enabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1
WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64
WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512
WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192
WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WDTSPGM	Watchdog Timer Stop During Flash Programming
WDTSPGM = RUN	WDT runs during Flash programming

WDTSPGM = STOP	WDT stops during Flash programming

WINDIS	Watchdog Timer Window Mode
WINDIS = NORMAL	Watchdog Timer is in non-Window mode
WINDIS = WINDOW	Watchdog Timer is in Window mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_25	Window size is 25%
FWDTWINSZ = WINSZ_37	Window size is 37.5%
FWDTWINSZ = WINSZ_50	Window size is 50%
FWDTWINSZ = WINSZ_75	Window size is 75%

DMTCNT	Deadman Timer Count Selection
DMTCNT = DMT8	2^8 (256)
DMTCNT = DMT9	2^9 (512)
DMTCNT = DMT10	2^10 (1024)
DMTCNT = DMT11	2^11 (2048)
DMTCNT = DMT12	2^12 (4096)
DMTCNT = DMT13	2^13 (8192)
DMTCNT = DMT14	2^14 (16384)
DMTCNT = DMT15	2^15 (32768)
DMTCNT = DMT16	2^16 (65536)
DMTCNT = DMT17	2^17 (131072)
DMTCNT = DMT18	2^18 (262144)
DMTCNT = DMT19	2^19 (524288)
DMTCNT = DMT20	2^20 (1048576)
DMTCNT = DMT21	2^21 (2097152)
DMTCNT = DMT22	2^22 (4194304)
DMTCNT = DMT23	2^23 (8388608)
DMTCNT = DMT24	2^24 (16777216)
DMTCNT = DMT25	2^25 (33554432)
DMTCNT = DMT26	2^26 (67108864)
DMTCNT = DMT27	2^27 (134217728)
DMTCNT = DMT28	2^28 (268435456)
DMTCNT = DMT29	2^29 (536870912)
DMTCNT = DMT30	2^30 (1073741824)
DMTCNT = DMT31	2^31 (2147483648)

FDMTEN	Deadman Timer Enable
FDMTEN = ON	Deadman Timer is enabled
FDMTEN = OFF	Deadman Timer is disabled

DEBUG	Background Debugger Enable
DEBUG = ON	Debugger is enabled
DEBUG = OFF	Debugger is disabled

JTAGEN	JTAG Enable
JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

TRCEN	Trace Enable
TRCEN = ON	Trace features in the CPU are enabled
TRCEN = OFF	Trace features in the CPU are disabled

BOOTISA	Boot ISA Selection
BOOTISA = MIPS32	Boot code and Exception code is MIPS32
BOOTISA = MICROMIPS	Boot code and Exception code is microMIPS

FECCCON	Dynamic Flash ECC Configuration
FECCCON = ON	Flash ECC is enabled (ECCCON bits are locked)
FECCCON = DYNAMIC	Dynamic Flash ECC is enabled (ECCCON bits are locked)
FECCCON = OFF_LOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are locked)
FECCCON = OFF_UNLOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are writable)

FSLEEP	Flash Sleep Mode
FSLEEP = OFF	Flash is powered down when the device is in Sleep mode
FSLEEP = VREGS	Flash power down is controlled by the VREGS bit

DBGPER	Debug Mode CPU Access Permission
DBGPER = ALLOW_PG2	Allow CPU access to Permission Group 2 permission regions
DBGPER = ALLOW_PG1	Allow CPU access to Permission Group 1 permission regions
DBGPER = ALLOW_PG0	Allow CPU access to Permission Group 0 permission regions
DBGPER = PG_1_0	PG0: Allow PG1: Allow PG2: Deny
DBGPER = PG_2_0	PG0: Allow PG1: Deny PG2: Allow
DBGPER = PG_2_1	PG0: Deny PG1: Allow PG2: Allow
DBGPER = PG_ALL	Allow CPU access to all permission regions
DBGPER = PG_NONE	Deny CPU access to all permission regions

SMCLR	Soft Master Clear Enable bit
SMCLR = MCLR_NORM	MCLR pin generates a normal system Reset
SMCLR = MCLR_POR	MCLR pin generates an emulated POR Reset

SOSCGAIN	Secondary Oscillator Gain Control bits
SOSCGAIN = GAIN_2X	2x gain setting
SOSCGAIN = GAIN_1_5X	1.5x gain setting
SOSCGAIN = GAIN_0_5X	0.5x gain setting
SOSCGAIN = GAIN_1X	1x gain setting
SOSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
SOSCGAIN = GAIN_LEVEL_2	Gain level 2
SOSCGAIN = GAIN_LEVEL_1	Gain level 1
SOSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

SOSCBOOST	Secondary Oscillator Boost Kick Start Enable bit
SOSCBOOST = ON	Boost the kick start of the oscillator
SOSCBOOST = OFF	Normal start of the oscillator

POSCGAIN	Primary Oscillator Gain Control bits
POSCGAIN = GAIN_2X	2x gain setting
POSCGAIN = GAIN_1_5X	1.5x gain setting
POSCGAIN = GAIN_0_5X	0.5x gain setting
POSCGAIN = GAIN_1X	1x gain setting
POSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
POSCGAIN = GAIN_LEVEL_2	Gain level 2
POSCGAIN = GAIN_LEVEL_1	Gain level 1
POSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

POSCBOOST	Primary Oscillator Boost Kick Start Enable bit
POSCBOOST = ON	Boost the kick start of the oscillator
POSCBOOST = OFF	Normal start of the oscillator

EJTAGBEN	EJTAG Boot
EJTAGBEN = NORMAL	Normal EJTAG functionality
EJTAGBEN = REDUCED	Reduced EJTAG functionality

CP	Code Protect

CP = ON	Protection Enabled
CP = OFF	Protection Disabled

TSEQ	Boot Flash True Sequence Number
TSEQ = 00000000	Range is from 0 to 0xffff

CSEQ	Boot Flash Complement Sequence Number
CSEQ = 00000000	Range is from 0 to 0xffff

USERID	
USERID = 00000000	Range is from 0 to 0xffff

FMIIEN	Ethernet RMII/MII Enable
FMIIEN = OFF	RMII Enabled
FMIIEN = ON	MII Enabled

FETHIO	Ethernet I/O Pin Select
FETHIO = OFF	Alternate Ethernet I/O
FETHIO = ON	Default Ethernet I/O

PGL1WAY	Permission Group Lock One Way Configuration
PGL1WAY = ON	Allow only one reconfiguration
PGL1WAY = OFF	Allow multiple reconfigurations

PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration
PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USBID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FPLLIDIV	System PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
FPLLIDIV = DIV_2	2x Divider
FPLLIDIV = DIV_3	3x Divider
FPLLIDIV = DIV_4	4x Divider
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FPLLIDIV = DIV_6	6x Divider
FPLLIDIV = DIV_7	7x Divider
FPLLIDIV = DIV_8	8x Divider

FPLLRNG	System PLL Input Range
FPLLRNG = RANGE_BYPASS	Bypass
FPLLRNG = RANGE_5_10_MHZ	5-10 MHz Input
FPLLRNG = RANGE_8_16_MHZ	8-16 MHz Input
FPLLRNG = RANGE_13_26_MHZ	13-26 MHz Input
FPLLRNG = RANGE_21_42_MHZ	21-42 MHz Input
FPLLRNG = RANGE_34_68_MHZ	34-68 MHz Input

FPLLICLK	System PLL Input Clock Selection
FPLLICLK = PLL_FRC	FRC is input to the System PLL
FPLLICLK = PLL_POSC	POSC is input to the System PLL

FPLLMULT	System PLL Multiplier
FPLLMULT = MUL_1	PLL Multiply by 1
FPLLMULT = MUL_2	PLL Multiply by 2
FPLLMULT = MUL_3	PLL Multiply by 3
FPLLMULT = MUL_4	PLL Multiply by 4

FPLLMULT = MUL_5	PLL Multiply by 5
FPLLMULT = MUL_6	PLL Multiply by 6
FPLLMULT = MUL_7	PLL Multiply by 7
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FPLLMULT = MUL_107	PLL Multiply by 107
FPLLMULT = MUL_108	PLL Multiply by 108
FPLLMULT = MUL_109	PLL Multiply by 109
FPLLMULT = MUL_110	PLL Multiply by 110
FPLLMULT = MUL_111	PLL Multiply by 111
FPLLMULT = MUL_112	PLL Multiply by 112
FPLLMULT = MUL_113	PLL Multiply by 113
FPLLMULT = MUL_114	PLL Multiply by 114
FPLLMULT = MUL_115	PLL Multiply by 115
FPLLMULT = MUL_116	PLL Multiply by 116
FPLLMULT = MUL_117	PLL Multiply by 117
FPLLMULT = MUL_118	PLL Multiply by 118
FPLLMULT = MUL_119	PLL Multiply by 119
FPLLMULT = MUL_120	PLL Multiply by 120

FPLLMULT = MUL_121	PLL Multiply by 121
FPLLMULT = MUL_122	PLL Multiply by 122
FPLLMULT = MUL_123	PLL Multiply by 123
FPLLMULT = MUL_124	PLL Multiply by 124
FPLLMULT = MUL_125	PLL Multiply by 125
FPLLMULT = MUL_126	PLL Multiply by 126
FPLLMULT = MUL_127	PLL Multiply by 127
FPLLMULT = MUL_128	PLL Multiply by 128

FPLLODIV	System PLL Output Clock Divider
FPLLODIV = DIV_2	2x Divider
FPLLODIV = DIV_4	4x Divider
FPLLODIV = DIV_8	8x Divider
FPLLODIV = DIV_16	16x Divider
FPLLODIV = DIV_32	32x Divider

UPLLFSEL	USB PLL Input Frequency Selection
UPLLFSEL = FREQ_24MHZ	USB PLL input is 24 MHz
UPLLFSEL = FREQ_12MHZ	USB PLL input is 12 MHz

FNOSC	Oscillator Selection Bits
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)
FNOSC = SPLL	System PLL
FNOSC = POSC	Primary Osc (HS,EC)
FNOSC = SOSC	Low Power Secondary Osc (SOSC)
FNOSC = LPRC	Low Power RC Osc (LPRC)

DMTINTV	DMT Count Window Interval
DMTINTV = WIN_0	Window/Interval value is zero
DMTINTV = WIN_1_2	Window/Interval value is 1/2 counter value
DMTINTV = WIN_3_4	Window/Interval value is 3/4 counter value
DMTINTV = WIN_7_8	Window/Interval value is 7/8 counter value
DMTINTV = WIN_15_16	Window/Interval value is 15/16 counter value
DMTINTV = WIN_31_32	Window/Interval value is 31/32 counter value
DMTINTV = WIN_63_64	Window/Interval value is 63/64 counter value
DMTINTV = WIN_127_128	Window/Interval value is 127/128 counter value

FSOSCEN	Secondary Oscillator Enable
FSOSCEN = OFF	Disable SOSC
FSOSCEN = ON	Enable SOSC

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = HS	HS osc mode
POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled
OSCIOFNC = ON	Enabled

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSDCMD	Clock Switch Disabled, FSCM Disabled
FCKSM = CSECMD	Clock Switch Enabled, FSCM Disabled
FCKSM = CSDCME	Clock Switch Disabled, FSCM Enabled
FCKSM = CSECME	Clock Switch Enabled, FSCM Enabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1

WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64
WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512
WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192
WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WDTSPGM	Watchdog Timer Stop During Flash Programming
WDTSPGM = RUN	WDT runs during Flash programming
WDTSPGM = STOP	WDT stops during Flash programming

WINDIS	Watchdog Timer Window Mode
WINDIS = NORMAL	Watchdog Timer is in non-Window mode
WINDIS = WINDOW	Watchdog Timer is in Window mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_25	Window size is 25%
FWDTWINSZ = WINSZ_37	Window size is 37.5%
FWDTWINSZ = WINSZ_50	Window size is 50%
FWDTWINSZ = WINSZ_75	Window size is 75%

DMTCNT	Deadman Timer Count Selection
DMTCNT = DMT8	2^8 (256)
DMTCNT = DMT9	2^9 (512)
DMTCNT = DMT10	2^10 (1024)
DMTCNT = DMT11	2^11 (2048)
DMTCNT = DMT12	2^12 (4096)
DMTCNT = DMT13	2^13 (8192)
DMTCNT = DMT14	2^14 (16384)
DMTCNT = DMT15	2^15 (32768)
DMTCNT = DMT16	2^16 (65536)
DMTCNT = DMT17	2^17 (131072)
DMTCNT = DMT18	2^18 (262144)
DMTCNT = DMT19	2^19 (524288)
DMTCNT = DMT20	2^20 (1048576)
DMTCNT = DMT21	2^21 (2097152)
DMTCNT = DMT22	2^22 (4194304)
DMTCNT = DMT23	2^23 (8388608)
DMTCNT = DMT24	2^24 (16777216)
DMTCNT = DMT25	2^25 (33554432)
DMTCNT = DMT26	2^26 (67108864)
DMTCNT = DMT27	2^27 (134217728)

DMTCNT = DMT28	2^28 (268435456)
DMTCNT = DMT29	2^29 (536870912)
DMTCNT = DMT30	2^30 (1073741824)
DMTCNT = DMT31	2^31 (2147483648)

FDMTEN	Deadman Timer Enable
FDMTEN = ON	Deadman Timer is enabled
FDMTEN = OFF	Deadman Timer is disabled

DEBUG	Background Debugger Enable
DEBUG = ON	Debugger is enabled
DEBUG = OFF	Debugger is disabled

JTAGEN	JTAG Enable
JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

TRCEN	Trace Enable
TRCEN = ON	Trace features in the CPU are enabled
TRCEN = OFF	Trace features in the CPU are disabled

BOOTISA	Boot ISA Selection
BOOTISA = MIPS32	Boot code and Exception code is MIPS32
BOOTISA = MICROMIPS	Boot code and Exception code is microMIPS

FECCCON	Dynamic Flash ECC Configuration
FECCCON = ON	Flash ECC is enabled (ECCCON bits are locked)
FECCCON = DYNAMIC	Dynamic Flash ECC is enabled (ECCCON bits are locked)
FECCCON = OFF_LOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are locked)
FECCCON = OFF_UNLOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are writable)

FSLEEP	Flash Sleep Mode
FSLEEP = OFF	Flash is powered down when the device is in Sleep mode
FSLEEP = VREGS	Flash power down is controlled by the VREGS bit

DBGPER	Debug Mode CPU Access Permission
DBGPER = ALLOW_PG2	Allow CPU access to Permission Group 2 permission regions
DBGPER = ALLOW_PG1	Allow CPU access to Permission Group 1 permission regions
DBGPER = ALLOW_PG0	Allow CPU access to Permission Group 0 permission regions
DBGPER = PG_1_0	PG0: Allow PG1: Allow PG2: Deny
DBGPER = PG_2_0	PG0: Allow PG1: Deny PG2: Allow
DBGPER = PG_2_1	PG0: Deny PG1: Allow PG2: Allow
DBGPER = PG_ALL	Allow CPU access to all permission regions
DBGPER = PG_NONE	Deny CPU access to all permission regions

SMCLR	Soft Master Clear Enable bit
SMCLR = MCLR_NORM	MCLR pin generates a normal system Reset
SMCLR = MCLR_POR	MCLR pin generates an emulated POR Reset

SOSCGAIN	Secondary Oscillator Gain Control bits
SOSCGAIN = GAIN_2X	2x gain setting
SOSCGAIN = GAIN_1_5X	1.5x gain setting
SOSCGAIN = GAIN_0_5X	0.5x gain setting
SOSCGAIN = GAIN_1X	1x gain setting
SOSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
SOSCGAIN = GAIN_LEVEL_2	Gain level 2
SOSCGAIN = GAIN_LEVEL_1	Gain level 1
SOSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

SOSCBOOST	Secondary Oscillator Boost Kick Start Enable bit
SOSCBOOST = ON	Boost the kick start of the oscillator
SOSCBOOST = OFF	Normal start of the oscillator

POSCGAIN	Primary Oscillator Gain Control bits
POSCGAIN = GAIN_2X	2x gain setting
POSCGAIN = GAIN_1_5X	1.5x gain setting
POSCGAIN = GAIN_0_5X	0.5x gain setting
POSCGAIN = GAIN_1X	1x gain setting
POSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
POSCGAIN = GAIN_LEVEL_2	Gain level 2
POSCGAIN = GAIN_LEVEL_1	Gain level 1
POSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

POSCBOOST	Primary Oscillator Boost Kick Start Enable bit
POSCBOOST = ON	Boost the kick start of the oscillator
POSCBOOST = OFF	Normal start of the oscillator

EJTAGBEN	EJTAG Boot
EJTAGBEN = NORMAL	Normal EJTAG functionality
EJTAGBEN = REDUCED	Reduced EJTAG functionality

CP	Code Protect
CP = ON	Protection Enabled
CP = OFF	Protection Disabled

TSEQ	Boot Flash True Sequence Number
TSEQ = 00000000	Range is from 0 to 0xffff

CSEQ	Boot Flash Complement Sequence Number
CSEQ = 00000000	Range is from 0 to 0xffff

USERID	
USERID = 00000000	Range is from 0 to 0xffff

FMIIEN	Ethernet RMII/MII Enable
FMIIEN = OFF	RMII Enabled
FMIIEN = ON	MII Enabled

FETHIO	Ethernet I/O Pin Select
FETHIO = OFF	Alternate Ethernet I/O
FETHIO = ON	Default Ethernet I/O

PGL1WAY	Permission Group Lock One Way Configuration
PGL1WAY = ON	Allow only one reconfiguration
PGL1WAY = OFF	Allow multiple reconfigurations

PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration
PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USBID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FPLLIDIV	System PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
FPLLIDIV = DIV_2	2x Divider
FPLLIDIV = DIV_3	3x Divider

FPLLIDIV = DIV_4	4x Divider
FPLLIDIV = DIV_5	5x Divider
FPLLIDIV = DIV_6	6x Divider
FPLLIDIV = DIV_7	7x Divider
FPLLIDIV = DIV_8	8x Divider

FPLLRNG	System PLL Input Range
FPLLRNG = RANGE_BYPASS	Bypass
FPLLRNG = RANGE_5_10_MHZ	5-10 MHz Input
FPLLRNG = RANGE_8_16_MHZ	8-16 MHz Input
FPLLRNG = RANGE_13_26_MHZ	13-26 MHz Input
FPLLRNG = RANGE_21_42_MHZ	21-42 MHz Input
FPLLRNG = RANGE_34_68_MHZ	34-68 MHz Input

FPLLICLK	System PLL Input Clock Selection
FPLLICLK = PLL_FRC	FRC is input to the System PLL
FPLLICLK = PLL_POSC	POSC is input to the System PLL

FPLLMULT	System PLL Multiplier
FPLLMULT = MUL_1	PLL Multiply by 1
FPLLMULT = MUL_2	PLL Multiply by 2
FPLLMULT = MUL_3	PLL Multiply by 3
FPLLMULT = MUL_4	PLL Multiply by 4
FPLLMULT = MUL_5	PLL Multiply by 5
FPLLMULT = MUL_6	PLL Multiply by 6
FPLLMULT = MUL_7	PLL Multiply by 7
FPLLMULT = MUL_8	PLL Multiply by 8
FPLLMULT = MUL_9	PLL Multiply by 9
FPLLMULT = MUL_10	PLL Multiply by 10
FPLLMULT = MUL_11	PLL Multiply by 11
FPLLMULT = MUL_12	PLL Multiply by 12
FPLLMULT = MUL_13	PLL Multiply by 13
FPLLMULT = MUL_14	PLL Multiply by 14
FPLLMULT = MUL_15	PLL Multiply by 15
FPLLMULT = MUL_16	PLL Multiply by 16
FPLLMULT = MUL_17	PLL Multiply by 17
FPLLMULT = MUL_18	PLL Multiply by 18
FPLLMULT = MUL_19	PLL Multiply by 19
FPLLMULT = MUL_20	PLL Multiply by 20
FPLLMULT = MUL_21	PLL Multiply by 21
FPLLMULT = MUL_22	PLL Multiply by 22
FPLLMULT = MUL_23	PLL Multiply by 23
FPLLMULT = MUL_24	PLL Multiply by 24
FPLLMULT = MUL_25	PLL Multiply by 25
FPLLMULT = MUL_26	PLL Multiply by 26
FPLLMULT = MUL_27	PLL Multiply by 27
FPLLMULT = MUL_28	PLL Multiply by 28
FPLLMULT = MUL_29	PLL Multiply by 29
FPLLMULT = MUL_30	PLL Multiply by 30
FPLLMULT = MUL_31	PLL Multiply by 31
FPLLMULT = MUL_32	PLL Multiply by 32
FPLLMULT = MUL_33	PLL Multiply by 33
FPLLMULT = MUL_34	PLL Multiply by 34
FPLLMULT = MUL_35	PLL Multiply by 35
FPLLMULT = MUL_36	PLL Multiply by 36
FPLLMULT = MUL_37	PLL Multiply by 37
FPLLMULT = MUL_38	PLL Multiply by 38
FPLLMULT = MUL_39	PLL Multiply by 39
FPLLMULT = MUL_40	PLL Multiply by 40

FPLLMULT = MUL_41	PLL Multiply by 41
FPLLMULT = MUL_42	PLL Multiply by 42
FPLLMULT = MUL_43	PLL Multiply by 43
FPLLMULT = MUL_44	PLL Multiply by 44
FPLLMULT = MUL_45	PLL Multiply by 45
FPLLMULT = MUL_46	PLL Multiply by 46
FPLLMULT = MUL_47	PLL Multiply by 47
FPLLMULT = MUL_48	PLL Multiply by 48
FPLLMULT = MUL_49	PLL Multiply by 49
FPLLMULT = MUL_50	PLL Multiply by 50
FPLLMULT = MUL_51	PLL Multiply by 51
FPLLMULT = MUL_52	PLL Multiply by 52
FPLLMULT = MUL_53	PLL Multiply by 53
FPLLMULT = MUL_54	PLL Multiply by 54
FPLLMULT = MUL_55	PLL Multiply by 55
FPLLMULT = MUL_56	PLL Multiply by 56
FPLLMULT = MUL_57	PLL Multiply by 57
FPLLMULT = MUL_58	PLL Multiply by 58
FPLLMULT = MUL_59	PLL Multiply by 59
FPLLMULT = MUL_60	PLL Multiply by 60
FPLLMULT = MUL_61	PLL Multiply by 61
FPLLMULT = MUL_62	PLL Multiply by 62
FPLLMULT = MUL_63	PLL Multiply by 63
FPLLMULT = MUL_64	PLL Multiply by 64
FPLLMULT = MUL_65	PLL Multiply by 65
FPLLMULT = MUL_66	PLL Multiply by 66
FPLLMULT = MUL_67	PLL Multiply by 67
FPLLMULT = MUL_68	PLL Multiply by 68
FPLLMULT = MUL_69	PLL Multiply by 69
FPLLMULT = MUL_70	PLL Multiply by 70
FPLLMULT = MUL_71	PLL Multiply by 71
FPLLMULT = MUL_72	PLL Multiply by 72
FPLLMULT = MUL_73	PLL Multiply by 73
FPLLMULT = MUL_74	PLL Multiply by 74
FPLLMULT = MUL_75	PLL Multiply by 75
FPLLMULT = MUL_76	PLL Multiply by 76
FPLLMULT = MUL_77	PLL Multiply by 77
FPLLMULT = MUL_78	PLL Multiply by 78
FPLLMULT = MUL_79	PLL Multiply by 79
FPLLMULT = MUL_80	PLL Multiply by 80
FPLLMULT = MUL_81	PLL Multiply by 81
FPLLMULT = MUL_82	PLL Multiply by 82
FPLLMULT = MUL_83	PLL Multiply by 83
FPLLMULT = MUL_84	PLL Multiply by 84
FPLLMULT = MUL_85	PLL Multiply by 85
FPLLMULT = MUL_86	PLL Multiply by 86
FPLLMULT = MUL_87	PLL Multiply by 87
FPLLMULT = MUL_88	PLL Multiply by 88
FPLLMULT = MUL_89	PLL Multiply by 89
FPLLMULT = MUL_90	PLL Multiply by 90
FPLLMULT = MUL_91	PLL Multiply by 91
FPLLMULT = MUL_92	PLL Multiply by 92
FPLLMULT = MUL_93	PLL Multiply by 93
FPLLMULT = MUL_94	PLL Multiply by 94
FPLLMULT = MUL_95	PLL Multiply by 95
FPLLMULT = MUL_96	PLL Multiply by 96
FPLLMULT = MUL_97	PLL Multiply by 97
FPLLMULT = MUL_98	PLL Multiply by 98

FPLLMULT = MUL_99	PLL Multiply by 99
FPLLMULT = MUL_100	PLL Multiply by 100
FPLLMULT = MUL_101	PLL Multiply by 101
FPLLMULT = MUL_102	PLL Multiply by 102
FPLLMULT = MUL_103	PLL Multiply by 103
FPLLMULT = MUL_104	PLL Multiply by 104
FPLLMULT = MUL_105	PLL Multiply by 105
FPLLMULT = MUL_106	PLL Multiply by 106
FPLLMULT = MUL_107	PLL Multiply by 107
FPLLMULT = MUL_108	PLL Multiply by 108
FPLLMULT = MUL_109	PLL Multiply by 109
FPLLMULT = MUL_110	PLL Multiply by 110
FPLLMULT = MUL_111	PLL Multiply by 111
FPLLMULT = MUL_112	PLL Multiply by 112
FPLLMULT = MUL_113	PLL Multiply by 113
FPLLMULT = MUL_114	PLL Multiply by 114
FPLLMULT = MUL_115	PLL Multiply by 115
FPLLMULT = MUL_116	PLL Multiply by 116
FPLLMULT = MUL_117	PLL Multiply by 117
FPLLMULT = MUL_118	PLL Multiply by 118
FPLLMULT = MUL_119	PLL Multiply by 119
FPLLMULT = MUL_120	PLL Multiply by 120
FPLLMULT = MUL_121	PLL Multiply by 121
FPLLMULT = MUL_122	PLL Multiply by 122
FPLLMULT = MUL_123	PLL Multiply by 123
FPLLMULT = MUL_124	PLL Multiply by 124
FPLLMULT = MUL_125	PLL Multiply by 125
FPLLMULT = MUL_126	PLL Multiply by 126
FPLLMULT = MUL_127	PLL Multiply by 127
FPLLMULT = MUL_128	PLL Multiply by 128

FPLLODIV	System PLL Output Clock Divider
FPLLODIV = DIV_2	2x Divider
FPLLODIV = DIV_4	4x Divider
FPLLODIV = DIV_8	8x Divider
FPLLODIV = DIV_16	16x Divider
FPLLODIV = DIV_32	32x Divider

UPLLFSEL	USB PLL Input Frequency Selection
UPLLFSEL = FREQ_24MHZ	USB PLL input is 24 MHz
UPLLFSEL = FREQ_12MHZ	USB PLL input is 12 MHz

FNOSC	Oscillator Selection Bits
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)
FNOSC = SPLL	System PLL
FNOSC = POSC	Primary Osc (HS,EC)
FNOSC = SOSC	Low Power Secondary Osc (SOSC)
FNOSC = LPRC	Low Power RC Osc (LPRC)

DMTINTV	DMT Count Window Interval
DMTINTV = WIN_0	Window/Interval value is zero
DMTINTV = WIN_1_2	Window/Interval value is 1/2 counter value
DMTINTV = WIN_3_4	Window/Interval value is 3/4 counter value
DMTINTV = WIN_7_8	Window/Interval value is 7/8 counter value
DMTINTV = WIN_15_16	Window/Interval value is 15/16 counter value
DMTINTV = WIN_31_32	Window/Interval value is 31/32 counter value
DMTINTV = WIN_63_64	Window/Interval value is 63/64 counter value
DMTINTV = WIN_127_128	Window/Interval value is 127/128 counter value

FSOSCEN	Secondary Oscillator Enable

FSOSCEN = OFF	Disable SOSC
FSOSCEN = ON	Enable SOSC

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = HS	HS osc mode
POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled
OSCIOFNC = ON	Enabled

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSDCMD	Clock Switch Disabled, FSCM Disabled
FCKSM = CSECMD	Clock Switch Enabled, FSCM Disabled
FCKSM = CSDCME	Clock Switch Disabled, FSCM Enabled
FCKSM = CSECME	Clock Switch Enabled, FSCM Enabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1
WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64
WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512
WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192
WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WDTSPGM	Watchdog Timer Stop During Flash Programming
WDTSPGM = RUN	WDT runs during Flash programming
WDTSPGM = STOP	WDT stops during Flash programming

WINDIS	Watchdog Timer Window Mode
WINDIS = NORMAL	Watchdog Timer is in non-Window mode
WINDIS = WINDOW	Watchdog Timer is in Window mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_25	Window size is 25%
FWDTWINSZ = WINSZ_37	Window size is 37.5%
FWDTWINSZ = WINSZ_50	Window size is 50%

FWDTWINSZ = WINSZ_75	Window size is 75%

DMTCNT	Deadman Timer Count Selection
DMTCNT = DMT8	2^8 (256)
DMTCNT = DMT9	2^9 (512)
DMTCNT = DMT10	2^10 (1024)
DMTCNT = DMT11	2^11 (2048)
DMTCNT = DMT12	2^12 (4096)
DMTCNT = DMT13	2^13 (8192)
DMTCNT = DMT14	2^14 (16384)
DMTCNT = DMT15	2^15 (32768)
DMTCNT = DMT16	2^16 (65536)
DMTCNT = DMT17	2^17 (131072)
DMTCNT = DMT18	2^18 (262144)
DMTCNT = DMT19	2^19 (524288)
DMTCNT = DMT20	2^20 (1048576)
DMTCNT = DMT21	2^21 (2097152)
DMTCNT = DMT22	2^22 (4194304)
DMTCNT = DMT23	2^23 (8388608)
DMTCNT = DMT24	2^24 (16777216)
DMTCNT = DMT25	2^25 (33554432)
DMTCNT = DMT26	2^26 (67108864)
DMTCNT = DMT27	2^27 (134217728)
DMTCNT = DMT28	2^28 (268435456)
DMTCNT = DMT29	2^29 (536870912)
DMTCNT = DMT30	2^30 (1073741824)
DMTCNT = DMT31	2^31 (2147483648)

FDMTEN	Deadman Timer Enable
FDMTEN = ON	Deadman Timer is enabled
FDMTEN = OFF	Deadman Timer is disabled

DEBUG	Background Debugger Enable
DEBUG = ON	Debugger is enabled
DEBUG = OFF	Debugger is disabled

JTAGEN	JTAG Enable
JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

TRCEN	Trace Enable
TRCEN = ON	Trace features in the CPU are enabled
TRCEN = OFF	Trace features in the CPU are disabled

BOOTISA	Boot ISA Selection
BOOTISA = MIPS32	Boot code and Exception code is MIPS32
BOOTISA = MICROMIPS	Boot code and Exception code is microMIPS

FECCCON	Dynamic Flash ECC Configuration
FECCCON = ON	Flash ECC is enabled (ECCCON bits are locked)
FECCCON = DYNAMIC	Dynamic Flash ECC is enabled (ECCCON bits are locked)
FECCCON = OFF_LOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are locked)
FECCCON = OFF_UNLOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are writable)

FSLEEP	Flash Sleep Mode
FSLEEP = OFF	Flash is powered down when the device is in Sleep mode
FSLEEP = VREGS	Flash power down is controlled by the VREGS bit

DBGPER	Debug Mode CPU Access Permission
DBGPER = ALLOW_PG2	Allow CPU access to Permission Group 2 permission regions
DBGPER = ALLOW_PG1	Allow CPU access to Permission Group 1 permission regions
DBGPER = ALLOW_PG0	Allow CPU access to Permission Group 0 permission regions
DBGPER = PG_1_0	PG0: Allow PG1: Allow PG2: Deny
DBGPER = PG_2_0	PG0: Allow PG1: Deny PG2: Allow
DBGPER = PG_2_1	PG0: Deny PG1: Allow PG2: Allow
DBGPER = PG_ALL	Allow CPU access to all permission regions
DBGPER = PG_NONE	Deny CPU access to all permission regions

SMCLR	Soft Master Clear Enable bit
SMCLR = MCLR_NORM	MCLR pin generates a normal system Reset
SMCLR = MCLR_POR	MCLR pin generates an emulated POR Reset

SOSCGAIN	Secondary Oscillator Gain Control bits
SOSCGAIN = GAIN_2X	2x gain setting
SOSCGAIN = GAIN_1_5X	1.5x gain setting
SOSCGAIN = GAIN_0_5X	0.5x gain setting
SOSCGAIN = GAIN_1X	1x gain setting
SOSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
SOSCGAIN = GAIN_LEVEL_2	Gain level 2
SOSCGAIN = GAIN_LEVEL_1	Gain level 1
SOSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

SOSCBOOST	Secondary Oscillator Boost Kick Start Enable bit
SOSCBOOST = ON	Boost the kick start of the oscillator
SOSCBOOST = OFF	Normal start of the oscillator

POSCGAIN	Primary Oscillator Gain Control bits
POSCGAIN = GAIN_2X	2x gain setting
POSCGAIN = GAIN_1_5X	1.5x gain setting
POSCGAIN = GAIN_0_5X	0.5x gain setting
POSCGAIN = GAIN_1X	1x gain setting
POSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
POSCGAIN = GAIN_LEVEL_2	Gain level 2
POSCGAIN = GAIN_LEVEL_1	Gain level 1
POSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

POSCBOOST	Primary Oscillator Boost Kick Start Enable bit
POSCBOOST = ON	Boost the kick start of the oscillator
POSCBOOST = OFF	Normal start of the oscillator

EJTAGBEN	EJTAG Boot
EJTAGBEN = NORMAL	Normal EJTAG functionality
EJTAGBEN = REDUCED	Reduced EJTAG functionality

CP	Code Protect
CP = ON	Protection Enabled
CP = OFF	Protection Disabled

TSEQ	Boot Flash True Sequence Number
TSEQ = 00000000	Range is from 0 to 0xffff

CSEQ	Boot Flash Complement Sequence Number
CSEQ = 00000000	Range is from 0 to 0xffff

USERID	
USERID = 00000000	Range is from 0 to 0xffff

FMIIEN	Ethernet RMII/MII Enable
FMIIEN = OFF	RMII Enabled
FMIIEN = ON	MII Enabled

FETHIO	Ethernet I/O Pin Select
FETHIO = OFF	Alternate Ethernet I/O
FETHIO = ON	Default Ethernet I/O

PGL1WAY	Permission Group Lock One Way Configuration
PGL1WAY = ON	Allow only one reconfiguration
PGL1WAY = OFF	Allow multiple reconfigurations

PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration
PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USBID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FPLLIDIV	System PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
FPLLIDIV = DIV_2	2x Divider
FPLLIDIV = DIV_3	3x Divider
FPLLIDIV = DIV_4	4x Divider
FPLLIDIV = DIV_5	5x Divider
FPLLIDIV = DIV_6	6x Divider
FPLLIDIV = DIV_7	7x Divider
FPLLIDIV = DIV_8	8x Divider

FPLLRNG	System PLL Input Range
FPLLRNG = RANGE_BYPASS	Bypass
FPLLRNG = RANGE_5_10_MHZ	5-10 MHz Input
FPLLRNG = RANGE_8_16_MHZ	8-16 MHz Input
FPLLRNG = RANGE_13_26_MHZ	13-26 MHz Input
FPLLRNG = RANGE_21_42_MHZ	21-42 MHz Input
FPLLRNG = RANGE_34_68_MHZ	34-68 MHz Input

FPLLICLK	System PLL Input Clock Selection
FPLLICLK = PLL_FRC	FRC is input to the System PLL
FPLLICLK = PLL_POSC	POSC is input to the System PLL

FPLLMULT	System PLL Multiplier
FPLLMULT = MUL_1	PLL Multiply by 1
FPLLMULT = MUL_2	PLL Multiply by 2
FPLLMULT = MUL_3	PLL Multiply by 3
FPLLMULT = MUL_4	PLL Multiply by 4
FPLLMULT = MUL_5	PLL Multiply by 5
FPLLMULT = MUL_6	PLL Multiply by 6
FPLLMULT = MUL_7	PLL Multiply by 7
FPLLMULT = MUL_8	PLL Multiply by 8
FPLLMULT = MUL_9	PLL Multiply by 9
FPLLMULT = MUL_10	PLL Multiply by 10
FPLLMULT = MUL_11	PLL Multiply by 11
FPLLMULT = MUL_12	PLL Multiply by 12
FPLLMULT = MUL_13	PLL Multiply by 13
FPLLMULT = MUL_14	PLL Multiply by 14
FPLLMULT = MUL_15	PLL Multiply by 15
FPLLMULT = MUL_16	PLL Multiply by 16
FPLLMULT = MUL_17	PLL Multiply by 17
FPLLMULT = MUL_18	PLL Multiply by 18

FPLLMULT = MUL_19	PLL Multiply by 19
FPLLMULT = MUL_20	PLL Multiply by 20
FPLLMULT = MUL_21	PLL Multiply by 21
FPLLMULT = MUL_22	PLL Multiply by 22
FPLLMULT = MUL_23	PLL Multiply by 23
FPLLMULT = MUL_24	PLL Multiply by 24
FPLLMULT = MUL_25	PLL Multiply by 25
FPLLMULT = MUL_26	PLL Multiply by 26
FPLLMULT = MUL_27	PLL Multiply by 27
FPLLMULT = MUL_28	PLL Multiply by 28
FPLLMULT = MUL_29	PLL Multiply by 29
FPLLMULT = MUL_30	PLL Multiply by 30
FPLLMULT = MUL_31	PLL Multiply by 31
FPLLMULT = MUL_32	PLL Multiply by 32
FPLLMULT = MUL_33	PLL Multiply by 33
FPLLMULT = MUL_34	PLL Multiply by 34
FPLLMULT = MUL_35	PLL Multiply by 35
FPLLMULT = MUL_36	PLL Multiply by 36
FPLLMULT = MUL_37	PLL Multiply by 37
FPLLMULT = MUL_38	PLL Multiply by 38
FPLLMULT = MUL_39	PLL Multiply by 39
FPLLMULT = MUL_40	PLL Multiply by 40
FPLLMULT = MUL_41	PLL Multiply by 41
FPLLMULT = MUL_42	PLL Multiply by 42
FPLLMULT = MUL_43	PLL Multiply by 43
FPLLMULT = MUL_44	PLL Multiply by 44
FPLLMULT = MUL_45	PLL Multiply by 45
FPLLMULT = MUL_46	PLL Multiply by 46
FPLLMULT = MUL_47	PLL Multiply by 47
FPLLMULT = MUL_48	PLL Multiply by 48
FPLLMULT = MUL_49	PLL Multiply by 49
FPLLMULT = MUL_50	PLL Multiply by 50
FPLLMULT = MUL_51	PLL Multiply by 51
FPLLMULT = MUL_52	PLL Multiply by 52
FPLLMULT = MUL_53	PLL Multiply by 53
FPLLMULT = MUL_54	PLL Multiply by 54
FPLLMULT = MUL_55	PLL Multiply by 55
FPLLMULT = MUL_56	PLL Multiply by 56
FPLLMULT = MUL_57	PLL Multiply by 57
FPLLMULT = MUL_58	PLL Multiply by 58
FPLLMULT = MUL_59	PLL Multiply by 59
FPLLMULT = MUL_60	PLL Multiply by 60
FPLLMULT = MUL_61	PLL Multiply by 61
FPLLMULT = MUL_62	PLL Multiply by 62
FPLLMULT = MUL_63	PLL Multiply by 63
FPLLMULT = MUL_64	PLL Multiply by 64
FPLLMULT = MUL_65	PLL Multiply by 65
FPLLMULT = MUL_66	PLL Multiply by 66
FPLLMULT = MUL_67	PLL Multiply by 67
FPLLMULT = MUL_68	PLL Multiply by 68
FPLLMULT = MUL_69	PLL Multiply by 69
FPLLMULT = MUL_70	PLL Multiply by 70
FPLLMULT = MUL_71	PLL Multiply by 71
FPLLMULT = MUL_72	PLL Multiply by 72
FPLLMULT = MUL_73	PLL Multiply by 73
FPLLMULT = MUL_74	PLL Multiply by 74
FPLLMULT = MUL_75	PLL Multiply by 75
FPLLMULT = MUL_76	PLL Multiply by 76

FPLLMULT = MUL_77	PLL Multiply by 77
FPLLMULT = MUL_78	PLL Multiply by 78
FPLLMULT = MUL_79	PLL Multiply by 79
FPLLMULT = MUL_80	PLL Multiply by 80
FPLLMULT = MUL_81	PLL Multiply by 81
FPLLMULT = MUL_82	PLL Multiply by 82
FPLLMULT = MUL_83	PLL Multiply by 83
FPLLMULT = MUL_84	PLL Multiply by 84
FPLLMULT = MUL_85	PLL Multiply by 85
FPLLMULT = MUL_86	PLL Multiply by 86
FPLLMULT = MUL_87	PLL Multiply by 87
FPLLMULT = MUL_88	PLL Multiply by 88
FPLLMULT = MUL_89	PLL Multiply by 89
FPLLMULT = MUL_90	PLL Multiply by 90
FPLLMULT = MUL_91	PLL Multiply by 91
FPLLMULT = MUL_92	PLL Multiply by 92
FPLLMULT = MUL_93	PLL Multiply by 93
FPLLMULT = MUL_94	PLL Multiply by 94
FPLLMULT = MUL_95	PLL Multiply by 95
FPLLMULT = MUL_96	PLL Multiply by 96
FPLLMULT = MUL_97	PLL Multiply by 97
FPLLMULT = MUL_98	PLL Multiply by 98
FPLLMULT = MUL_99	PLL Multiply by 99
FPLLMULT = MUL_100	PLL Multiply by 100
FPLLMULT = MUL_101	PLL Multiply by 101
FPLLMULT = MUL_102	PLL Multiply by 102
FPLLMULT = MUL_103	PLL Multiply by 103
FPLLMULT = MUL_104	PLL Multiply by 104
FPLLMULT = MUL_105	PLL Multiply by 105
FPLLMULT = MUL_106	PLL Multiply by 106
FPLLMULT = MUL_107	PLL Multiply by 107
FPLLMULT = MUL_108	PLL Multiply by 108
FPLLMULT = MUL_109	PLL Multiply by 109
FPLLMULT = MUL_110	PLL Multiply by 110
FPLLMULT = MUL_111	PLL Multiply by 111
FPLLMULT = MUL_112	PLL Multiply by 112
FPLLMULT = MUL_113	PLL Multiply by 113
FPLLMULT = MUL_114	PLL Multiply by 114
FPLLMULT = MUL_115	PLL Multiply by 115
FPLLMULT = MUL_116	PLL Multiply by 116
FPLLMULT = MUL_117	PLL Multiply by 117
FPLLMULT = MUL_118	PLL Multiply by 118
FPLLMULT = MUL_119	PLL Multiply by 119
FPLLMULT = MUL_120	PLL Multiply by 120
FPLLMULT = MUL_121	PLL Multiply by 121
FPLLMULT = MUL_122	PLL Multiply by 122
FPLLMULT = MUL_123	PLL Multiply by 123
FPLLMULT = MUL_124	PLL Multiply by 124
FPLLMULT = MUL_125	PLL Multiply by 125
FPLLMULT = MUL_126	PLL Multiply by 126
FPLLMULT = MUL_127	PLL Multiply by 127
FPLLMULT = MUL_128	PLL Multiply by 128

FPLLODIV	System PLL Output Clock Divider
FPLLODIV = DIV_2	2x Divider
FPLLODIV = DIV_4	4x Divider
FPLLODIV = DIV_8	8x Divider
FPLLODIV = DIV_16	16x Divider

FPLLODIV = DIV_32	32x Divider

UPLLFSEL	USB PLL Input Frequency Selection
UPLLFSEL = FREQ_24MHZ	USB PLL input is 24 MHz
UPLLFSEL = FREQ_12MHZ	USB PLL input is 12 MHz

FNOSC	Oscillator Selection Bits
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)
FNOSC = SPLL	System PLL
FNOSC = POSC	Primary Osc (HS,EC)
FNOSC = SOSC	Low Power Secondary Osc (SOSC)
FNOSC = LPRC	Low Power RC Osc (LPRC)

DMTINTV	DMT Count Window Interval
DMTINTV = WIN_0	Window/Interval value is zero
DMTINTV = WIN_1_2	Window/Interval value is 1/2 counter value
DMTINTV = WIN_3_4	Window/Interval value is 3/4 counter value
DMTINTV = WIN_7_8	Window/Interval value is 7/8 counter value
DMTINTV = WIN_15_16	Window/Interval value is 15/16 counter value
DMTINTV = WIN_31_32	Window/Interval value is 31/32 counter value
DMTINTV = WIN_63_64	Window/Interval value is 63/64 counter value
DMTINTV = WIN_127_128	Window/Interval value is 127/128 counter value

FSOSCEN	Secondary Oscillator Enable
FSOSCEN = OFF	Disable SOSC
FSOSCEN = ON	Enable SOSC

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = HS	HS osc mode
POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled
OSCIOFNC = ON	Enabled

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSDCMD	Clock Switch Disabled, FSCM Disabled
FCKSM = CSECMD	Clock Switch Enabled, FSCM Disabled
FCKSM = CSDCME	Clock Switch Disabled, FSCM Enabled
FCKSM = CSECME	Clock Switch Enabled, FSCM Enabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1
WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64
WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512
WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192

WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WDTSPGM	Watchdog Timer Stop During Flash Programming
WDTSPGM = RUN	WDT runs during Flash programming
WDTSPGM = STOP	WDT stops during Flash programming

WINDIS	Watchdog Timer Window Mode
WINDIS = NORMAL	Watchdog Timer is in non-Window mode
WINDIS = WINDOW	Watchdog Timer is in Window mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_25	Window size is 25%
FWDTWINSZ = WINSZ_37	Window size is 37.5%
FWDTWINSZ = WINSZ_50	Window size is 50%
FWDTWINSZ = WINSZ_75	Window size is 75%

DMTCNT	Deadman Timer Count Selection
DMTCNT = DMT8	2^8 (256)
DMTCNT = DMT9	2^9 (512)
DMTCNT = DMT10	2^10 (1024)
DMTCNT = DMT11	2^11 (2048)
DMTCNT = DMT12	2^12 (4096)
DMTCNT = DMT13	2^13 (8192)
DMTCNT = DMT14	2^14 (16384)
DMTCNT = DMT15	2^15 (32768)
DMTCNT = DMT16	2^16 (65536)
DMTCNT = DMT17	2^17 (131072)
DMTCNT = DMT18	2^18 (262144)
DMTCNT = DMT19	2^19 (524288)
DMTCNT = DMT20	2^20 (1048576)
DMTCNT = DMT21	2^21 (2097152)
DMTCNT = DMT22	2^22 (4194304)
DMTCNT = DMT23	2^23 (8388608)
DMTCNT = DMT24	2^24 (16777216)
DMTCNT = DMT25	2^25 (33554432)
DMTCNT = DMT26	2^26 (67108864)
DMTCNT = DMT27	2^27 (134217728)
DMTCNT = DMT28	2^28 (268435456)
DMTCNT = DMT29	2^29 (536870912)
DMTCNT = DMT30	2^30 (1073741824)
DMTCNT = DMT31	2^31 (2147483648)

FDMTEN	Deadman Timer Enable
FDMTEN = ON	Deadman Timer is enabled
FDMTEN = OFF	Deadman Timer is disabled

DEBUG	Background Debugger Enable
DEBUG = ON	Debugger is enabled
DEBUG = OFF	Debugger is disabled

JTAGEN	JTAG Enable

JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

TRCEN	Trace Enable
TRCEN = ON	Trace features in the CPU are enabled
TRCEN = OFF	Trace features in the CPU are disabled

BOOTISA	Boot ISA Selection
BOOTISA = MIPS32	Boot code and Exception code is MIPS32
BOOTISA = MICROMIPS	Boot code and Exception code is microMIPS

FECCCON	Dynamic Flash ECC Configuration
FECCCON = ON	Flash ECC is enabled (ECCCON bits are locked)
FECCCON = DYNAMIC	Dynamic Flash ECC is enabled (ECCCON bits are locked)
FECCCON = OFF_LOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are locked)
FECCCON = OFF_UNLOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are writable)

FSLEEP	Flash Sleep Mode
FSLEEP = OFF	Flash is powered down when the device is in Sleep mode
FSLEEP = VREGS	Flash power down is controlled by the VREGS bit

DBGPER	Debug Mode CPU Access Permission
DBGPER = ALLOW_PG2	Allow CPU access to Permission Group 2 permission regions
DBGPER = ALLOW_PG1	Allow CPU access to Permission Group 1 permission regions
DBGPER = ALLOW_PG0	Allow CPU access to Permission Group 0 permission regions
DBGPER = PG_1_0	PG0: Allow PG1: Allow PG2: Deny
DBGPER = PG_2_0	PG0: Allow PG1: Deny PG2: Allow
DBGPER = PG_2_1	PG0: Deny PG1: Allow PG2: Allow
DBGPER = PG_ALL	Allow CPU access to all permission regions
DBGPER = PG_NONE	Deny CPU access to all permission regions

SMCLR	Soft Master Clear Enable bit
SMCLR = MCLR_NORM	MCLR pin generates a normal system Reset
SMCLR = MCLR_POR	MCLR pin generates an emulated POR Reset

SOSCGAIN	Secondary Oscillator Gain Control bits
SOSCGAIN = GAIN_2X	2x gain setting
SOSCGAIN = GAIN_1_5X	1.5x gain setting
SOSCGAIN = GAIN_0_5X	0.5x gain setting
SOSCGAIN = GAIN_1X	1x gain setting
SOSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
SOSCGAIN = GAIN_LEVEL_2	Gain level 2
SOSCGAIN = GAIN_LEVEL_1	Gain level 1
SOSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

SOSCBOOST	Secondary Oscillator Boost Kick Start Enable bit
SOSCBOOST = ON	Boost the kick start of the oscillator
SOSCBOOST = OFF	Normal start of the oscillator

POSCGAIN	Primary Oscillator Gain Control bits
POSCGAIN = GAIN_2X	2x gain setting
POSCGAIN = GAIN_1_5X	1.5x gain setting
POSCGAIN = GAIN_0_5X	0.5x gain setting
POSCGAIN = GAIN_1X	1x gain setting
POSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
POSCGAIN = GAIN_LEVEL_2	Gain level 2
POSCGAIN = GAIN_LEVEL_1	Gain level 1
POSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

POSCBOOST	Primary Oscillator Boost Kick Start Enable bit
POSCBOOST = ON	Boost the kick start of the oscillator
POSCBOOST = OFF	Normal start of the oscillator

EJTAGBEN	EJTAG Boot
EJTAGBEN = NORMAL	Normal EJTAG functionality
EJTAGBEN = REDUCED	Reduced EJTAG functionality

CP	Code Protect
CP = ON	Protection Enabled
CP = OFF	Protection Disabled

TSEQ	Boot Flash True Sequence Number
TSEQ = 00000000	Range is from 0 to 0xffff

CSEQ	Boot Flash Complement Sequence Number
CSEQ = 00000000	Range is from 0 to 0xffff

USERID	
USERID = 00000000	Range is from 0 to 0xffff

FMIIEN	Ethernet RMII/MII Enable
FMIIEN = OFF	RMII Enabled
FMIIEN = ON	MII Enabled

FETHIO	Ethernet I/O Pin Select
FETHIO = OFF	Alternate Ethernet I/O
FETHIO = ON	Default Ethernet I/O

PGL1WAY	Permission Group Lock One Way Configuration
PGL1WAY = ON	Allow only one reconfiguration
PGL1WAY = OFF	Allow multiple reconfigurations

PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration
PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USBID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FPLLIDIV	System PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
FPLLIDIV = DIV_2	2x Divider
FPLLIDIV = DIV_3	3x Divider
FPLLIDIV = DIV_4	4x Divider
FPLLIDIV = DIV_5	5x Divider
FPLLIDIV = DIV_6	6x Divider
FPLLIDIV = DIV_7	7x Divider
FPLLIDIV = DIV_8	8x Divider

FPLLRNG	System PLL Input Range
FPLLRNG = RANGE_BYPASS	Bypass
FPLLRNG = RANGE_5_10_MHZ	5-10 MHz Input
FPLLRNG = RANGE_8_16_MHZ	8-16 MHz Input
FPLLRNG = RANGE_13_26_MHZ	13-26 MHz Input
FPLLRNG = RANGE_21_42_MHZ	21-42 MHz Input
FPLLRNG = RANGE_34_68_MHZ	34-68 MHz Input

FPLLICLK	System PLL Input Clock Selection
FPLLICLK = PLL_FRC	FRC is input to the System PLL
FPLLICLK = PLL_POSC	POSC is input to the System PLL

FPLLMULT	System PLL Multiplier
FPLLMULT = MUL_1	PLL Multiply by 1
FPLLMULT = MUL_2	PLL Multiply by 2
FPLLMULT = MUL_3	PLL Multiply by 3
FPLLMULT = MUL_4	PLL Multiply by 4
FPLLMULT = MUL_5	PLL Multiply by 5
FPLLMULT = MUL_6	PLL Multiply by 6
FPLLMULT = MUL_7	PLL Multiply by 7
FPLLMULT = MUL_8	PLL Multiply by 8
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FPLLMULT = MUL_11	PLL Multiply by 11
FPLLMULT = MUL_12	PLL Multiply by 12
FPLLMULT = MUL_13	PLL Multiply by 13
FPLLMULT = MUL_14	PLL Multiply by 14
FPLLMULT = MUL_15	PLL Multiply by 15
FPLLMULT = MUL_16	PLL Multiply by 16
FPLLMULT = MUL_17	PLL Multiply by 17
FPLLMULT = MUL_18	PLL Multiply by 18
FPLLMULT = MUL_19	PLL Multiply by 19
FPLLMULT = MUL_20	PLL Multiply by 20
FPLLMULT = MUL_21	PLL Multiply by 21
FPLLMULT = MUL_22	PLL Multiply by 22
FPLLMULT = MUL_23	PLL Multiply by 23
FPLLMULT = MUL_24	PLL Multiply by 24
FPLLMULT = MUL_25	PLL Multiply by 25
FPLLMULT = MUL_26	PLL Multiply by 26
FPLLMULT = MUL_27	PLL Multiply by 27
FPLLMULT = MUL_28	PLL Multiply by 28
FPLLMULT = MUL_29	PLL Multiply by 29
FPLLMULT = MUL_30	PLL Multiply by 30
FPLLMULT = MUL_31	PLL Multiply by 31
FPLLMULT = MUL_32	PLL Multiply by 32
FPLLMULT = MUL_33	PLL Multiply by 33
FPLLMULT = MUL_34	PLL Multiply by 34
FPLLMULT = MUL_35	PLL Multiply by 35
FPLLMULT = MUL_36	PLL Multiply by 36
FPLLMULT = MUL_37	PLL Multiply by 37
FPLLMULT = MUL_38	PLL Multiply by 38
FPLLMULT = MUL_39	PLL Multiply by 39
FPLLMULT = MUL_40	PLL Multiply by 40
FPLLMULT = MUL_41	PLL Multiply by 41
FPLLMULT = MUL_42	PLL Multiply by 42
FPLLMULT = MUL_43	PLL Multiply by 43
FPLLMULT = MUL_44	PLL Multiply by 44
FPLLMULT = MUL_45	PLL Multiply by 45
FPLLMULT = MUL_46	PLL Multiply by 46
FPLLMULT = MUL_47	PLL Multiply by 47
FPLLMULT = MUL_48	PLL Multiply by 48
FPLLMULT = MUL_49	PLL Multiply by 49
FPLLMULT = MUL_50	PLL Multiply by 50
FPLLMULT = MUL_51	PLL Multiply by 51
FPLLMULT = MUL_52	PLL Multiply by 52
FPLLMULT = MUL_53	PLL Multiply by 53

FPLLMULT = MUL_54	PLL Multiply by 54
FPLLMULT = MUL_55	PLL Multiply by 55
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FPLLMULT = MUL_58	PLL Multiply by 58
FPLLMULT = MUL_59	PLL Multiply by 59
FPLLMULT = MUL_60	PLL Multiply by 60
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FPLLMULT = MUL_62	PLL Multiply by 62
FPLLMULT = MUL_63	PLL Multiply by 63
FPLLMULT = MUL_64	PLL Multiply by 64
FPLLMULT = MUL_65	PLL Multiply by 65
FPLLMULT = MUL_66	PLL Multiply by 66
FPLLMULT = MUL_67	PLL Multiply by 67
FPLLMULT = MUL_68	PLL Multiply by 68
FPLLMULT = MUL_69	PLL Multiply by 69
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FPLLMULT = MUL_74	PLL Multiply by 74
FPLLMULT = MUL_75	PLL Multiply by 75
FPLLMULT = MUL_76	PLL Multiply by 76
FPLLMULT = MUL_77	PLL Multiply by 77
FPLLMULT = MUL_78	PLL Multiply by 78
FPLLMULT = MUL_79	PLL Multiply by 79
FPLLMULT = MUL_80	PLL Multiply by 80
FPLLMULT = MUL_81	PLL Multiply by 81
FPLLMULT = MUL_82	PLL Multiply by 82
FPLLMULT = MUL_83	PLL Multiply by 83
FPLLMULT = MUL_84	PLL Multiply by 84
FPLLMULT = MUL_85	PLL Multiply by 85
FPLLMULT = MUL_86	PLL Multiply by 86
FPLLMULT = MUL_87	PLL Multiply by 87
FPLLMULT = MUL_88	PLL Multiply by 88
FPLLMULT = MUL_89	PLL Multiply by 89
FPLLMULT = MUL_90	PLL Multiply by 90
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FPLLMULT = MUL_92	PLL Multiply by 92
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FPLLMULT = MUL_97	PLL Multiply by 97
FPLLMULT = MUL_98	PLL Multiply by 98
FPLLMULT = MUL_99	PLL Multiply by 99
FPLLMULT = MUL_100	PLL Multiply by 100
FPLLMULT = MUL_101	PLL Multiply by 101
FPLLMULT = MUL_102	PLL Multiply by 102
FPLLMULT = MUL_103	PLL Multiply by 103
FPLLMULT = MUL_104	PLL Multiply by 104
FPLLMULT = MUL_105	PLL Multiply by 105
FPLLMULT = MUL_106	PLL Multiply by 106
FPLLMULT = MUL_107	PLL Multiply by 107
FPLLMULT = MUL_108	PLL Multiply by 108
FPLLMULT = MUL_109	PLL Multiply by 109
FPLLMULT = MUL_110	PLL Multiply by 110
FPLLMULT = MUL_111	PLL Multiply by 111

FPLLMULT = MUL_112	PLL Multiply by 112
FPLLMULT = MUL_113	PLL Multiply by 113
FPLLMULT = MUL_114	PLL Multiply by 114
FPLLMULT = MUL_115	PLL Multiply by 115
FPLLMULT = MUL_116	PLL Multiply by 116
FPLLMULT = MUL_117	PLL Multiply by 117
FPLLMULT = MUL_118	PLL Multiply by 118
FPLLMULT = MUL_119	PLL Multiply by 119
FPLLMULT = MUL_120	PLL Multiply by 120
FPLLMULT = MUL_121	PLL Multiply by 121
FPLLMULT = MUL_122	PLL Multiply by 122
FPLLMULT = MUL_123	PLL Multiply by 123
FPLLMULT = MUL_124	PLL Multiply by 124
FPLLMULT = MUL_125	PLL Multiply by 125
FPLLMULT = MUL_126	PLL Multiply by 126
FPLLMULT = MUL_127	PLL Multiply by 127
FPLLMULT = MUL_128	PLL Multiply by 128

FPLLODIV	System PLL Output Clock Divider
FPLLODIV = DIV_2	2x Divider
FPLLODIV = DIV_4	4x Divider
FPLLODIV = DIV_8	8x Divider
FPLLODIV = DIV_16	16x Divider
FPLLODIV = DIV_32	32x Divider

UPLLFSEL	USB PLL Input Frequency Selection
UPLLFSEL = FREQ_24MHZ	USB PLL input is 24 MHz
UPLLFSEL = FREQ_12MHZ	USB PLL input is 12 MHz

FNOSC	Oscillator Selection Bits
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)
FNOSC = SPLL	System PLL
FNOSC = POSC	Primary Osc (HS,EC)
FNOSC = SOSC	Low Power Secondary Osc (SOSC)
FNOSC = LPRC	Low Power RC Osc (LPRC)

DMTINTV	DMT Count Window Interval
DMTINTV = WIN_0	Window/Interval value is zero
DMTINTV = WIN_1_2	Window/Interval value is 1/2 counter value
DMTINTV = WIN_3_4	Window/Interval value is 3/4 counter value
DMTINTV = WIN_7_8	Window/Interval value is 7/8 counter value
DMTINTV = WIN_15_16	Window/Interval value is 15/16 counter value
DMTINTV = WIN_31_32	Window/Interval value is 31/32 counter value
DMTINTV = WIN_63_64	Window/Interval value is 63/64 counter value
DMTINTV = WIN_127_128	Window/Interval value is 127/128 counter value

FSOSCEN	Secondary Oscillator Enable
FSOSCEN = OFF	Disable SOSC
FSOSCEN = ON	Enable SOSC

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = HS	HS osc mode
POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled

OSCIOFNC = ON	Enabled

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSDCMD	Clock Switch Disabled, FSCM Disabled
FCKSM = CSECMD	Clock Switch Enabled, FSCM Disabled
FCKSM = CSDCME	Clock Switch Disabled, FSCM Enabled
FCKSM = CSECME	Clock Switch Enabled, FSCM Enabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1
WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64
WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512
WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192
WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WDTSPGM	Watchdog Timer Stop During Flash Programming
WDTSPGM = RUN	WDT runs during Flash programming
WDTSPGM = STOP	WDT stops during Flash programming

WINDIS	Watchdog Timer Window Mode
WINDIS = NORMAL	Watchdog Timer is in non-Window mode
WINDIS = WINDOW	Watchdog Timer is in Window mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_25	Window size is 25%
FWDTWINSZ = WINSZ_37	Window size is 37.5%
FWDTWINSZ = WINSZ_50	Window size is 50%
FWDTWINSZ = WINSZ_75	Window size is 75%

DMTCNT	Deadman Timer Count Selection
DMTCNT = DMT8	2^8 (256)
DMTCNT = DMT9	2^9 (512)
DMTCNT = DMT10	2^10 (1024)
DMTCNT = DMT11	2^11 (2048)
DMTCNT = DMT12	2^12 (4096)
DMTCNT = DMT13	2^13 (8192)
DMTCNT = DMT14	2^14 (16384)
DMTCNT = DMT15	2^15 (32768)
DMTCNT = DMT16	2^16 (65536)
DMTCNT = DMT17	2^17 (131072)
DMTCNT = DMT18	2^18 (262144)

DMTCNT = DMT19	2^19 (524288)
DMTCNT = DMT20	2^20 (1048576)
DMTCNT = DMT21	2^21 (2097152)
DMTCNT = DMT22	2^22 (4194304)
DMTCNT = DMT23	2^23 (8388608)
DMTCNT = DMT24	2^24 (16777216)
DMTCNT = DMT25	2^25 (33554432)
DMTCNT = DMT26	2^26 (67108864)
DMTCNT = DMT27	2^27 (134217728)
DMTCNT = DMT28	2^28 (268435456)
DMTCNT = DMT29	2^29 (536870912)
DMTCNT = DMT30	2^30 (1073741824)
DMTCNT = DMT31	2^31 (2147483648)

FDMTEN	Deadman Timer Enable
FDMTEN = ON	Deadman Timer is enabled
FDMTEN = OFF	Deadman Timer is disabled

DEBUG	Background Debugger Enable
DEBUG = ON	Debugger is enabled
DEBUG = OFF	Debugger is disabled

JTAGEN	JTAG Enable
JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

TRCEN	Trace Enable
TRCEN = ON	Trace features in the CPU are enabled
TRCEN = OFF	Trace features in the CPU are disabled

BOOTISA	Boot ISA Selection
BOOTISA = MIPS32	Boot code and Exception code is MIPS32
BOOTISA = MICROMIPS	Boot code and Exception code is microMIPS

FECCCON	Dynamic Flash ECC Configuration
FECCCON = ON	Flash ECC is enabled (ECCCON bits are locked)
FECCCON = DYNAMIC	Dynamic Flash ECC is enabled (ECCCON bits are locked)
FECCCON = OFF_LOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are locked)
FECCCON = OFF_UNLOCKED	ECC and Dynamic ECC are disabled (ECCCON bits are writable)

FSLEEP	Flash Sleep Mode
FSLEEP = OFF	Flash is powered down when the device is in Sleep mode
FSLEEP = VREGS	Flash power down is controlled by the VREGS bit

DBGPER	Debug Mode CPU Access Permission
DBGPER = ALLOW_PG2	Allow CPU access to Permission Group 2 permission regions
DBGPER = ALLOW_PG1	Allow CPU access to Permission Group 1 permission regions
DBGPER = ALLOW_PG0	Allow CPU access to Permission Group 0 permission regions
DBGPER = PG_1_0	PG0: Allow PG1: Allow PG2: Deny
DBGPER = PG_2_0	PG0: Allow PG1: Deny PG2: Allow
DBGPER = PG_2_1	PG0: Deny PG1: Allow PG2: Allow
DBGPER = PG_ALL	Allow CPU access to all permission regions
DBGPER = PG_NONE	Deny CPU access to all permission regions

SMCLR	Soft Master Clear Enable bit
SMCLR = MCLR_NORM	MCLR pin generates a normal system Reset
SMCLR = MCLR_POR	MCLR pin generates an emulated POR Reset

SOSCGAIN	Secondary Oscillator Gain Control bits
SOSCGAIN = GAIN_2X	2x gain setting
SOSCGAIN = GAIN_1_5X	1.5x gain setting
SOSCGAIN = GAIN_0_5X	0.5x gain setting
SOSCGAIN = GAIN_1X	1x gain setting
SOSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
SOSCGAIN = GAIN_LEVEL_2	Gain level 2
SOSCGAIN = GAIN_LEVEL_1	Gain level 1
SOSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

SOSCBOOST	Secondary Oscillator Boost Kick Start Enable bit
SOSCBOOST = ON	Boost the kick start of the oscillator
SOSCBOOST = OFF	Normal start of the oscillator

POSCGAIN	Primary Oscillator Gain Control bits
POSCGAIN = GAIN_2X	2x gain setting
POSCGAIN = GAIN_1_5X	1.5x gain setting
POSCGAIN = GAIN_0_5X	0.5x gain setting
POSCGAIN = GAIN_1X	1x gain setting
POSCGAIN = GAIN_LEVEL_3	Gain level 3 (Highest)
POSCGAIN = GAIN_LEVEL_2	Gain level 2
POSCGAIN = GAIN_LEVEL_1	Gain level 1
POSCGAIN = GAIN_LEVEL_0	Gain level 0 (Lowest)

POSCBOOST	Primary Oscillator Boost Kick Start Enable bit
POSCBOOST = ON	Boost the kick start of the oscillator
POSCBOOST = OFF	Normal start of the oscillator

EJTAGBEN	EJTAG Boot
EJTAGBEN = NORMAL	Normal EJTAG functionality
EJTAGBEN = REDUCED	Reduced EJTAG functionality

CP	Code Protect
CP = ON	Protection Enabled
CP = OFF	Protection Disabled

TSEQ	Boot Flash True Sequence Number
TSEQ = 00000000	Range is from 0 to 0xffff

CSEQ	Boot Flash Complement Sequence Number
CSEQ = 00000000	Range is from 0 to 0xffff

[Documentation Index | Device index]