JEDEC STANDARD

Embedded MultiMediaCard (eMMC) Product Standard, High Capacity

JESD84-A42

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Embedded MultiMediaCard (eMMC) Product Standard, High Capacity

CONTENTS

Page

Foreword vii

Introduction vii

1 Scope. 1

2 Normative reference 1

3 Terms and definitions 1

4 eMMC Product Features 2
4.1 MMC-specific features 2

5 MMC Architecture 2

6 General description 3

7 Flash-memory-independent technology 4

8 Defect and error management 5

9 Operation modes 5

10 Device signals 5

11 Physical description 7

12 Electrical interface 9
12.1 Power-up. 9
12.1.1 Power-up guidelines 10

Embedded MultiMediaCard (eMMC) Product Standard, High Capacity

CONTENTS*(continued)*

Page

12.2 Power cycling 11

13 Bus operating conditions 11
13.1 Power supply voltage 12
13.2 Bus signal line load. 12
13.3 Bus signal levels 12
13.3.1 Push-pull bus signal level 13
13.3.2 Bus timing 13

14 Package Information 15

Embedded MultiMediaCard (eMMC) Product Standard, High Capacity

FIGURES

Page

Figure 1 — MMC architecture 3
Figure 2 — Functional block diagram 4
Figure 3 — Ball assignment for AA and AB devices (see MO-276 drawings for details) 6
Figure 4 — Ball assignment for BA devices (see MO-276 drawings for details) 7
Figure 5 — Power-up diagram 10
Figure 6 — eMMC power cycle 11
Figure 7 — Bus signal levels 12
Figure 8 — Bus and device interface timing 13

Embedded MultiMediaCard (eMMC) Product Standard, High Capacity

TABLES

Page

Table 1 — Communication signals 5
Table 2 — Ball assignments 8
Table 3 — Bus operating parameters/conditions 11
Table 4 — JEDEC eMMC power supply voltage 12
Table 5 — Open-drain mode bus signal level 13
Table 6 — Push-pull bus signal level 13
Table 7 — Interface timing (high-speed interface) 13
Table 8 — Interface timing (standard interface) 14

Foreword

This top-level specification provides detailed information for aspects of the eMMC that differ from the standard JEDEC/MMC Electrical Specification. For eMMC applications, the content of this product specification supersedes content of the lower-level JESD84-B42 electrical specification to which it refers.

Introduction

In embedded applications, eMMC devices will be soldered directly on the PCB. The lower-level specification includes information unique to card form factors, making this top-level document essential for embedded application designers.

This specification covers a broad range of possible system configurations and voltage ranges. Be sure to contact your silicon provider for implementation details prior to initiating design work.

Embedded MultiMediaCard (eMMC) Product Standard, High Capacity

1 Scope

This document provides a definition of the Embedded MultiMediaCard product, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

This document references the MMC electrical specification JESD84-B42.

3 Terms and definitions

For the purposes of this publication, the following abbreviations for common terms apply:

Block a number of bytes, basic data transfer unit

Broadcast a command sent to all cards on the MultiMediaCard bus[1]

CID Card IDentification number register

CLK clock signal

CMD command line or MultiMediaCard bus command (if extended CMDXX)

CRC Cyclic Redundancy Check

CSD Card Specific Data register

DAT data line

DSR Driver Stage Register

Flash a type of multiple time programmable non volatile memory

Group a number of write blocks, composite erase and write protect unit

LOW, HIGH binary interface states with defined assignment to a voltage level

NSAC defines the worst case for the clock rate dependent factor of the data access time

MSB, LSB the Most Significant Bit or Least Significant Bit

OCR Operation Conditions Register

open-drain a logical interface operation mode. An external resistor or current source is used to pull the interface level to HIGH, the internal transistor pushes it to LOW

payload net data

1. Broadcast occurs only in MultiMediaCard systems supporting versions prior to 4.0. In version 4.0 and later only one card can be present on the bus.

push-pull	a logical interface operation mode, a complementary pair of transistors is used to push the interface level to HIGH or LOW
RCA	Relative Card Address register
ROM	Read Only Memory
stuff bit	filling 0 bits to ensure fixed length frames for commands and responses
SPI	Serial Peripheral Interface
TAAC	defines the time dependent factor of the data access time
three-state driver	a driver stage which has three output driver states: HIGH, LOW and high impedance (which means that the interface does not have any influence on the interface level)
token	code word representing a command
V_{DD}	+ power supply
V_{SS}	power supply ground

4 eMMC Product Features

Embedded MultiMediaCard product features include:

- **MMC interface**
- **Space-saving multiple-chip package**
- **Memory controller and Flash**
- **Temperature range: –25C° to +85C°**
- **Offered in three LFBGA packages (see MO-276A for details):**
- **AA: 12mm x 16mm x 1.4mm**
- **AB: 12mm x 18mm x 1.4mm**
- **BA: 11.5mm x 13mm x 1.3mm**
- **System voltage**
- **Vcc: 1.7–1.95V or 2.7–3.6V**
- **VccQ: 1.7–1.95V or 2.7–3.6V**

4.1 MMC-specific features

- **JEDEC Electrical Specification, version 4.2**

5 MMC Architecture

Standard MMC architecture is depicted in Figure 1 on page 3.

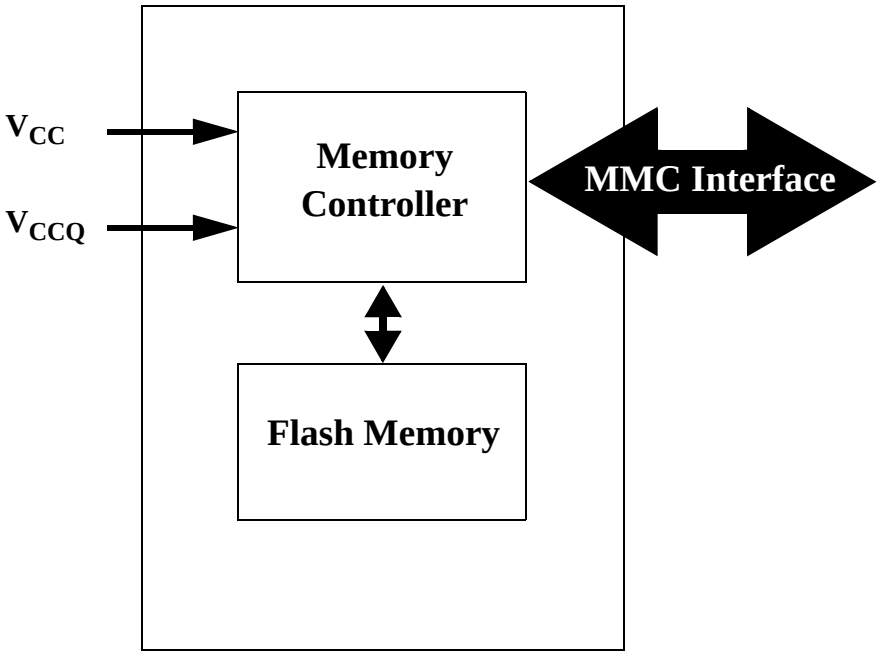

Figure 1 — MMC architecture

6 General description

JEDEC eMMC is a mass data storage device that utilizes a MultiMediaCard (MMC) interface, as shown in Figure 2 on page 4. It features low cost, small size, Flash-technology independence, and high data throughput. These features make JEDEC eMMC ideal for smart phones, digital cameras, PDAs, MP3 players, and countless other portable applications.

The nonvolatile JEDEC eMMC draws no power to maintain stored data, delivers high performance across a wide range of operating temperatures, and resists shock and vibration disruption.

A JEDEC eMMC device includes a Flash memory component and a controller on an advanced 10-signal bus.

Flash-technology independence is supported by compliance with this specification. The specification defines the communication protocol for MMC mode. This ensures ongoing compatibility between evolving Flash memory components and existing microcontrollers.

The eMMC functional block diagram is shown in Figure 2 on page 4.

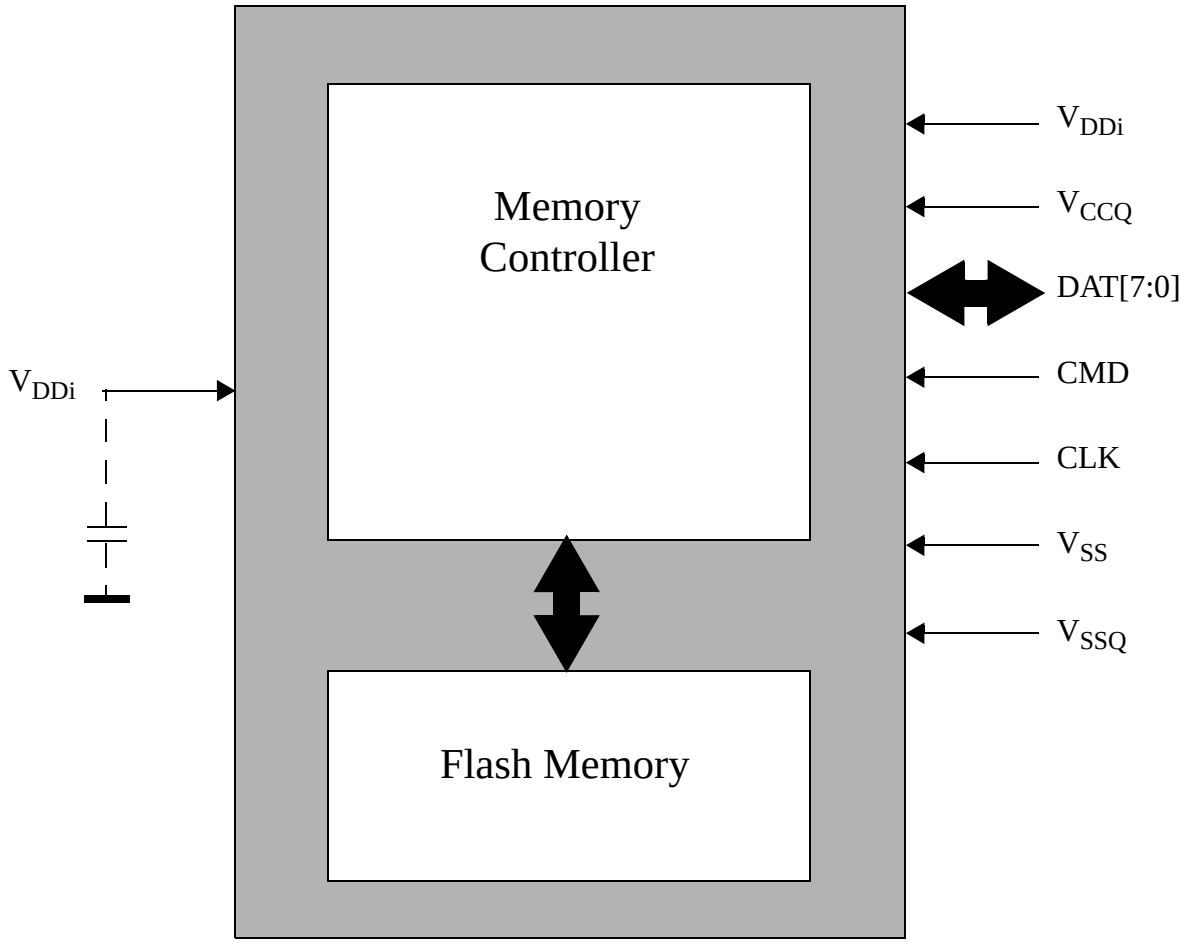

Figure 2 — Functional block diagram

7 Flash-memory-independent technology

The MMC specification defines the communication protocol between a host and a device. The protocol is independent of the Flash memory features included in the device. The JEDEC eMMC has an intelligent on-board controller that manages the MMC communication protocol.

The controller also handles block-management functions such as logical-block allocation and wear leveling. These management functions require complex algorithms and depend entirely on the Flash memory technology (generation or memory cell type).

JEDEC eMMC handles these management functions internally, making them invisible to the host processor.

8 Defect and error management

JEDEC eMMC incorporates advanced technology for defect and error management. If a defective block is identified, JEDEC eMMC completely replaces the defective block with one of the spare blocks. This process is invisible to the host and generally does not affect data space allocated for the user.

JEDEC eMMC also includes a built-in error correction code (ECC) algorithm to ensure that data integrity is maintained.

9 Operation modes

JEDEC eMMC supports MMC mode as well as SPI mode. The details are described in the following section.

10 Device signals

JEDEC eMMC devices transfer data via a configurable number of data-bus signals. The communication signals are shown in Table 1.

Table 1 — Communication signals

Signal	Symbol	Description
Clock	CLK	Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency.
Command	CMD	This signal is a bidirectional command channel used for device initialization and command transfers. The CMD signal has two operating modes: open-drain for initialization, and push-pull for command transfer. Commands are sent from the MultiMediaCard bus master to the device, and responses are sent from the device to the host.
Data	DAT[7:0]	These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-up or RESET, only DAT0 is used for data transfer. The memory controller can configure a wider data bus for data transfer using either DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). JEDEC eMMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT1 and DAT2 lines. (The DAT3 line internal pull-up is left connected.) Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT1, DAT2, and DAT[7:4] lines.

Device initialization uses only the CMD channel and is, therefore, compatible with all devices.

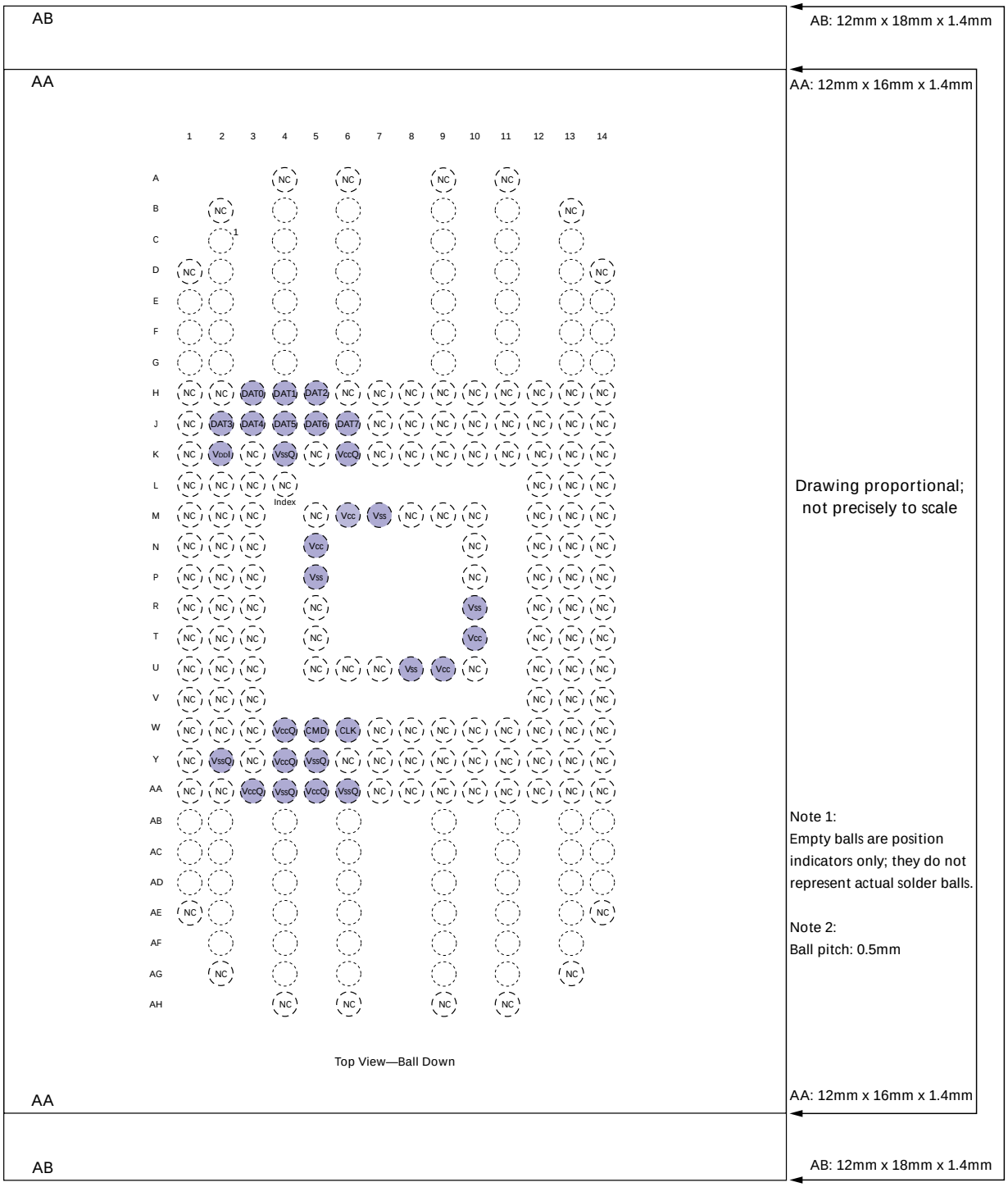

Figure 3 — Ball assignment for AA and AB devices (see MO-276 drawings for details)

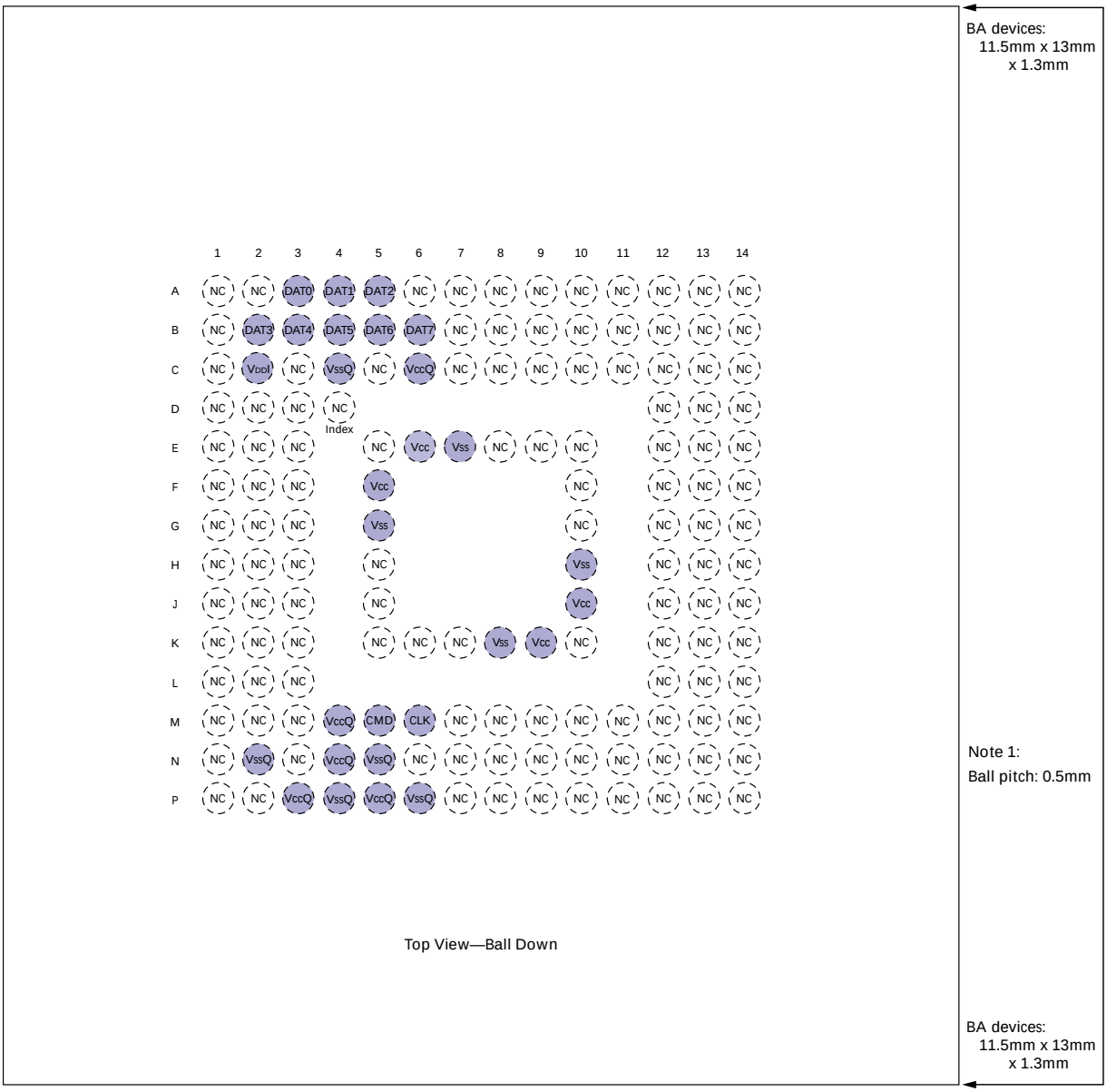

Figure 4 — Ball assignment for BA devices (see MO-276 drawings for details)

11 Physical description

JEDEC eMMC has 10 signals. The host is connected to the device using a dedicated 10-ball connector. Ball assignments are shown in Table 2 on page 8. Note that Table 2 continues on the next two pages.

Table 2 — Ball assignments

169-Ball Devices	153-Ball Devices	Symbol	Type	Ball Function
AA and AB Devices	BA Devices			
W6	M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
W5	M5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
H3	A3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
H4	A4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
H5	A5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
J2	B2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
J3	B3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
J4	B4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
J5	B5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
J6	B6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
M6, N5, T10, U9	E6, F5, J10, K9	V_{CC}	Supply	V_{CC}: Flash I/O and memory power supply
K6, W4, Y4, AA3, AA5	C6, M4, N4, P3, P5	$V_{CC}Q$	Supply	$V_{CC}Q$: Memory controller core and MMC I/F I/O power supply.
M7, P5, R10, U8	E7, G5, H10, K8	V_{SS}	Supply	V_{SS}: Flash I/O and memory ground connection.
K4, Y2, Y5, AA4, AA6	C4, N2, N5, P4, P6	$V_{SS}Q$	Supply	$V_{SS}Q$: Memory controller core and MMC I/F ground connection.
K2	C2	$V_{DD}i$		$V_{DD}i$: Connect 0.1µF capacitor from $V_{DD}i$ to ground.

Table 2 — Ball assignments (continued)

169-Ball Devices	153-Ball Devices	Symbol	Type	Ball Function
Miscellaneous				
A4, A6, A9, A11, B2, B13, D1, D14, H1, H2, H6, H7, H8, H9, H10, H11, H12, H13, H14, J1, J7, J8, J9, J10, J11, J12, J13, J14, K1, K3, K5, K7, K8, K9, K10, K11, K12, K13, K14, L1, L2, L3, L12, L13, L14, M1, M2, M3, M5, M8, M9, M10, M12, M13, M14, N1, N2, N3, N10, N12, N13, N14, P1, P2, P3, P10, P12, P13, P14, R1, R2, R3, R5, R12, R13, R14, T1, T2, T3, T5, T12, T13, T14, U1, U2, U3, U5, U6, U7, U10, U12, U13, U14, V1, V2, V3, V12, V13, V14, W1, W2, W3, W7, W8, W9, W10, W11, W12, W13, W14, Y1, Y3, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, AA1, AA2, AA7, AA8, AA9, AA10, AA11, AA12, AA13, AA14, AE1, AE14, AG2, AG13, AH4, AH6, AH9, AH11	A1, A2, A6, A7, A8, A9, A10, A11, A12, A13, A14, B1, B7, B8, B9, B10, B11, B12, B13, B14, C1, C3, C5, C7, C8, C9, C10, C11, C12, C13, C14, D1, D2, D3, D12, D13, D14, E1, E2, E3, E5, E8, E9, E10, E12, E13, E14, F1, F2, F3, F10, F12, F13, F14, G1, G2, G3, G10, G12, G13, G14, H1, H2, H3, H5, H12, H13, H14, J1, J2, J3, J5, J12, J13, J14, K1, K2, K3, K5, K6, K7, K10, K12, K13, K14, L1, L2, L3, L12, L13, L14, M1, M2, M3, M7, M8, M9, M10, M11, M12, M13, M14, N1, N3, N6, N7, N8, N9, N10, N11, N12, N13, N14, P1, P2, P7, P8, P9, P10, P11, P12, P13, P14	NC	–	No connect: Can be connected to ground or left floating.

12 Electrical interface

The following sections provide detailed information regarding the electrical interface.

12.1 Power-up

MMC bus power-up is handled locally in each device and in the bus master. Figure 5 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence.

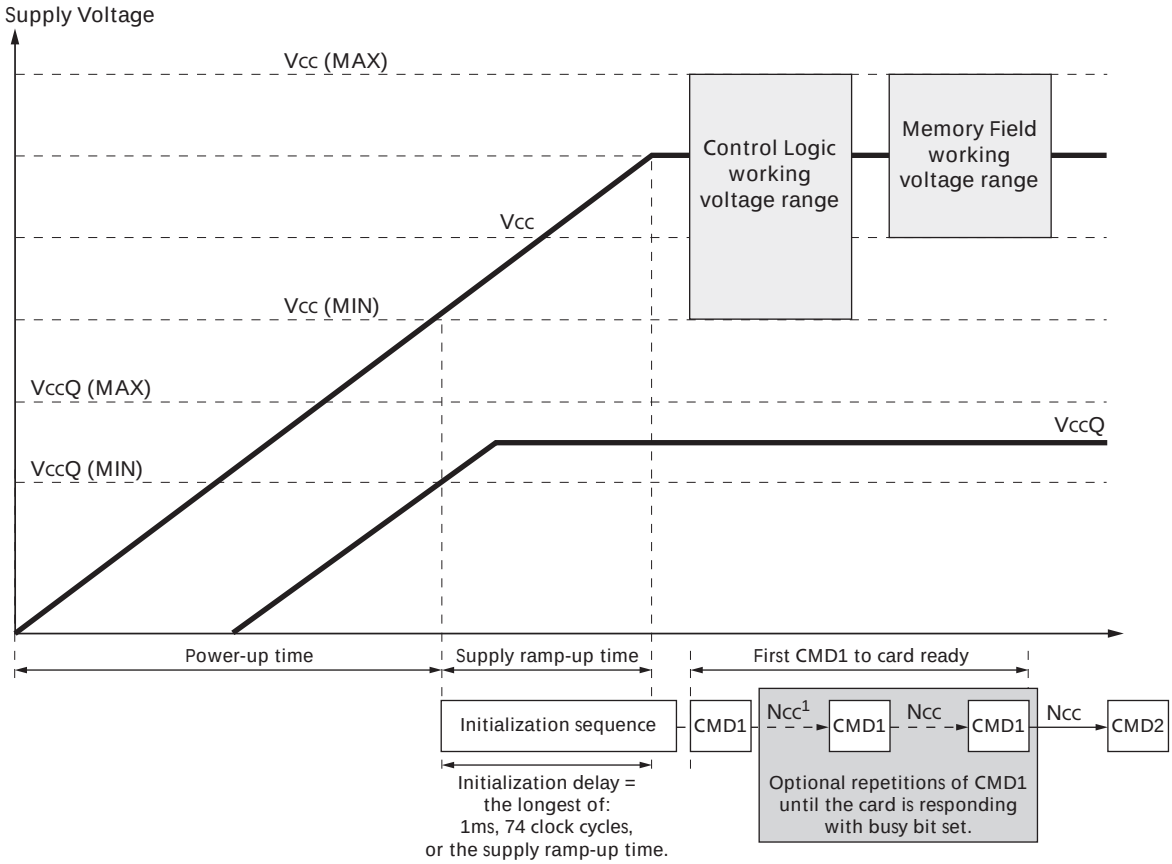

Figure 5 — Power-up diagram

12.1.1 Power-up guidelines

Power-up must adhere to the following guidelines:

- When power-up is initiated, VCC ramp-up must occur before or simultaneously with VCCQ going high.
- After power-up, the device enters the idle state. During this state the device ignores all bus transactions until CMD1 is received.
- After power-up, the maximum initial load the JEDEC eMMC can present on the VDD line is 10µF, in parallel with a minimum of 330Ω. During operation, device capacitanceon the VDD line must not exceed 10µF.
- CMD1 is a special synchronization command used to negotiate the operation voltage range and to poll the device until it is out of its power-up sequence. Besides the operation voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready; the host must wait until this bit is cleared. The device must complete its initialization within 1 second from the first CMD1 with a valid OCR range.
- The bus master moves the device out of idle state. Because the power-up time and the supply ramp-up time depend on application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.

- After power-up, the host starts the clock and sends the initializing sequence on the CMD line. This sequence is a contiguous stream of logical “1s”. The sequence length is the longest of: 1ms, 74 clocks, or the supply ramp-up time. An additional 10 clocks are provided to eliminate power-up synchronization problems (beyond the 64 clocks of the power-up sequence).
- Every bus master must implement CMD1.

12.2 Power cycling

VCC must be ramped up before or simultaneously with VCCQ going high when power is supplied. The host must not issue any commands until VCCQ and VCC are stable within each operating voltage range. At power-down, VCCQ must go LOW before or simultaneously with VCC going low.

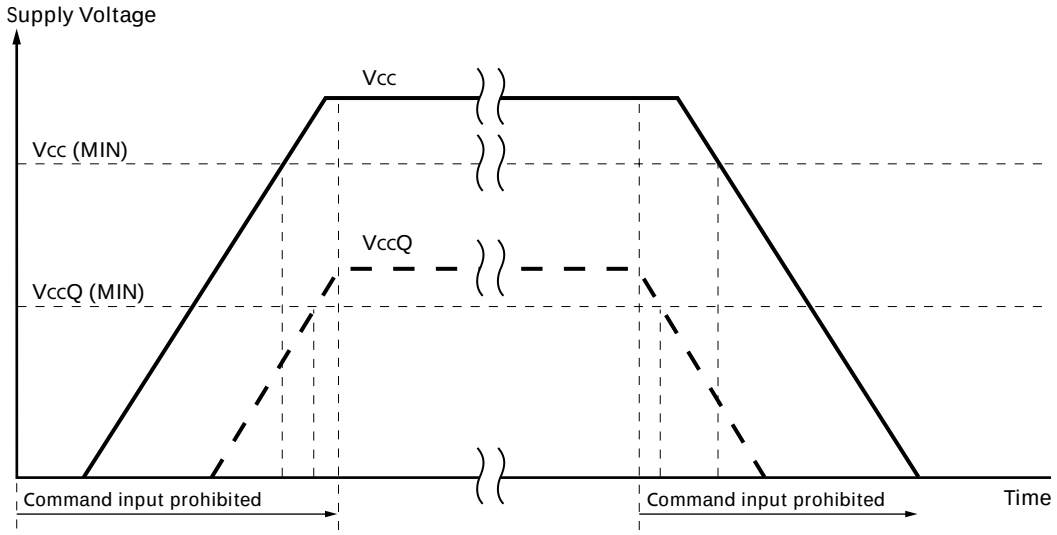

Figure 6 — eMMC power cycle

13 Bus operating conditions

The eMMC bus operating conditions are provided in Table 3.

Table 3 — Bus operating parameters/conditions

Parameters/Conditions	Min	Max	Unit	Notes
Peak voltage on all lines	-0.5	1.95	V	
Input leakage current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA	Except DAT3 pin[1]
Input leakage current (after changing the bus width and disconnecting the internal pull-up resistors)	-10	10	µA	
Output leakage current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA	

Table 3 — Bus operating parameters/conditions (continued)

Parameters/Conditions	Min	Max	Unit	Notes
Output leakage current (after changing the bus width and disconnecting the internal pull-up resistors)			µA	

NOTE 1 To ensure entering the MMC mode, DAT3 signal has an internal pull-up resistor. For DAT3 signal, the specification for input/output leakage current = –100µA (min) to +100µA (max).

13.1 Power supply voltage

The device current consumption for various device configurations is defined in the power class fields of the EXT_CSD register.During power-up, the current consumption of any device must not exceed 10mA before the host sends a valid OCR range.

Table 4 — JEDEC eMMC power supply voltage

Parameters	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage (I/O and core)	$V_{CC}Q$	1.70	–	1.95	V	
		2.70	–	3.6		
Supply voltage (Flash memory)	V_{CC}	1.70	–	1.95	V	
		2.70	–	3.6		
Supply voltage differentials (V_{SS}–$V_{SS}Q$)	V_{SS}–$V_{SS}Q$	–0.5		0.5	V	

13.2 Bus signal line load

The total load capacitance (C_L) of each line of the MMC bus is the sum of the bus master capacitance (C_{HOST}), plus the bus capacitance (C_{BUS}), and the capacitance (C_{DEVICE}) of the device connected to this line, so: $C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$.The sum of the host and bus capacitances must not exceed 30pF.

13.3 Bus signal levels

The bus can be supplied with a variable supply voltage; all signal levels relate to the supply voltage.

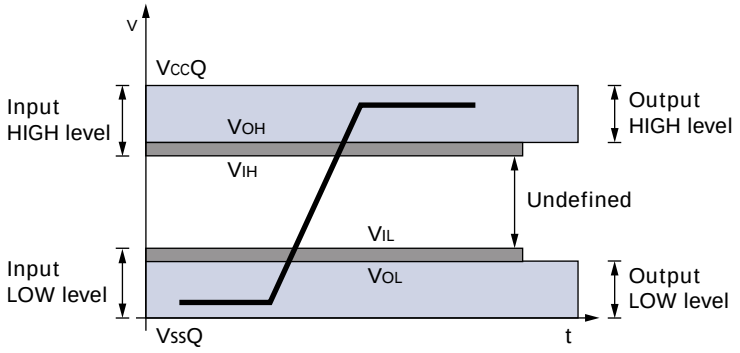

Figure 7 — Bus signal levels

Table 5 — Open-drain mode bus signal level

Parameter	Symbol	Min	Max	Unit	Conditions
Output high voltage	VOH	V_{CCQ} - 0.2		V	I_{OH} = –100 µA
Output low voltage	VOL		0.3	V	I_{OL} = 2 mA

The input levels are identical with the push-pull mode bus signal lines.

13.3.1 Push-pull bus signal level

The I/O signal level definitions for the JEDEC eMMC change as a function of V_{CCQ}, as shown in Table 6.

Table 6 — Push-pull bus signal level

Parameter	Symbol	Min	Max	Unit	Conditions
Output high voltage	V_{OH}	V_{CCQ} - 0.2		V	I_{OH} = –100µA at V_{DD} (MIN)
Output low voltage	V_{OL}		0.2	V	I_{OL} = –100µA at V_{DD} (MIN)
Input high voltage	V_{IH}	0.7 × V_{CCQ}	V_{CCQ} + 0.3	V	
Input low voltage	V_{IL}	V_{SSQ} - 0.3	0.3 × V_{CCQ}	V	

13.3.2 Bus timing

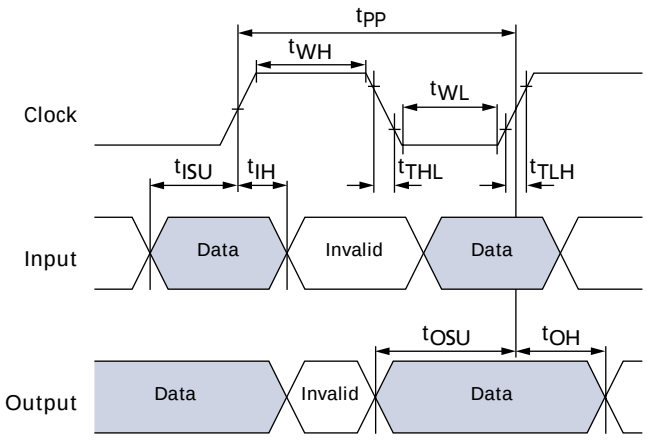

Figure 8 — Bus and device interface timing

Table 7 — Interface timing (high-speed interface)

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
Clock	**CLK**					1
Clock frequency data transfer mode (PP)[2]	F_{PP}	0	26/52	MHz	CL ≤ 30pF tolerance: +100 KHz	2
Clock frequency identification mode (OD)	F_{OD}	0	400	KHz	Tolerance: 20 KHz	
Clock low time	^{t}WL	6.5		ns	CL ≤ 30pF tolerance	
Clock rise time	^{t}TLH		3	ns	CL ≤ 30pF tolerance	3
Clock fall time	^{t}THL		3	ns	CL ≤ 30pF tolerance	

Table 7 — Interface timing (high-speed interface (continued))

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
Inputs: CMD, DAT (in reference to CLK)						
Input set-up time	^{t}ISU	3		ns	CL ≤ 30pF tolerance	
Input hold time	^{t}IH	3		ns	CL ≤ 30pF tolerance	
Outputs: CMD, DAT (in reference to CLK)						
Output set-up time	^{t}OSU	5		ns	CL ≤ 30pF tolerance	
Output hold time	^{t}OH	5		ns	CL ≤ 30pF tolerance	
Signal rise time	^{t}RISE		3	ns	CL ≤ 30pF tolerance	3
Signal fall time	^{t}FALL		3	ns	CL ≤ 30pF tolerance	

NOTE 1 All timing values are measured relative to 50 percent of voltage level.
NOTE 2 .JEDEC eMMC devices will support the full frequency range, from 0 through 52 MHZ.
NOTE 3 Rise and fall times are measured from 10 percent through 90 percent of voltage level.

Table 8 — Interface timing (standard interface)

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
Clock	**CLK**					1
Clock frequency data transfer mode (PP)[2]	F_{PP}	0	20	MHz	CL ≤ 30pF tolerance: +100 KHz	
Clock frequency identification mode (OD)	F_{OD}	0	400	KHz	Tolerance: 20 KHz	
Clock LOW time	^{t}WL	10		ns	CL ≤ 30pF tolerance	
Clock rise time	^{t}TLH		10	ns	CL ≤ 30pF tolerance	2
Clock fall time	^{t}THL		10	ns	CL ≤ 30pF tolerance	
Inputs: CMD, DAT (in reference to CLK)						
Input set-up time	^{t}ISU	3		ns	CL ≤ 30pF tolerance	
Input hold time	^{t}IH	3		ns	CL ≤ 30pF tolerance	
Outputs: CMD, DAT (in reference to CLK)						
Output set-up time	^{t}OSU	13.1		ns	CL ≤ 30pF tolerance	
Output hold time	^{t}OH	9.7		ns	CL ≤ 30pF tolerance	

NOTE 1 All timing values are measured relative to 50 percent of voltage level.
NOTE 2 Clock rise and fall times are measured from VIL (MAX) to VIH (MIN) of voltage level.

14 Package Information

For package dimensions and other detailed information, refer to the September 2006 MO-276 specification.

Standard Improvement Form JEDEC JCESD84-A42

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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