Timers

Why do we need timers?

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- PWM
- For Delays
- Keeping track of something

Timers in Atmega328p

- Timer0 - 8 bit
- Timer1 - 16 bit
- Timer2 - 8 bit

- What's the minimum and maximum time each can count ……???

  8-bit → 0 - 2^8

  16bit → 0 - 2^16

Few Definitions and Terminologies

- Bottom: The counter reaches the BOTTOM when it becomes 0x0000
- Max: The counter reaches its MAXimum when it becomes 0xFFFF (decimal 65535) for 16 bit
- Top: Value assigned by us

- OCRxn: register in which we assign values
- TCNTx: counter
- OCxn: PWM pins on Arduino
- Pre-scalar: divides the clock to provide a much lower frequency

Modes of Operation

1. Normal Mode
2. Clear Timer on Compare Match (CTC) Mode
3. Fast PWM Mode
4. Phase Correct PWM Mode

Normal Mode

- In this counter direction is always incrementing
- No counter clear is performed even after compare match
- Interrupt flag is set, hence interrupt can be generated

So will it run to infinity ….??

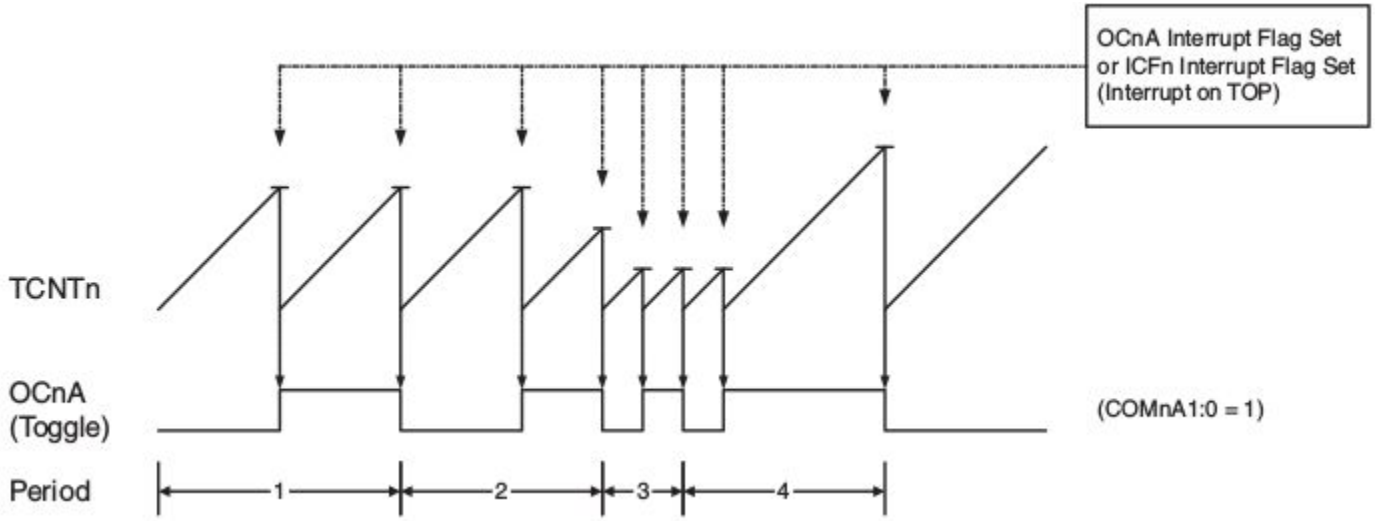
It overflows and starts from bottom again

How ….??

1110 + 1 → 1111 + 1→ 0000|1 + 1 → 0001|1 ….. and so on ….

Clear Timer on Compare Match (CTC) Mode

In CTC mode the counter is cleared to zero when the counter value (TCNT1) matches user defined value (either in OCR1A or ICR1)



And if we toggle OCnA at every compare match we can generate a waveform

Frequency in CTC mode

$$f_{OCnA} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot (1 + OCRnA)}$$

N is the pre-scalar

WHY …???

OCR1A → OCR1A → OCR1A

0 → 1 → 0

(1+OCR1A) + (1+OCR1A) = 2*(1+OCR1A)

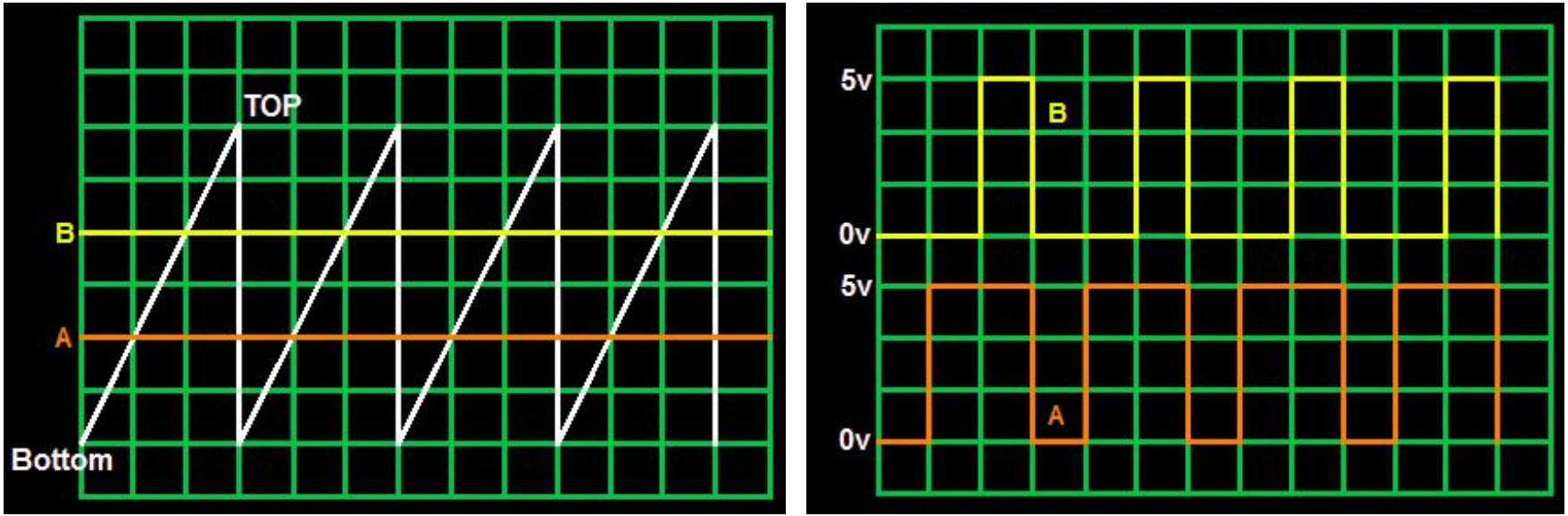
Fast PWM Mode

Counter (TCNT1) counts from BOTTOM to MAX

In non-inverting Compare Output mode, the Output Compare (OC1x) is cleared on the compare match between counter(TCNT1) and user defined value(OCR1x), and set at BOTTOM

In inverting Compare Output mode, the Output Compare (OC1x) is set on the compare match between counter(TCNT1) and user defined value(OCR1x), and cleared at BOTTOM

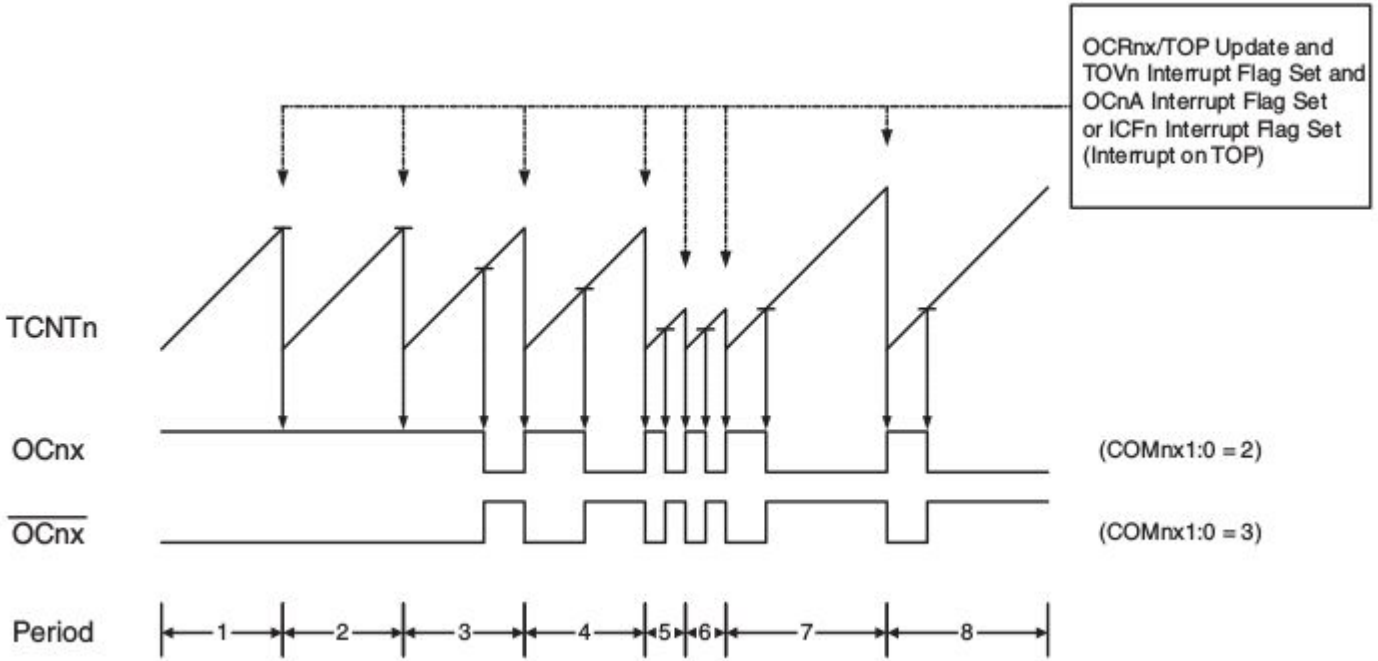
Inverted Fast PWM



In Inverted PWM, output is negated

*image courtesy: maxembedded

Timing Diagram of Fast PWM



Frequency of Fast PWM

$$f_{OCnxPWM} = \frac{f_{clk\_I/O}}{N \cdot (1 + TOP)}$$

Why ……???

OCR1A → Top → Bottom → OCR1A

0 → 0 → 1 → 0

(TOP-OCR1A+1) +OCR1A = TOP+1

That’s why (TOP+1)

Phase Correct PWM Mode

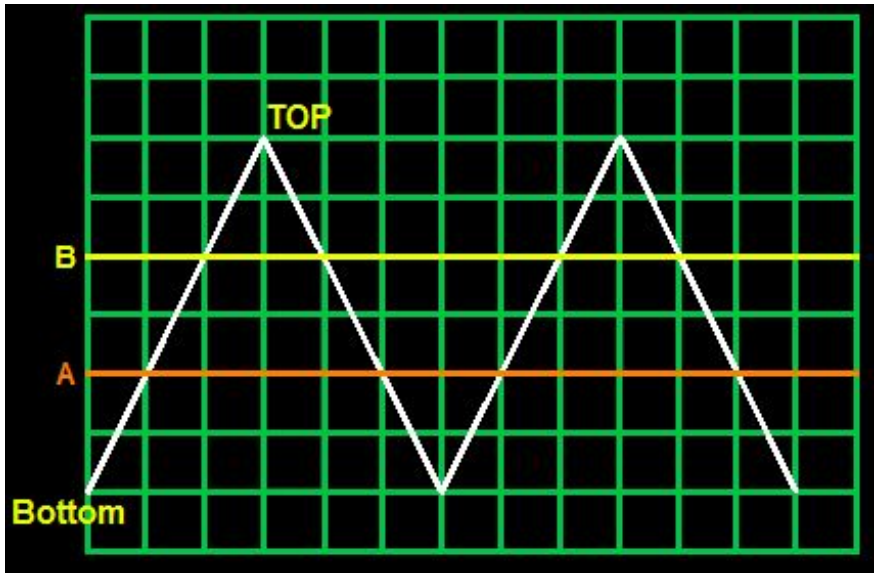
Based on a dual-slope operation

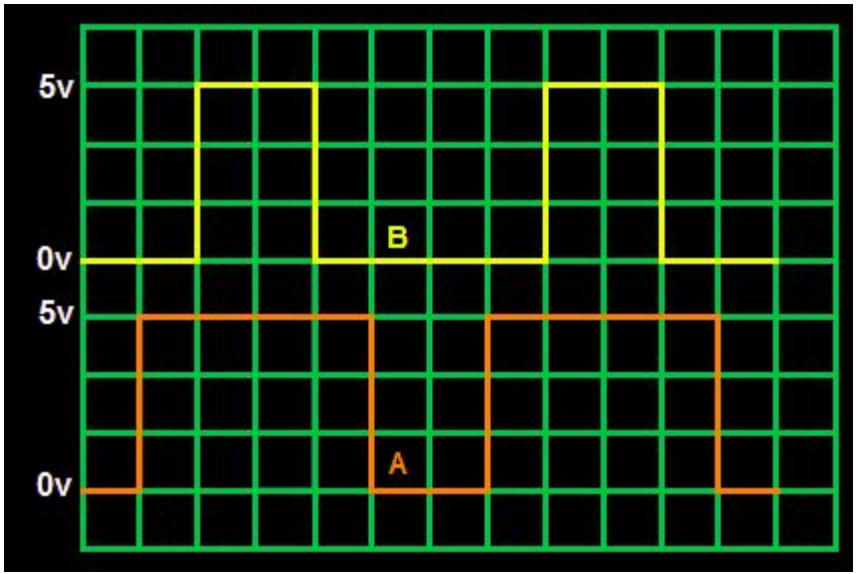
The counter counts repeatedly from BOTTOM (0x0000) to TOP and then from TOP to BOTTOM

In non-inverting Compare Output mode, the Output Compare (OC1x) is cleared on the compare match between TCNT1 and OCR1x while up-counting, and set on the compare match while down-counting.

In inverting Compare Output mode, the Output Compare (OC1x) is set on the compare match between TCNT1 and OCR1x while up-counting, and cleared on the compare match while down-counting.

Inverted Phase Correct PWM

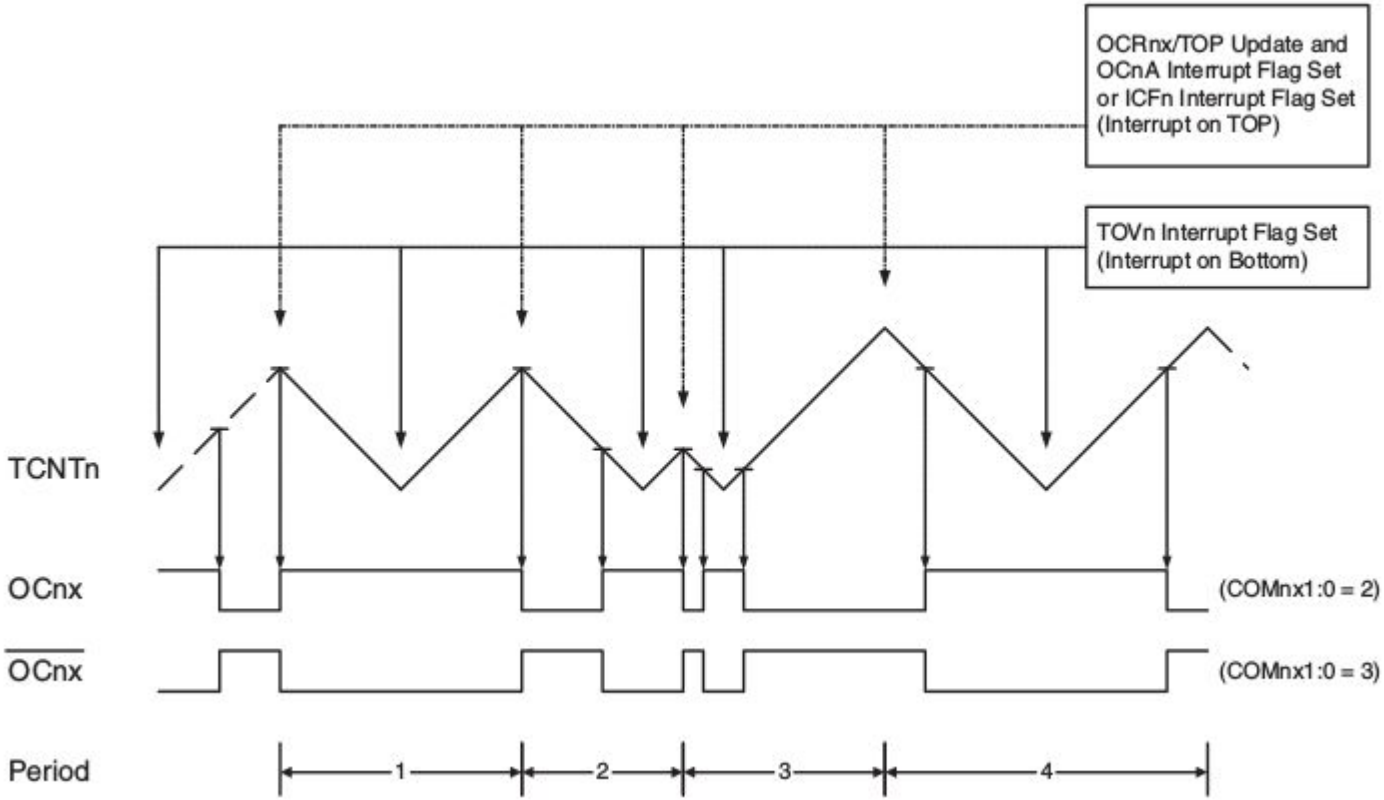




In Inverted PWM, output is negated

*image courtesy: maxembedded

Timing Diagram of Fast PWM



Frequency of Phase Correct PWM

$$f_{OCnxPCPWM} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot TOP}$$

Why …???

OCR1A → TOP → OCR1A → BOTTOM → OCR1A

0 → 0 → 1 → 1 → 0

That’s Why 2* TOP

Let’s get hands on

We’ll work on Timer1 ,ie, 16 bit timer

TCCR1A – Timer/Counter1 Control Register A

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Bit	7	6	5	4	3	2	1	0	
(0x80)	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	TCCR1A
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

WGM bits selects non pwm, pwm and phase correct PWM

Table 16-1. Compare Output Mode, non-PWM

COM1A1/COM1B1	COM1A0/COM1B0	Description
0	0	Normal port operation, OC1A/OC1B disconnected.
0	1	Toggle OC1A/OC1B on Compare Match.
1	0	Clear OC1A/OC1B on Compare Match (Set output to low level).
1	1	Set OC1A/OC1B on Compare Match (Set output to high level).

WGM bits selects non pwm, pwm and phase correct PWM

Table 16-2. Compare Output Mode, Fast PWM[(1)]

COM1A1/COM1B1	COM1A0/COM1B0	Description
0	0	Normal port operation, OC1A/OC1B disconnected.
0	1	WGM13:0 = 14 or 15: Toggle OC1A on Compare Match, OC1B disconnected (normal port operation). For all other WGM1 settings, normal port operation, OC1A/OC1B disconnected.
1	0	Clear OC1A/OC1B on Compare Match, set OC1A/OC1B at BOTTOM (non-inverting mode)
1	1	Set OC1A/OC1B on Compare Match, clear OC1A/OC1B at BOTTOM (inverting mode)

WGM bits selects non pwm, pwm and phase correct PWM

Table 16-3. Compare Output Mode, Phase Correct and Phase and Frequency Correct PWM[1]

COM1A1/COM1B1	COM1A0/COM1B0	Description
0	0	Normal port operation, OC1A/OC1B disconnected.
0	1	WGM13:0 = 9 or 11: Toggle OC1A on Compare Match, OC1B disconnected (normal port operation). For all other WGM1 settings, normal port operation, OC1A/OC1B disconnected.
1	0	Clear OC1A/OC1B on Compare Match when up-counting. Set OC1A/OC1B on Compare Match when downcounting.
1	1	Set OC1A/OC1B on Compare Match when up-counting. Clear OC1A/OC1B on Compare Match when downcounting.

WGM bits

Table 16-4. Waveform Generation Mode Bit Description[(1)]

Mode	WGM13	WGM12 (CTC1)	WGM11 (PWM11)	WGM10 (PWM10)	Timer/Counter Mode of Operation	TOP	Update of OCR1x at	TOV1 Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICR1	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCR1A	BOTTOM	TOP

TCCR1B – Timer/Counter1 Control Register B

Bit	7	6	5	4	3	2	1	0	
(0x81)	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Table 16-5. Clock Select Bit Description

CS12	CS11	CS10	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	$clk_{I/O}$/1 (No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T1 pin. Clock on falling edge.
1	1	1	External clock source on T1 pin. Clock on rising edge.

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