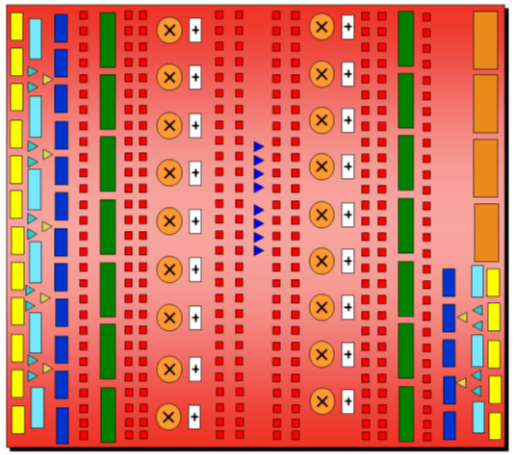
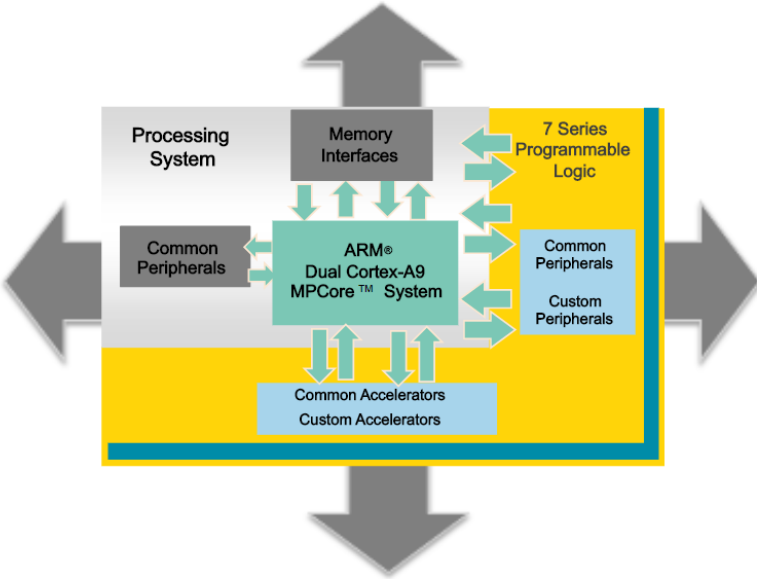
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

A2A
Algorithms to Architecture

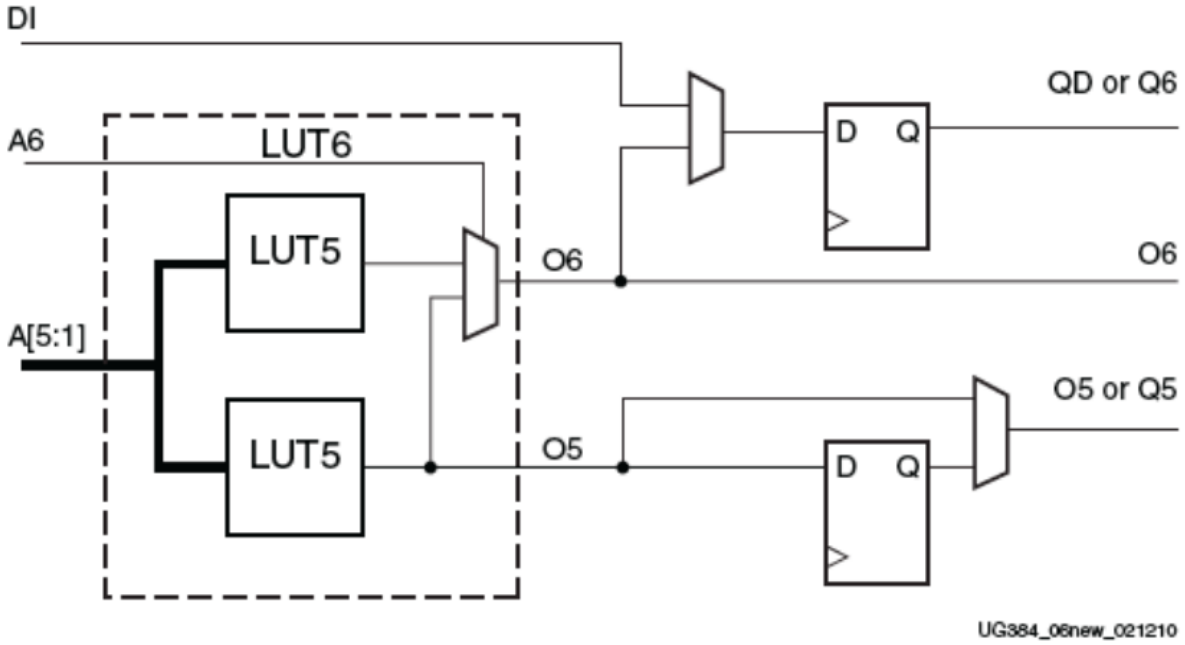
ECE 270: Embedded Logic Design





LUT

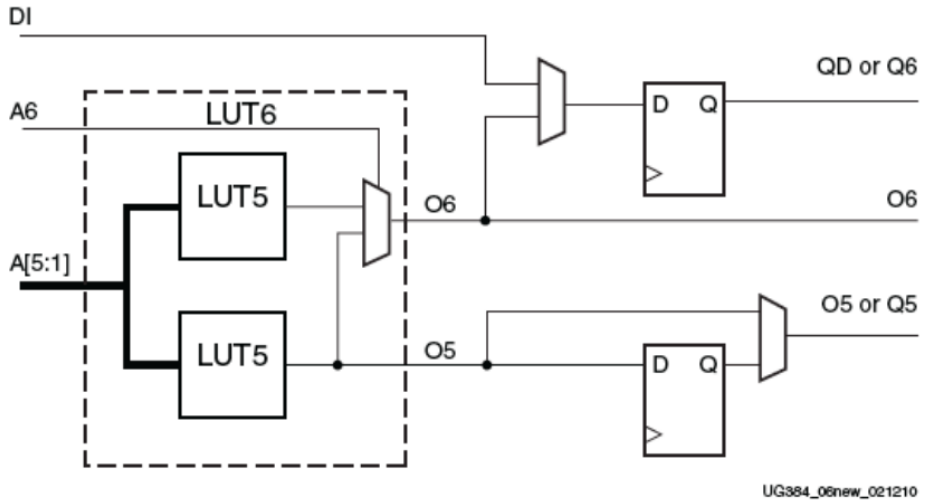
- There are six independent inputs (A inputs - A1 to A6) and two independent outputs (O5 and O6)



3-Input LUT for Logic

- Any single arbitrarily defined 3-input Boolean function
- A 3-input function uses: A1-A3 inputs and O3 output
- Two arbitrarily defined 2-input Boolean functions, as long as these two functions share common inputs
- Two 2-input or less functions use: A1–A2 inputs, A3 driven High, O2 and O3 outputs
- Two arbitrarily defined Boolean functions of 1 input

6-Input LUT for Logic



- Any arbitrarily defined six-input Boolean function
- A six-input function uses: A1-A6 inputs and O6 output
- Two arbitrarily defined five-input Boolean functions, as long as these two functions share common inputs
- Two five-input or less functions use: A1–A5 inputs, A6 driven High, O5 and O6 outputs
- Two arbitrarily defined Boolean functions of 3 and 2 inputs or less

What is Memory?

LUT as Memory

- Only in SLICEM
- Multiple LUTs in a SLICEM can be combined in various ways to store large amount of data
- Synchronous write operation, WEN must be high
- Asynchronous or synchronous read (using flip-flop in the same slice)

LUT as Memory

- **Single port:** Common address port for synch write and asynch read i.e. read and write addresses share the same address bus

LUT as Memory

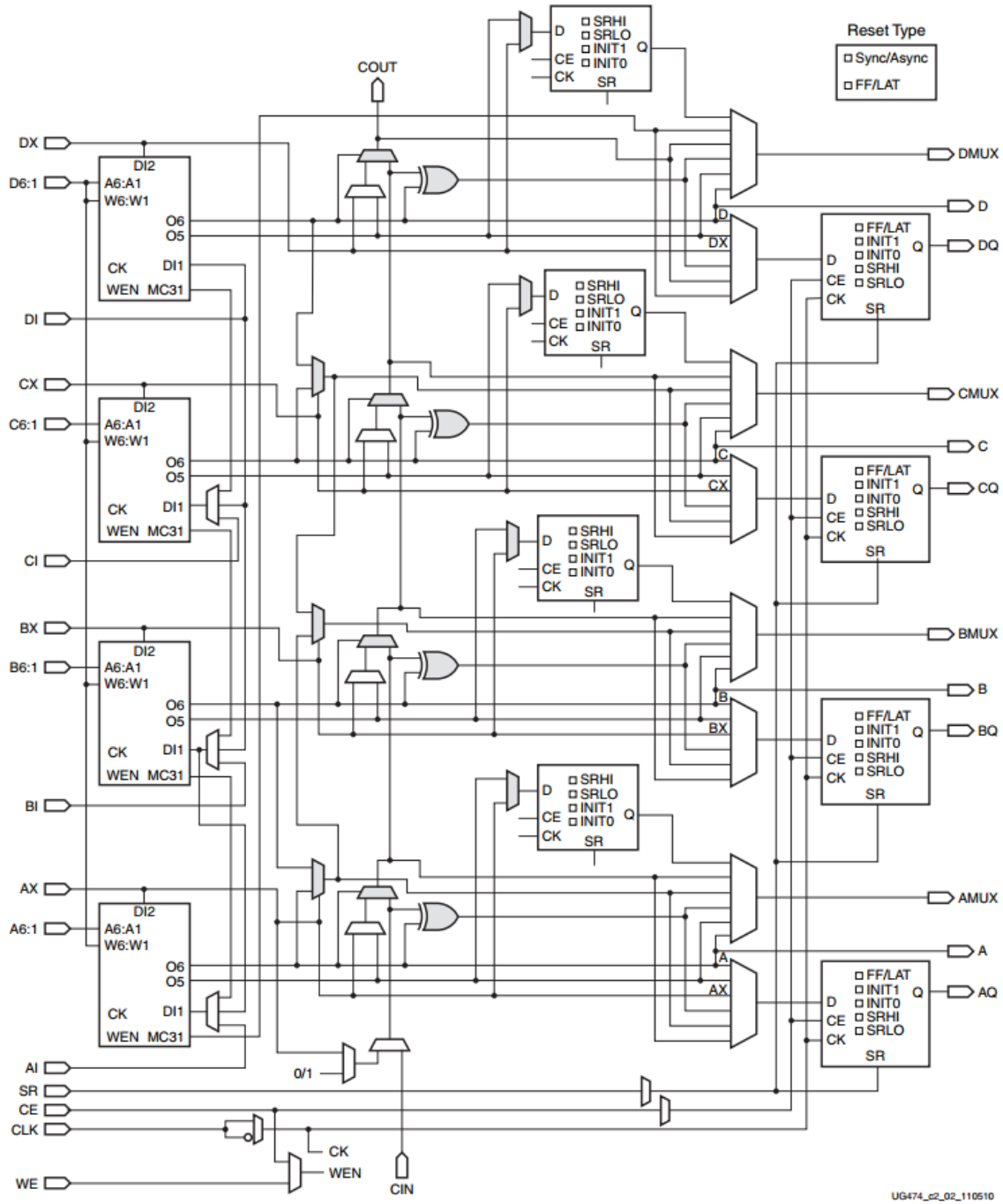
- **Dual port:** One port for synch write and asynch read, one port for asynch read

LUT as Memory

- **Quad port:** One port for synchronous write and asynchronous read and three ports for asynchronous reads

LUT as Memory

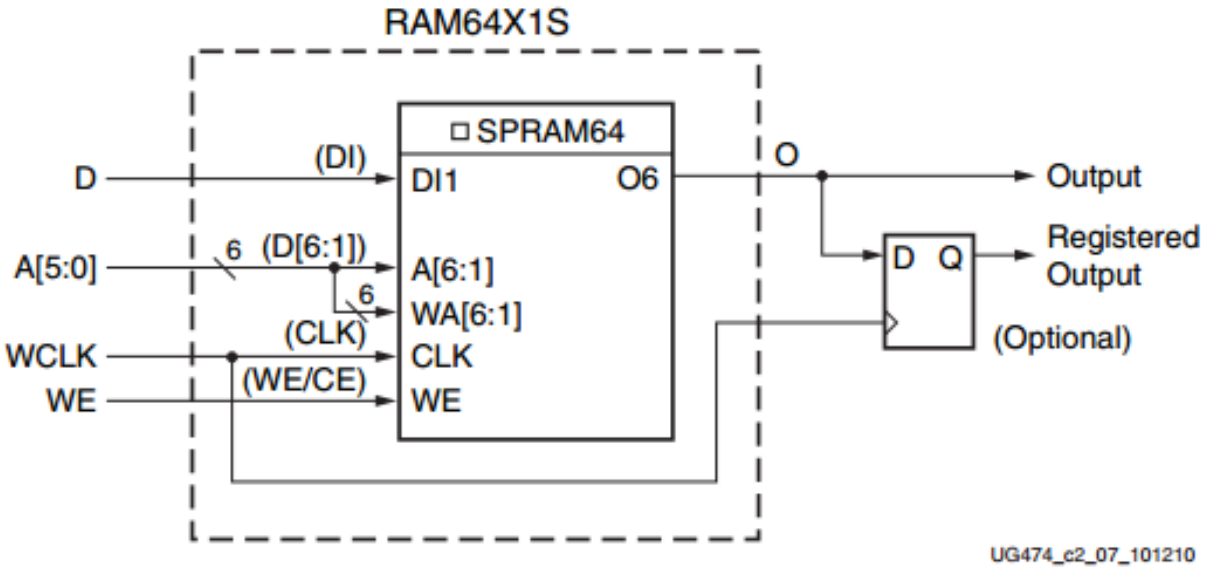
- **Simple dual port:** One port for synchronous write (no data out/read port from the write port) and one port for asynchronous reads


Reset Type
Sync/Async
FF/LAT
COUT
DX
D6:1
DI
CX
C6:1
CI
BX
B6:1
BI
AX
A6:1
AI
SR
CE
CLK
WE
DI2
A6:A1
W6:W1
O6
O5
CK
DI1
WEN
MC31
SRHI
SRLO
INIT1
INIT0
D
CE
Q
FF/LAT
0/1
CIN
DMUX
DQ
CMUX
CQ
BMUX
BQ
AMUX
AQ
UG474_c2_02_110510

LUT as Memory: 64X1 Single Port

LUT as Memory: 64X1 Single Port

- **Single port:** Common address port for synch write and asynch read
- One SLICEM can have FOUR 64 x 1-bit memories as long as they share the same clock, write enable, and shared read and write port address inputs
- This configuration equates to a 64 x 4-bit single-port distributed RAM.
- What about O5 output?

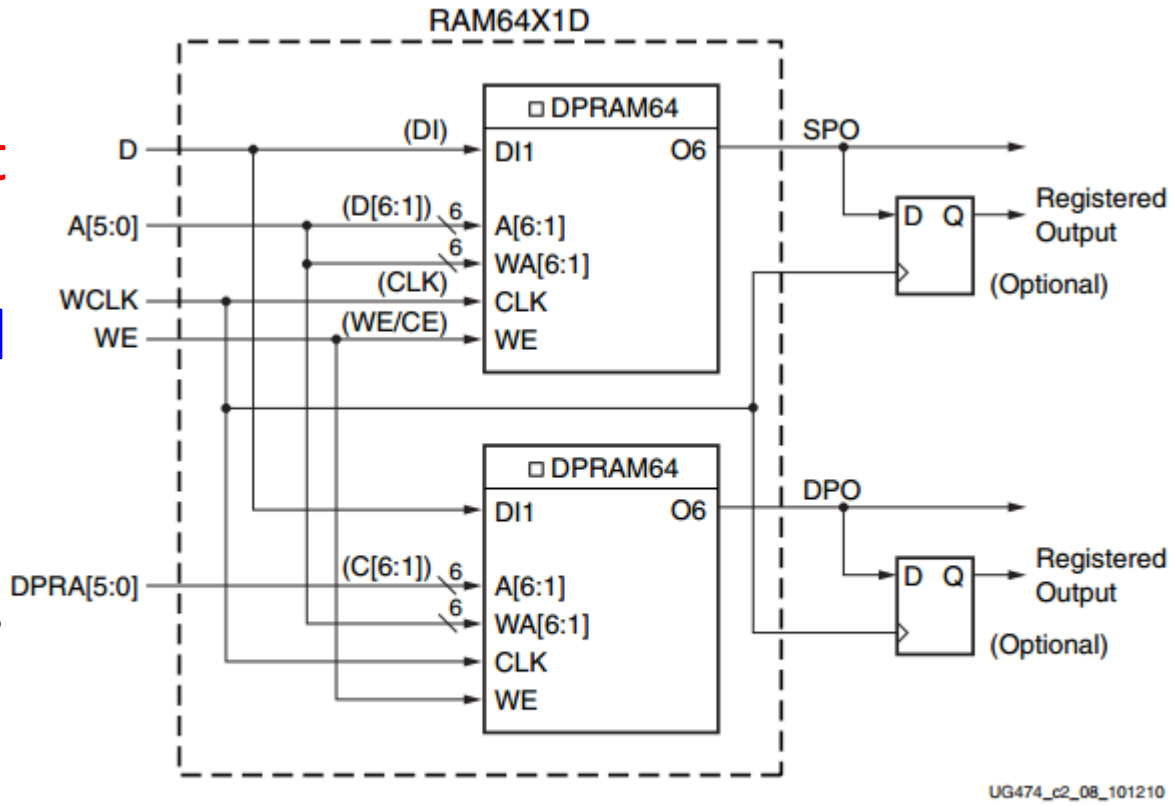


64 X 1 Single Port Distributed RAM (RAM64X1S)

LUT as Memory: 64X1 Dual Port

LUT as Memory: 64X1 Dual Port

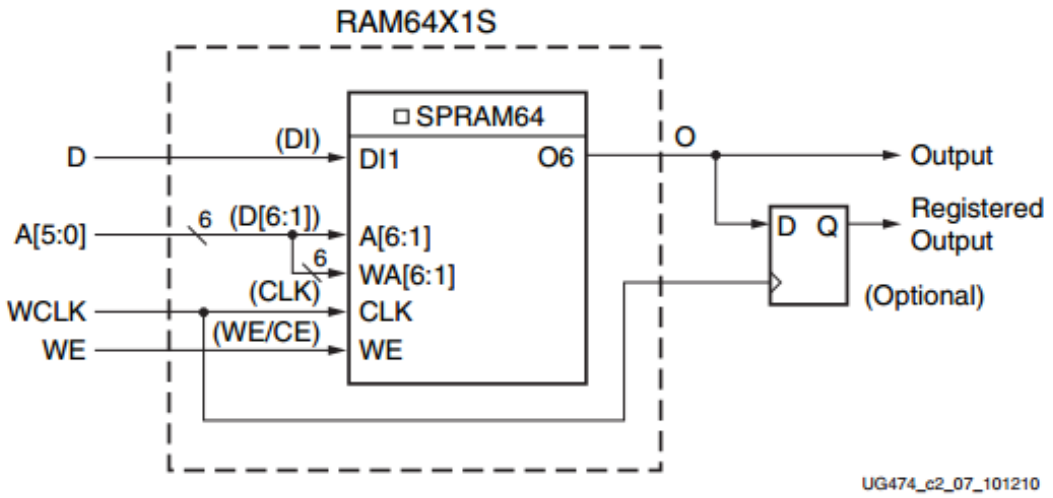
- One SLICEM can have TWO 64 x 1-bit memories as long as they share the same clock, write enable, and shared read and write port address inputs
- This configuration equates to a 64 x 2-bit dual-port distributed RAM.



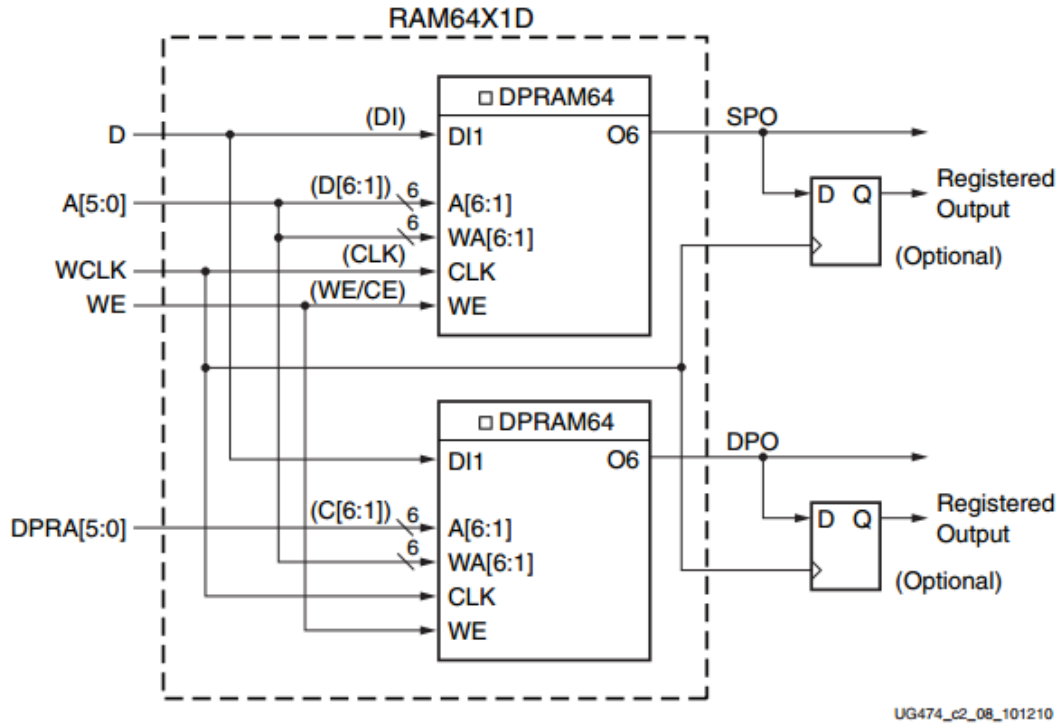
64 X 1 Dual Port Distributed RAM (RAM64X1D)

LUT as Memory

- **Synchronous Write Operation**
  The synchronous write operation is a single clock-edge operation with an active-High write-enable (WE) feature. When WE is High, the input (D) is loaded into the memory location at address A.



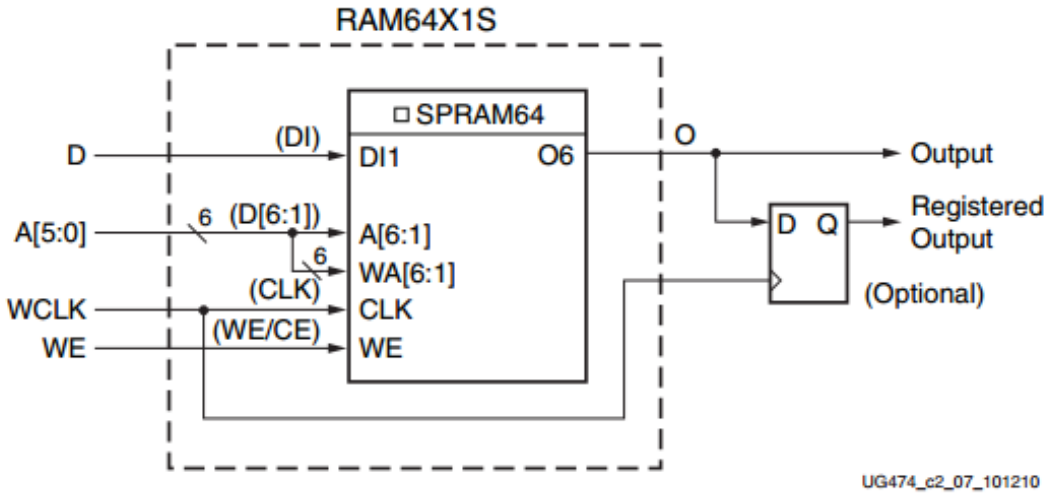
64 X 1 Single Port Distributed RAM (RAM64X1S)



64 X 1 Dual Port Distributed RAM (RAM64X1D)

LUT as Memory

- **Asynchronous Read Operation**
  The output (or output SPO of dual-port mode) is determined by the address A for the single-port mode or address DPRA determines the DPO output of dual-port mode.
- Each time a new address is applied to the address pins, the data value in the memory location of that address is available on the output.
- This operation is asynchronous and independent of the clock signal.



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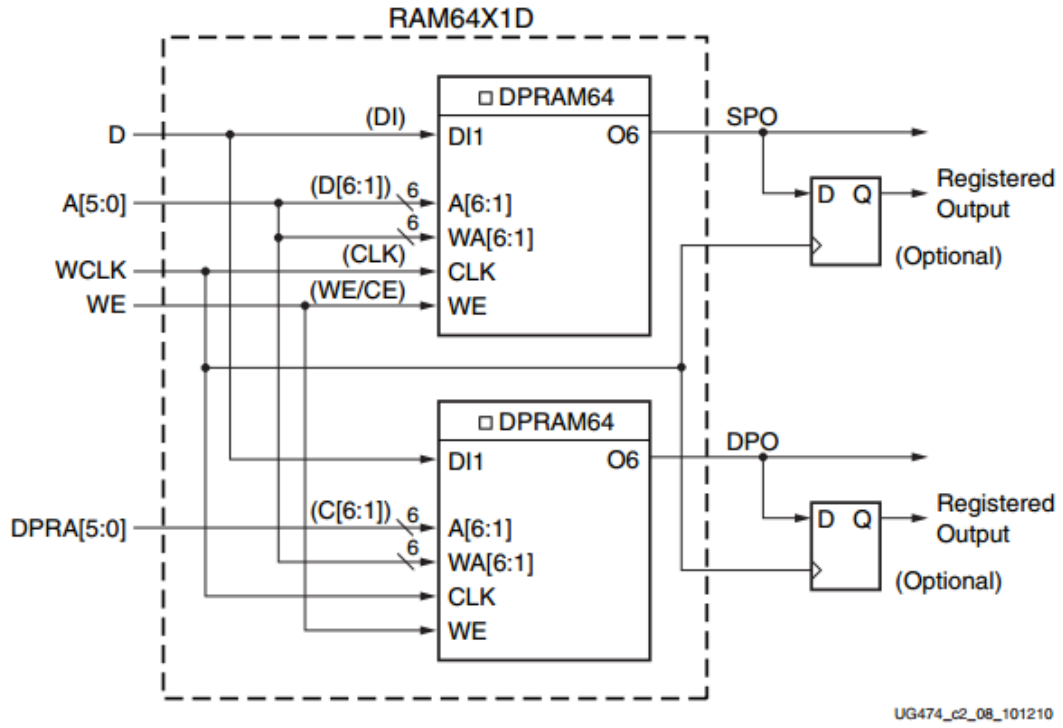
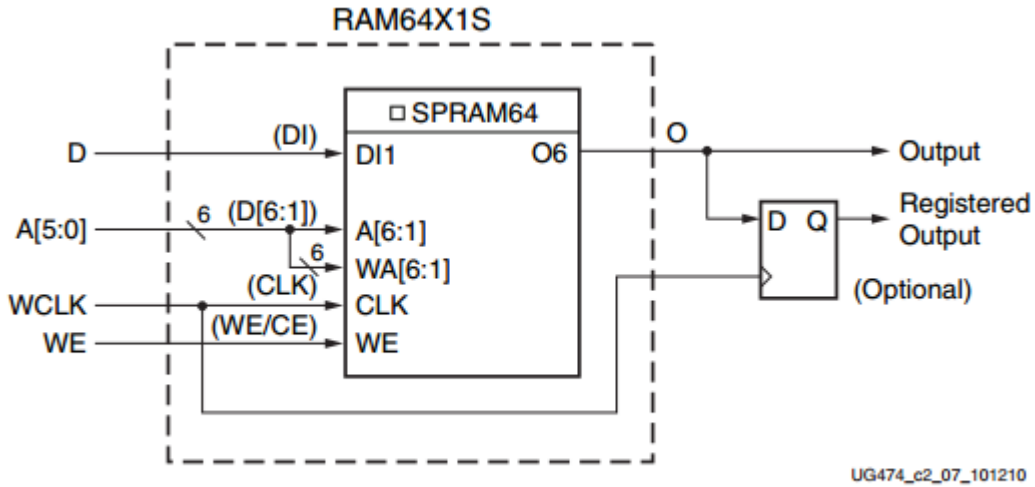
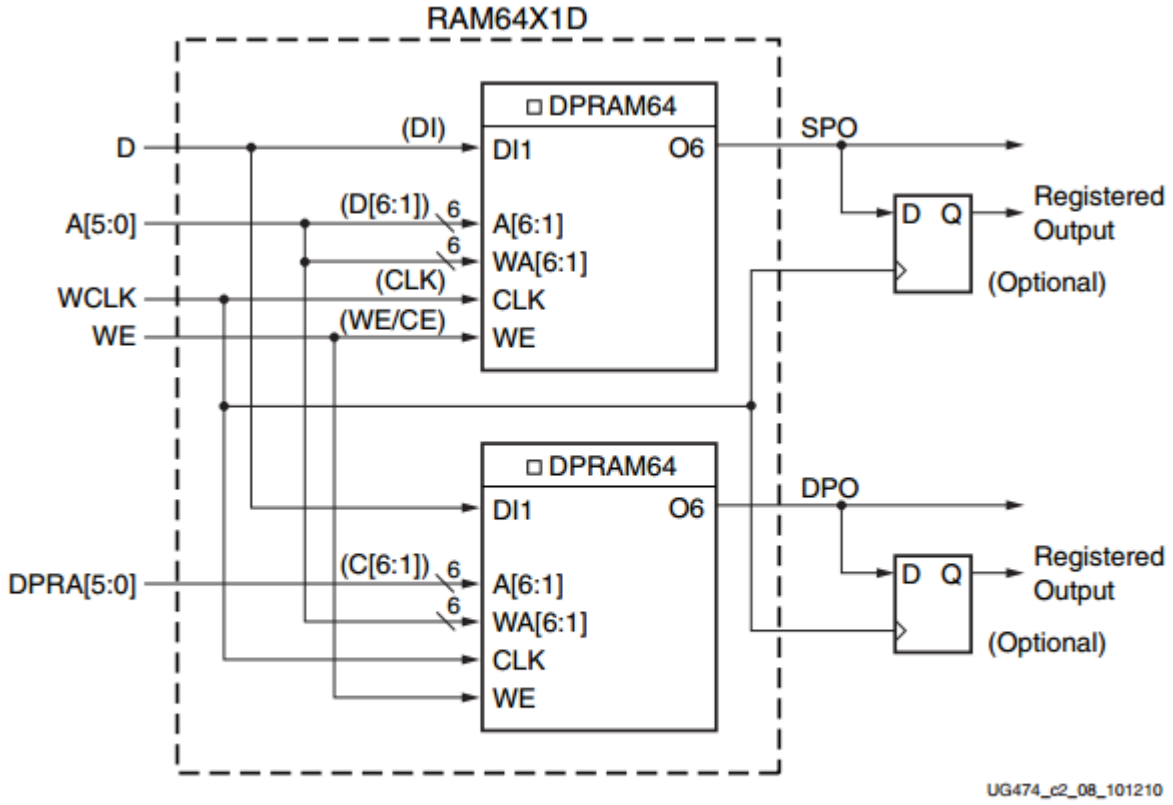


64 X 1 Dual Port Distributed RAM (RAM64X1D)

LUT as Memory: 64X1 Dual Port



64 X 1 Single Port Distributed RAM (RAM64X1S)



64 X 1 Dual Port Distributed RAM (RAM64X1D)