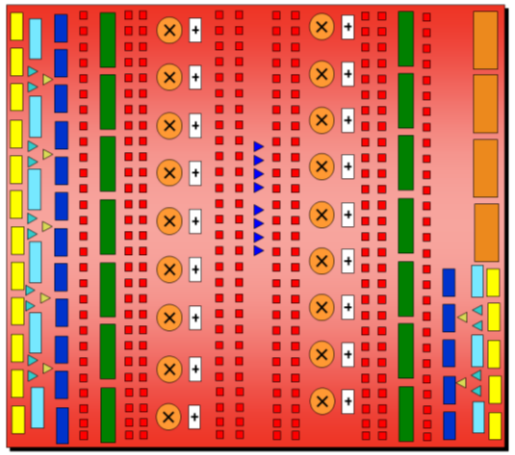
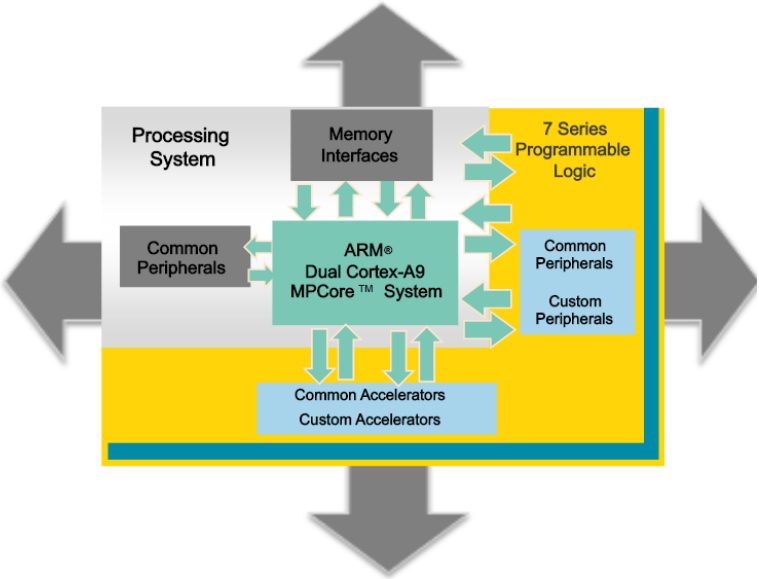
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

A2A
Algorithms to Architecture

ECE 270: Embedded Logic Design





AXI Interface: Burst

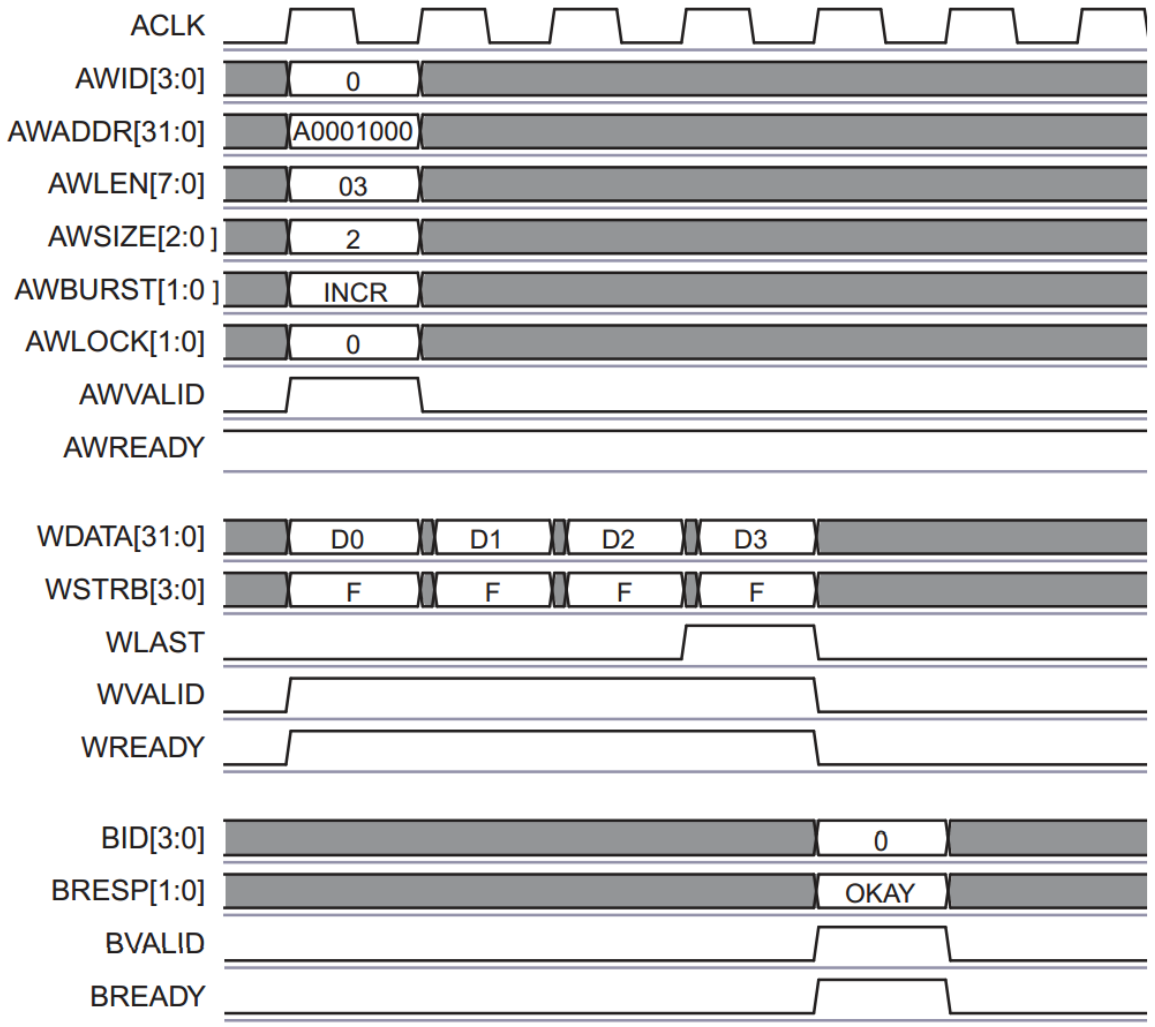
ARBURST[1:0] AWBURST[1:0]	Burst type	Description	Access
b00	FIXED	Fixed-address burst	FIFO-type
b01	INCR	Incrementing-address burst	Normal sequential memory
b10	WRAP	Incrementing-address burst that wraps to a lower address at the wrap boundary	Cache line
b11	Reserved	-	-

AXI Interface: Write

AxSIZE[2:0]	Bytes in transfer
0b000	1
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	64
0b111	128

The burst length for AXI4 is defined as,

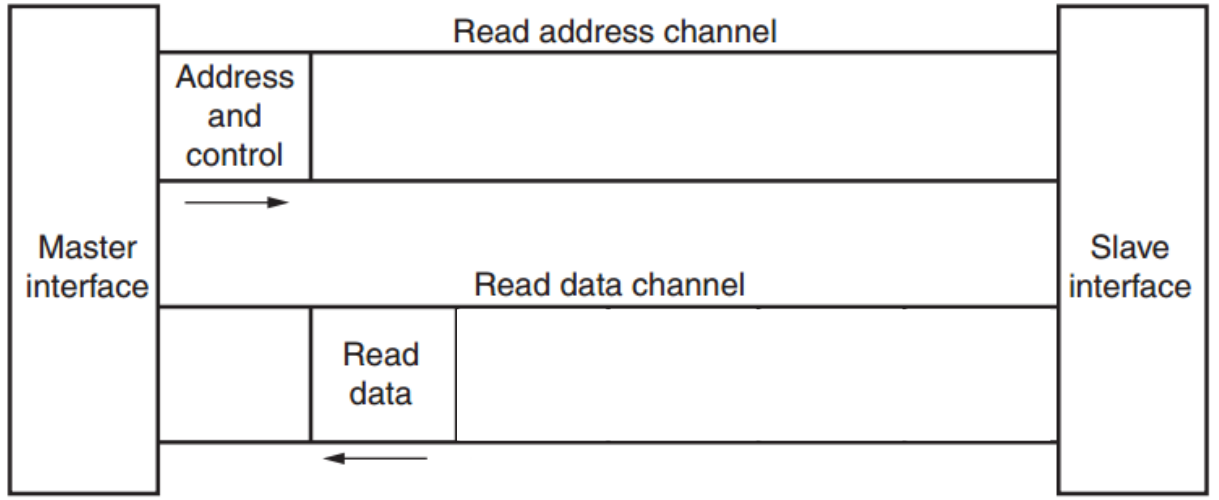
Burst_Length = **AxLEN[7:0]** + 1

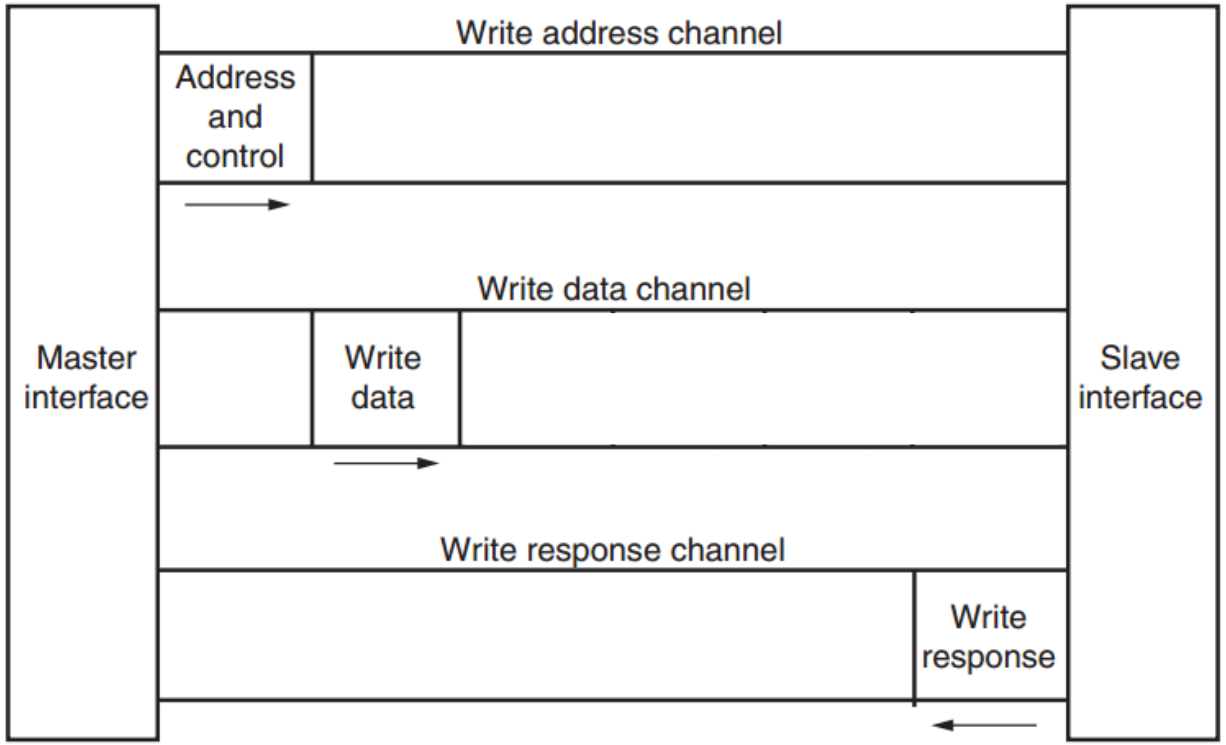


Example of AXI4 write burst transaction

AXI Lite

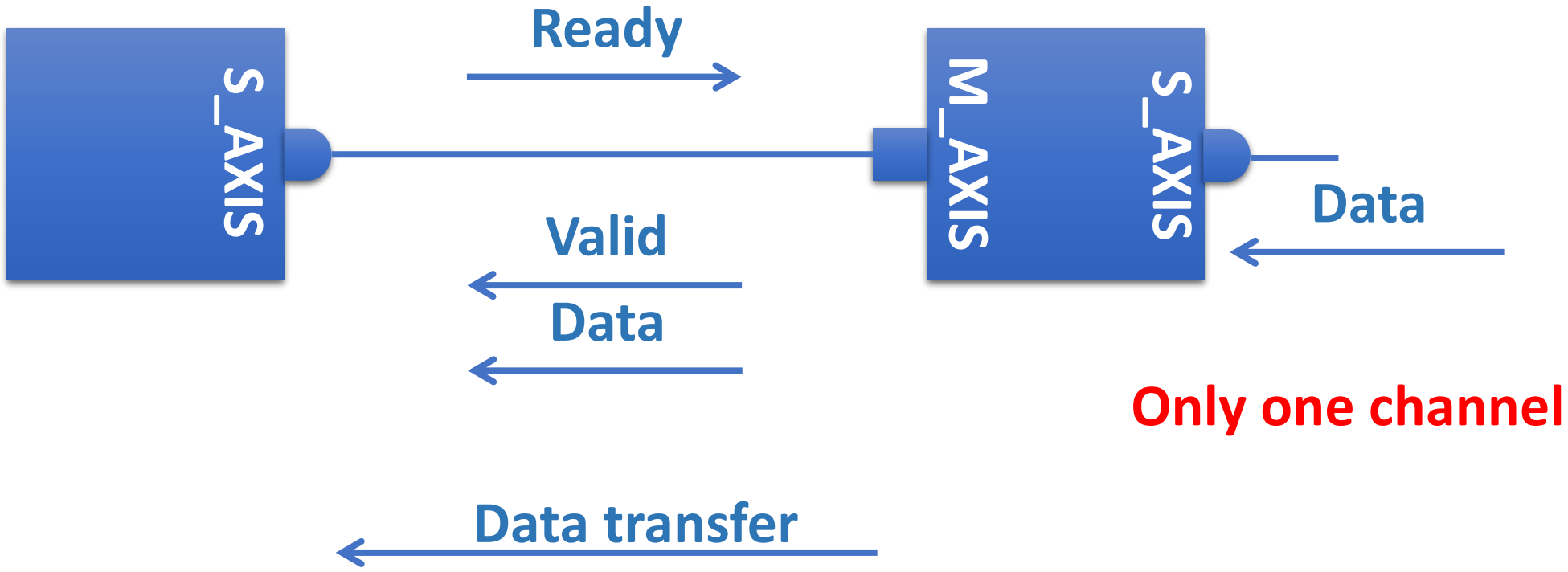
- Bursting is not supported
- Subset of the AXI4 interface intended for communication with control registers and have small footprint



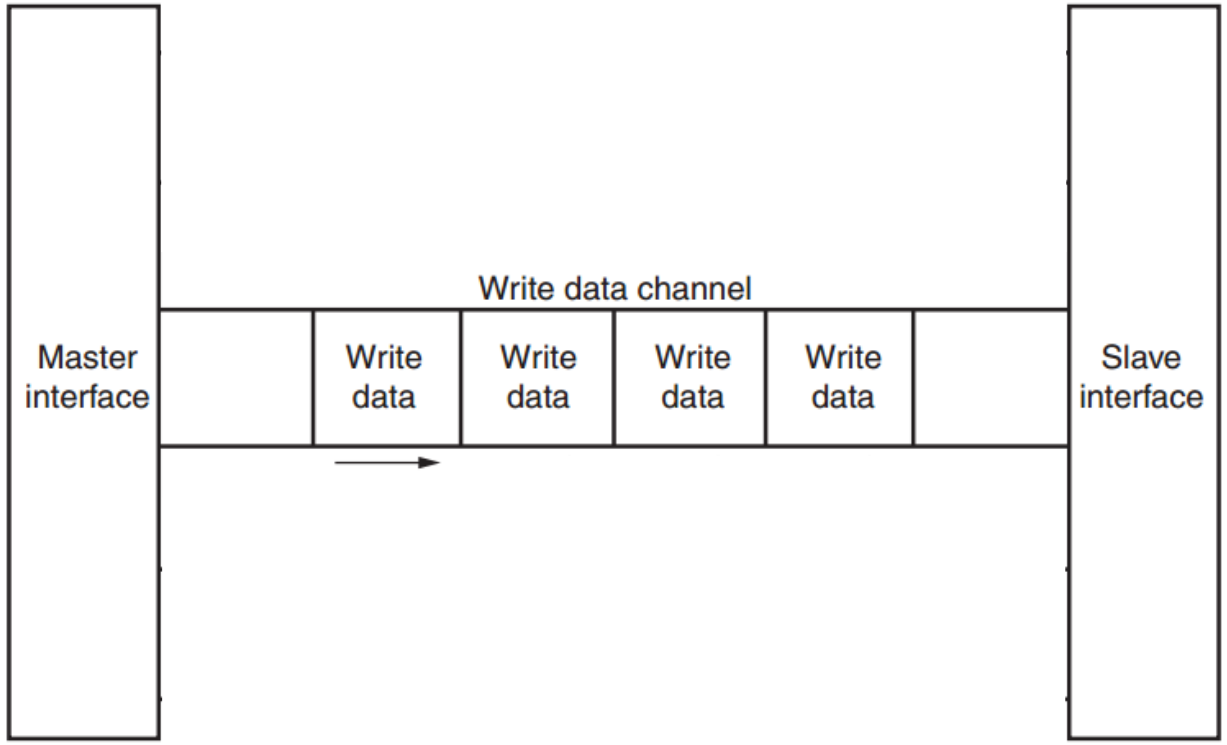


AXI Stream

- The AXI4-Stream protocol defines a single channel for transmission of streaming data (unlimited burst).

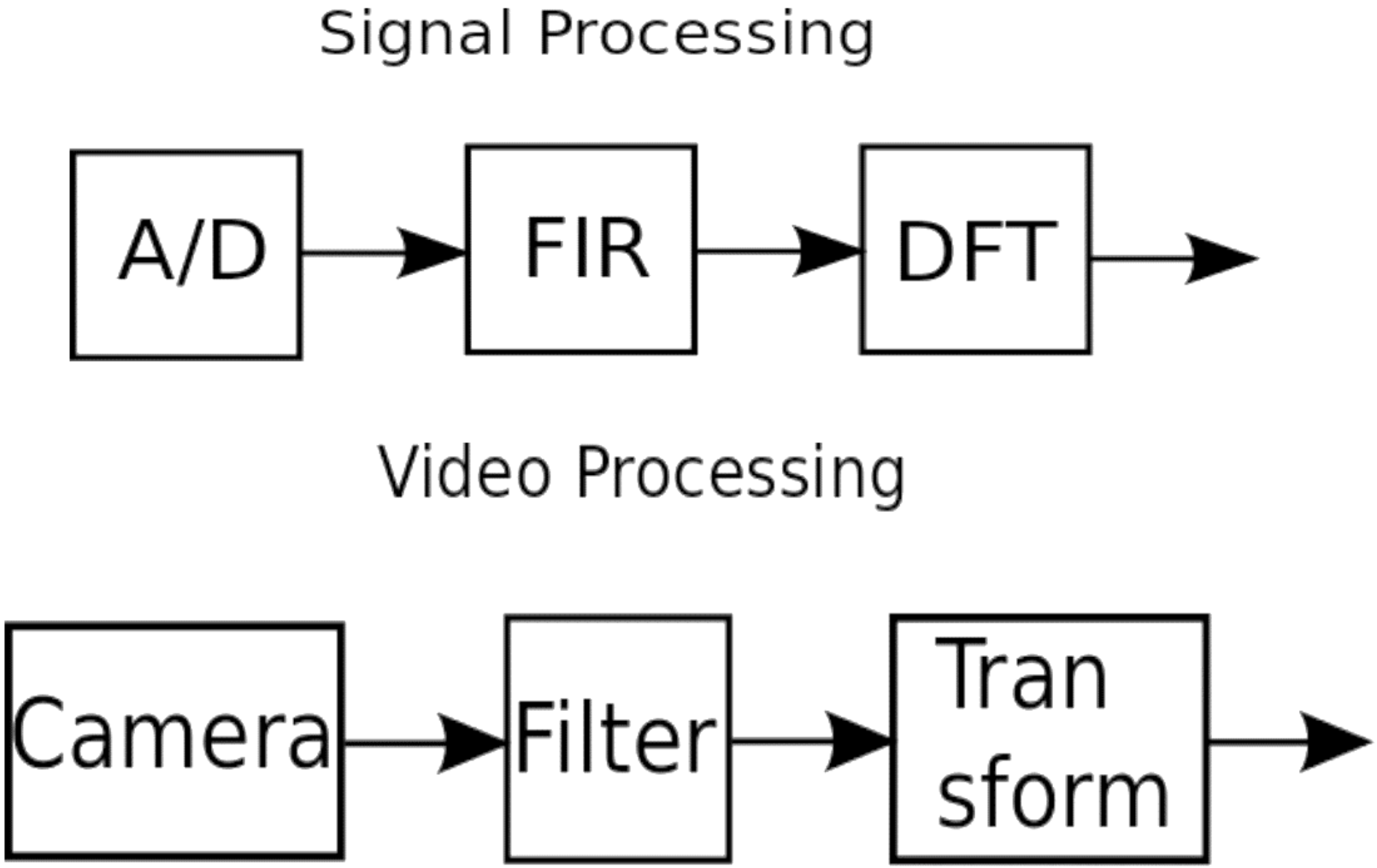


AXI Stream

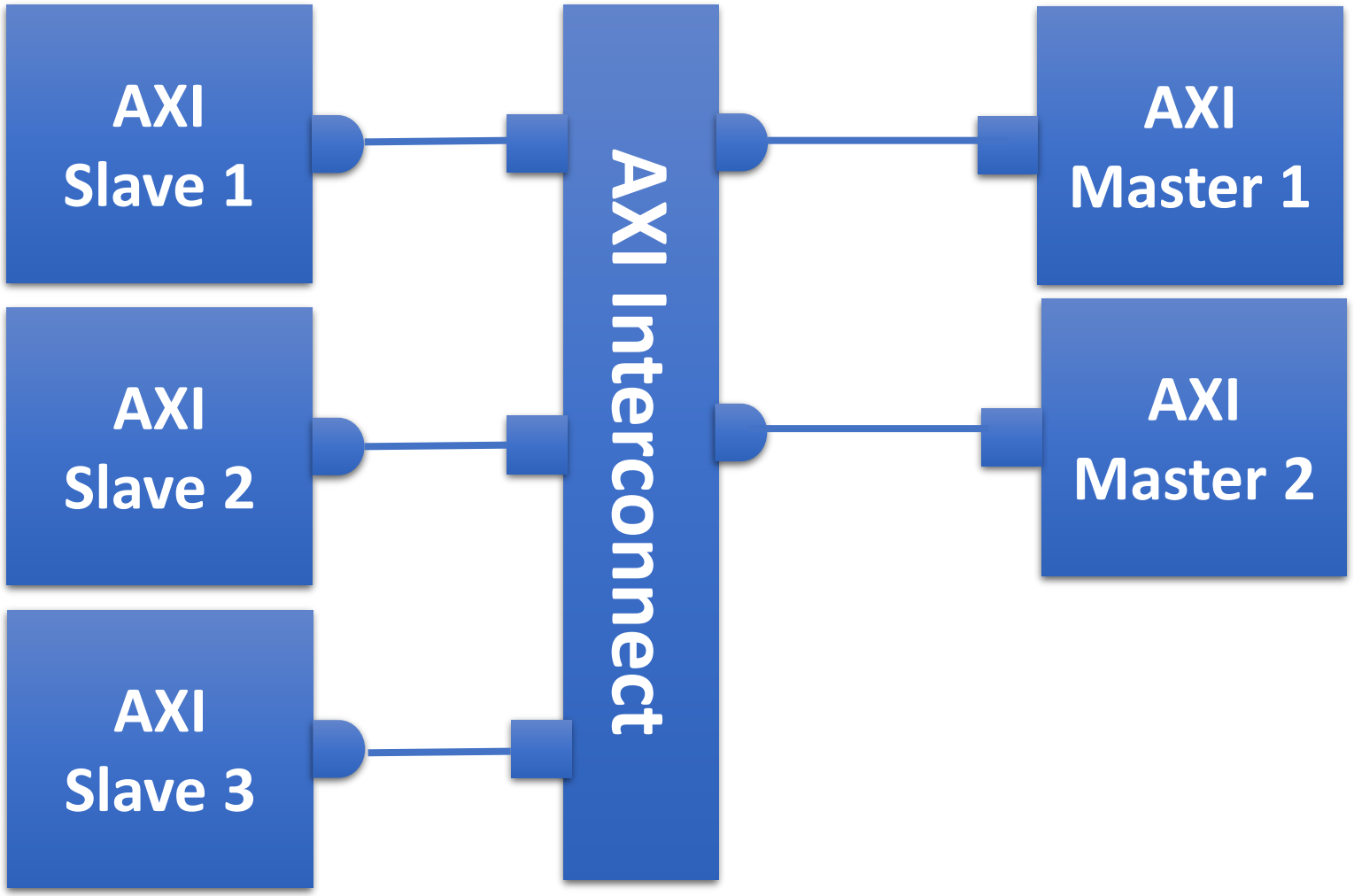


- The AXI4-Stream channel is modeled after the Write Data channel of the AXI4.
- Unlike AXI4, AXI4-Stream interfaces can burst an **unlimited** amount of data.

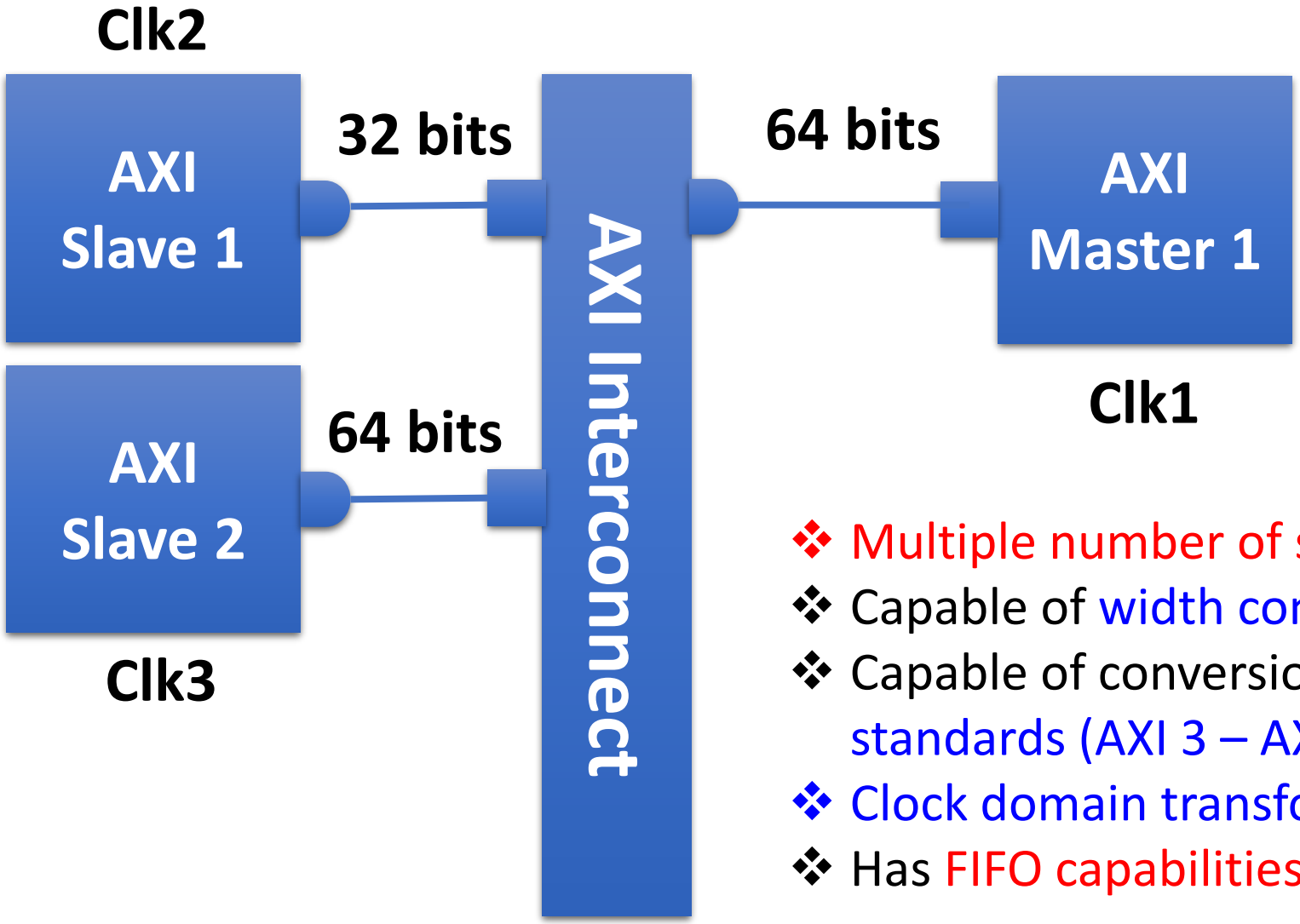
AXI Stream


Signal Processing
A/D
FIR
DFT
Video Processing
Camera
Filter
Tran
sform

AXI Interconnect

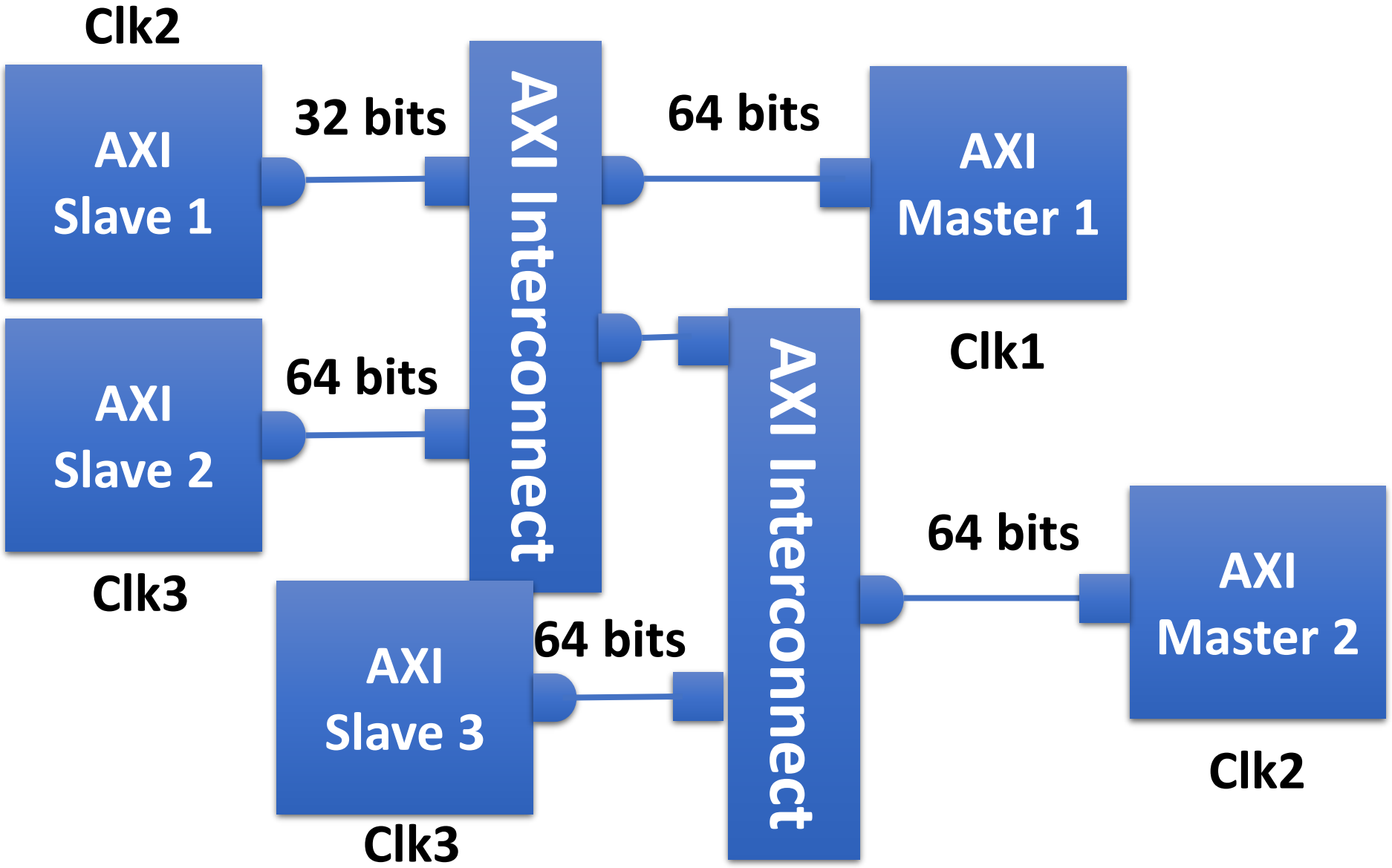


AXI Interconnect

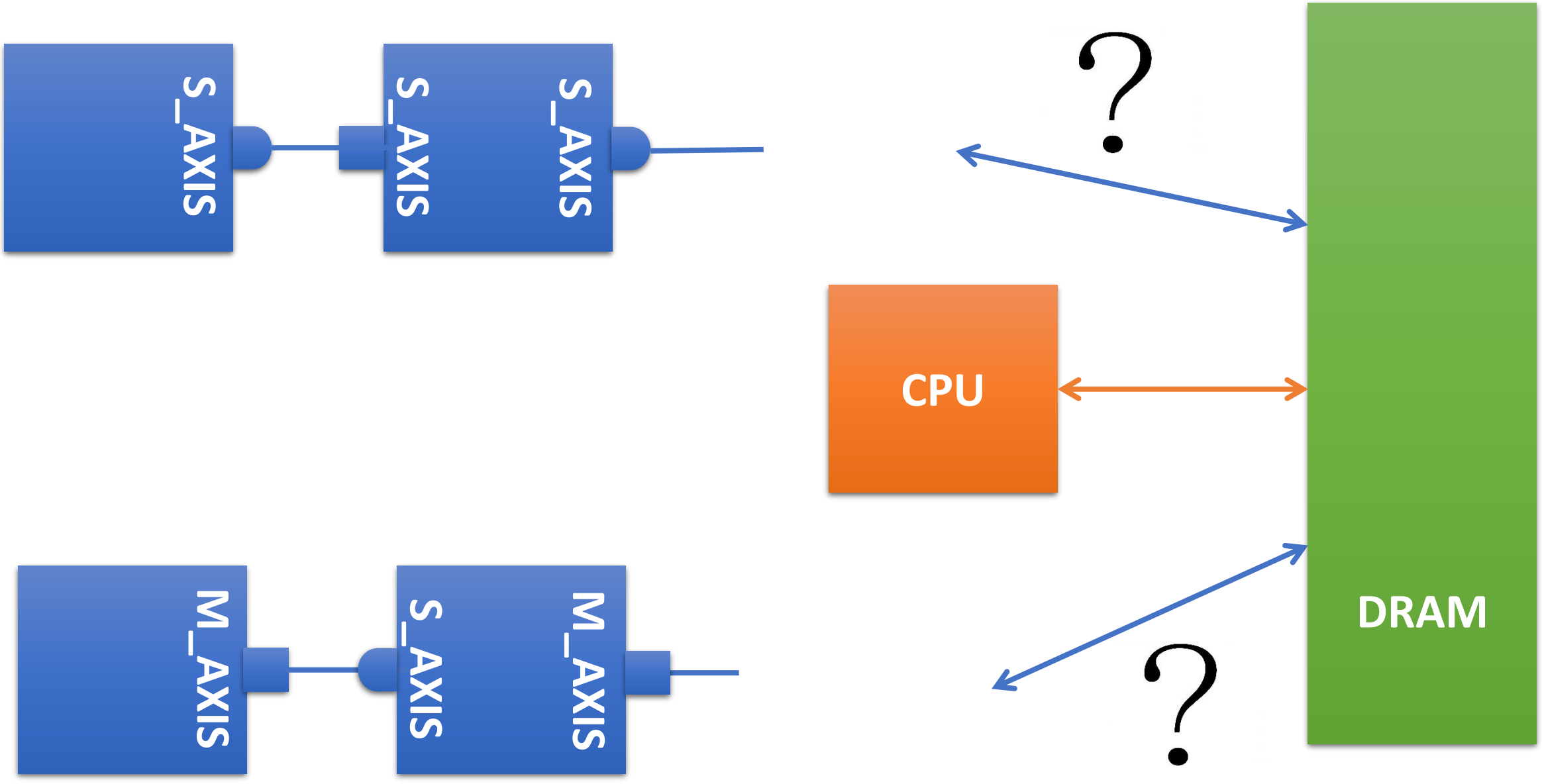


- Multiple number of slave and master ports
- Capable of width conversion
- Capable of conversion between different AXI standards (AXI 3 – AXI 4)
- Clock domain transformations
- Has FIFO capabilities, registers for pipelining

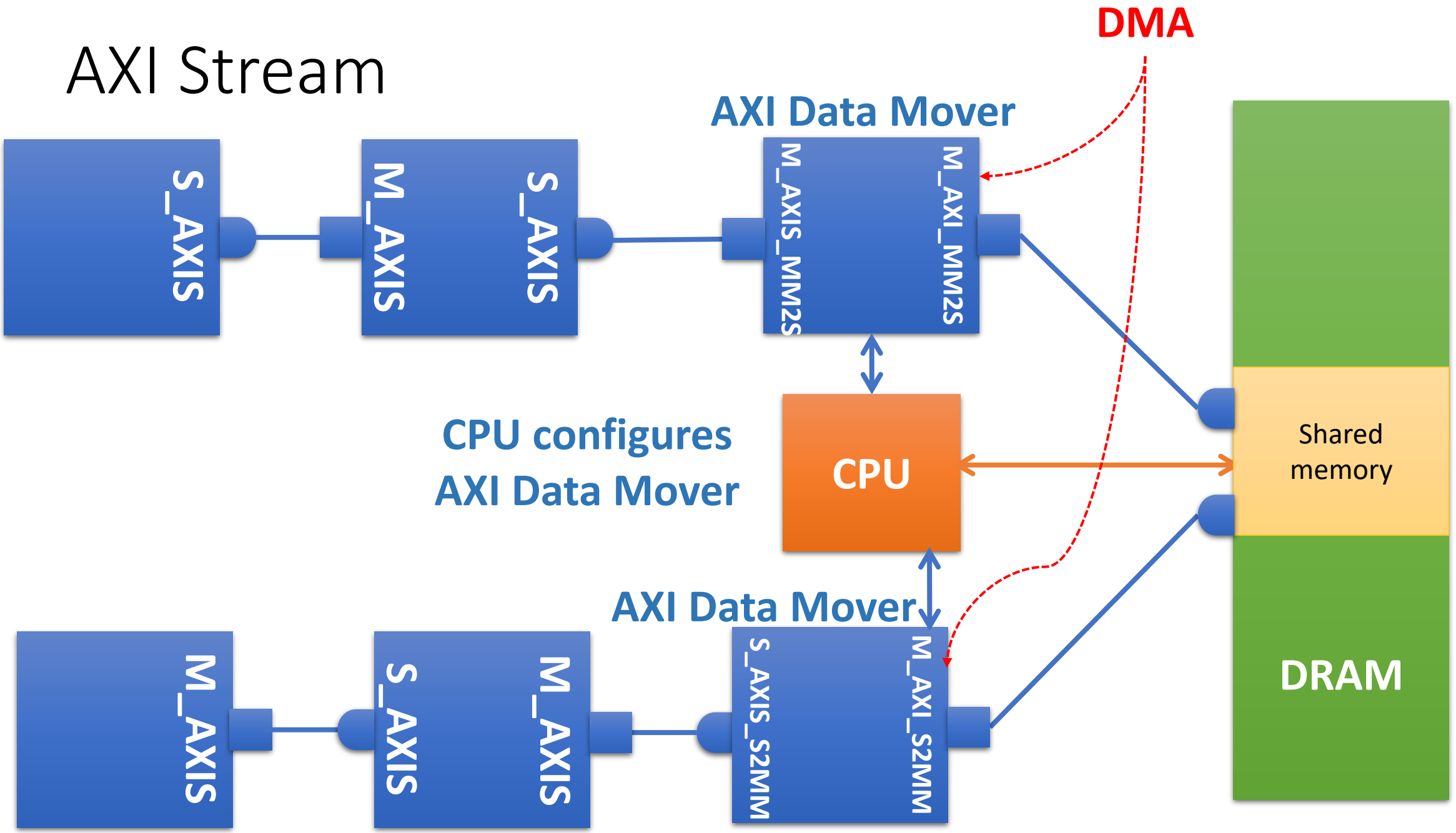
Hierarchical AXI Interconnect



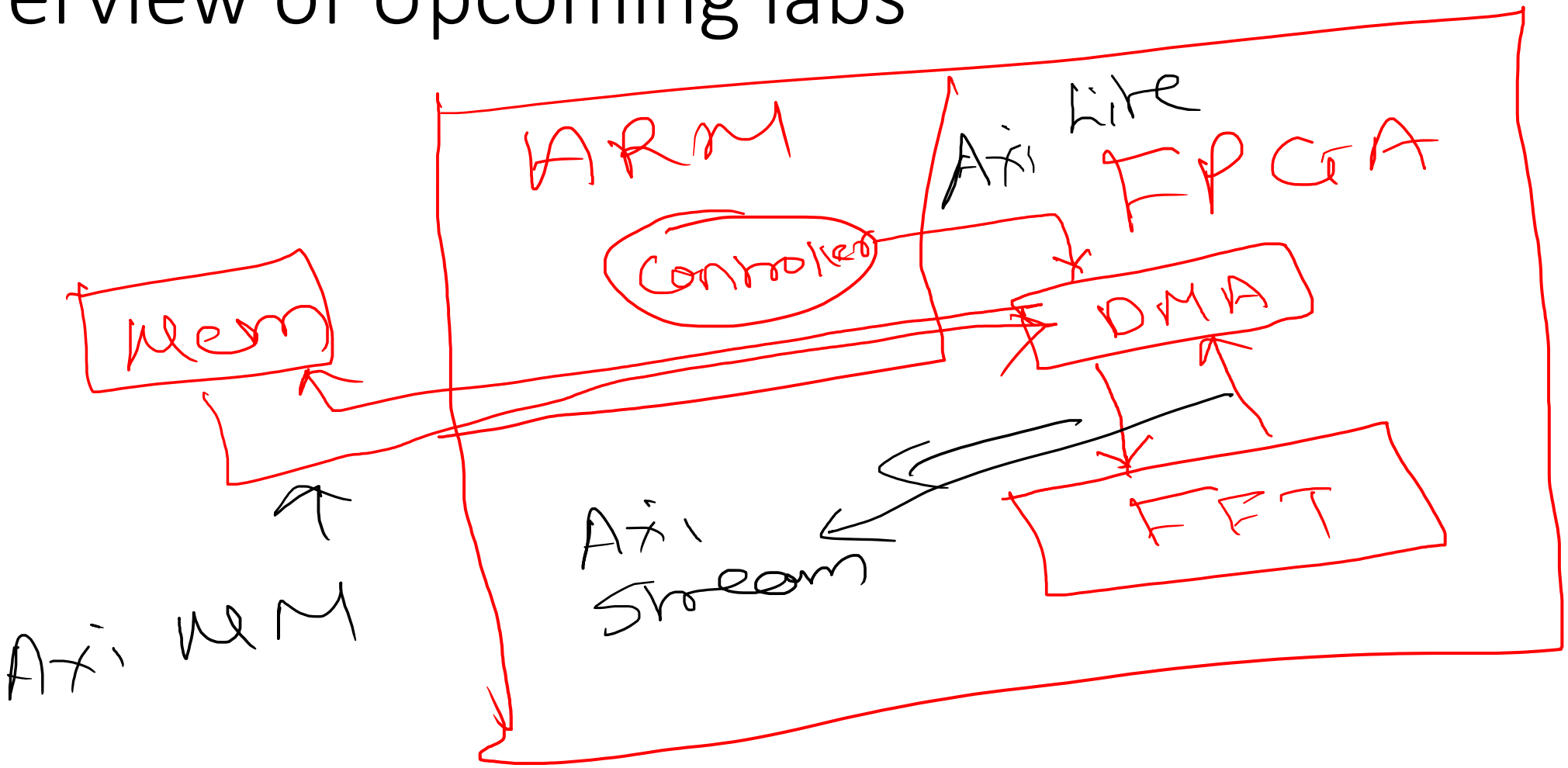
AXI Stream



AXI Stream


DMA
AXI Data Mover
S_AXIS
M_AXIS
S_AXIS
M_AXIS_MM2S
M_AXI_MM2S
CPU configures
AXI Data Mover
CPU
Shared
memory
AXI Data Mover
M_AXIS
S_AXIS
M_AXIS
S_AXIS_S2MM
M_AXI_S2MM
DRAM

Overview of Upcoming labs



Embedded Logic Design

- What do you mean by word Embedded?
- Why FPGAs are part of Embedded Systems?
- What are other components of Embedded Systems?
- How to build FPGA based accelerators for Embedded Systems?

What is a system?

- A system is a way of working, organizing or doing one or many tasks according to a fixed plan, program or set of rules.
- It is an arrangement in which all its units assemble and work together according to the plan or program.
- **Embedded System** is a combination of hardware and software which together form a component of a larger machine.
- An embedded system is designed to run on its own without human intervention, and may be required to respond to events in real time.

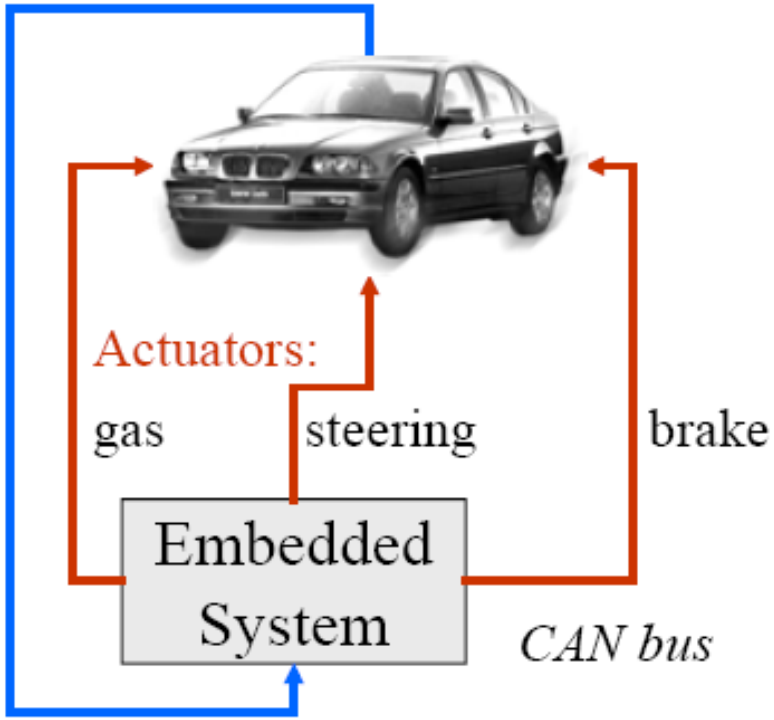
A “short list” of embedded systems

Anti-lock brakes
Auto-focus cameras
Automatic teller machines
Automatic toll systems
Automatic transmission
Avionic systems
Battery chargers
Camcorders
Cell phones
Cell-phone base stations
Cordless phones
Cruise control
Curbside check-in systems
Digital cameras
Disk drives
Electronic card readers
Electronic instruments
Electronic toys/games
Factory control
Fax machines
Fingerprint identifiers
Home security systems
Life-support systems
Medical testing systems

Modems
MPEG decoders
Network cards
Network switches/routers
On-board navigation
Pagers
Photocopiers
Point-of-sale systems
Portable video games
Printers
Satellite phones
Scanners
Smart ovens/dishwashers
Speech recognizers
Stereo systems
Teleconferencing systems
Televisions
Temperature controllers
Theft tracking systems
TV set-top boxes
VCR’s, DVD players
Video game consoles
Video phones
Washers and dryers

And the list goes on and on

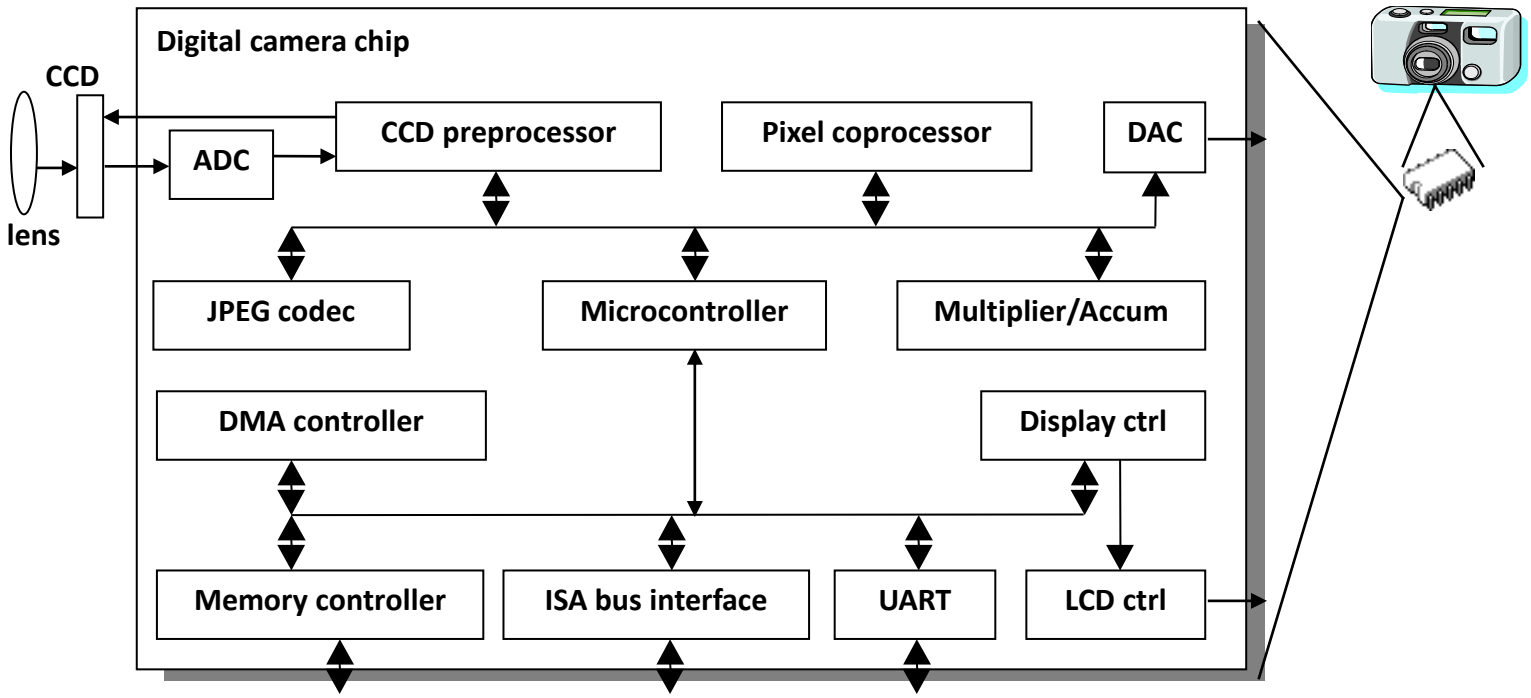
Automobiles



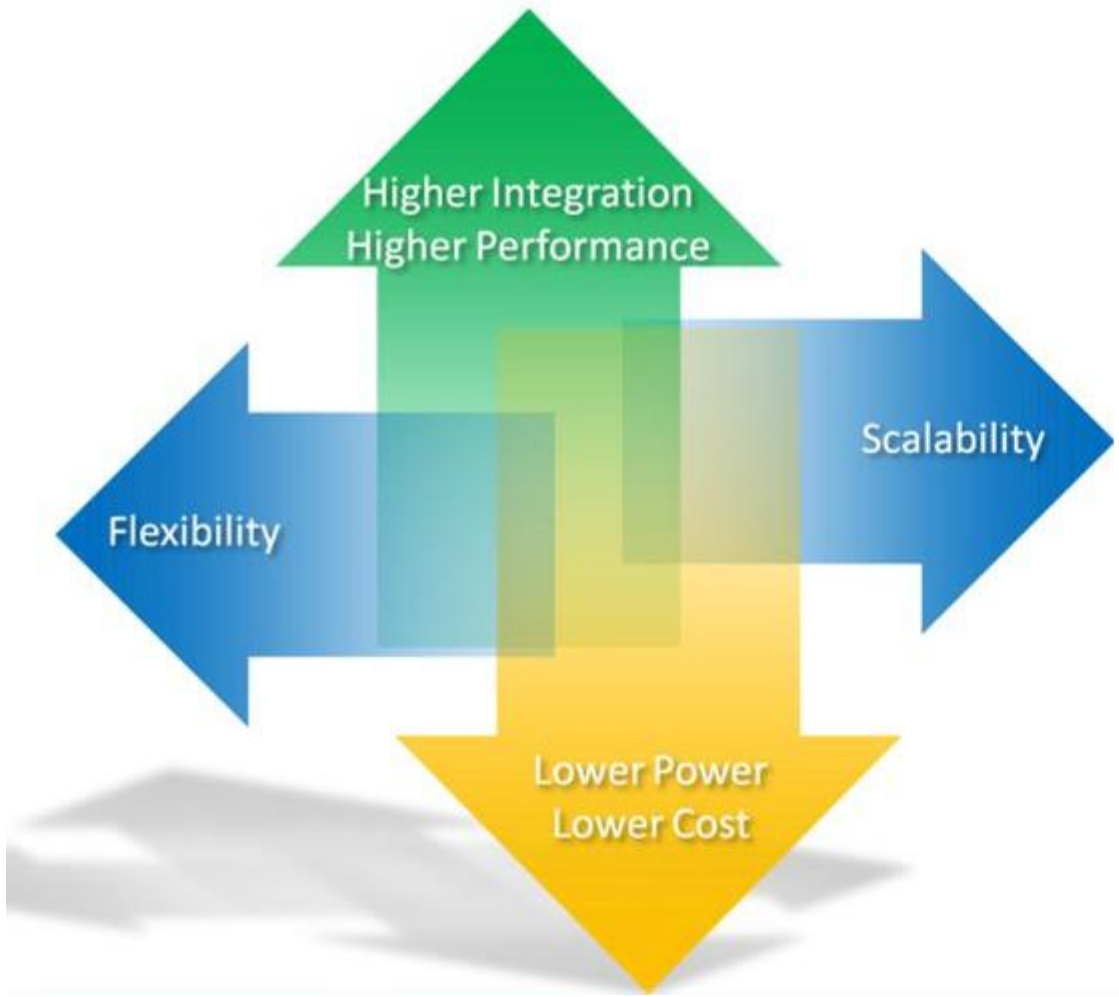
Sensors: Stereo-cameras, speedometer, accelerometers, signalling

2002: Opel Vectra has over 40 sensors (25 types)

Digital Camera

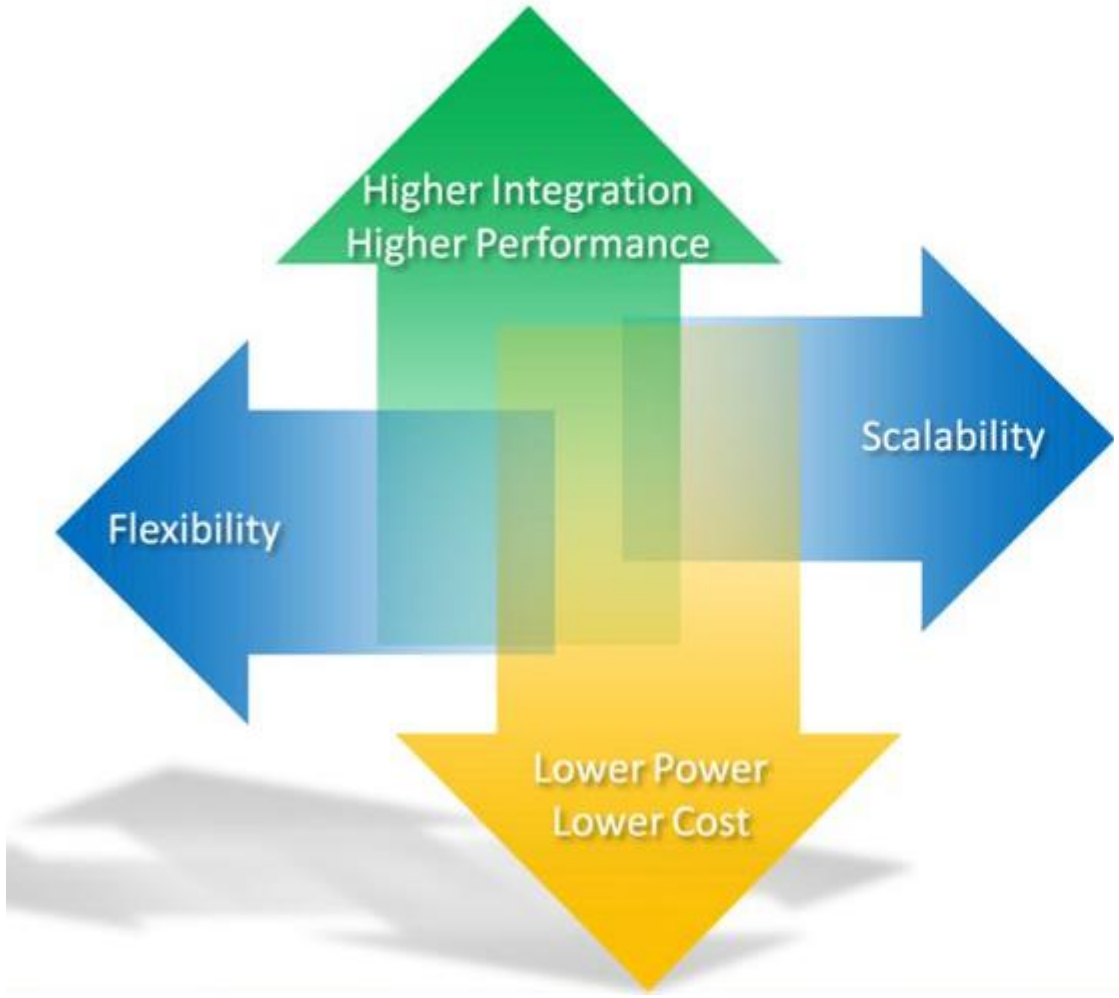


Demands of Today's Technology

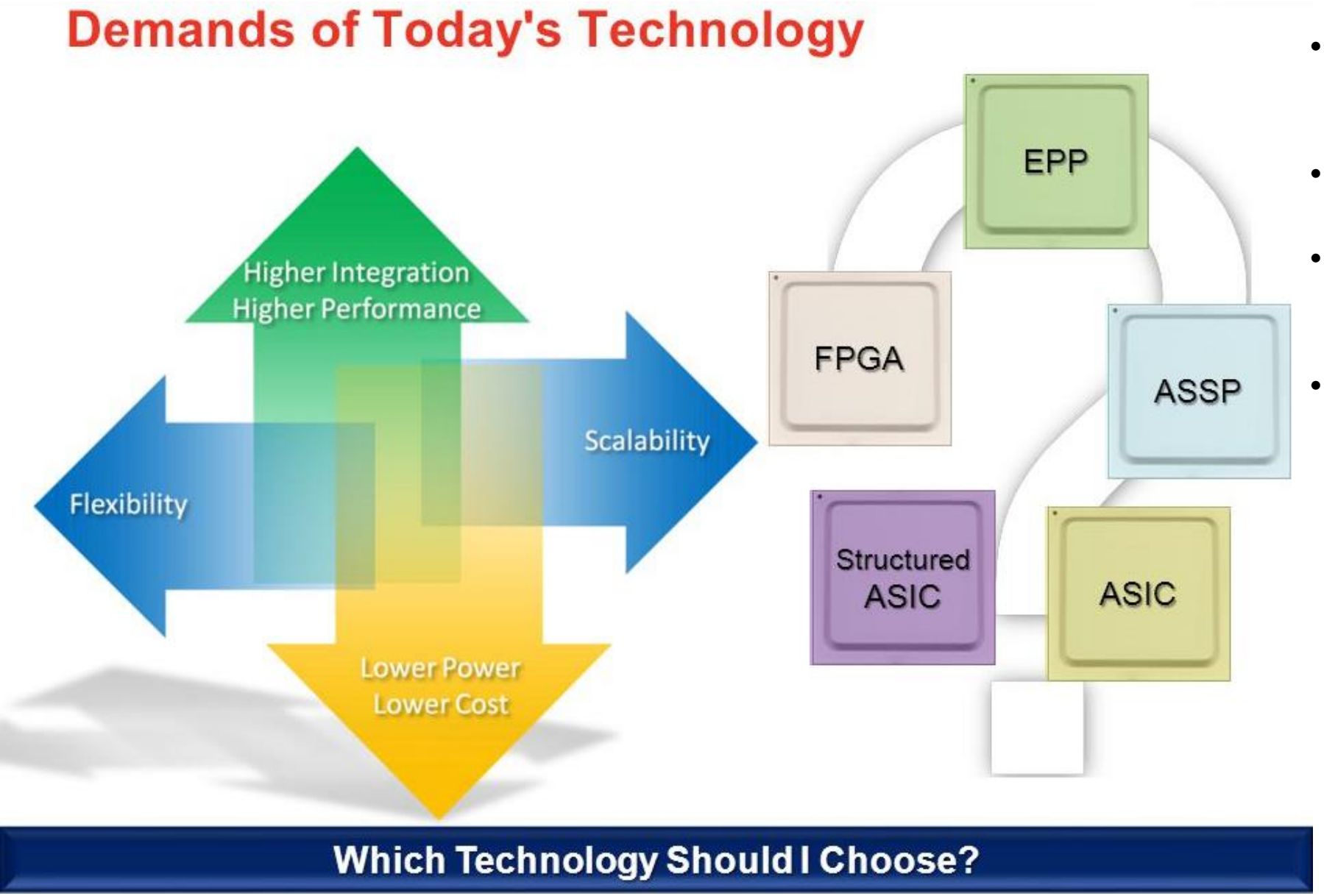


- Over the years, industries are facing the same challenges and pressure: *Next generation system must improve the **performance** and should offer higher level of **integration**.*
- Furthermore, the *cost and power should be reduced*.
- These challenges have been addressed till now efficiently.

Demands of Today's Technology



- However, there is additional requirements of *flexibility* and *scalability* in the upcoming applications in order to tune your design to meet customer requirements efficiently.
- Need of single platform that can be scaled from low-end to high-end



- **ASSP**: application specific system processor: Fixed function
- **ASIC**: Application specific integrated circuits: can not changed once build
- **FPGA:** Completely flexible but expensive (limited size)
- **SASIC:** Between ASIC and FPGA. But mask-programmable instead of field-programmable
- **EPP:** Extensible Processing Platform

ASIC Vs ASSP

	ASIC	ASSP
Performance	+	+
Power	+	+
Unit Cost	+	+
TCO	■	+

- TCO: Total cost of ownership
- Takes into account all the cost associated with development with such solution
- TCO is high for ASIC and depends on the how many units to be produced

+ positive, - negative, ■ neutral

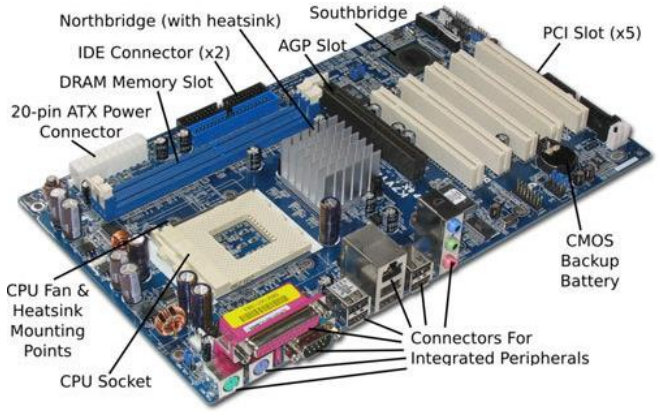
ASIC Vs ASSP

	ASIC	ASSP
Performance	+	+
Power	+	+
Unit Cost	+	+
TCO	■	+
Risk	-	+
TTM	-	+
Flexibility	-	-
Scalability	-	■

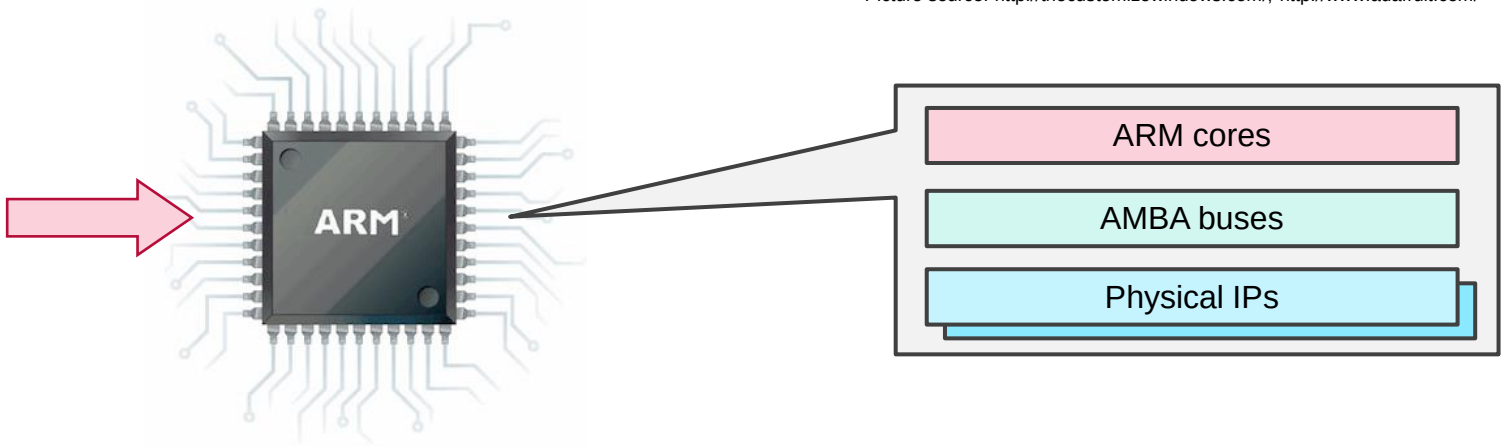
+ positive, - negative, ■ neutral

What is a System-on-Chip

Picture source: http://thecustomizewindows.com/, http://www.adafruit.com/



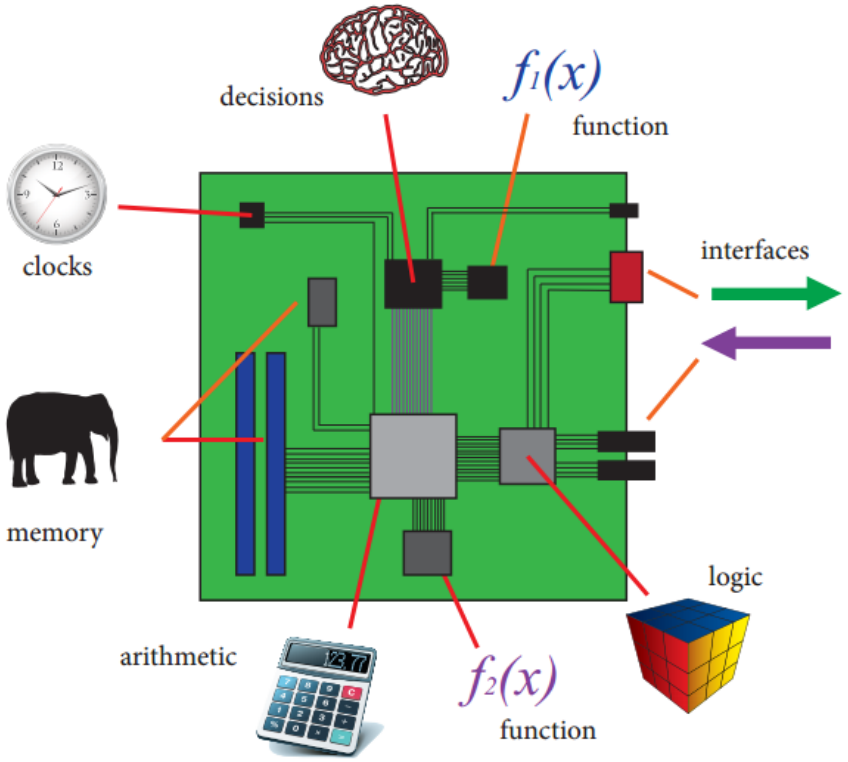
Mother board of a PC

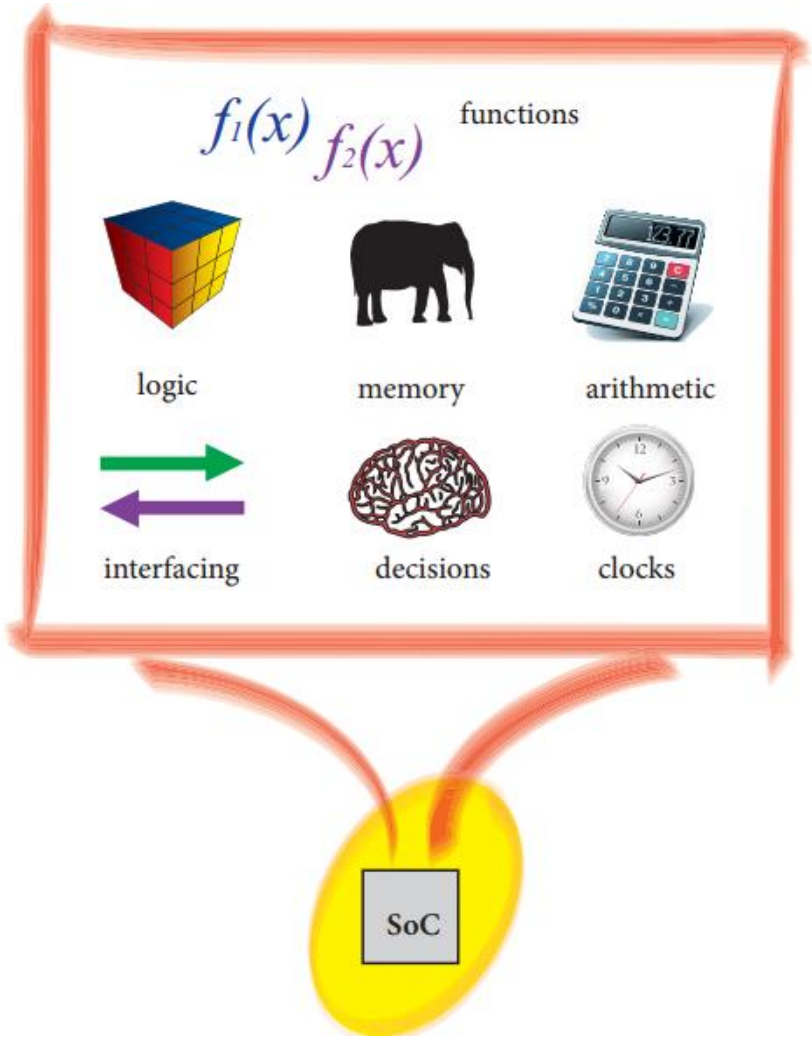


System on a Chip

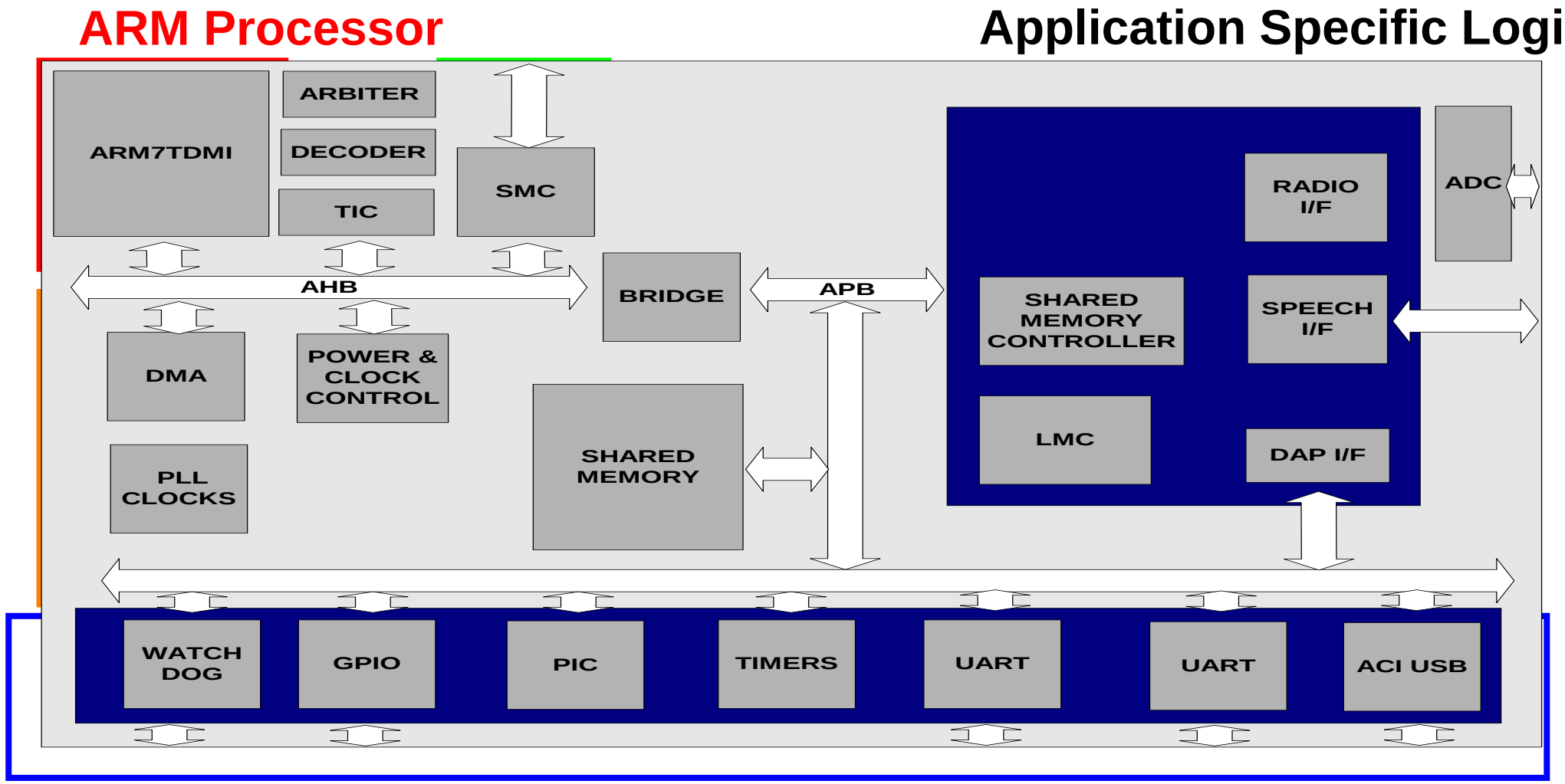
SoC is a single silicon chip that can be used to implement the functionality of an entire system, rather than using several different physical chips on a board.

System on-a-board and System-on-chip





Bluetooth SoC



Picture source: http://www.ecs.soton.ac.uk/, SoC Advance design Technique

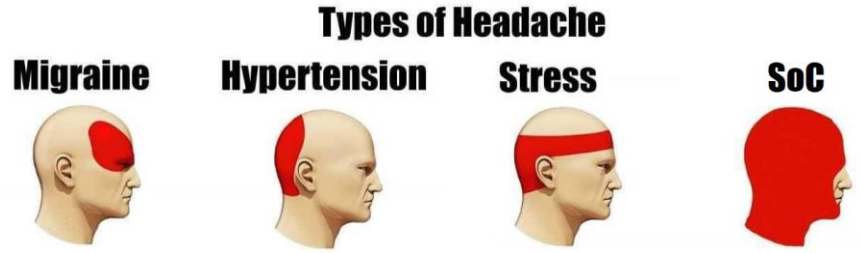
Advantages of SoC

- **Higher performance benefiting from:**
  - Less propagation delay since internal wires are shorter.
  - Less gate delay as internal transistors have lower electrical impedance.
- **Power efficiency benefiting from:**
  - Lower voltage required (typically < 2.0 volts) compared with external chip voltage (typically >3.0 volts).
  - Less capacitance.
- **Lighter footprint:**
  - Device size and weight is reduced.
- **Higher reliability:**
  - All encapsulated in a single chip package, less interference from the external world.
- **Low cost:**
  - The cost per unit is reduced since a single chip design can be fabricated in a large volumes.

Credits: ARM Univ. Prog.

Limitations of SoC

- **Less flexibility**
  - Unlike a PC or a laptop, which allows you to upgrade a single component, such as RAM or graphic card, a SoC cannot be easily upgraded after manufacture. Though external components can be added, it is no longer SoC
- **Application Specific**
  - Most SoCs are created for particular applications thus they are not easily adapted to other applications.
- **Complexity**
  - A SoC design usually requires advanced skills compared with board-level development.

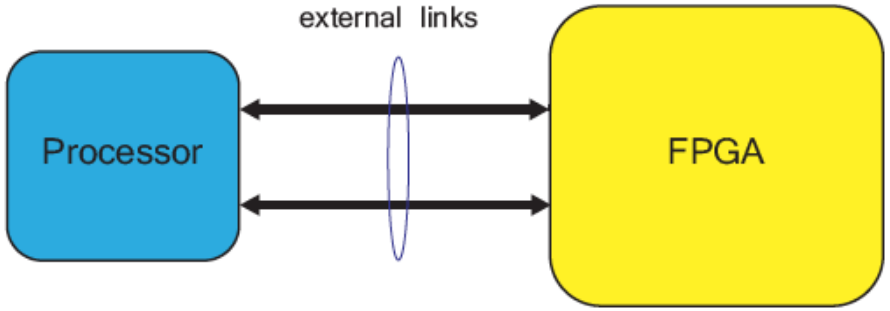


Credits: ARM Univ. Prog.

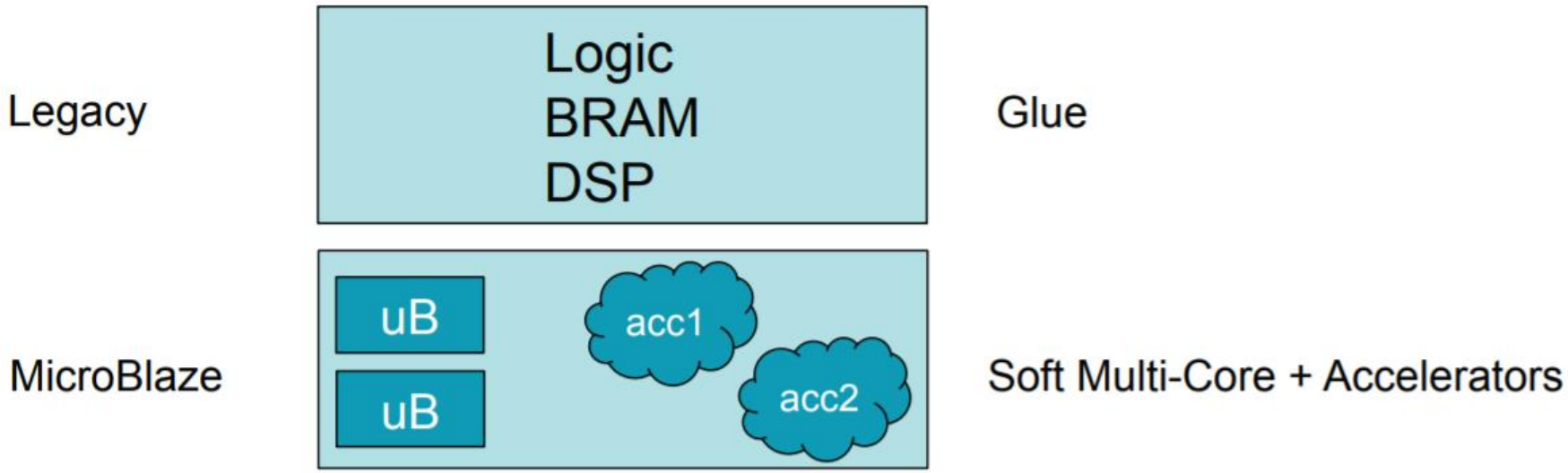
ASIC Vs ASSP Vs 2 Chip Solution

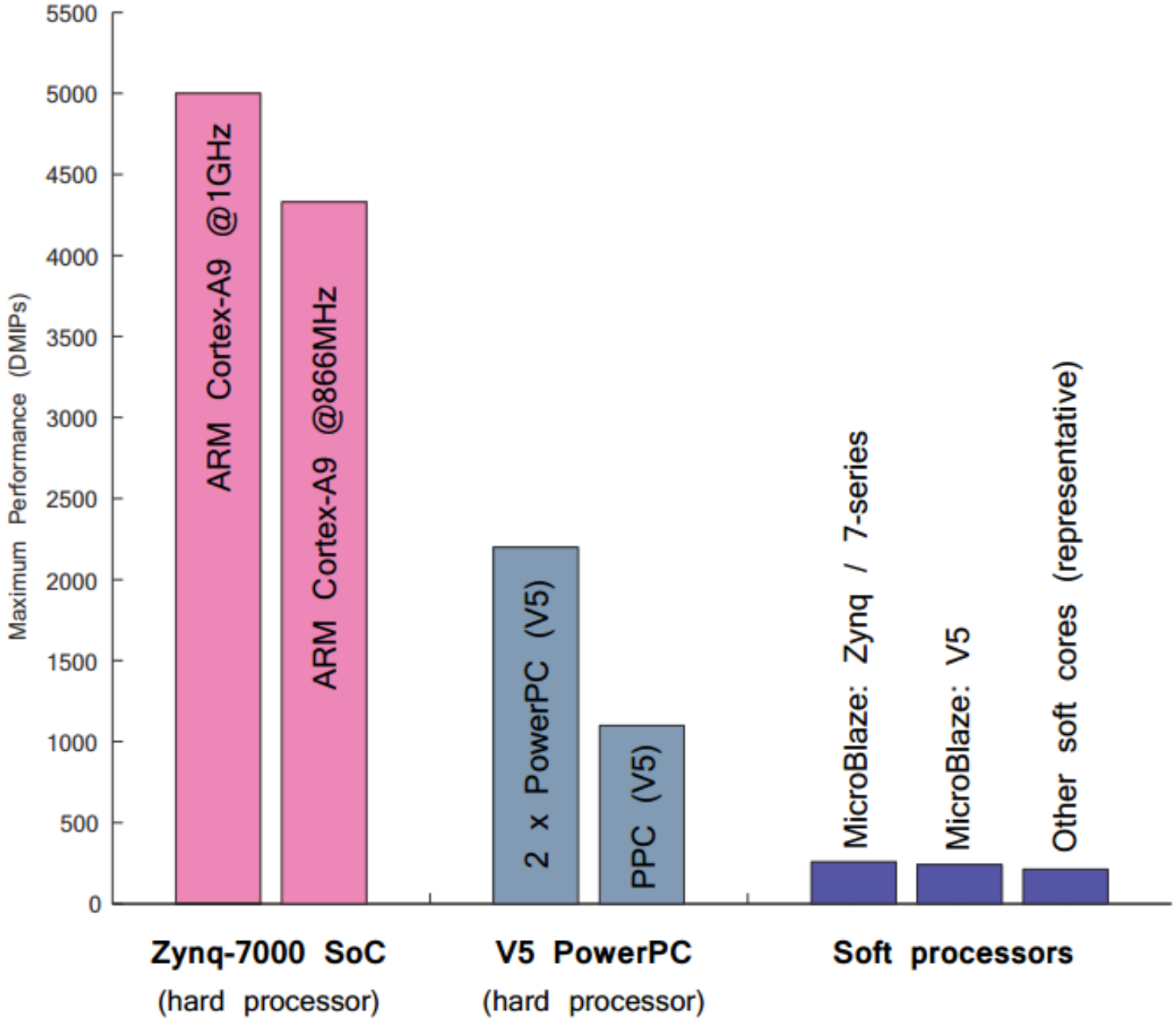
	ASIC	ASSP	2 Chip Solution
Performance	+	+	■
Power	+	+	-
Unit Cost	+	+	-
TCO	■	+	+
Risk	-	+	+
TTM	-	+	+
Flexibility	-	-	+
Scalability	-	■	+

+ positive, - negative, ■ neutral

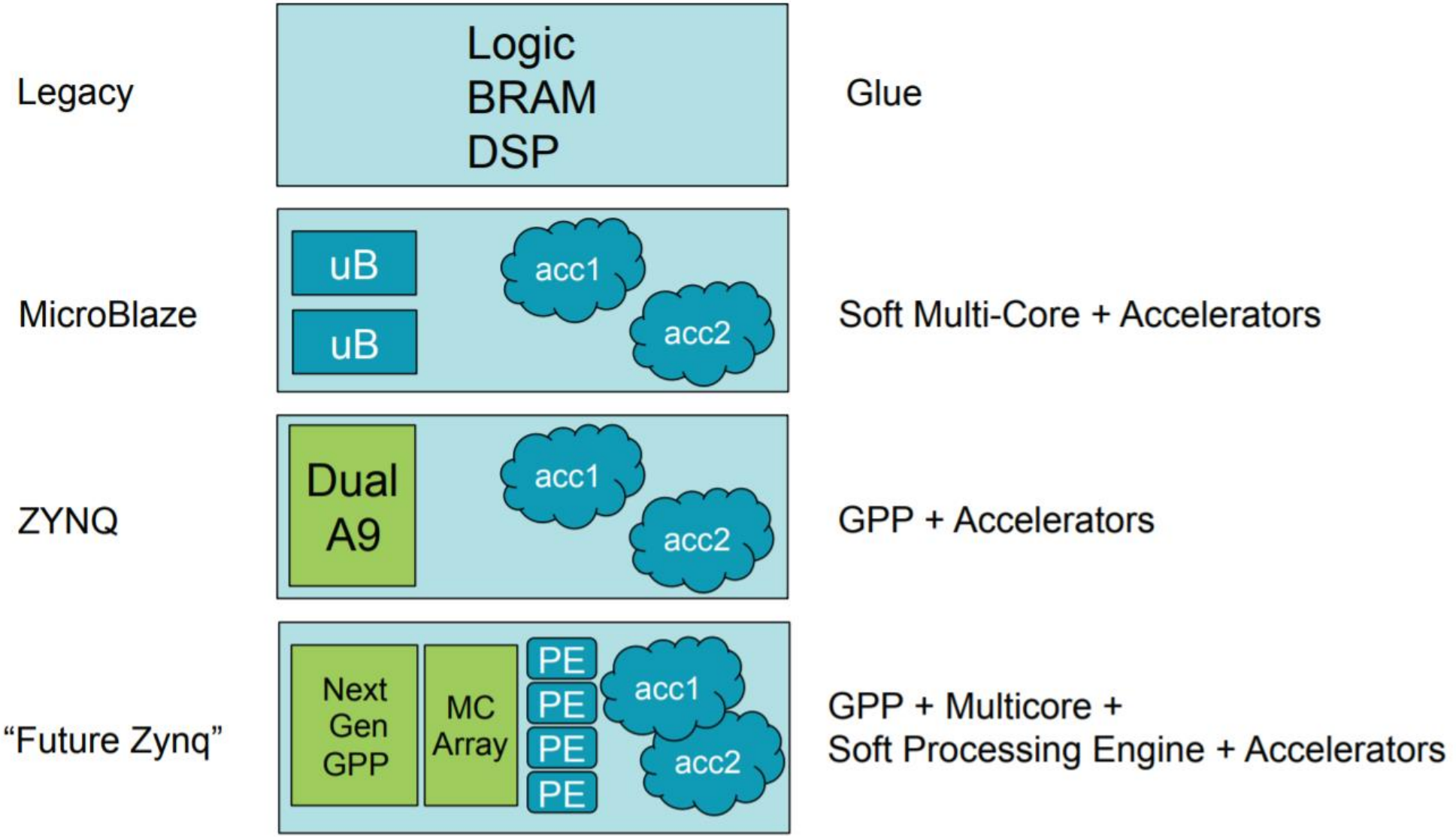


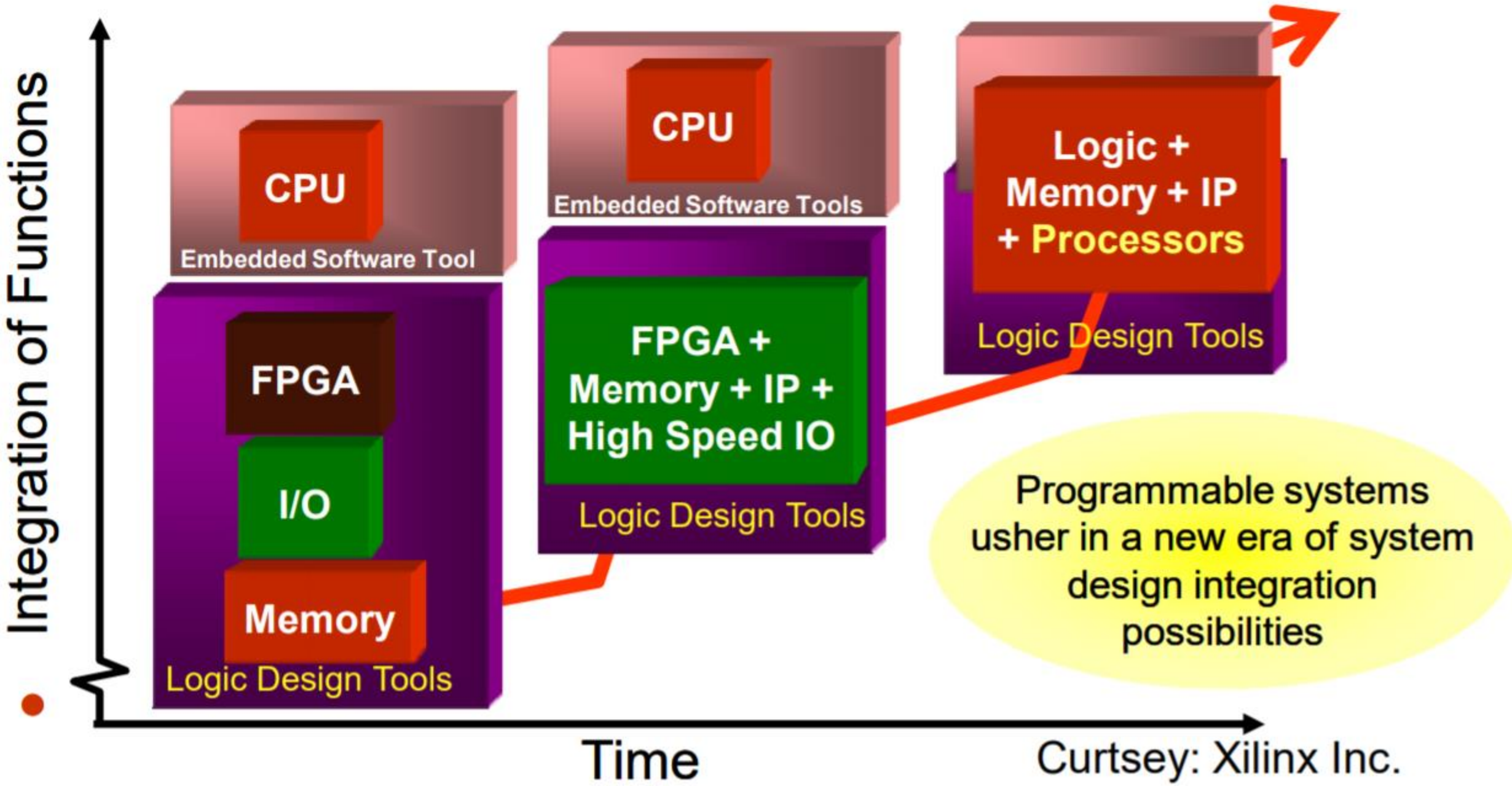
Zynq EPP


Legacy
Logic
BRAM
DSP
Glue
MicroBlaze
uB
uB
acc1
acc2
Soft Multi-Core + Accelerators

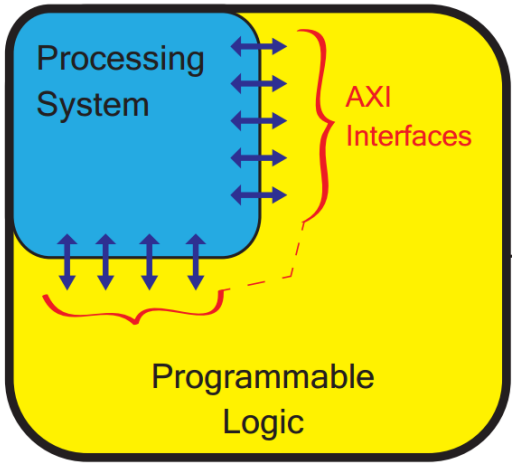

Maximum Performance (DMIPs)
5500
5000
4500
4000
3500
3000
2500
2000
1500
1000
500
0
ARM Cortex-A9 @1GHz
ARM Cortex-A9 @866MHz
2 x PowerPC (V5)
PPC (V5)
MicroBlaze: Zynq / 7-series
MicroBlaze: V5
Other soft cores (representative)
Zynq-7000 SoC
(hard processor)
V5 PowerPC
(hard processor)
Soft processors

Zynq EPP


Legacy
Logic
BRAM
DSP
Glue
MicroBlaze
uB
uB
acc1
acc2
Soft Multi-Core + Accelerators
ZYNQ
Dual
A9
acc1
acc2
GPP + Accelerators
"Future Zynq"
Next
Gen
GPP
MC
Array
PE
PE
PE
PE
acc1
acc2
GPP + Multicore +
Soft Processing Engine + Accelerators


Integration of Functions
CPU
Embedded Software Tool
FPGA
I/O
Memory
Logic Design Tools
CPU
Embedded Software Tools
FPGA +
Memory + IP +
High Speed IO
Logic Design Tools
Logic +
Memory + IP
+ Processors
Logic Design Tools
Programmable systems
usher in a new era of system
design integration
possibilities
Time
Curtsey: Xilinx Inc.

Zynq EPP



	ASIC	ASSP	2 Chip Solution	Zynq-7000
Performance	+	+	■	+
Power	+	+	-	+
Unit Cost	+	+	-	■
TCO	■	+	+	+
Risk	-	+	+	+
TTM	-	+	+	+
Flexibility	-	-	+	+
Scalability	-	■	+	+

+ positive, - negative, ■ neutral