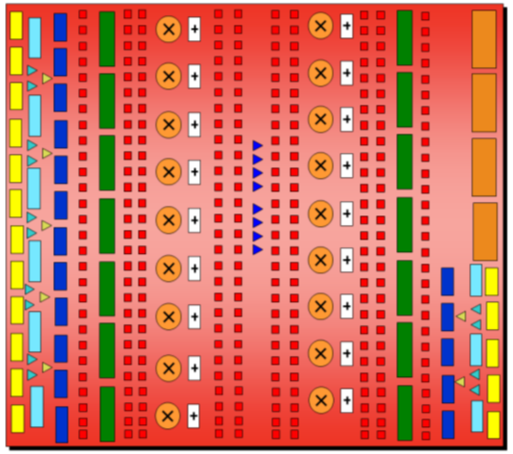
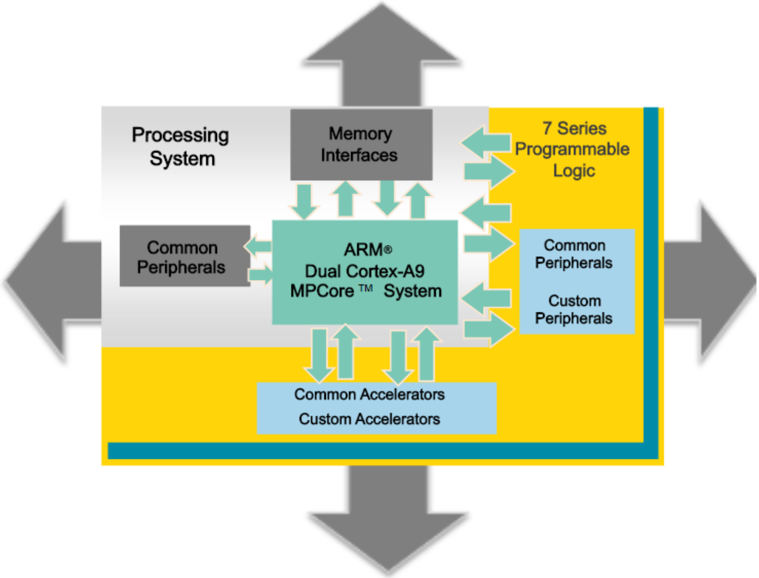
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

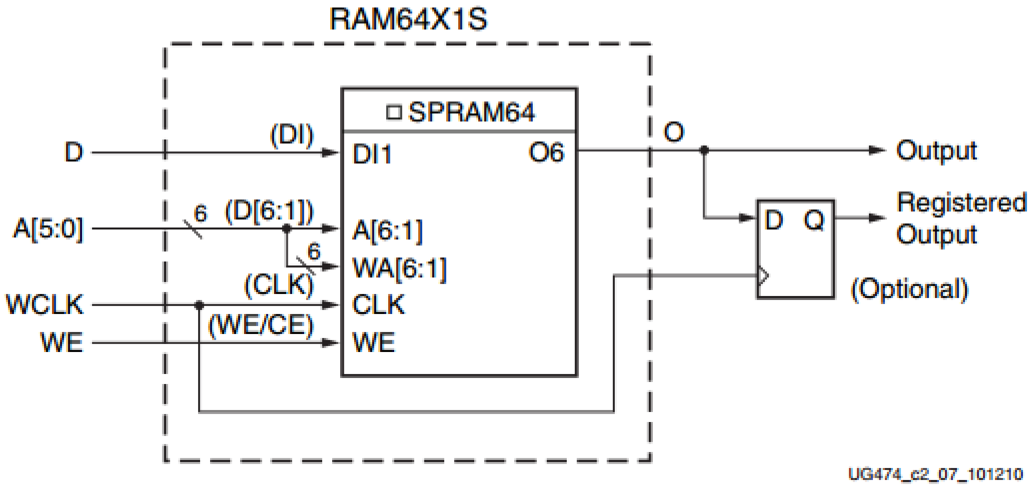
A2A
Algorithms to Architecture

ECE 270: Embedded Logic Design

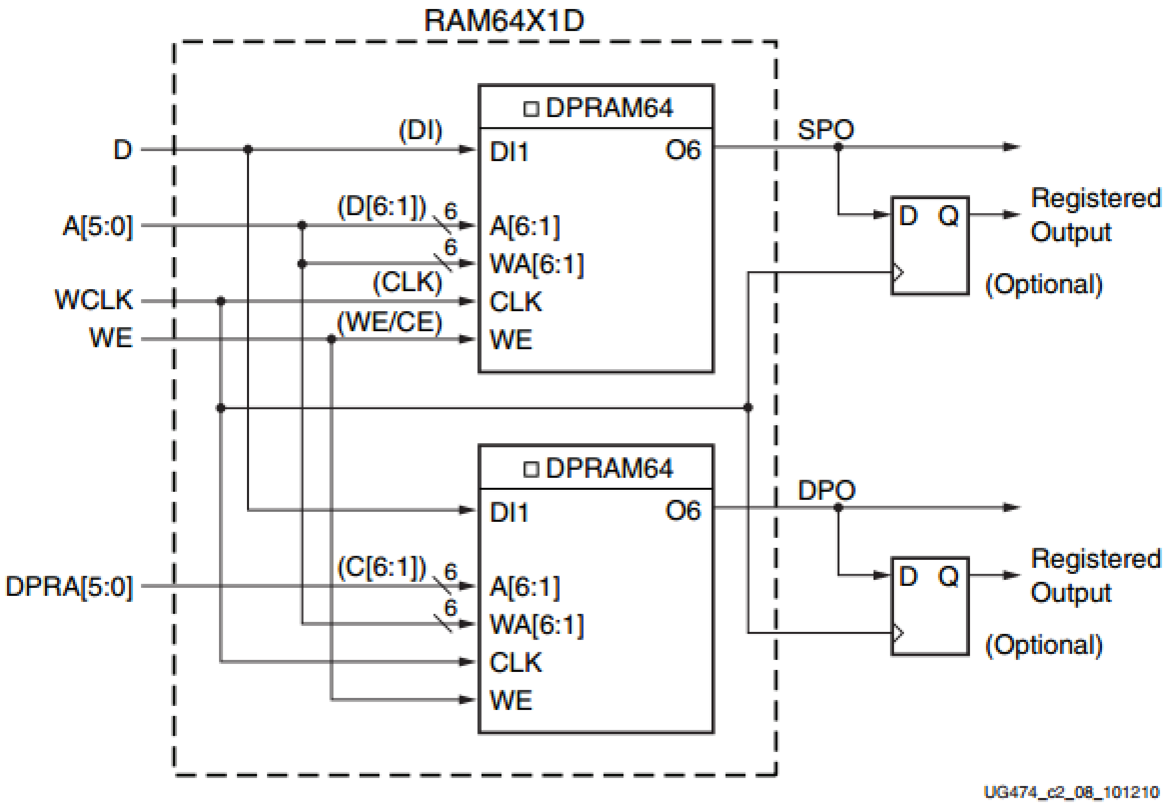




LUT as Memory: 64X1 Dual Port

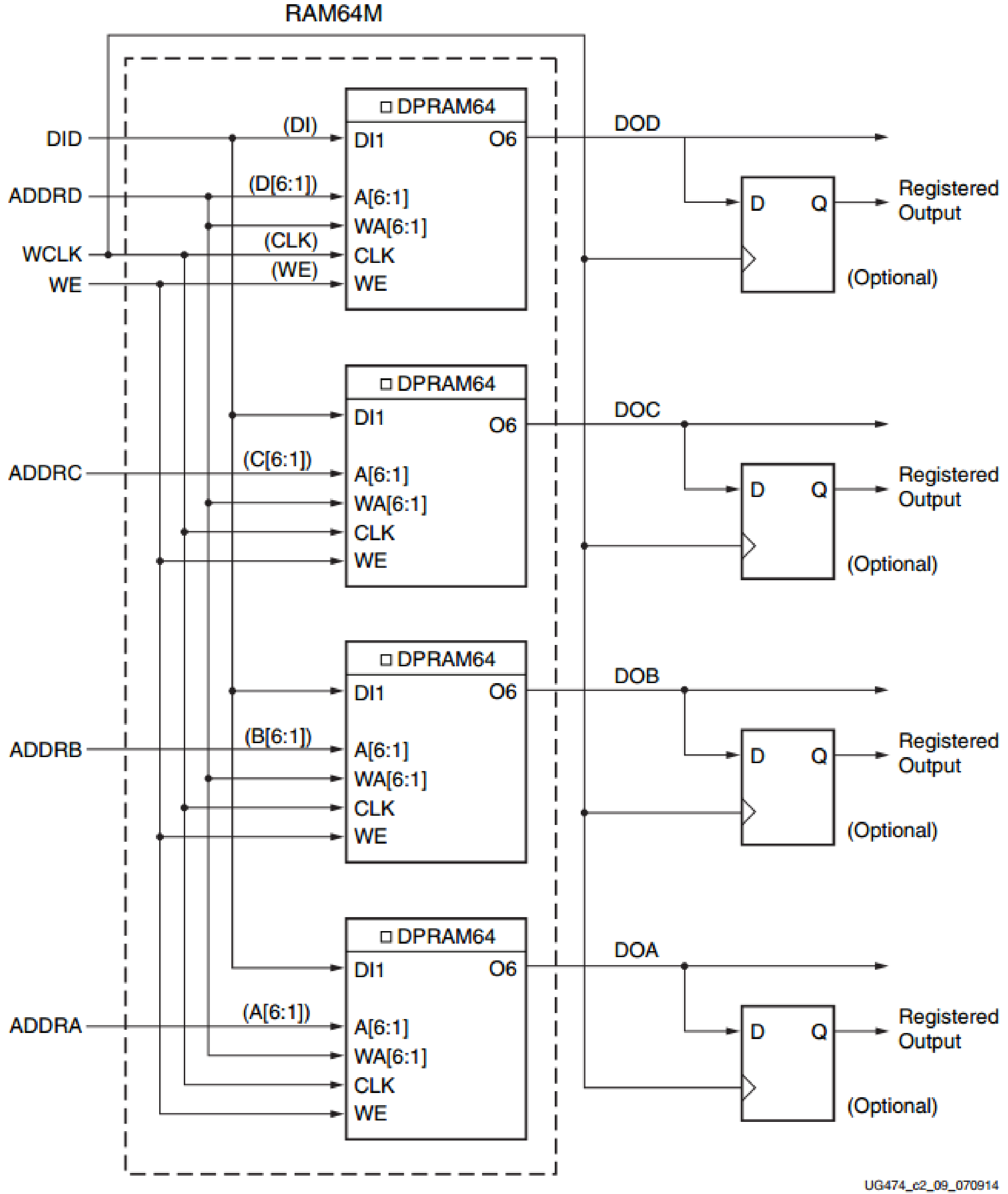


64 X 1 Single Port Distributed RAM (RAM64X1S)



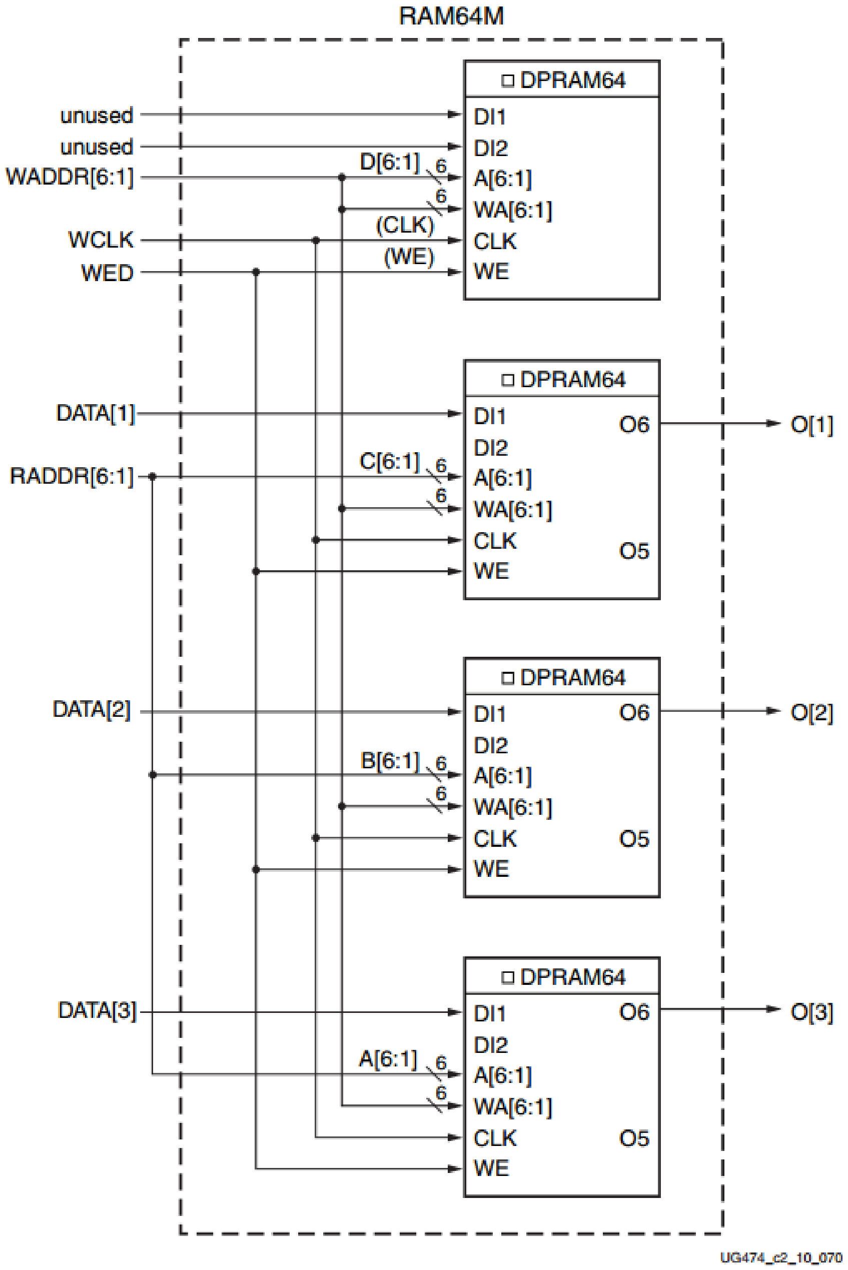
64 X 1 Dual Port Distributed RAM (RAM64X1D)

LUT as Memory: 64X1 Quad Port



64 X 1 Quad Port Distributed RAM (RAM64M)

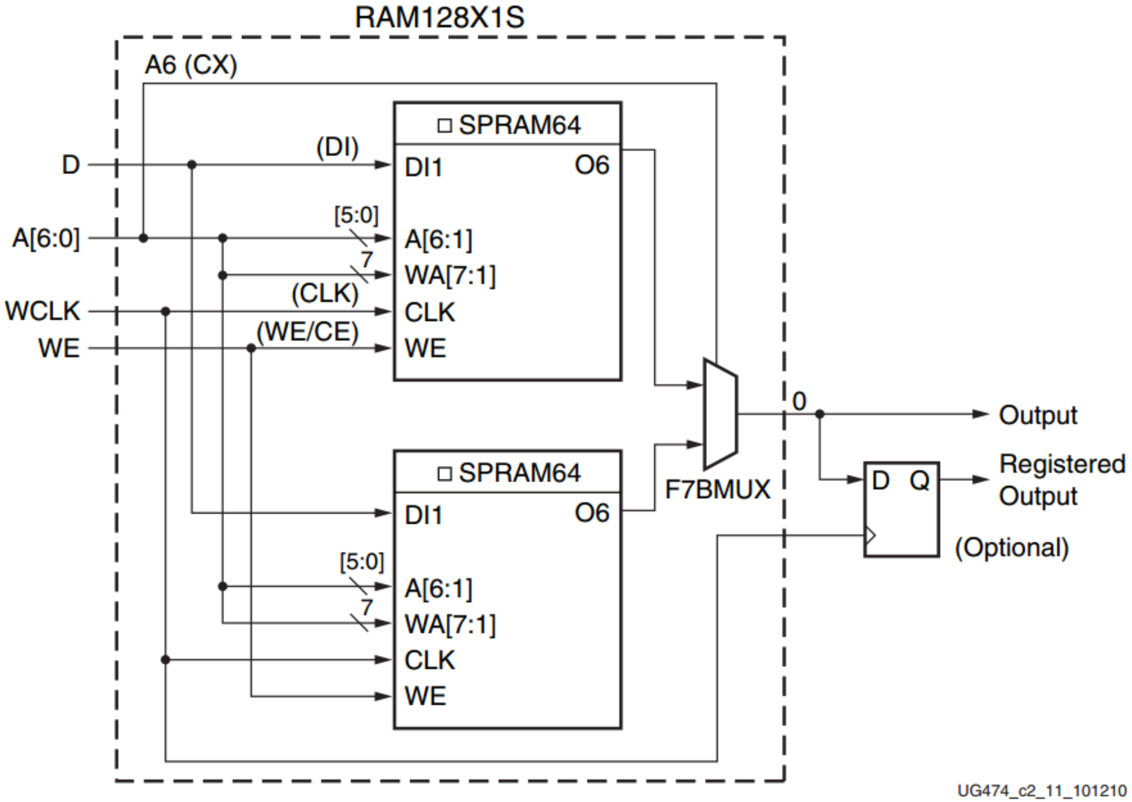
LUT as Memory:
64X3 Simple Dual Port



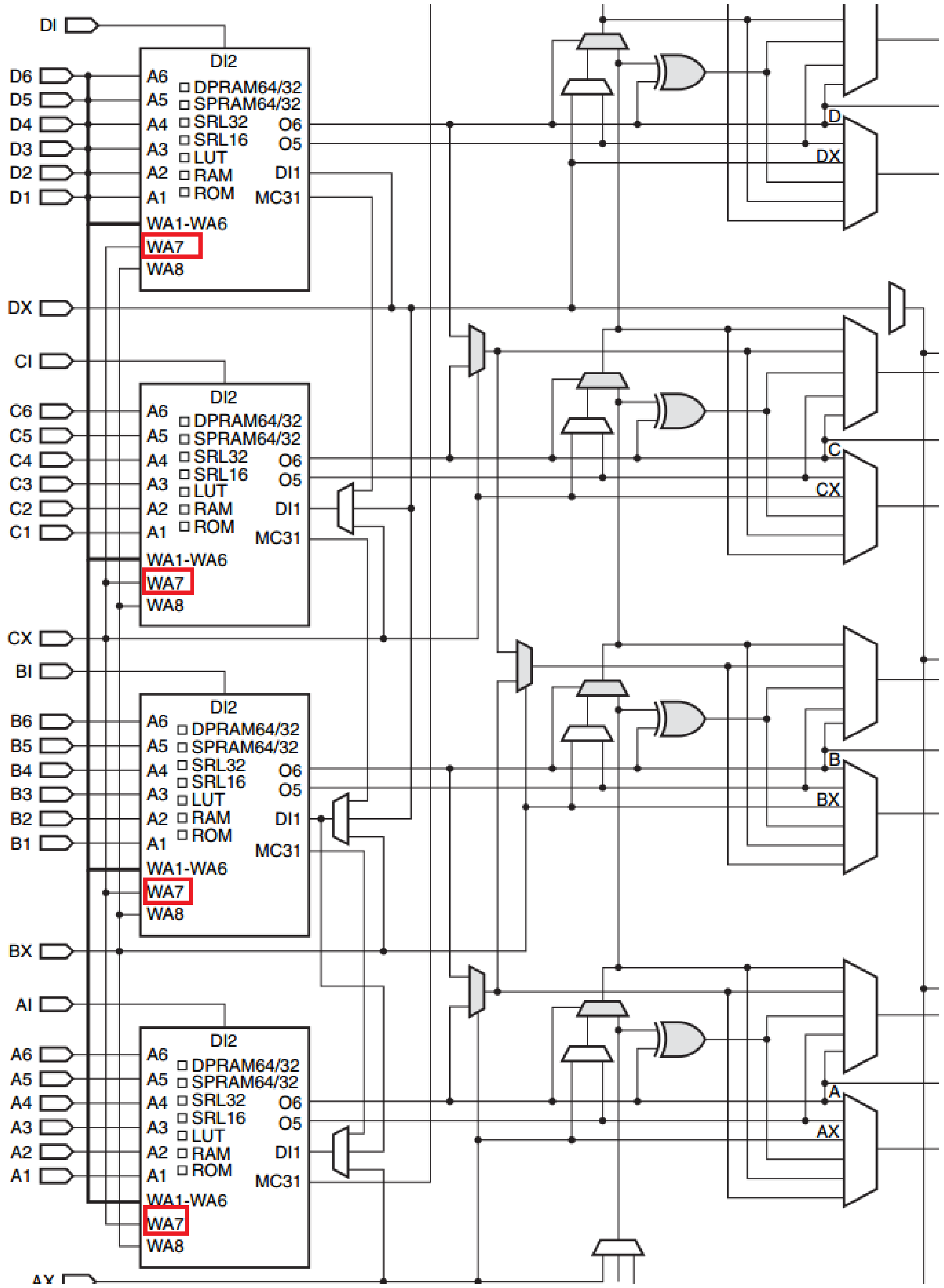
64 X 3 Simple Dual Port Distributed RAM (RAM64I

LUT as Memory: 128X1 Single Port

- Implementation of distributed RAM configurations with depth greater than 64 requires the usage of wide-function multiplexers (F7AMUX, F7BMUX, and F8MUX)
- One SLICEM can have TWO single port 128 x 1-bit memories as long as they share the same clock, write enable, and shared read and write port address inputs
- This configuration equates to a 128 x 2-bit single-port distributed RAM.

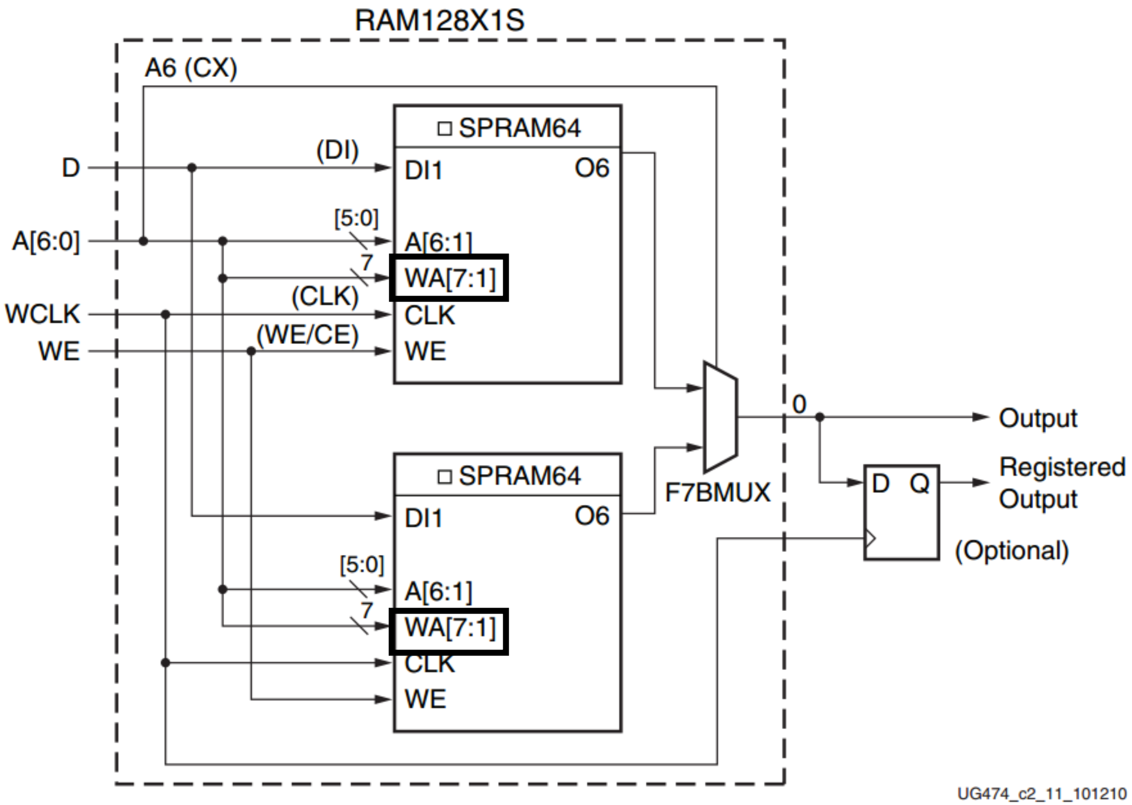


128 X 1 Single Port Distributed RAM (RAM128X1S)



WA7: Enable for 7-input LUT

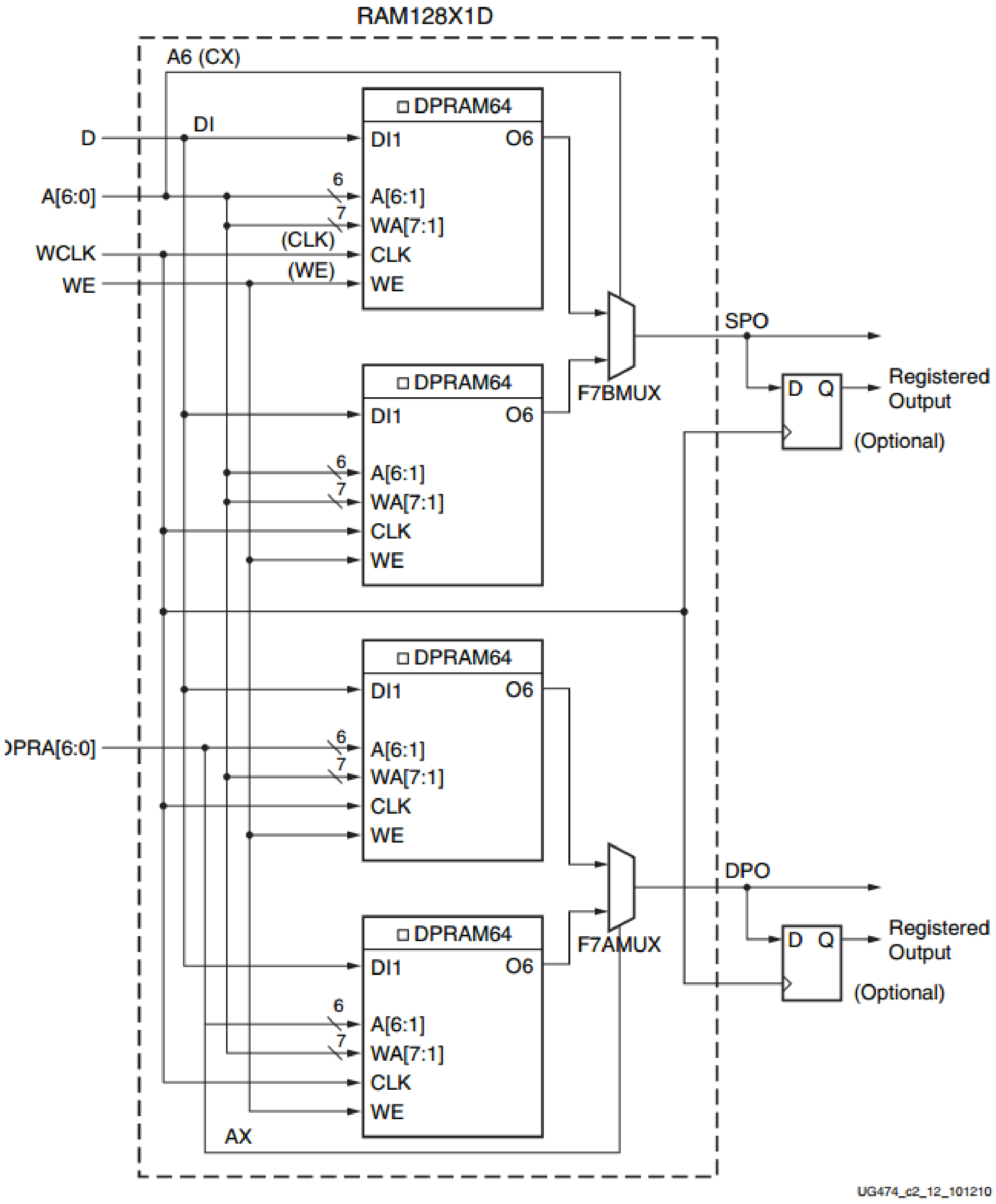
WA8: Enable for 8-input LUT



128 X 1 Single Port Distributed RAM (RAM128X1S)

LUT as Memory: 128X1 Dual Port

- 128X1 Quad Port?
- 128X2 Dual Port?



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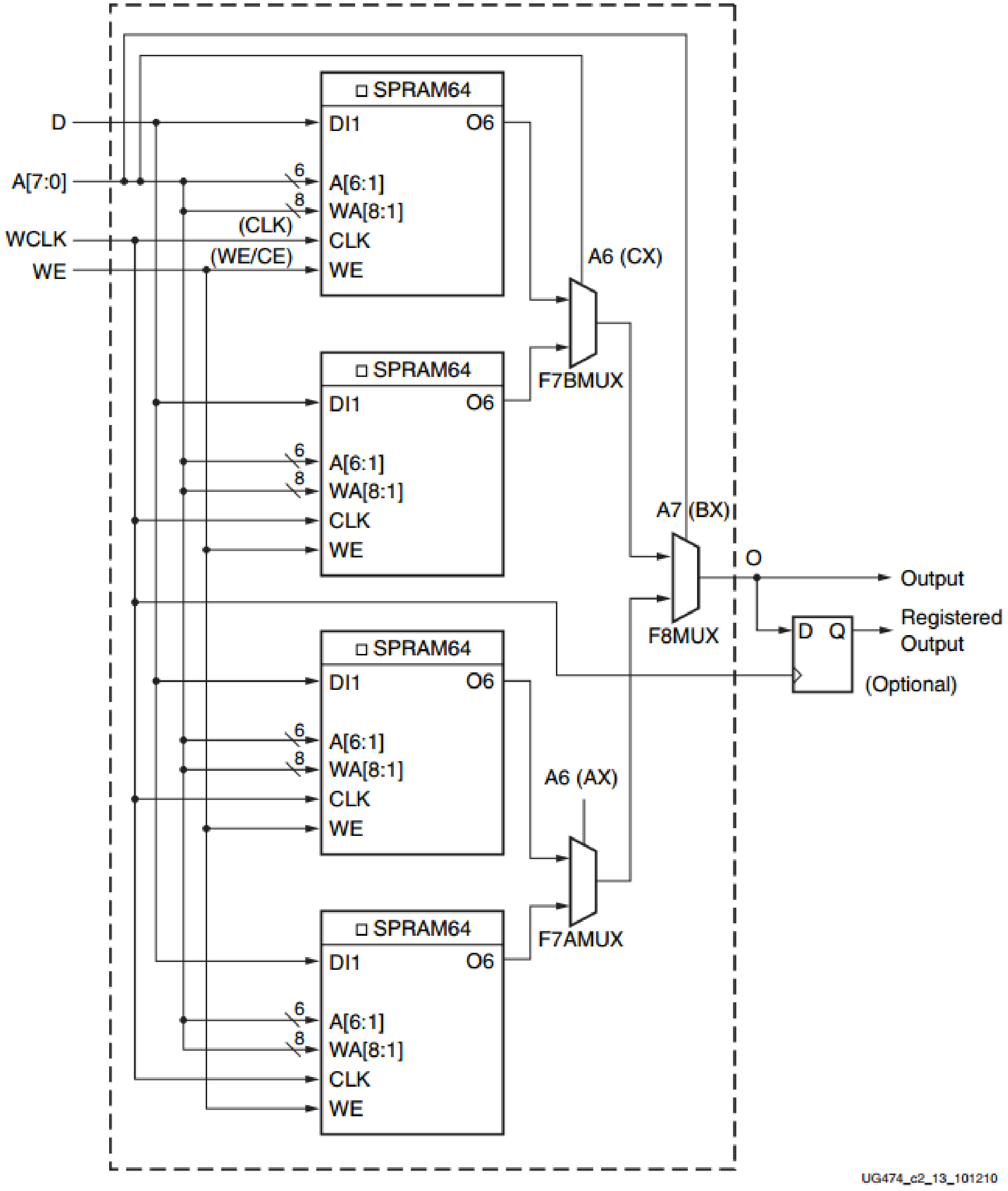
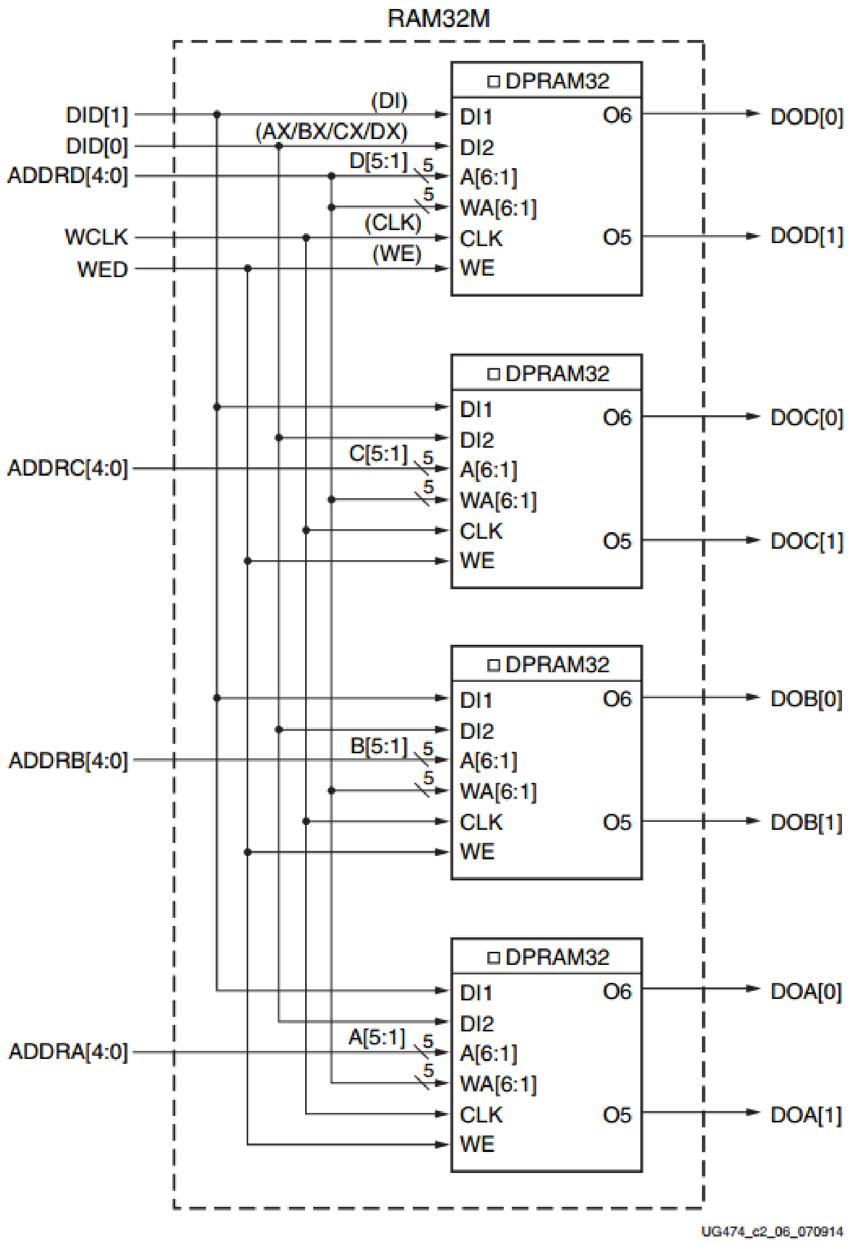
128 X 1 Dual Port Distributed RAM (RAM128X1D)

LUT as Memory: 256X1 Single Port



256 X 1 Single Port Distributed RAM (RAM256X1S)

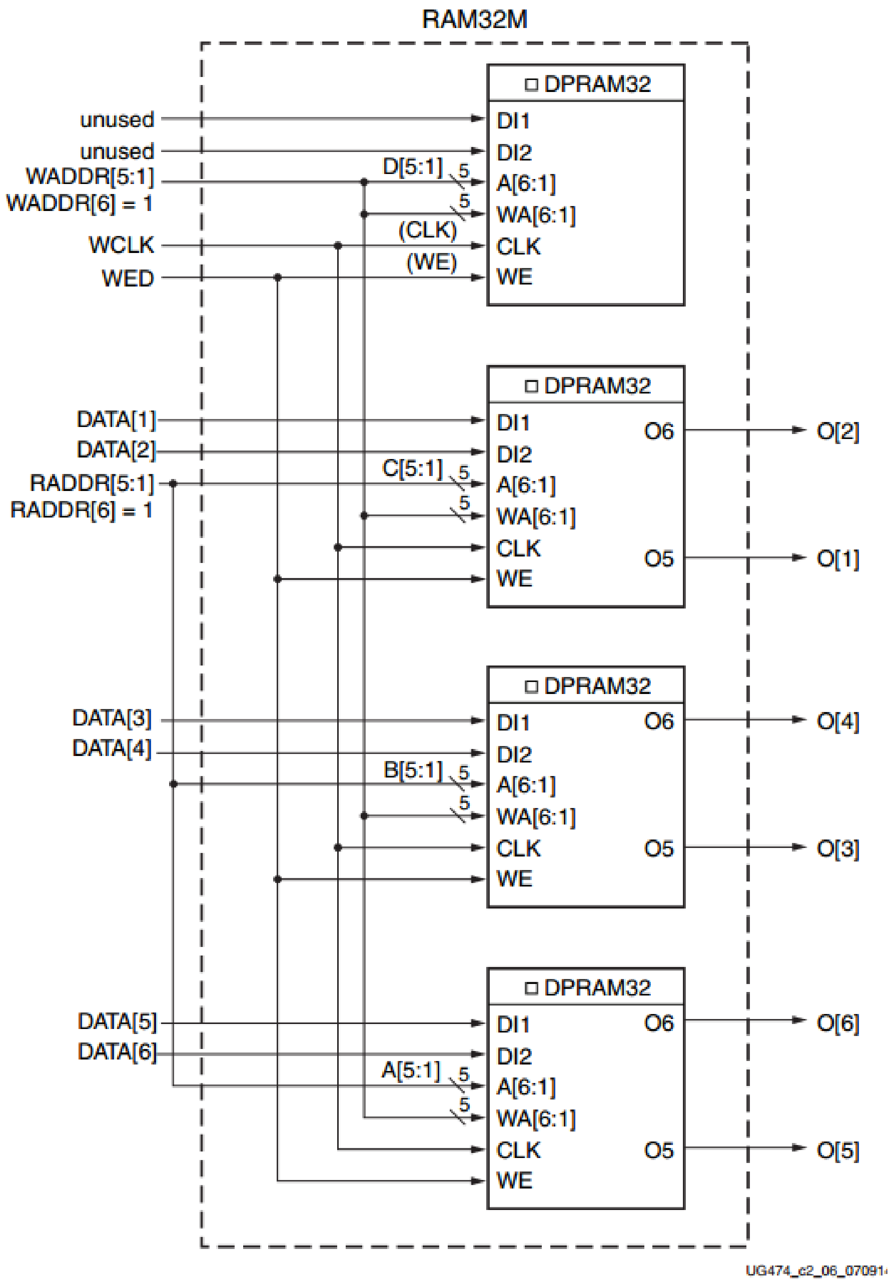
LUT as Memory: 32X2 Quad Port



32 X 2 Quad Port Distributed RAM (RAM32M)

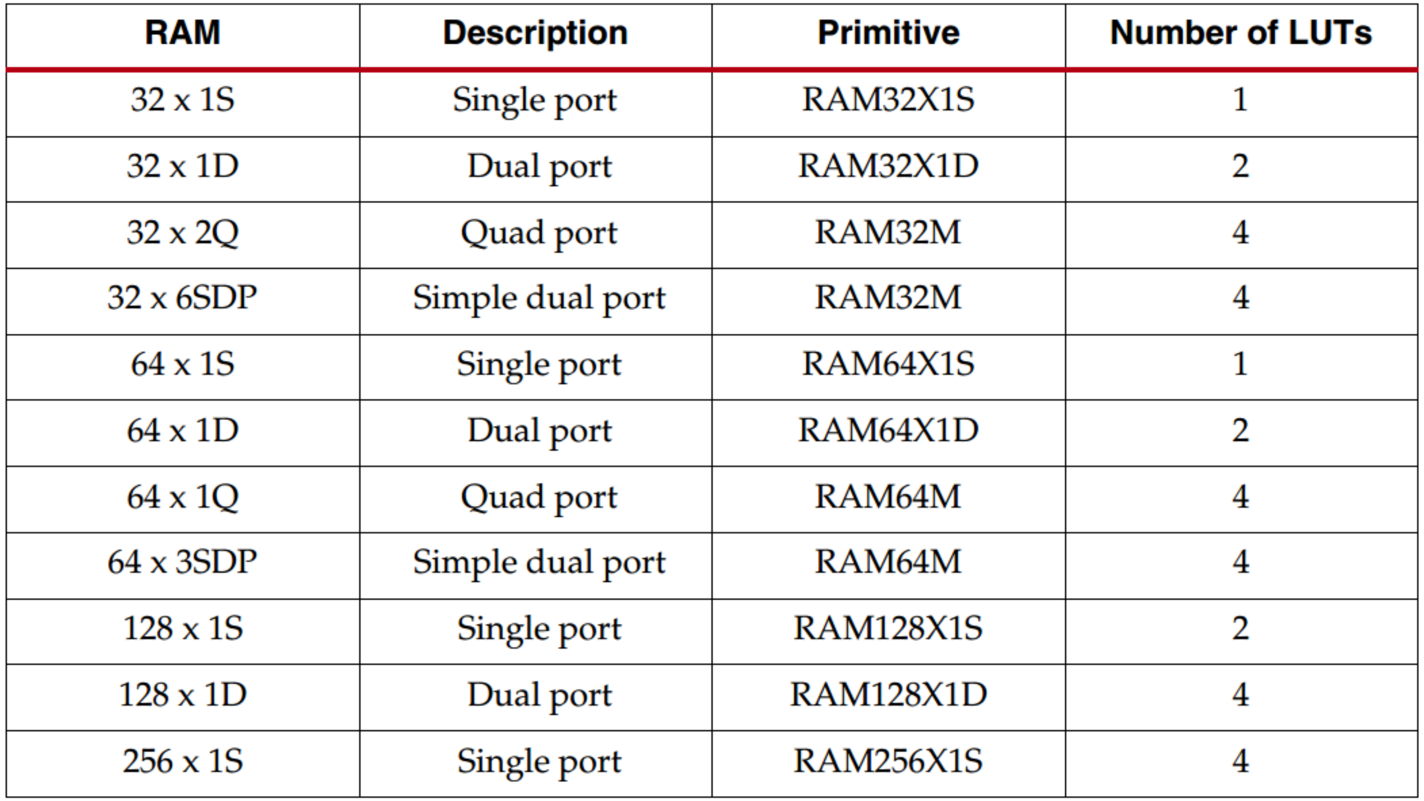
LUT as Memory:
32X8 Simple Dual Port

LUT as Memory: 32X6 Simple Dual Port

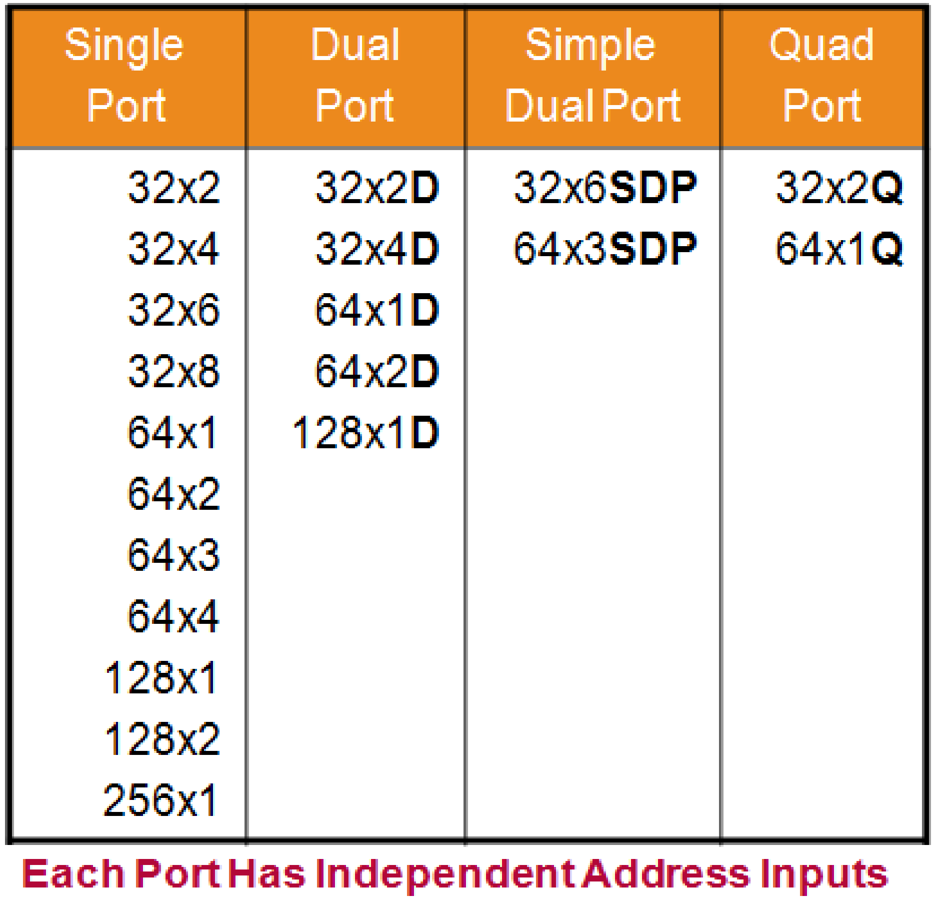


32 X 6 Simple Dual Port Distributed RAM (RAM32M)

LUT as Memory



RAM	Description	Primitive	Number of LUTs
32 x 1S	Single port	RAM32X1S	1
32 x 1D	Dual port	RAM32X1D	2
32 x 2Q	Quad port	RAM32M	4
32 x 6SDP	Simple dual port	RAM32M	4
64 x 1S	Single port	RAM64X1S	1
64 x 1D	Dual port	RAM64X1D	2
64 x 1Q	Quad port	RAM64M	4
64 x 3SDP	Simple dual port	RAM64M	4
128 x 1S	Single port	RAM128X1S	2
128 x 1D	Dual port	RAM128X1D	4
256 x 1S	Single port	RAM256X1S	4



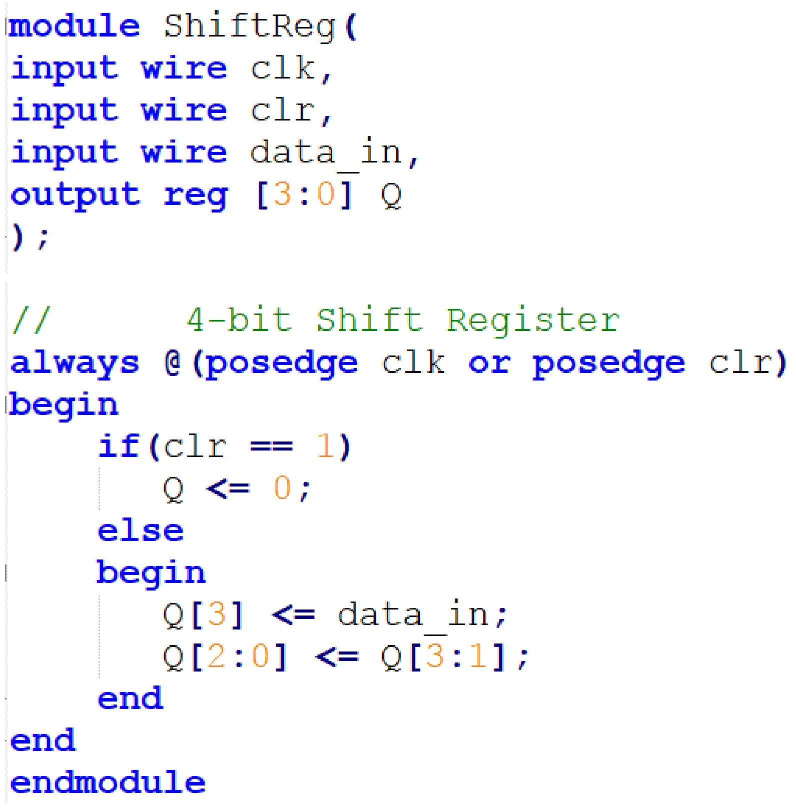
Single Port	Dual Port	Simple Dual Port	Quad Port
32x2	32x2**D**	32x6**SDP**	32x2**Q**
32x4	32x4**D**	64x3**SDP**	64x1**Q**
32x6	64x1**D**		
32x8	64x2**D**		
64x1	128x1**D**		
64x2			
64x3			
64x4			
128x1			
128x2			
256x1			

Each Port Has Independent Address Inputs

LUT as SRL

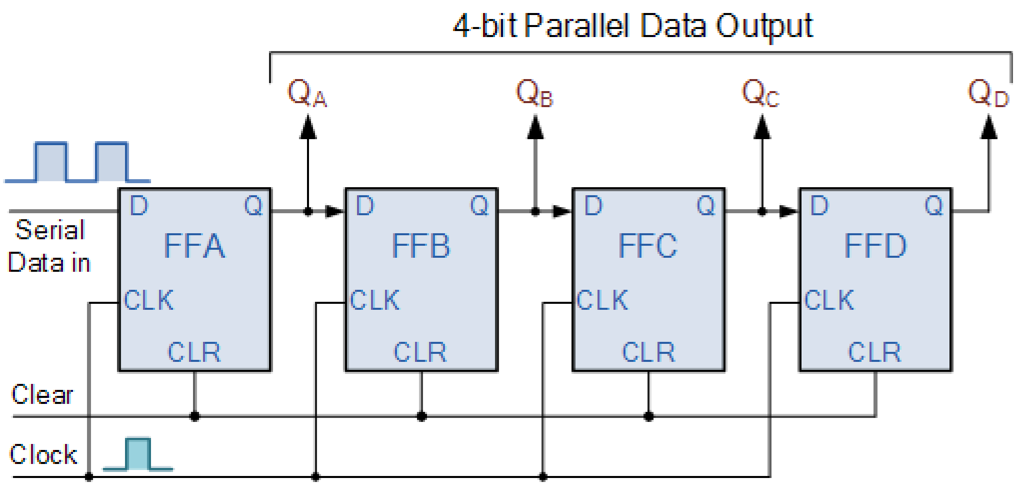
Sequential Circuits

- 4-bit serial shift register:



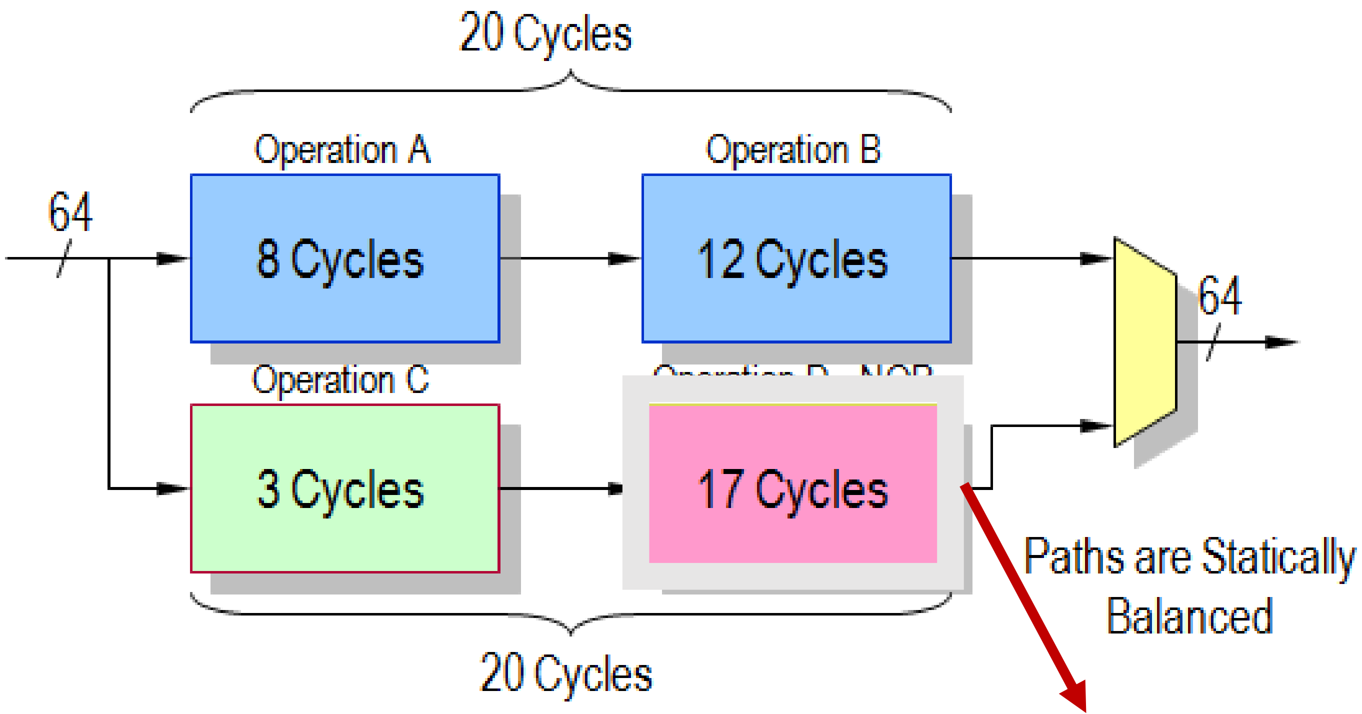
```
module ShiftReg(
input wire clk,
input wire clr,
input wire data_in,
output reg [3:0] Q
);

//       4-bit Shift Register
always @(posedge clk or posedge clr)
begin
    if(clr == 1)
        Q <= 0;
    else
    begin
        Q[3] <= data_in;
        Q[2:0] <= Q[3:1];
    end
end
endmodule
```



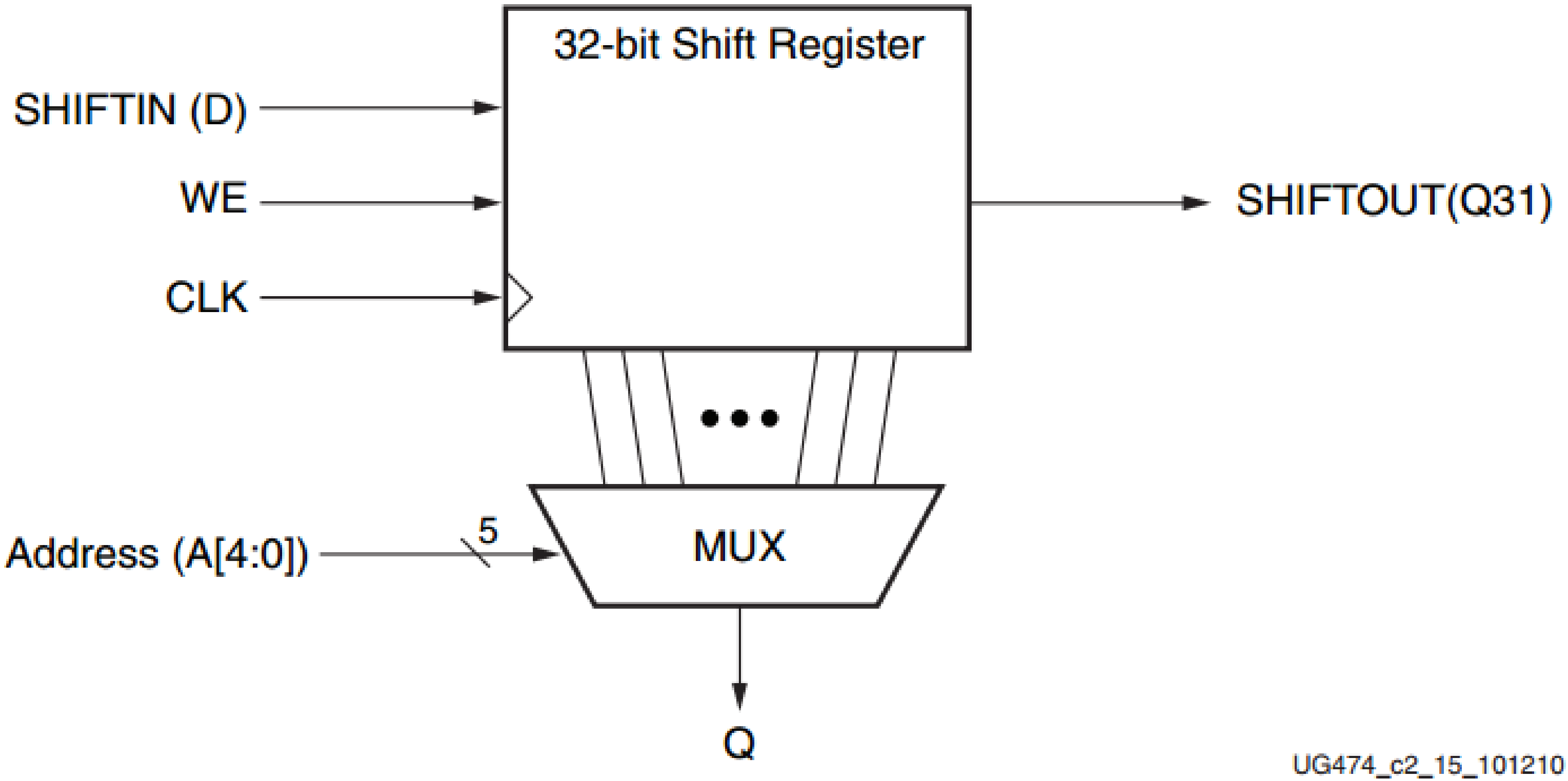
Shift Register Using FFs

- Operation D - NOP must add 17 pipeline stages of 64 bits each
  - 1,088 flip-flops (hence 136 slices)

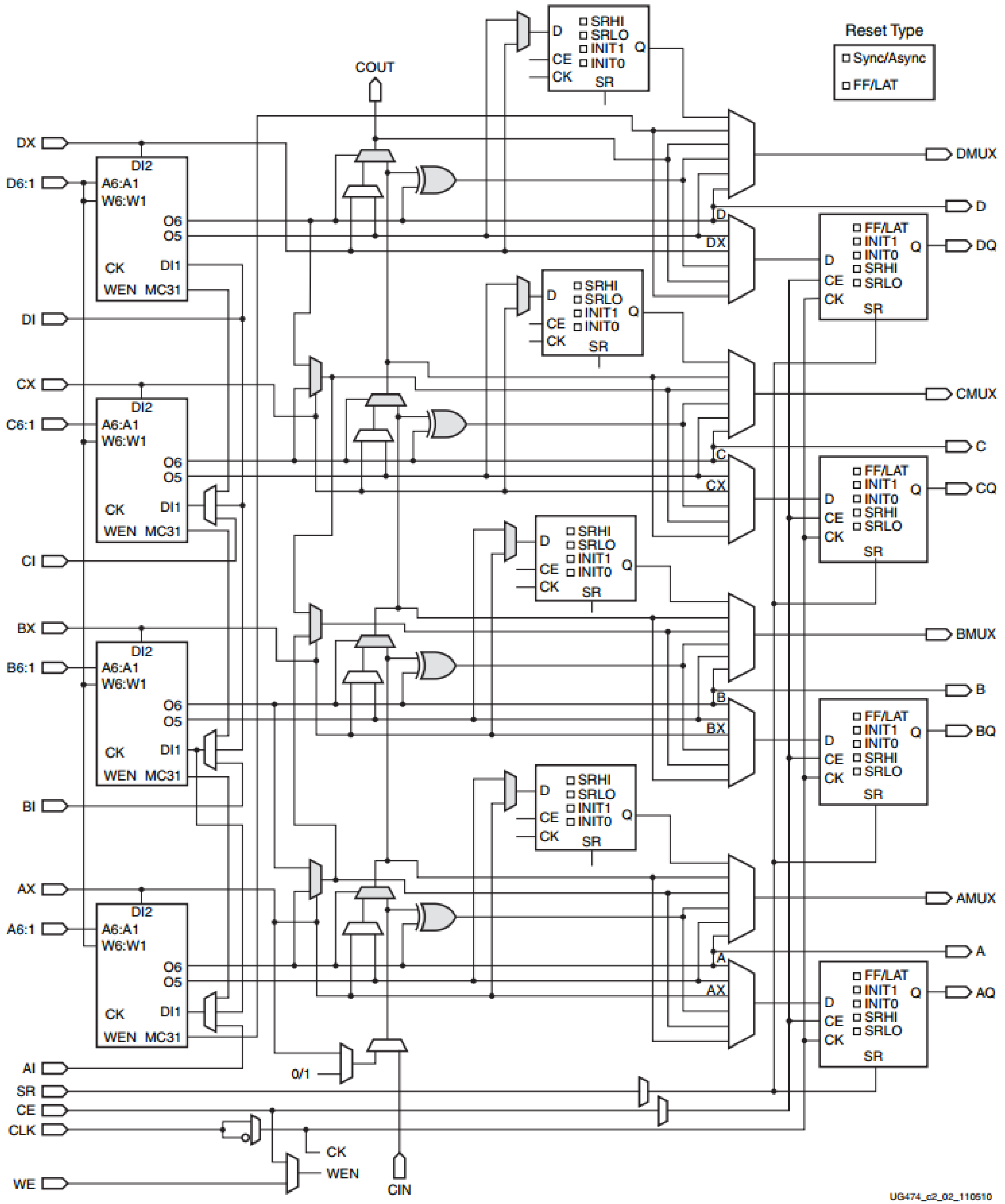


17-stage delay

LUT as Shift Registers (only in SLICEM)

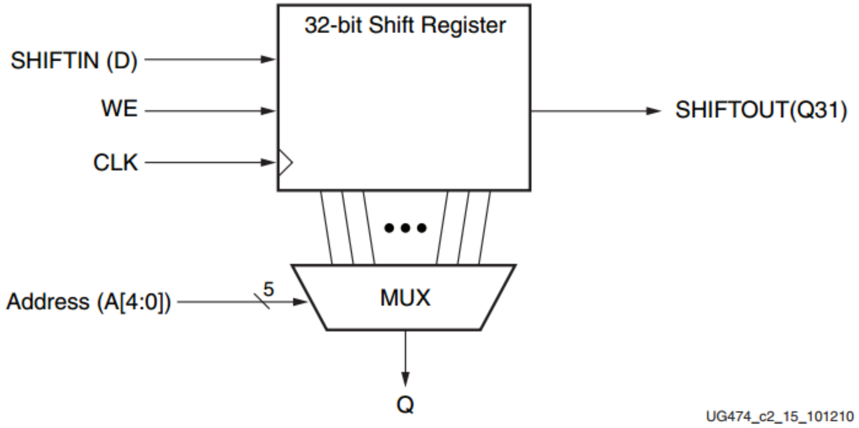


SLICEM


Reset Type
□ Sync/Async
□ FF/LAT
COUT
DX
D6:1
DI
CX
C6:1
CI
BX
B6:1
BI
AX
A6:1
AI
SR
CE
CLK
WE
DI2
A6:A1
W6:W1
O6
O5
CK
DI1
WEN
MC31
D
CE
CK
□ SRHI
□ SRLO
□ INIT1
□ INIT0
Q
SR
□ FF/LAT
DMUX
D
DQ
DX
CMUX
C
CQ
CX
BMUX
B
BQ
BX
AMUX
A
AQ
AX
0/1
CK
WEN
CIN
UG474_c2_02_110510

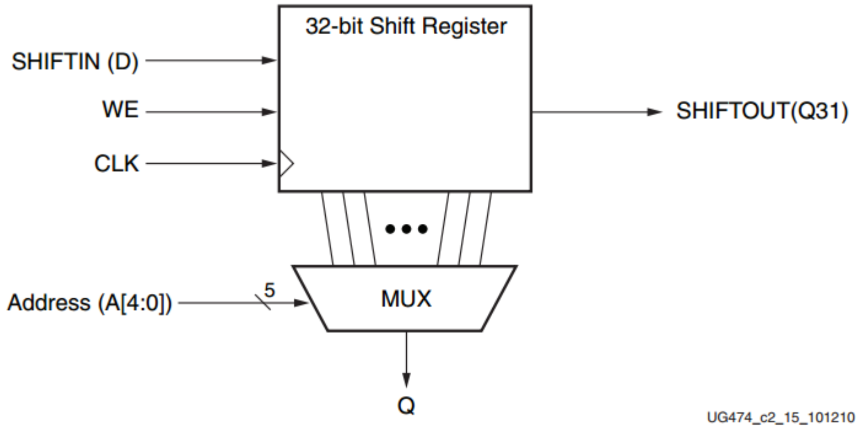
LUT as Shift Registers (only in SLICEM)

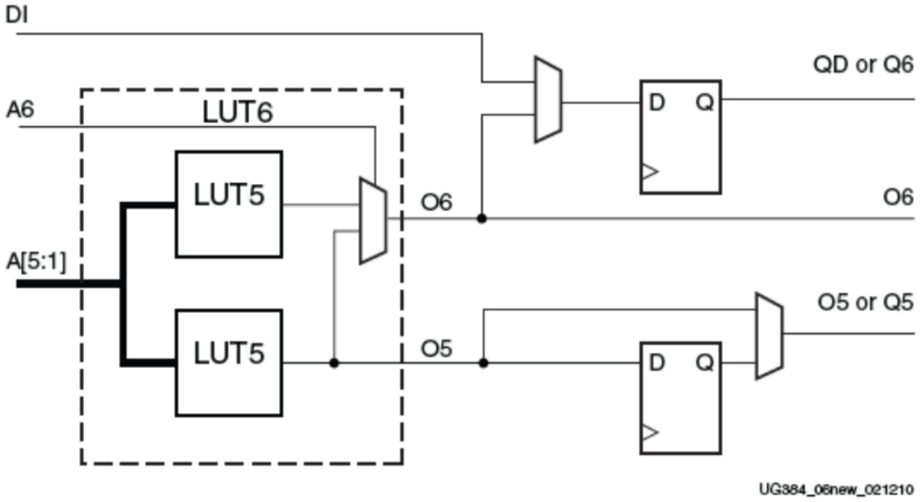
- Shift register functions include:
  - Write operation (Synchronous with a clock input and an optional clock enable)
  - Fixed read access to Q31
  - Dynamic read access:
    - Performed through 5-bit address bus (LSB is unused)
    - Any of the 32 bits can be read out asynchronously by controlling the address
    - Useful for smaller shift registers
  - Flip-flop can be used for synchronous read with one additional latency
  - **Set/reset is not supported**

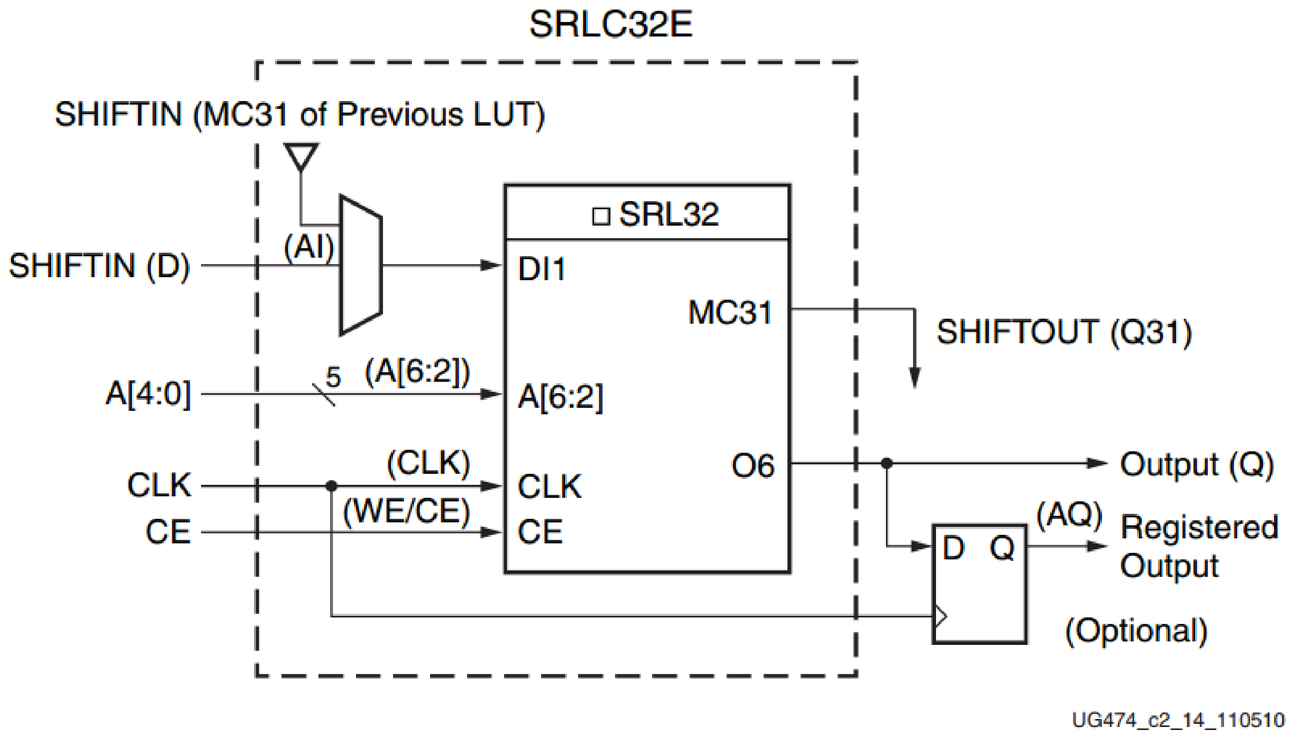


LUT as Shift Registers (only in SLICEM)

- A SLICEM LUT can be configured as a 32-bit shift register without using the flip-flops available in a slice.

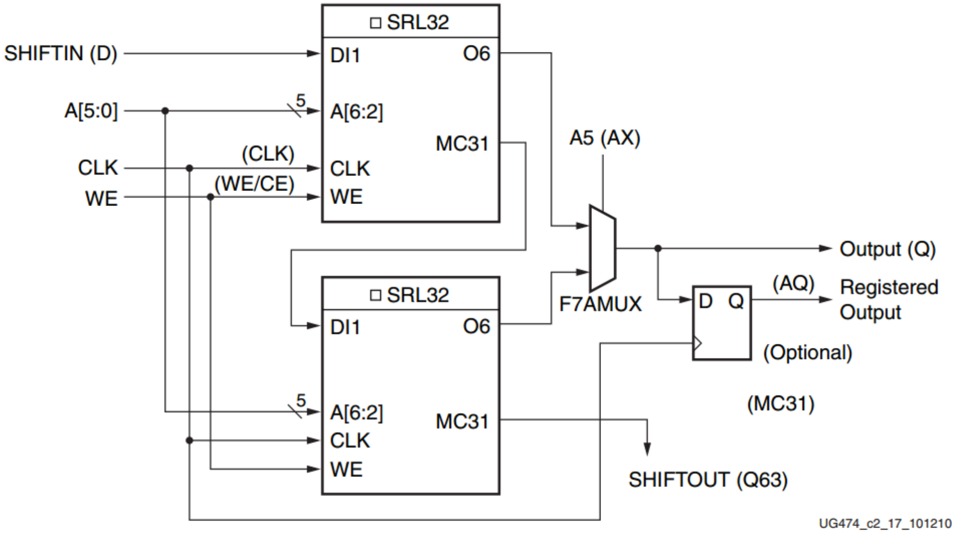






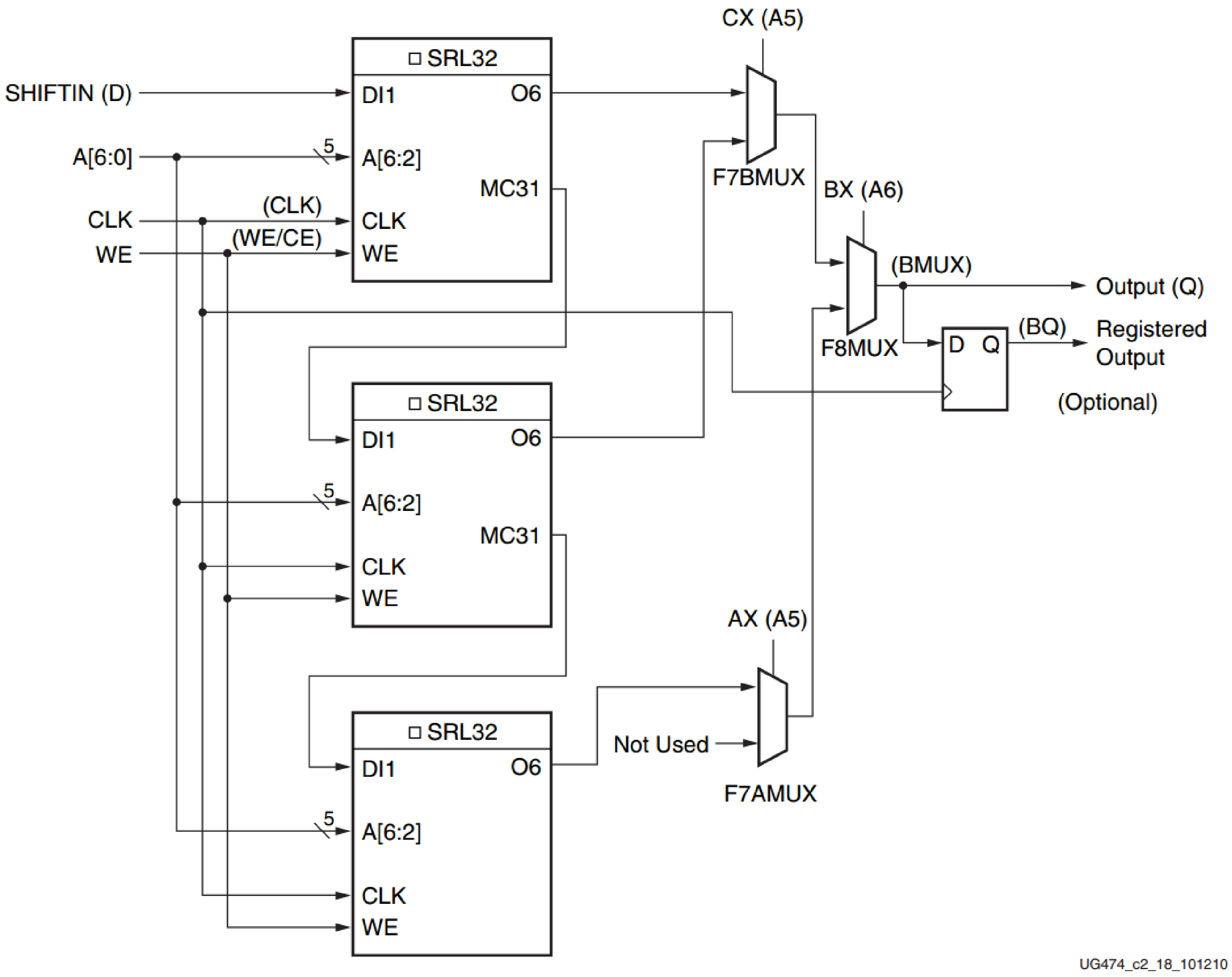
LUT as Shift Registers: 64 Bit

- MC31 output and a dedicated connection between LUTs allows connecting the last bit of one shift register to the first bit of the next, without using the LUT O6 output.
- Longer shift registers can be built with dynamic access to any bit in the chain.
- The shift register chaining and the F7AMUX F7BMUX, and F8MUX multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one SLICEM



64-Bit Shift Register Configuration

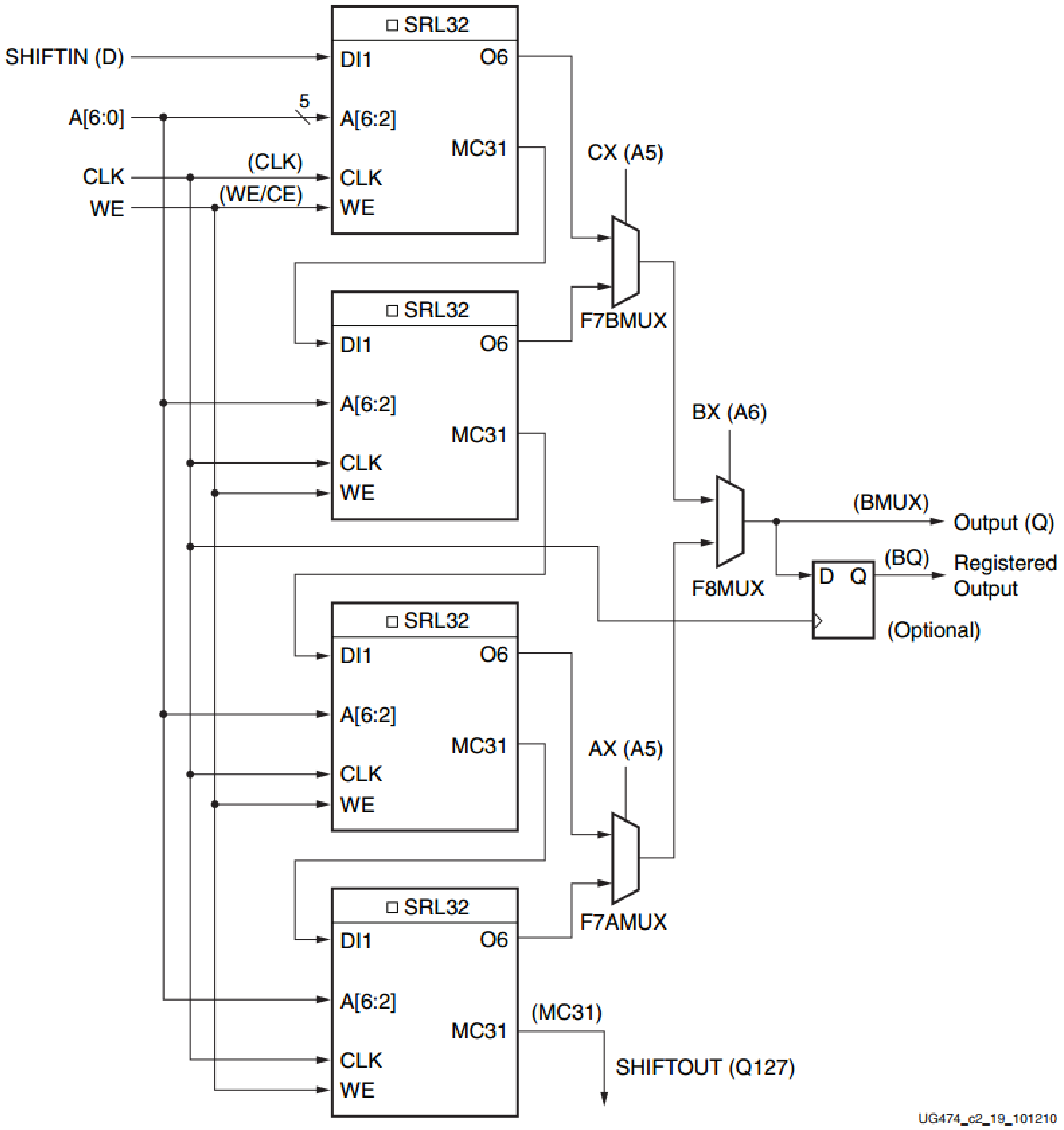
Shift Register
96 Bit



96-Bit Shift Register Configuration

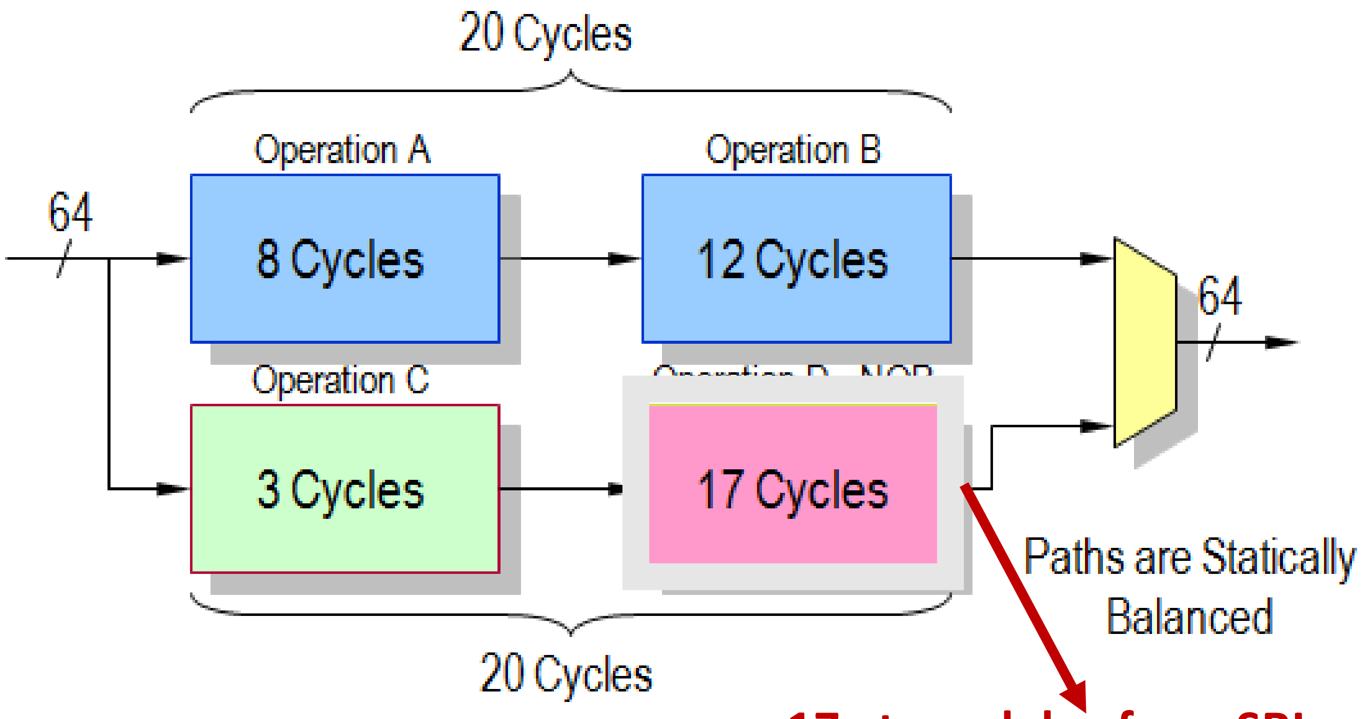
Shift Register
256 Bit

Shift Register
128 Bit



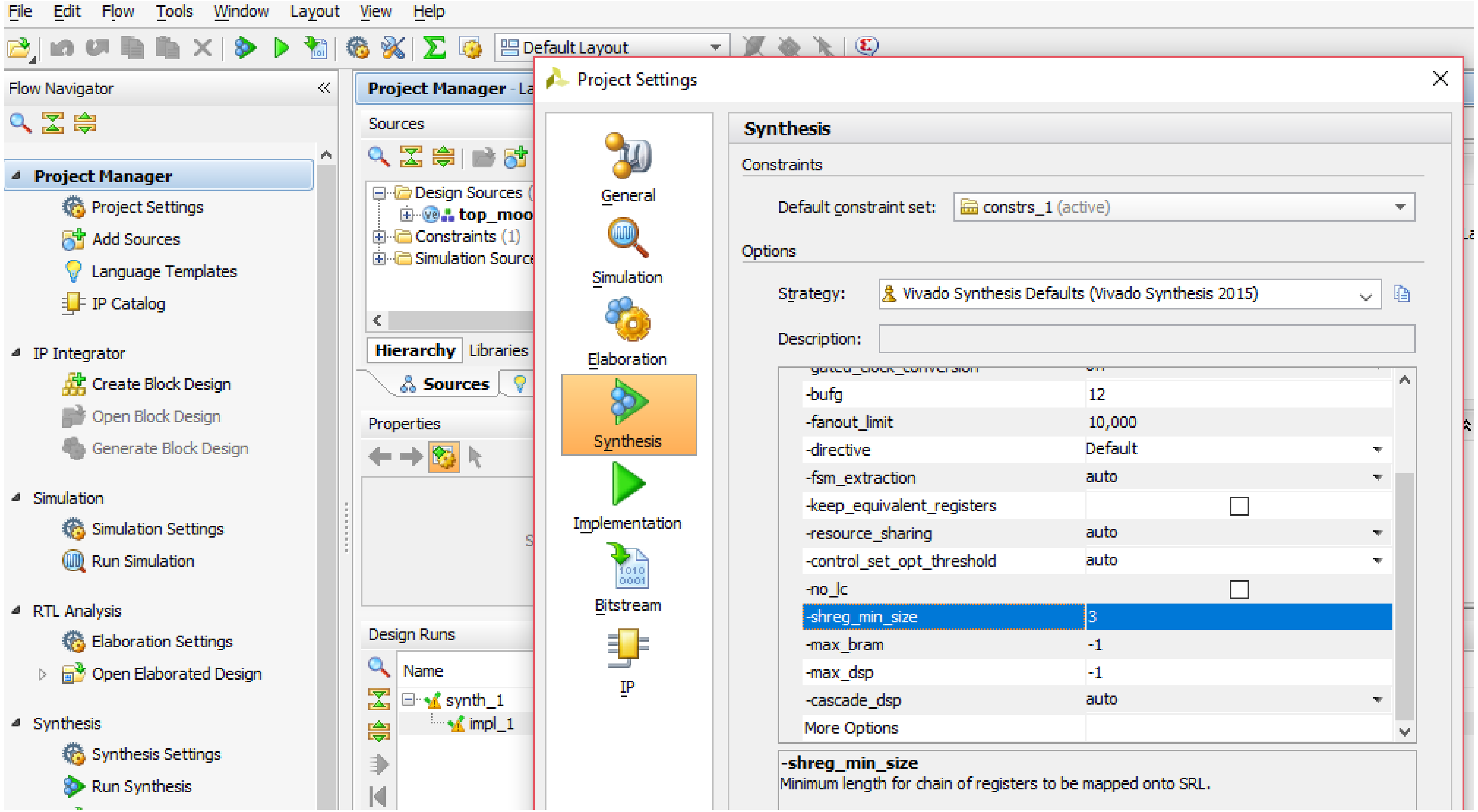
Shift Register LUT Example

- Operation D - NOP must add 17 pipeline stages of 64 bits each
  - 1,088 flip-flops (hence 136 slices) or
  - 64 SRLs (hence 16 slices)



17-stage delay from SRL

Shift Register LUT Example



Synthesis

Constraints

Default constraint set: constrs_1 (active)

Options

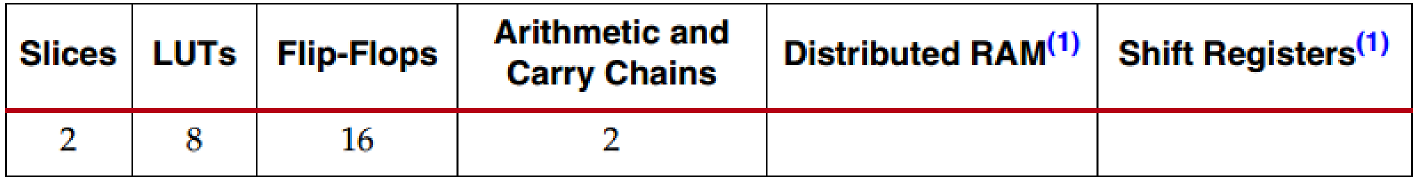
Strategy: Vivado Synthesis Defaults (Vivado Synthesis 2015)

Description:

-gated_clock_conversion	off
-bufg	12
-fanout_limit	10,000
-directive	Default
-fsm_extraction	auto
-keep_equivalent_registers	□
-resource_sharing	auto
-control_set_opt_threshold	auto
-no_lc	□
-shreg_min_size	3
-max_bram	-1
-max_dsp	-1
-cascade_dsp	auto
More Options	

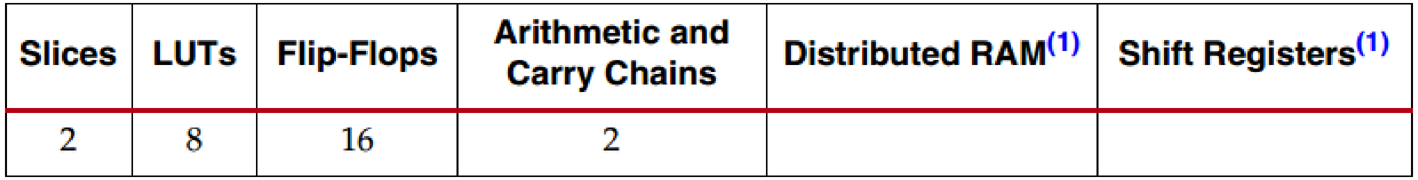
-shreg_min_size
Minimum length for chain of registers to be mapped onto SRL.

Types of CLB Slices

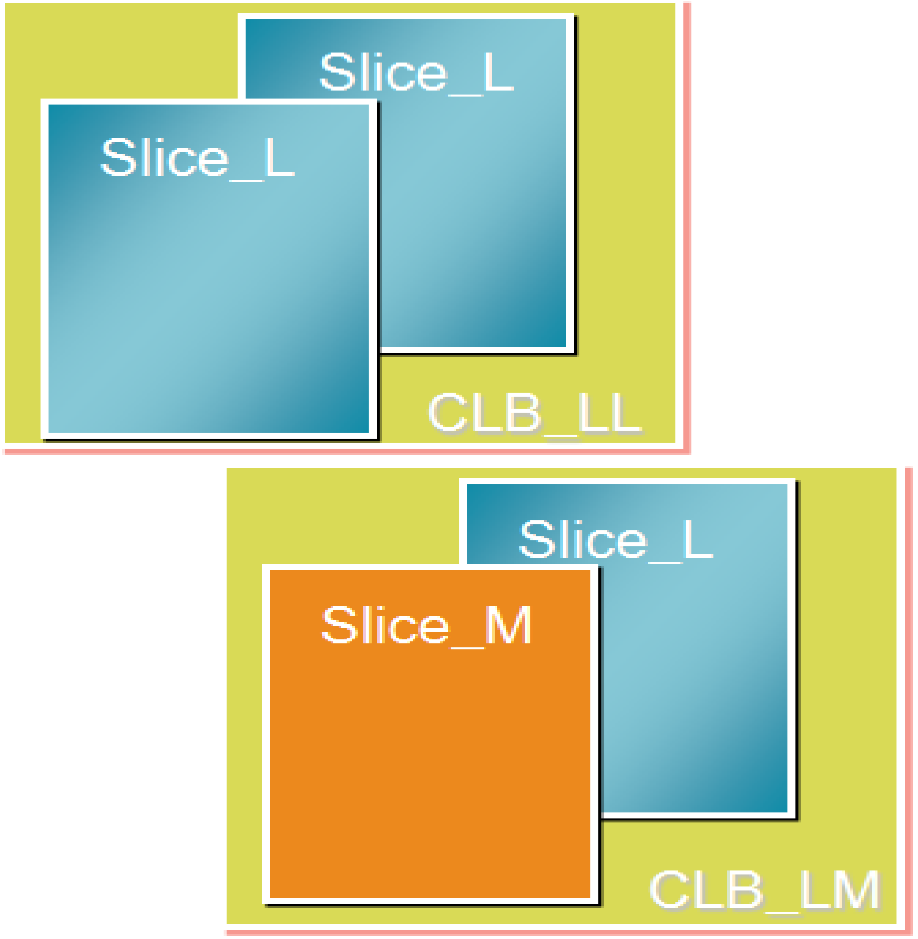


Slices	LUTs	Flip-Flops	Arithmetic and Carry Chains	Distributed RAM[1]	Shift Registers[1]
2	8	16	2		

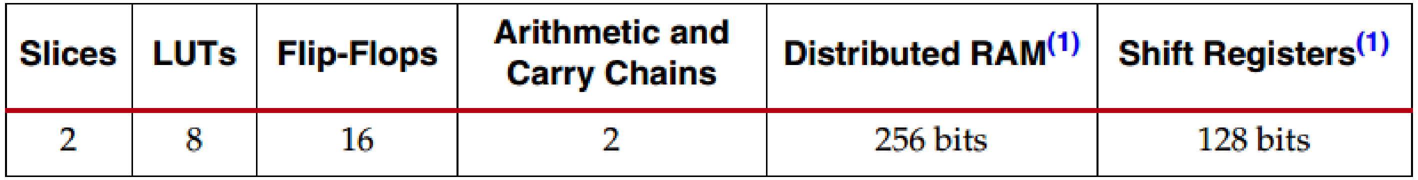
Types of CLB Slices



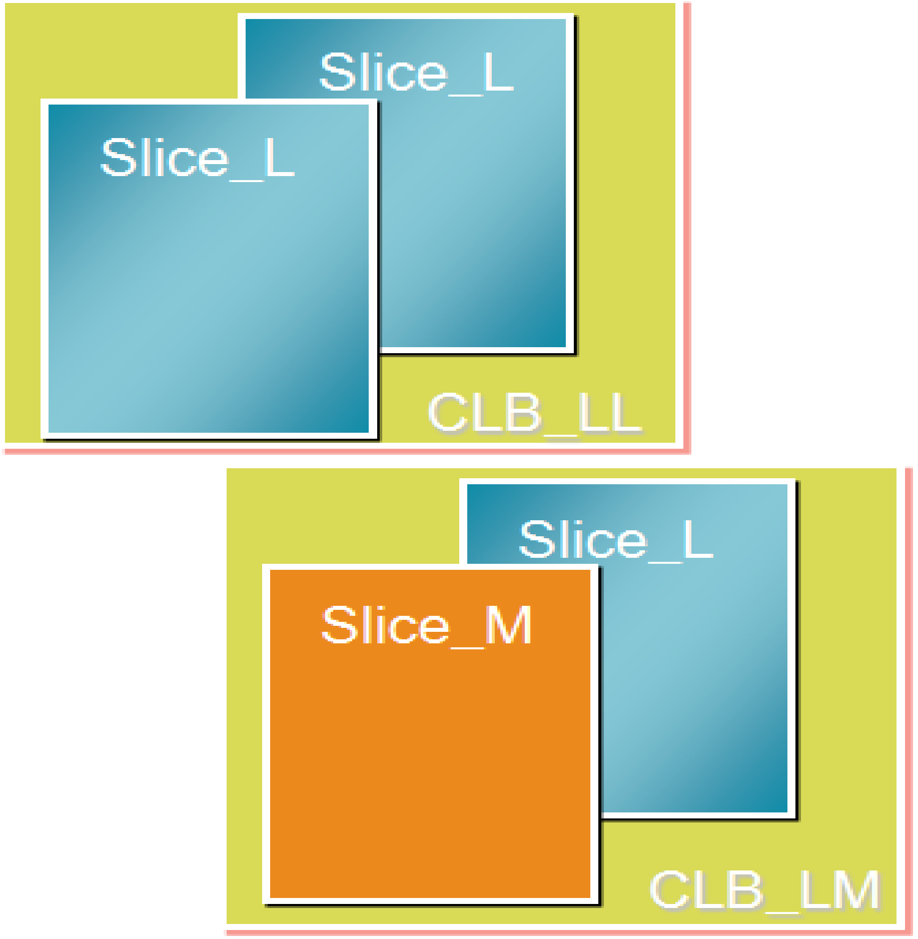
Slices	LUTs	Flip-Flops	Arithmetic and Carry Chains	Distributed RAM[(1)]	Shift Registers[(1)]
2	8	16	2		



Types of CLB Slices



Slices	LUTs	Flip-Flops	Arithmetic and Carry Chains	Distributed RAM[1]	Shift Registers[1]
2	8	16	2	256 bits	128 bits


Slice_L
Slice_L
CLB_LL
Slice_L
Slice_M
CLB_LM