

Quiz - 2

ECE214 - Integrated Electronics

• INSTRUCTIONS:

Total Marks = 100

Time Duration = 70 minutes for solving + 10 minutes uploading

1. The duration of the exam is 70 mins, and 10 mins for scanning and uploading the solutions. No further extension of time will be given regarding this. **Any late submission will be awarded 0 marks.**
2. This paper contains four questions, with their respective subparts. Some questions may also utilize the elementary level understanding of your previous courses.
3. The question paper will be uploaded in google classroom. Do not forget to turn it in. Solutions submitted by any other means (email etc.) won't be considered for evaluation.
4. Students are required to switch on their cameras and mute themselves. Make sure you are sitting in a well-lit room so that we are able to see your faces clearly. **If you are not clearly visible, you will be awarded 0 marks.**
5. The answers should be in your own handwriting and submission should be in PDF format only. No other mode of submissions will be accepted.
6. Write any assumption clearly, if any. Needless to say, only reasonable assumptions will be considered if any ambiguity is found in the question.
7. During the exam, if you have any queries, write them in the meet chatbox. It will be taken into notice by us. Don't unnecessarily unmute your mic for it creates a disturbance to others.
8. Calculators are NOT allowed during exam time. ONLY use pen and paper for writing the exam.
9. Students need to be present and visible for the whole exam duration (till the end of solution uploading time) even if they upload the solution before time.
10. **NAMING CONVENTION** - <Name>_<Roll No.>_ Quiz2.pdf
11. Show your calculations and justifications in each question.

Necessary assumptions and values

1. $V_{be}(\text{on}) = 0.7 \text{ V}$
2. $V_{ce}(\text{saturation}) = 0.2 \text{ V}$
3. Reverse saturation current = 0
4. MOSFET GATE leakage current = 0
5. Capacitors leakage current = 0
6. Batteries are ideal

Q 1. For the circuit given in Fig 2, diode D1 has forward voltage drop of 0.7 V, beta of all the BJTs are very large. Q1 and Q2 are perfectly matched. $I_c \approx I_e$ for the BJTs operating in active region.

- Find the values of R4 and R3 such that, the DC operating point for Q3 will be (3mA, 6V).
[15 Marks]
- Find the range of R4 such that Q3 will remain in active region. [15 Marks]
- Explain what is passive and active load biasing in BJT. Give at least one example of active load circuits.
[5 Marks]

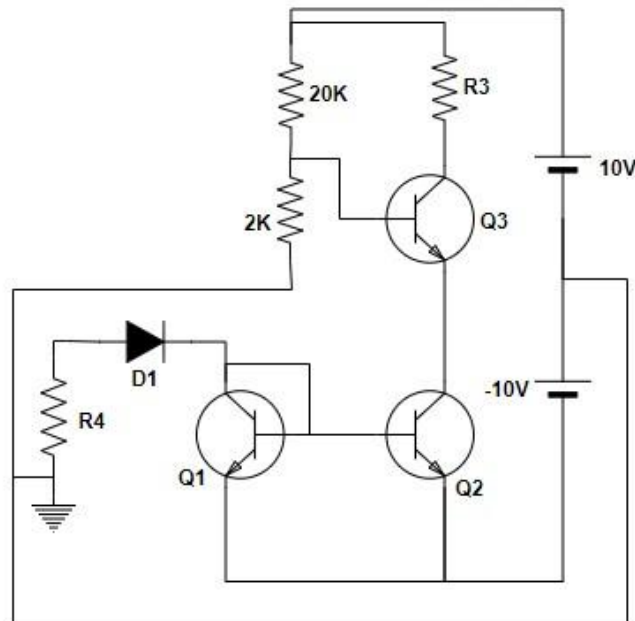


Fig 2

Q 2. For the NMOS given in circuit of Fig 3, threshold voltage (V_t) = 1 V, $\mu_n C_{ox} = 80 \mu A/V$, where μ_n is the electron mobility in the channel and C_{ox} is the oxide capacitance per unit area, aspect ratio (W/L) = 10. Channel length modulation effects are negligible ($\lambda = 0$). All the coupling capacitors are very large and they have negligible leakage current. All the node voltages are taken wrt ground.

- For a given bias current (I_D) of 0.1mA, find the value of R2 for a maximum possible voltage swing at node B.
[15 Marks]
- For the given bias conditions in “point a” and respective obtained R2, find overall voltage gain wrt node B(output) and node A(input). Given R1 = 10 Mega ohm and node C is grounded. [15 Marks]
- Explain what will happen to gain if node C is left open, keeping every other condition same as in “point b”. Justify your answer using appropriate equations (exact numerical calculation is not required). [5 Marks]

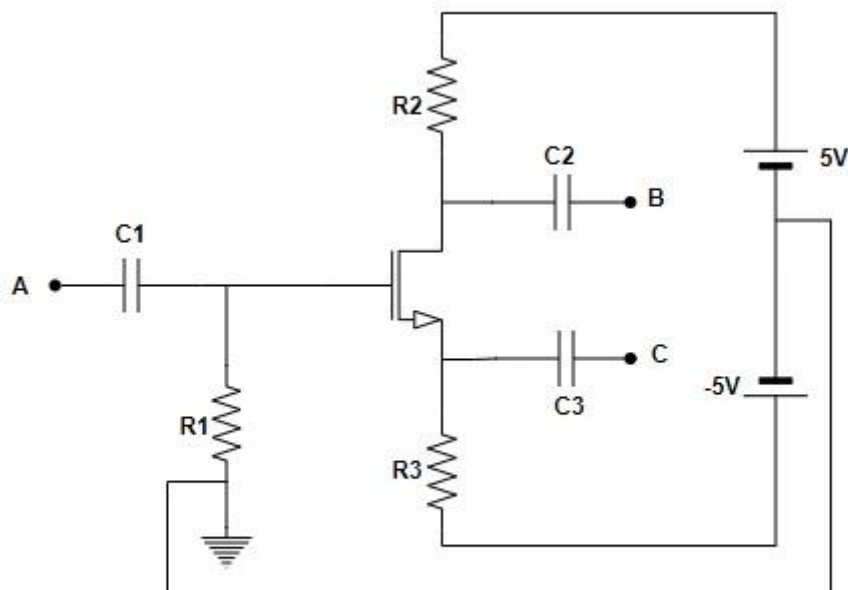


Fig 3

Q 3. For the circuit shown in Fig 4, beta of the BJT is specified in it's datasheet to be in the range of 50 to 150, with a typical value of 100 (take this typical value of beta while doing calculation for DC biasing). Assume that the range of V_{cc} and R_c is such that the BJT will remain in active region. $I_c \approx I_e$. All the coupling capacitors are very large and they have negligible leakage current. All the node voltages are taken wrt ground.

- What will be the ratio of maximum to minimum overall voltage gain at a bias point $I_{cq} = 0.5\text{mA}$. Node C is grounded, Node A is input and B is output. **[15 Marks]**
- Calculate the value of R_e such that the ratio of maximum to minimum overall voltage gain is limited to 1.5. Node C is open. **[15 Marks]**

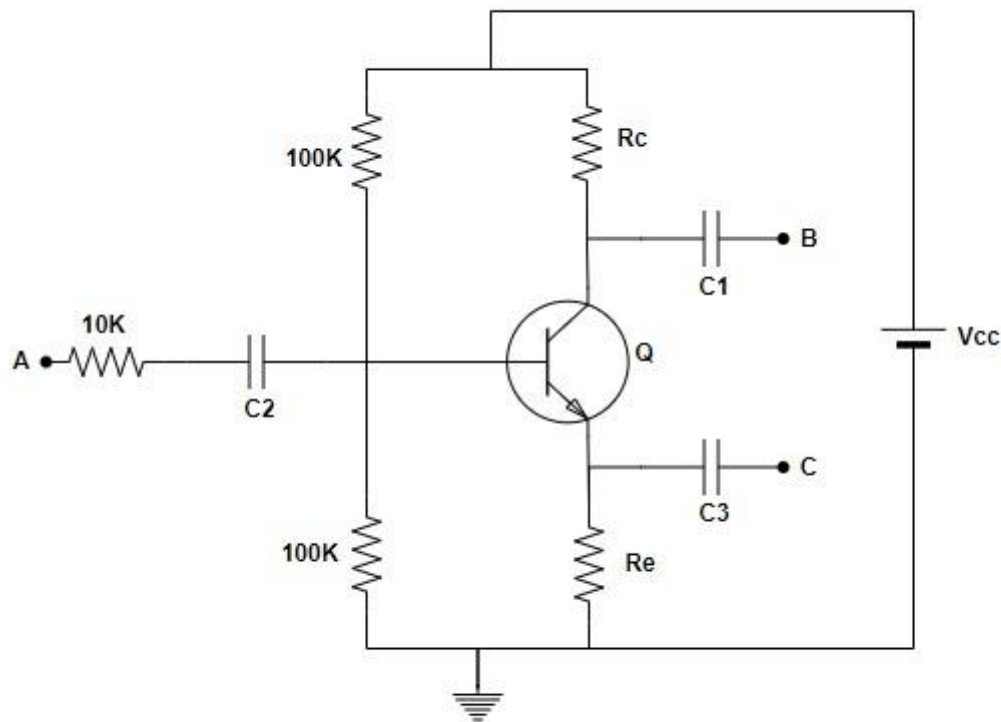


Fig 4