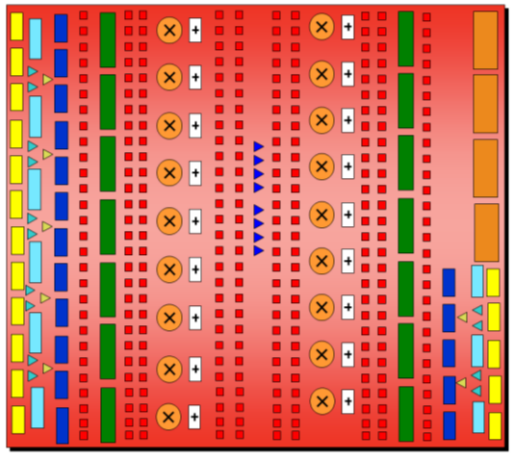
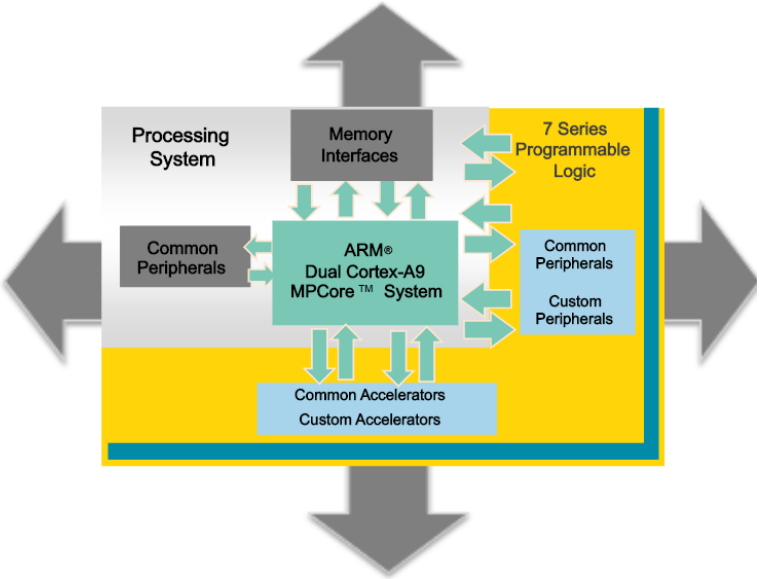
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

A2A
Algorithms to Architecture

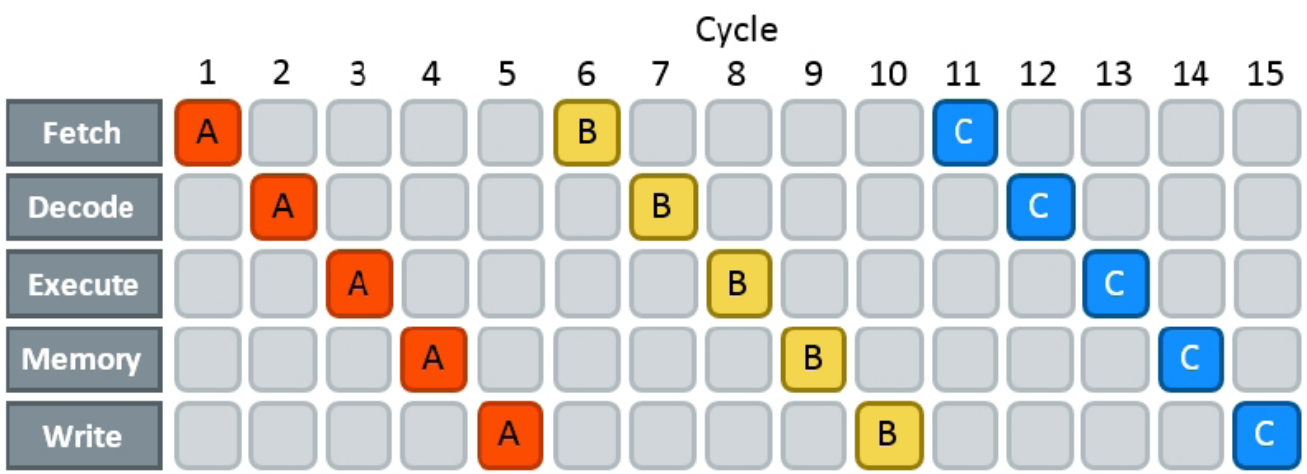
ECE 270: Embedded Logic Design

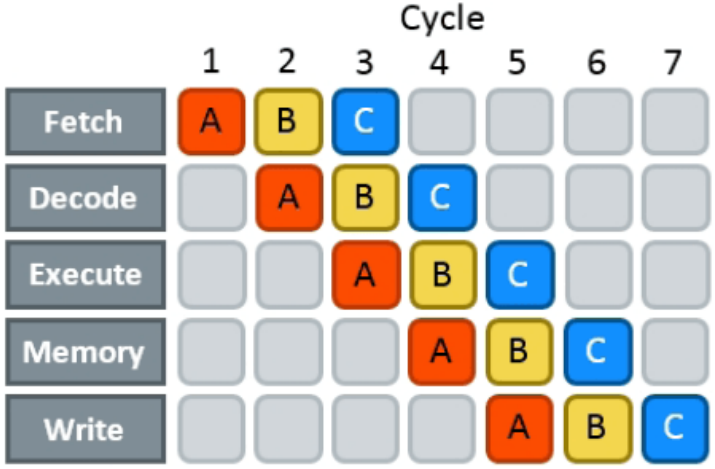




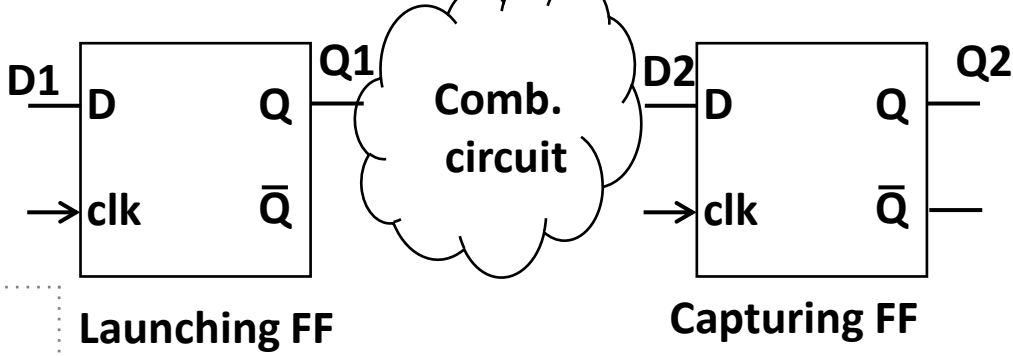
Pipelining

Why Pipelining?

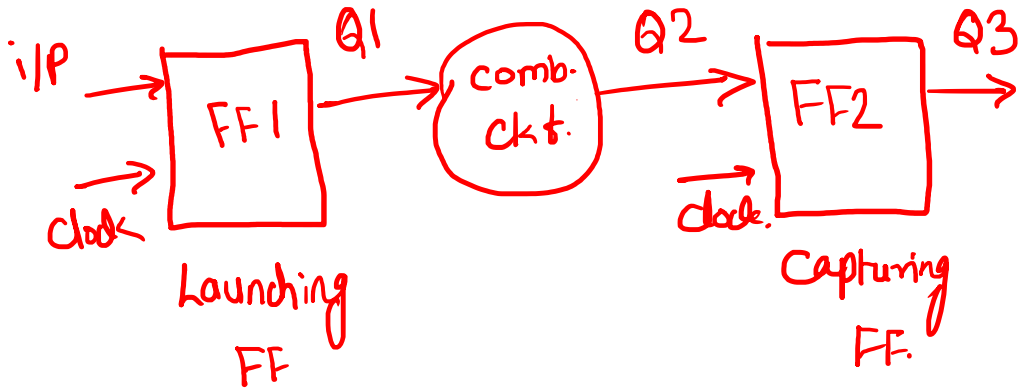


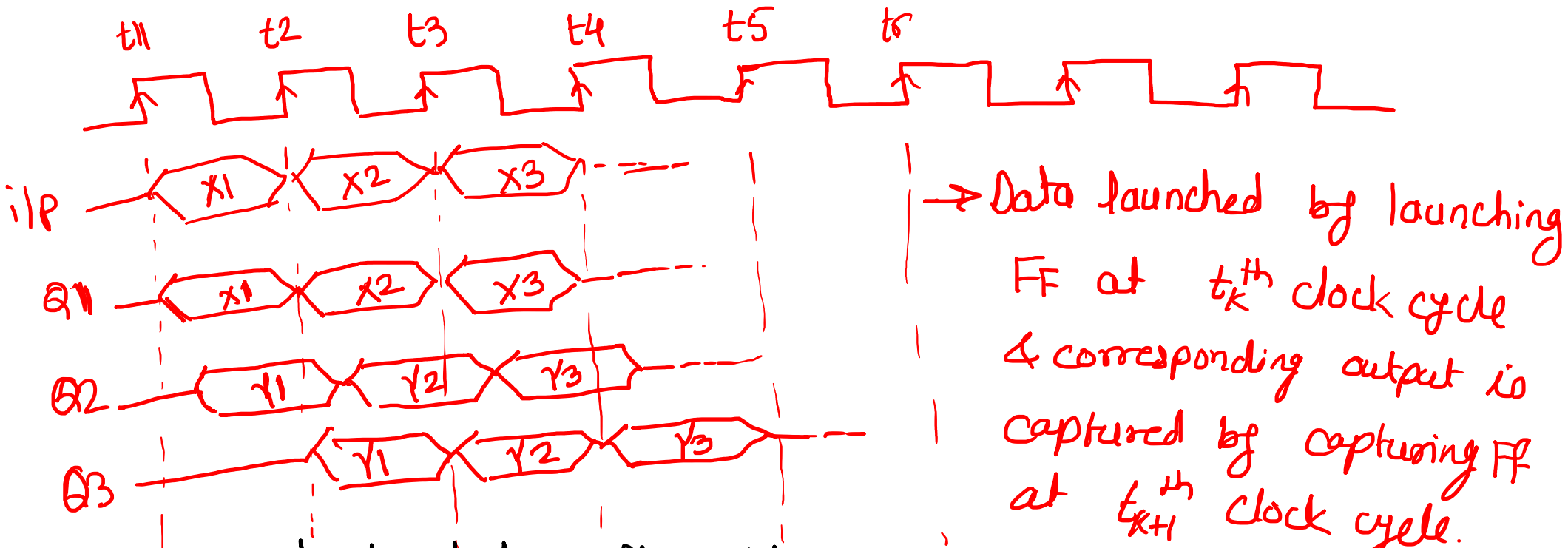


Pipelining Combinational Circuits



Pipelining

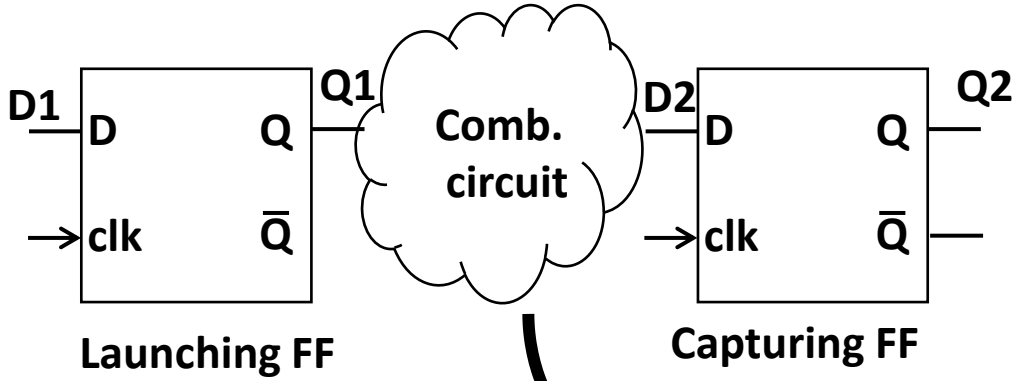


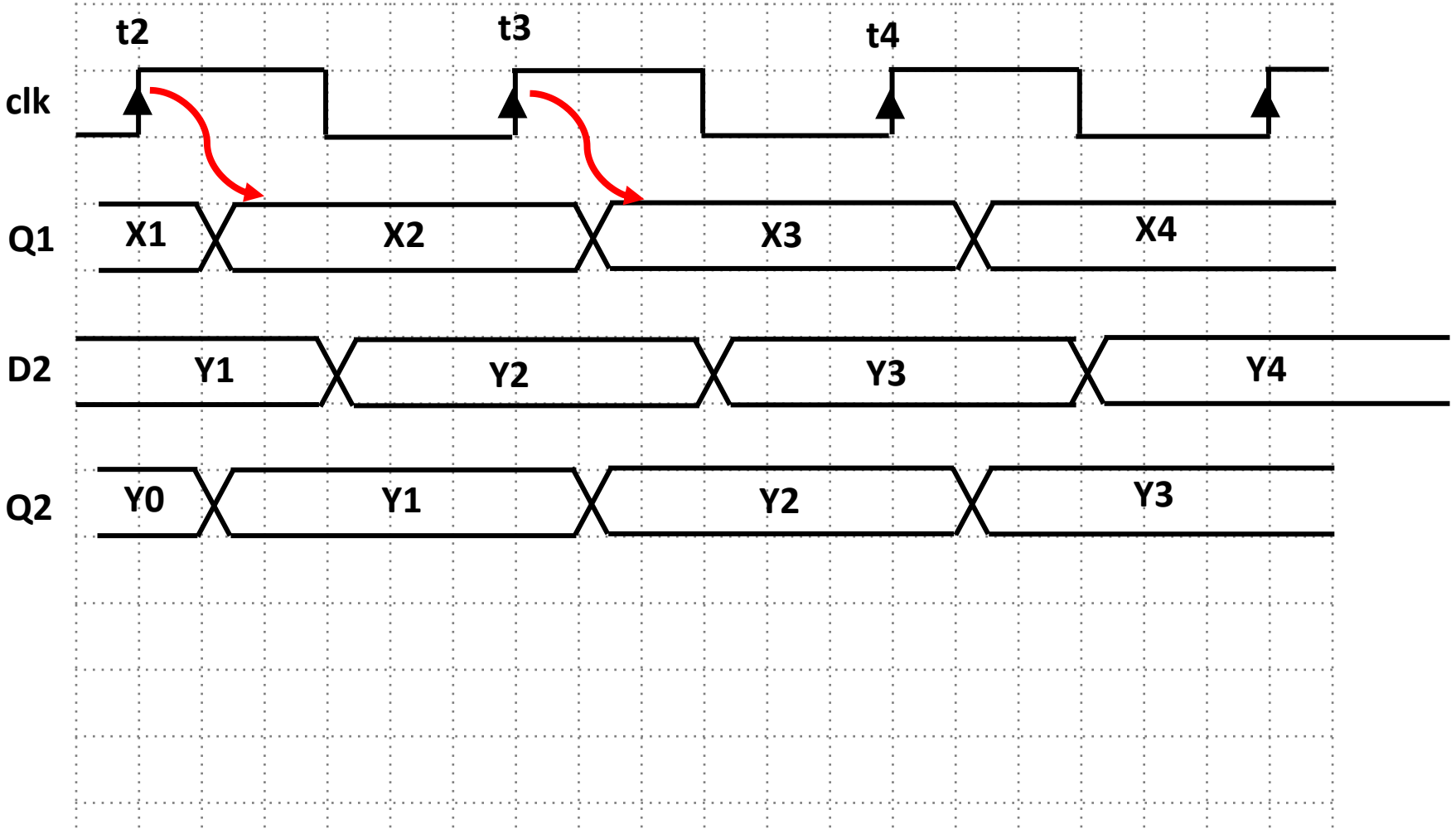


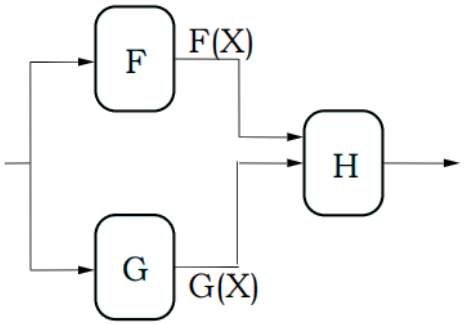
→ Data launched by launching FF at t_k^{th} clock cycle & corresponding output is captured by capturing FF at t_{k+1}^{th} clock cycle.

– Clock period should be sufficiently large so that correct data is captured. $(t_2 - t_1)$

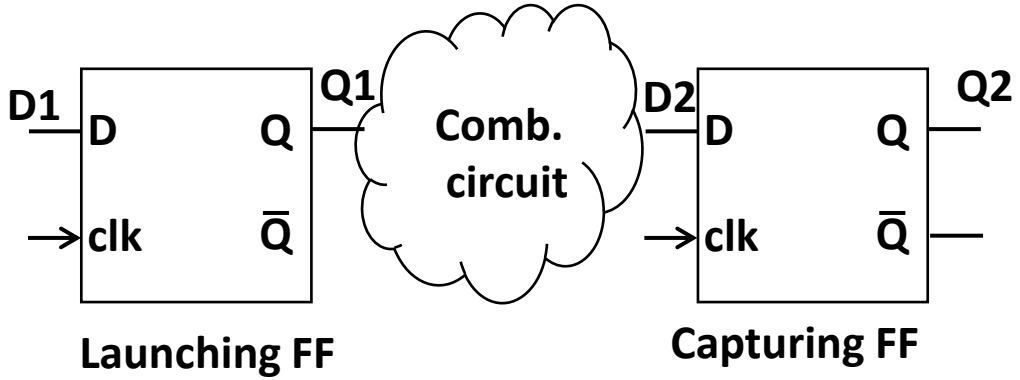
FF Timing Constraints

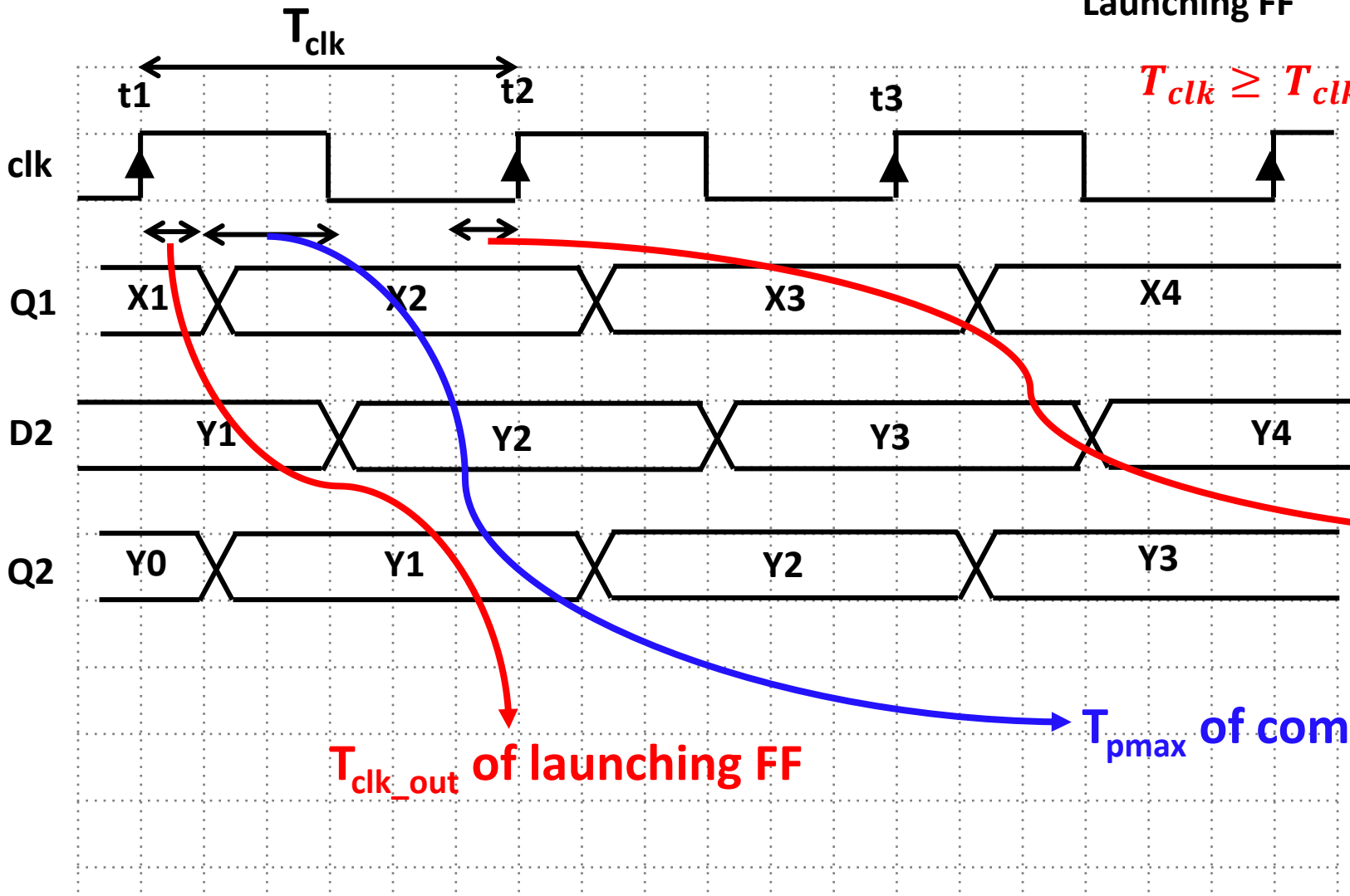






FF Timing Constraints

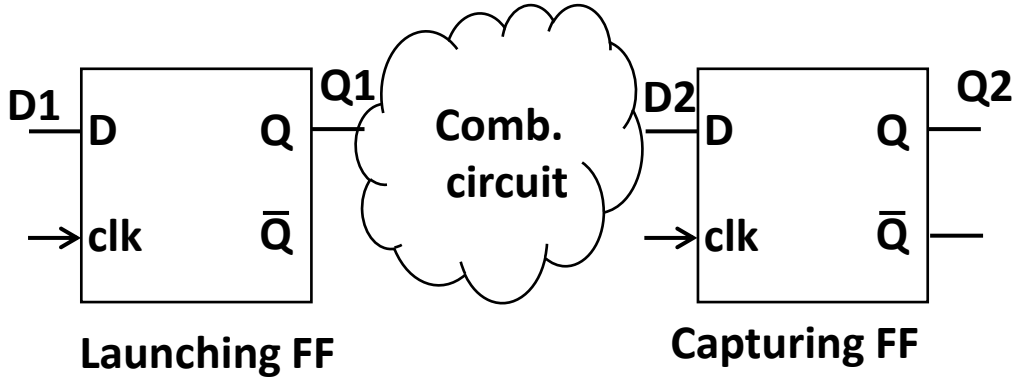


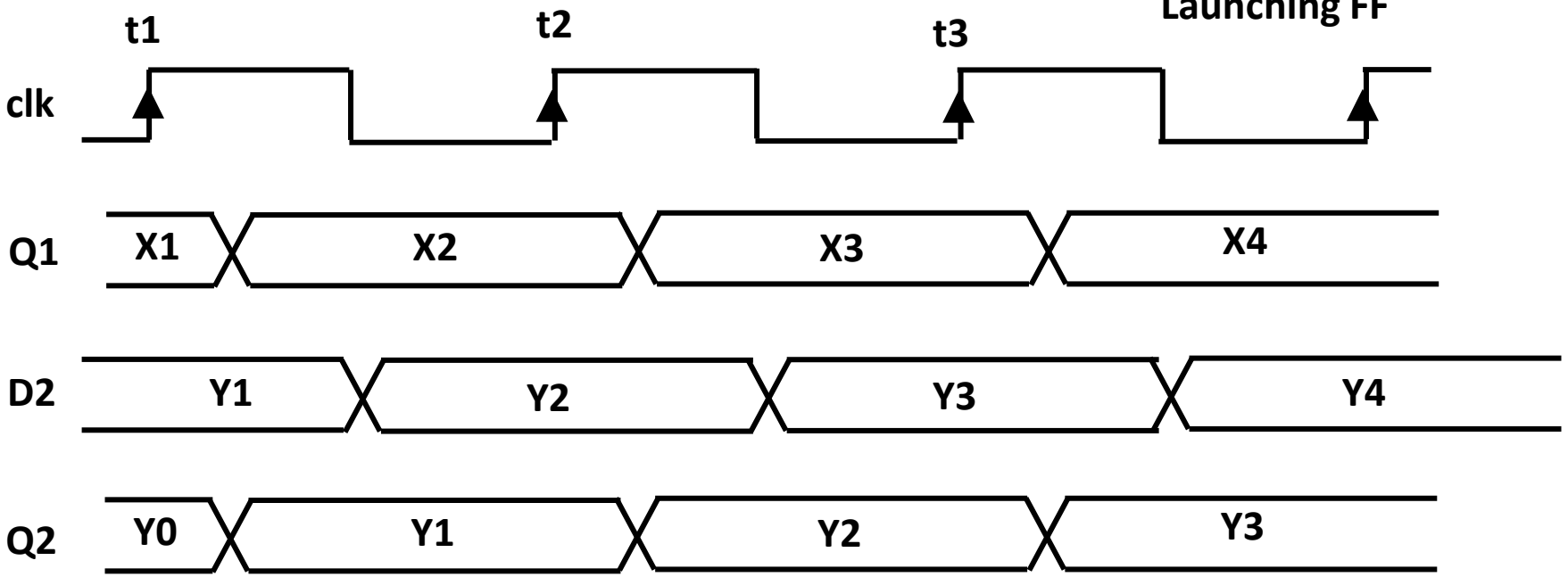


$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$

$$|\Delta_1 - \Delta_2|$$

FF Timing Constraints

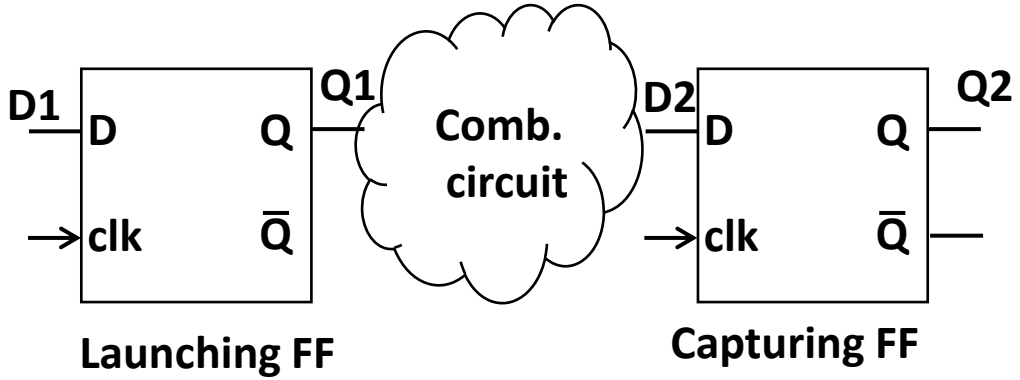


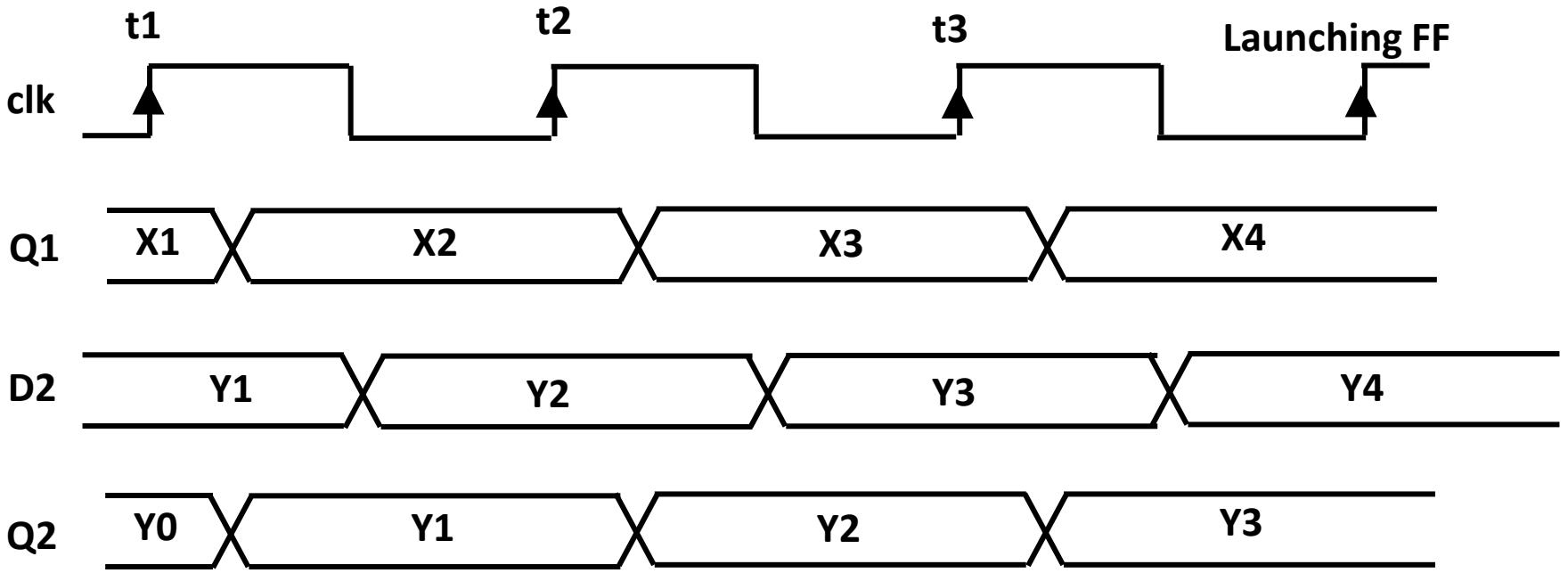


$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$

- This equation ensures that if the output of launching FF changes, this will make it to capturing FF before its set-up time.

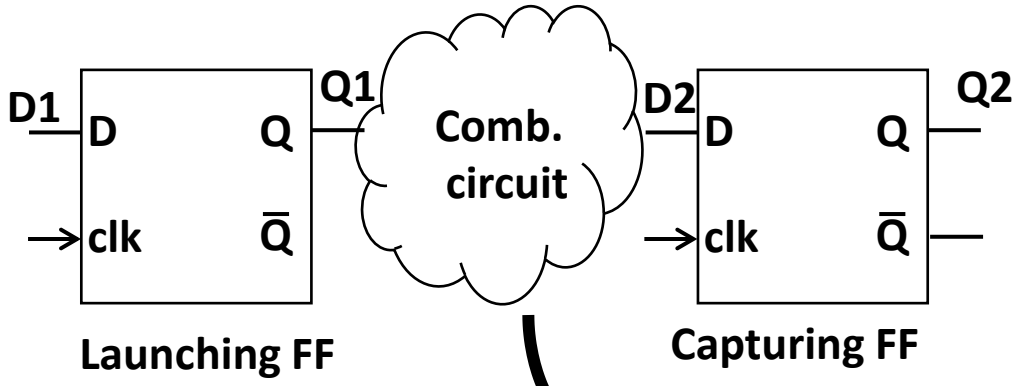
FF Timing Constraints





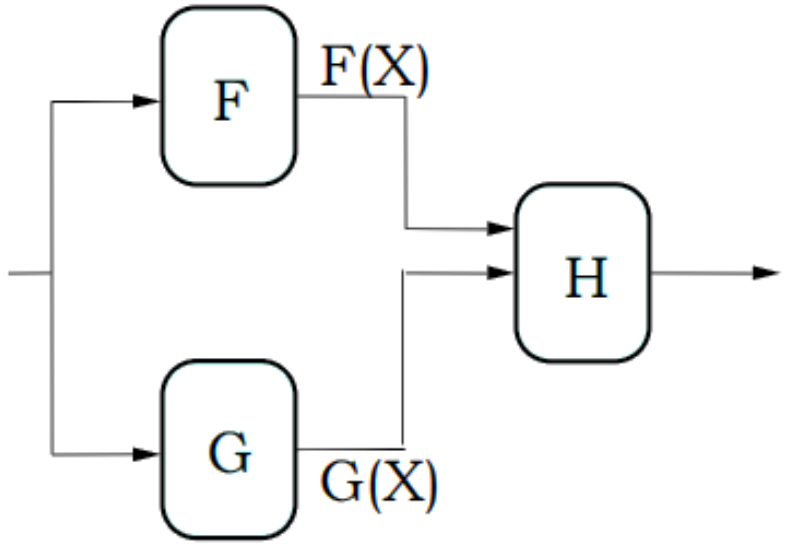
$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$

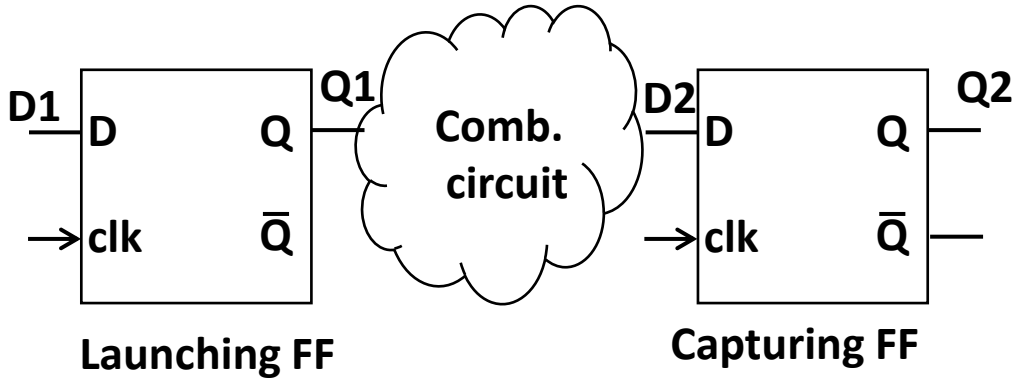
- This is very important equation since it puts limit on the minimum value of clock period and hence, maximum value of clock frequency.
- Limit on maximum value of clock frequency means limit on the speed at which the circuit can operates.



- How to increase the clock frequency or reduce the clock period?

$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$



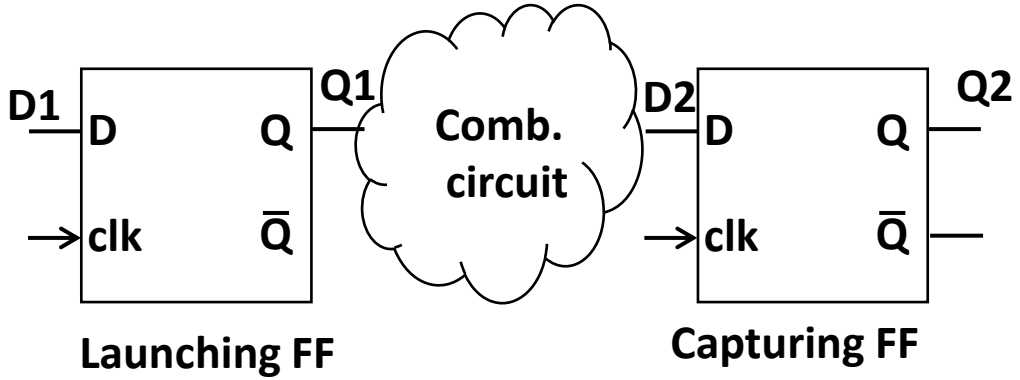


$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$

- Consider a travel from A-> C where there is vehicle changeover at B (A->B->C)
- The time from A->B is 30 minutes and from B->C is 60 minutes.
- Since there is a separate vehicle is used from each travel, we have two options:

1) Trip duration is 90 minutes where only one vehicle is active at a time. For N trips, total time required is 90N minutes.
2) Two vehicles are active simultaneously. Here, for N trips, the time required is **60N+30 minutes**. The second term is very small for large N and hence, ignored.

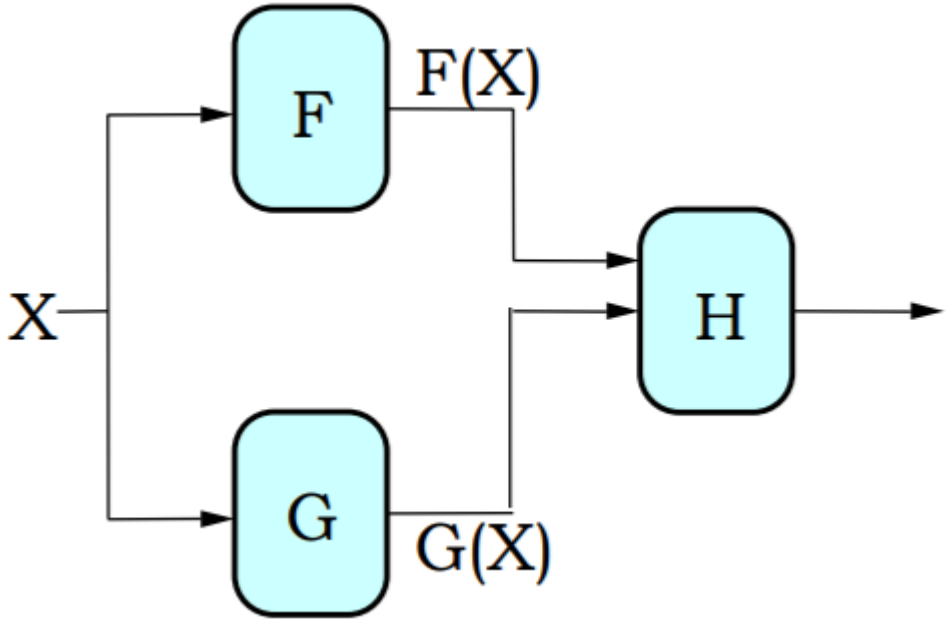
Pipelining



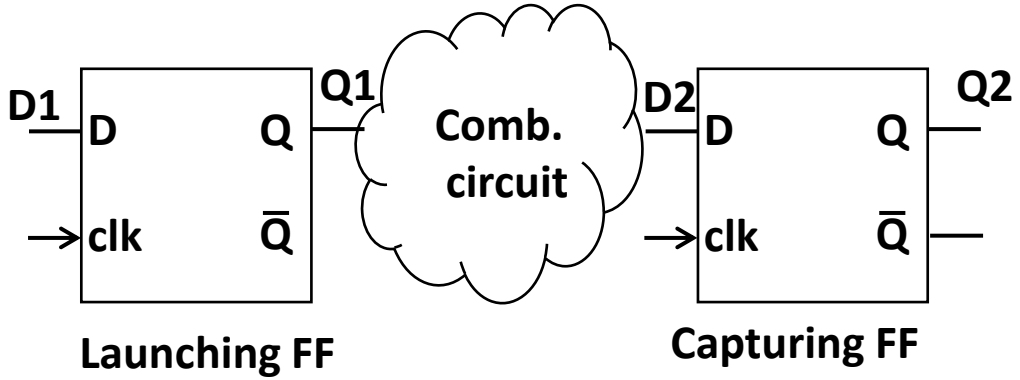
$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$

- Which approach is better???
- Lets discuss two more definitions:
- **Latency:** Delay when an input is established until the output associated with that input becomes valid
- Approach 1: 90 mins and Approach 2: 120 mins
- **Throughput**: The rate at which the new output is produced
- Approach 1: 1/90 mins and Approach 2: 1/60 mins
- Approach must be selected based on the application requirements.

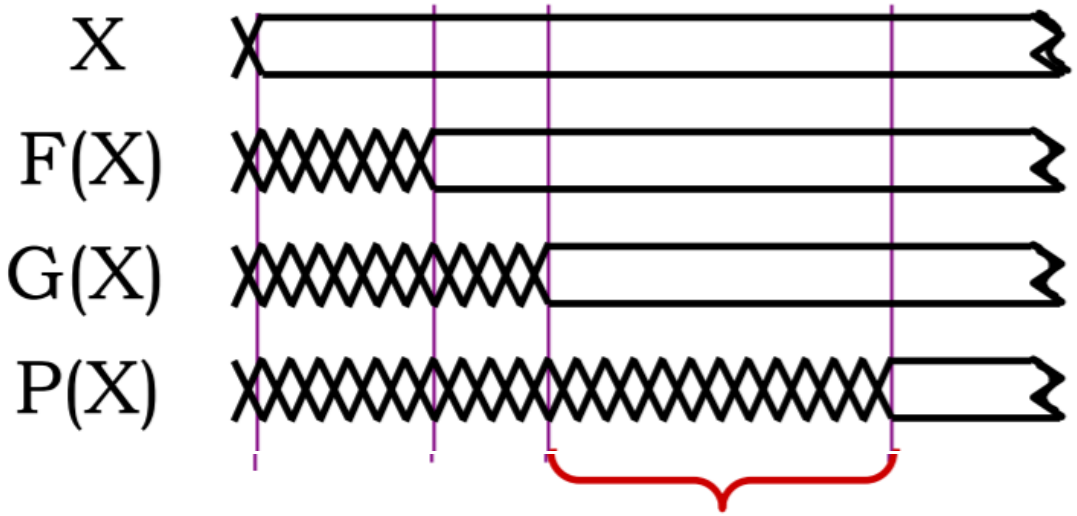
Pipelining



- **How to make F and G work concurrently with H?**

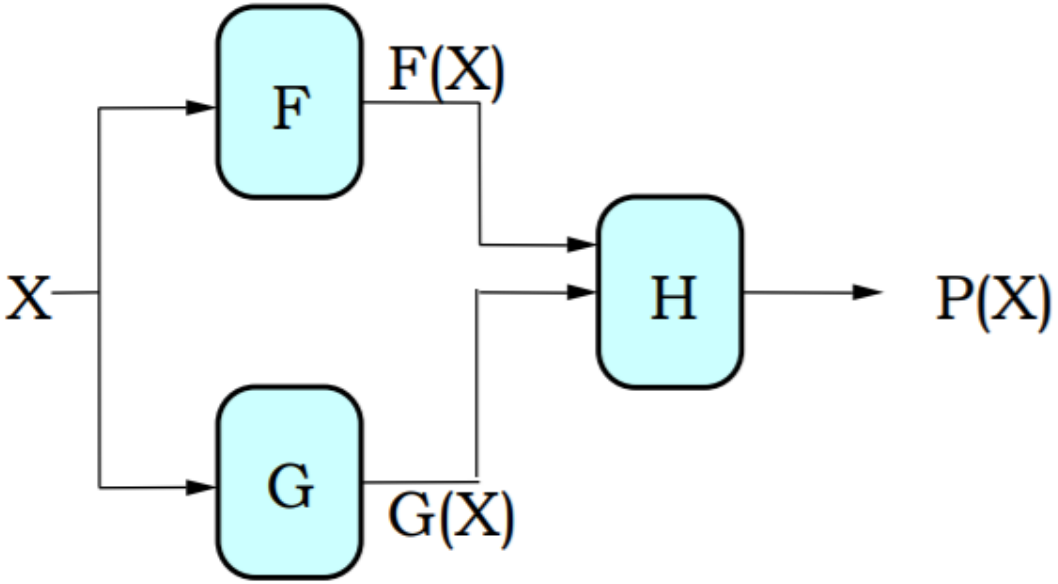


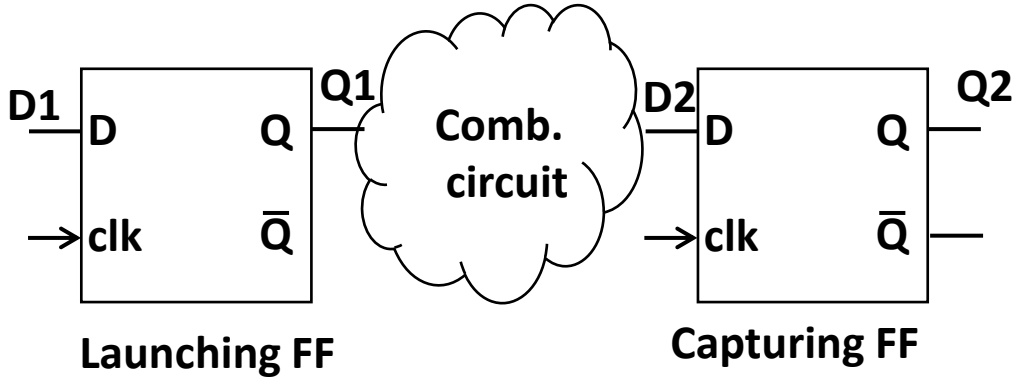
$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$



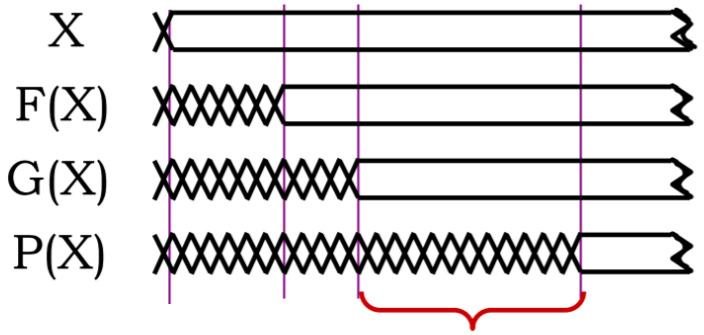
F & G are "idle", just holding their outputs stable while H performs its computation

Pipelining





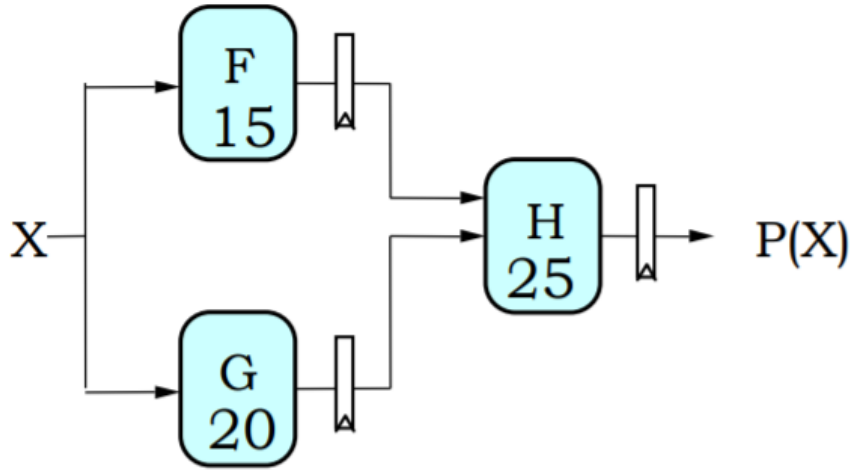
$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$



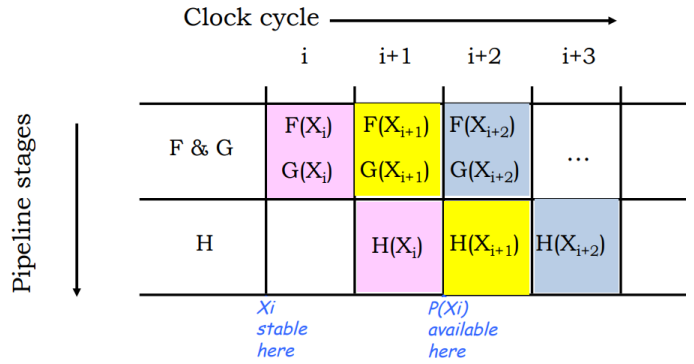
F & G are "idle", just holding their outputs stable while H performs its computation

- We need something which is good at holding or remembering the values of F and G outputs when H needs it as well it should free up F and G to do other computations.

Pipelining



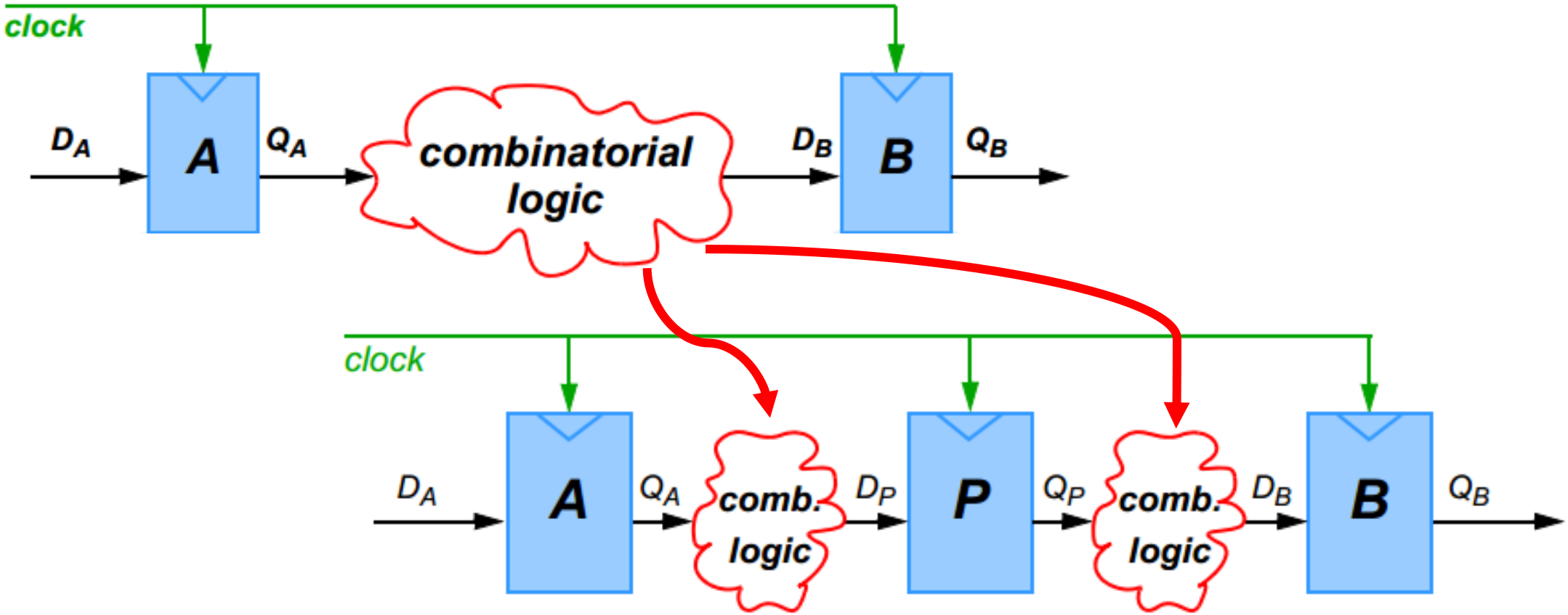
- Now, F and G can be working on input Xi+1 while H is performing its computations on Xi.
- This is 2-stage pipeline i.e. if we have valid input X during clock cycle j, P(X) is valid during clock cycle j+2.
- Assuming F, G and H have propagation delay of 15, 20 and 25 ns, and ideal registers i.e. FFs, then



	latency	throughput
unpipelined	45	1/45
2-stage pipeline	50	1/25

Pipelining

- Pipelining: Breaking of comb. Circuit by inserting additional registers



Pipelining (Summary)

- A well-formed K-Stage Pipeline ("K-pipeline") circuit have exactly K registers on every path from an input to an output.
- A COMBINATIONAL CIRCUIT is thus a 0-stage pipeline.
- Every pipeline stage, hence every K-Stage pipeline, has a register on its OUTPUT (not on its input).
- The CLOCK common to all registers must have a period sufficient to cover propagation delay of combinational circuit, clock-to-output delay of launching FF, setup time of capturing FF and clock skew.
- The LATENCY of a K-stage pipeline is K times the period of the system's clock. The THROUGHPUT of a K-stage pipeline is the frequency of the clock.

$$T_{clk} \geq \cancel{T_{clk-out}} + T_{pmax} + \cancel{T_{setup}} + \cancel{T_{skew}}$$