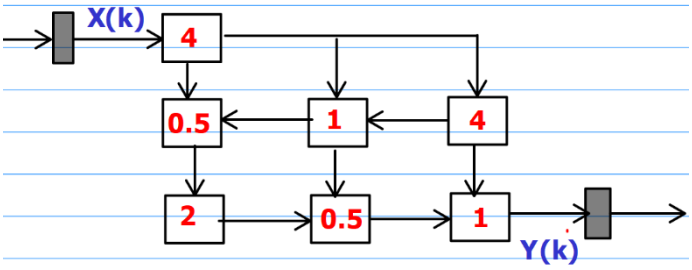
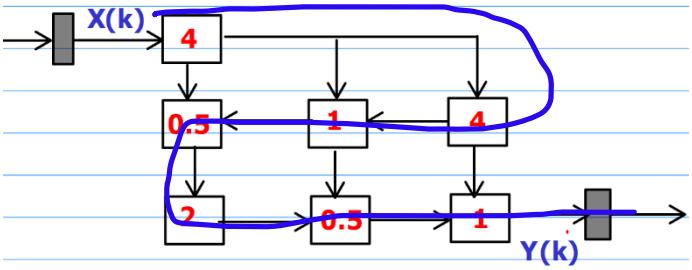
ECE270: ELD: End-Sem Theory Exam C and D (30 Minutes)

Date: December 2, 2023

1. For the circuit shown below, gray shaded block represents delay elements while white block indicates combinational circuit with logic delay mentioned inside the block using red numerical value.



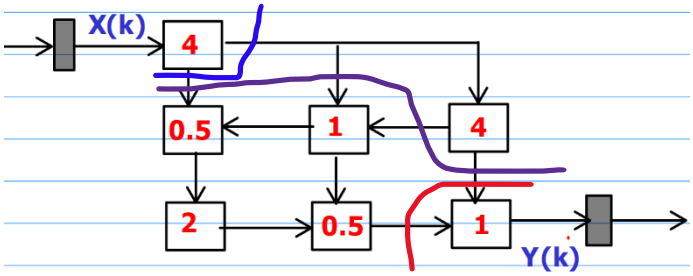
- Identify the critical path delay of the circuit and explain your answer.



Critical path of the circuit is the path which highest delay between the two registers. In this circuit, critical path delay is 13 units

1 Mark

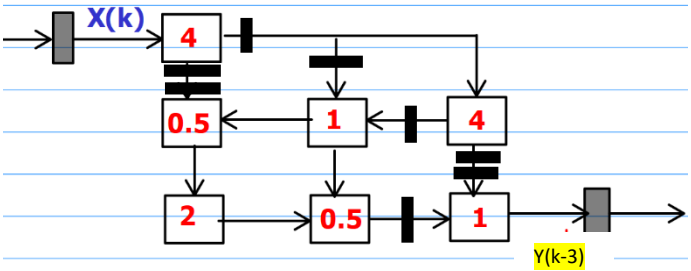
- Pipeline the circuit using minimum number of flip flops (show pipelined paths) and mention the critical path delay of the pipelined circuit. (Zero marks if cut-set retiming is wrong)



To pipeline this circuit, minimum possible critical path delay is 4 units. Hence, we need three cutset retiming as shown above.

4 Marks

- Draw the pipelined circuit



1 Mark

2. Consider Zynq SoC with memory mapped IO where the start or base address for any accelerator in PL must be equal to or higher than 0x0002_0002_0000. The example design consists of five accelerators and their memory requirements in Bytes are given in the table below. Assign appropriate starting or base address to each accelerator. And care must be taken to avoid memory wastage. Calculate the starting and end address of each IP. Support your answer with appropriate explanation. **Short answers will not be evaluated.**

9 Marks

Accelerator Name	Memory Requirement
AXI GPIO1	512M
AXI DMA	2G
AXI BRAM	256K
AXI CDMA	1G
AXI Timer	128K

- The starting address 0x0002_0002_0000 has 17 zeros from LSB. Thus, this address is valid SA only for IP with 128K memory size. Thus, starting and ending address of 128K memory is 0x0002_0002_0000 and 0x0002_0003_FFFF.

2 Marks

- Next, starting address is 0x0002_0004_0000. This has 18 zeros from LSB and hence, it is valid only for IP with 256K memory size. Thus, starting and ending address of 256K memory is 0x0002_0004_0000 and 0x0002_0007_FFFF.

2 Marks

- Next, starting address is 0x0002_0008_0000. This has 19 zeros from LSB and hence, it is not compatible with any of the IP. Next immediate address of 0x0002_2000_0000 is valid for 512M IP due to 29 zeros from LSB. Thus, starting and ending address of 512M memory is 0x0002_2000_0000 and 0x0002_3FFF_FFFF.

2 Marks

- Next, starting address is 0x0002_4000_0000. This has 30 zeros from LSB and hence, it is valid only for IP with 1G memory size. Thus, starting and ending address of 256K memory is 0x0002_4000_0000 and 0x0002_7FFF_FFFF.

2 Marks

- Next, starting address is 0x0002_8000_0000. This has 31 zeros from LSB and hence, it is valid only for IP with 2G memory size. Thus, starting and ending address of 256K memory is 0x0002_8000_0000 and 0x0002_FFFF_FFFF.

2 Marks

ECE270: ELD: End-Sem Lab Exam C (90 Minutes)

Date: December 2, 2023

1. Design an accelerator which performs FFT followed by increment by 1 operation on input data comprising of 16 complex samples of float data type.
   A. Implementation on processor and display the execution time (1 Marks)
   B. Implementation on PL, compare PS and PL outputs and display the execution time (6 marks)
   C. Demonstrate the outputs of logarithm and FFT on ILA (5 marks)
   D. Viva: Only if Part A and Part B is completed successfully. (2 marks)