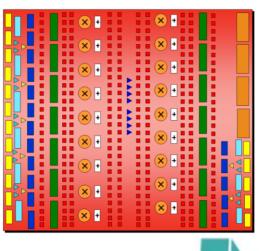


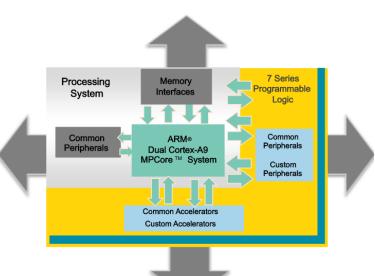




ECE 270: Embedded Logic Design



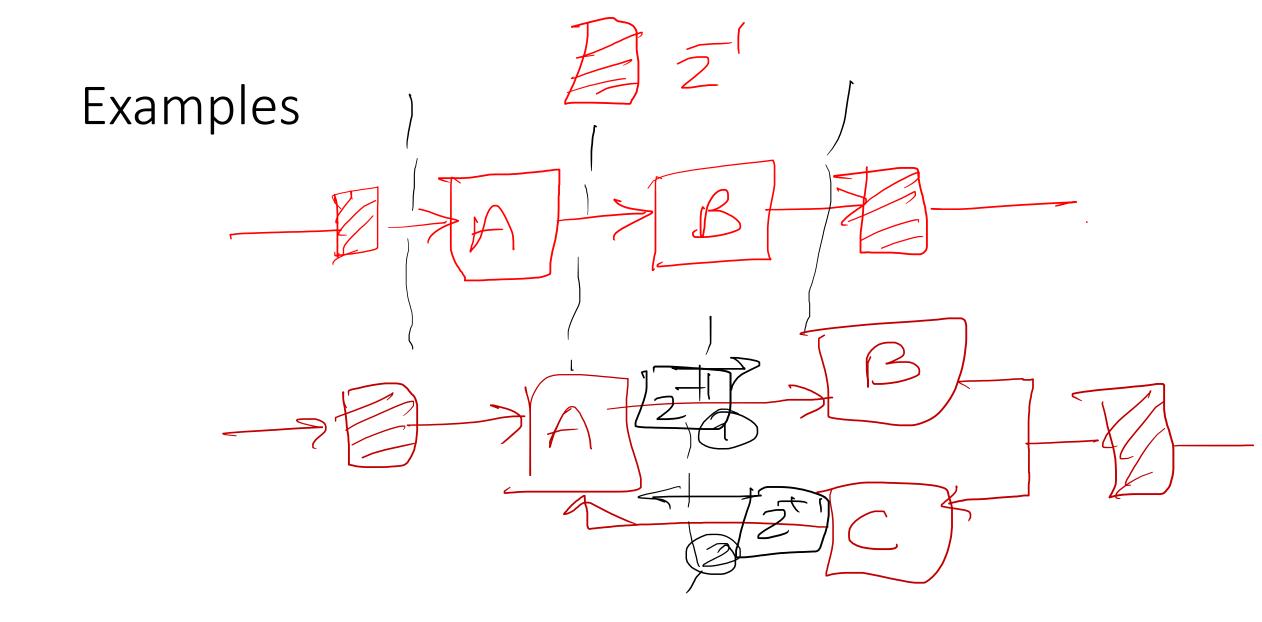




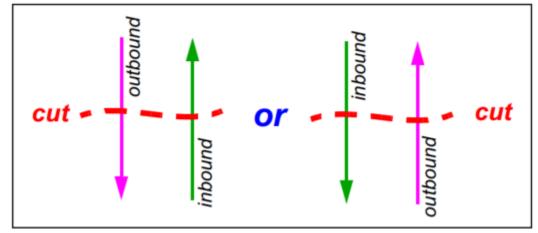
How to Pipeline Architecture?

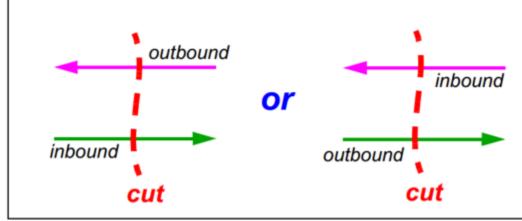
Pipelining Via Cut Set Retiming

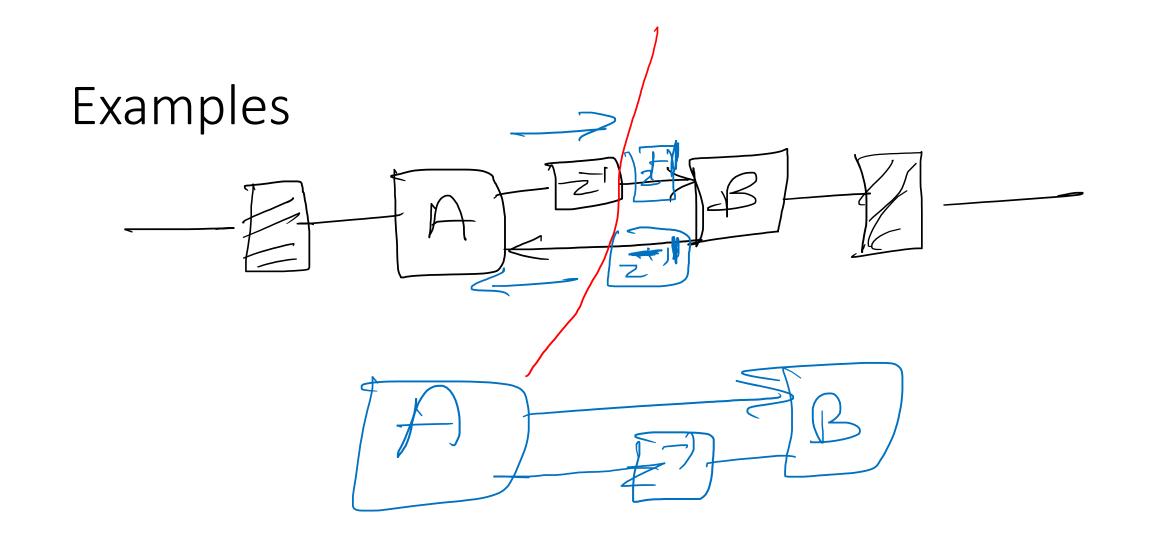
- One of the most powerful and valuable digital design strategies but simple to understand and use
- A cut-set is a minimal set of edges which partitions the architecture into two separable parts.

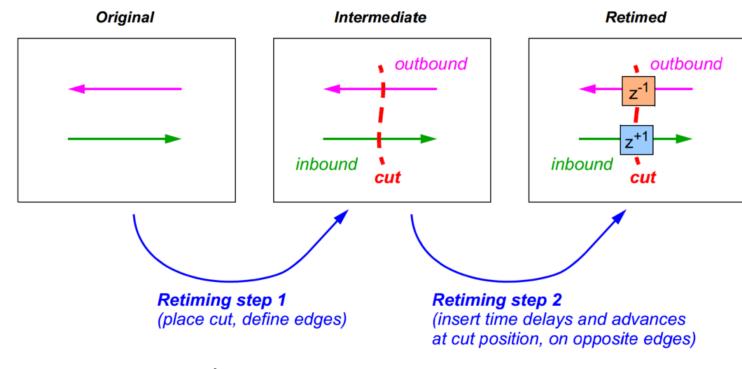


- Delay Transfer Rule: We can advance and/or delay the various edges in the architecture depending on their directions.
- A cut is drawn on the architecture and all signal connections passing into it from one direction are defined as inbound and those passing in the opposite direction as outbound.
- The cut can be drawn in any direction.

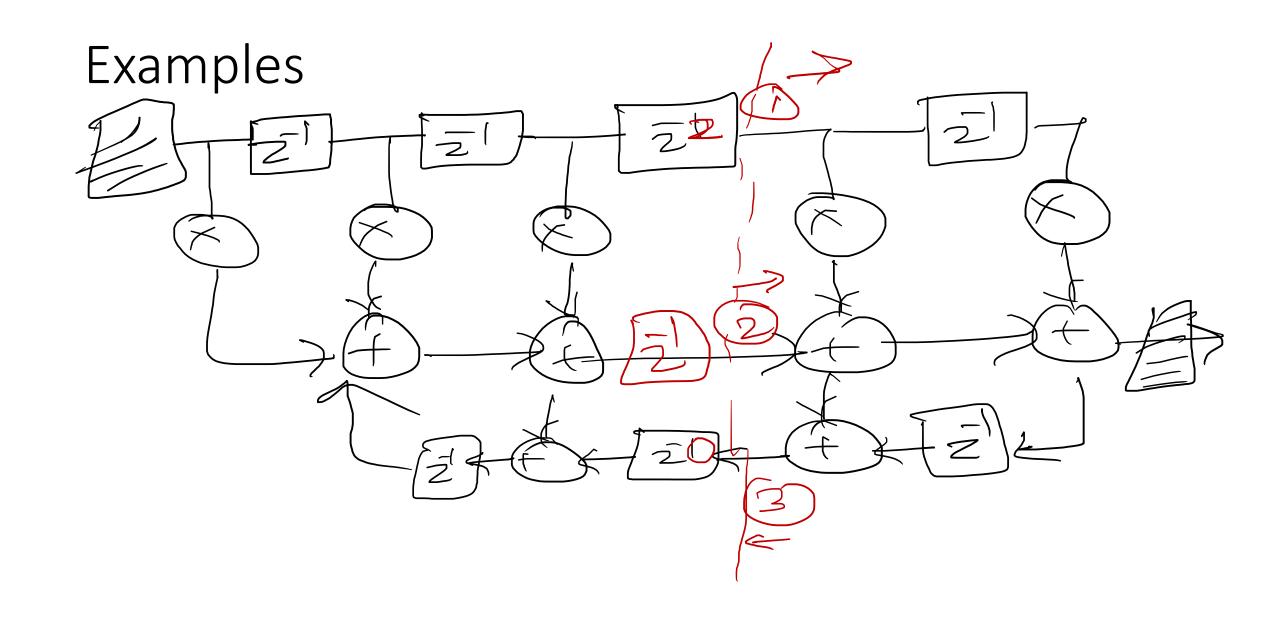


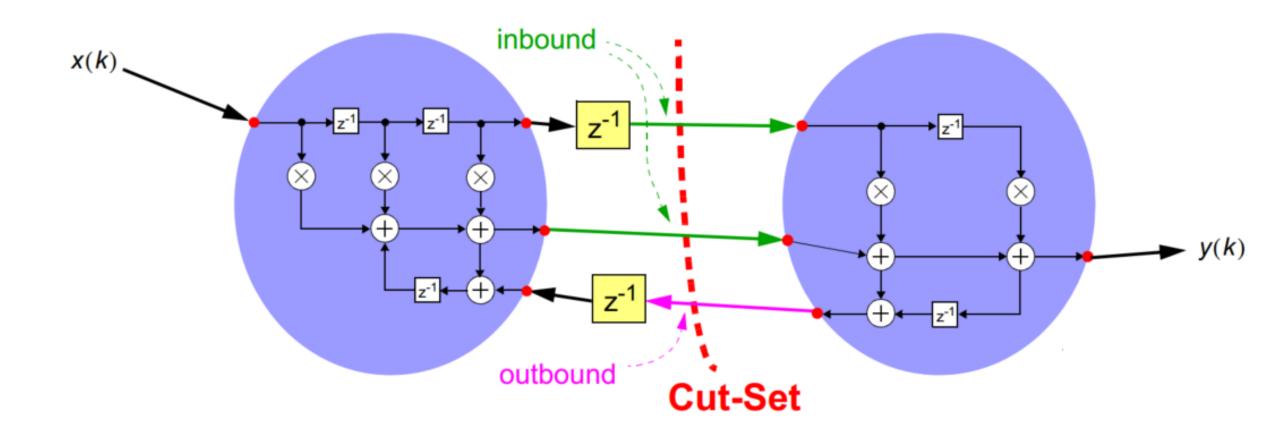


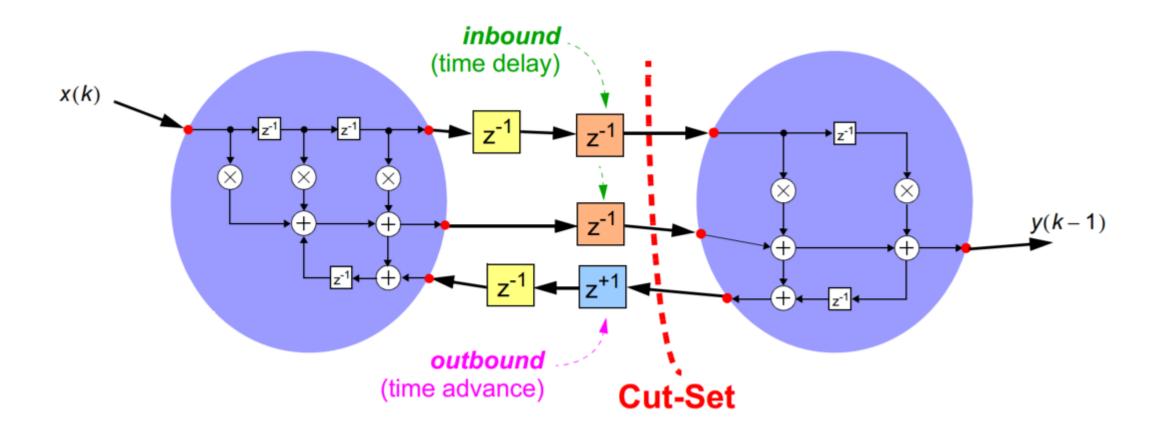




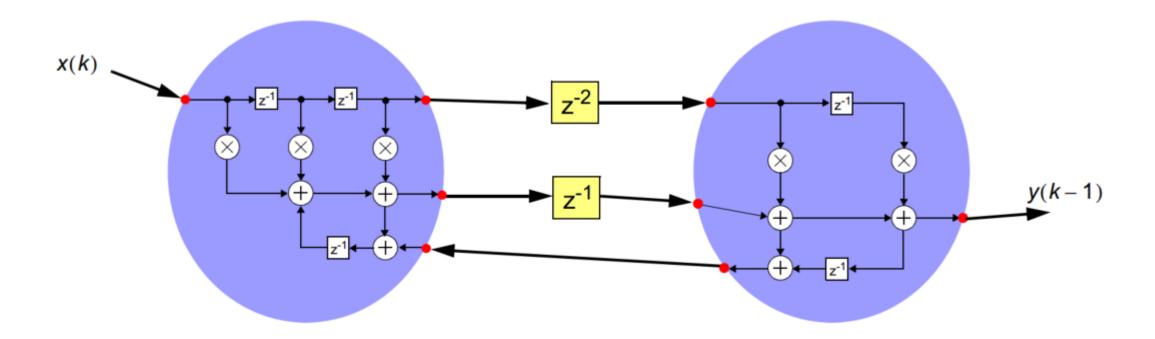
- Delay Transfer Rule: We can advance and/or delay the various edges in the architecture depending on their directions.
- We then apply a time advance to the inbound edges and a time delay to the outbound edges or vice-versa.
- We could also have chosen the opposite.
- New delays and advances are then consolidated with existing delays.



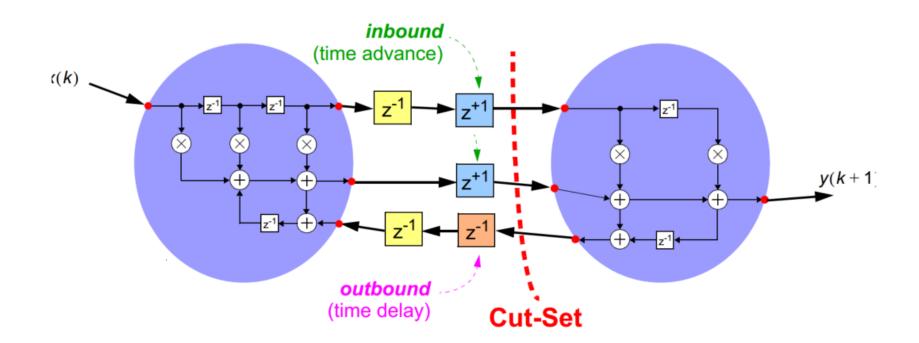




After Delay consolidation -> Successful cut set retiming



Examples



- Failed cut set retiming
- Architecture with advance delays is not synthesizable (Non-causal).
- Time advance is look ahead in time which is impossible.
- Care must be taken when performing cut set retiming: The delays and advances should be allocated to inbound and outbound edges such that resultant architecture is causal.

Cut Set Retiming: Latency

- 1 Sample of latency has been introduced as a result of the retiming
- In most applications, slight increase in latency is not usually a problem but we should keep track of it in order to maintain correct functionality.

