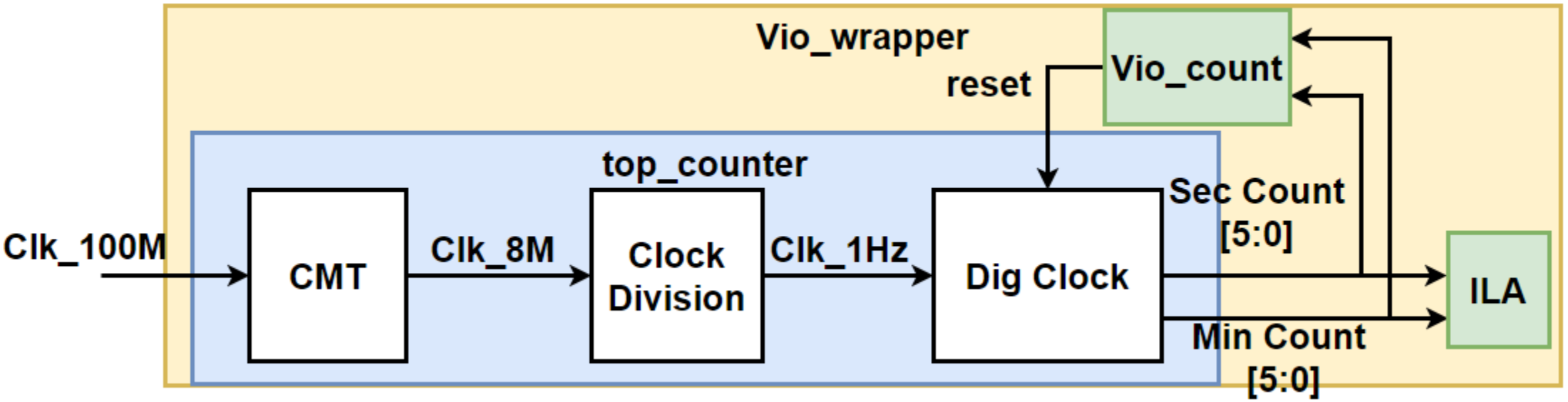
ELD Lab 5
Design of Digital Clock

Objective

- Design digital clock with Second and Minute Display using behavioral modelling
- Verify the circuit using virtual input and output (VIO) and Integrated Logic Analyzer.
- **Lab Homework:** Design the counter with output sequence as 4-> 6 -> 8 -> 4 -> 6 -> 8 …….

Lab

Proposed Approach (Extension of Lab 3)



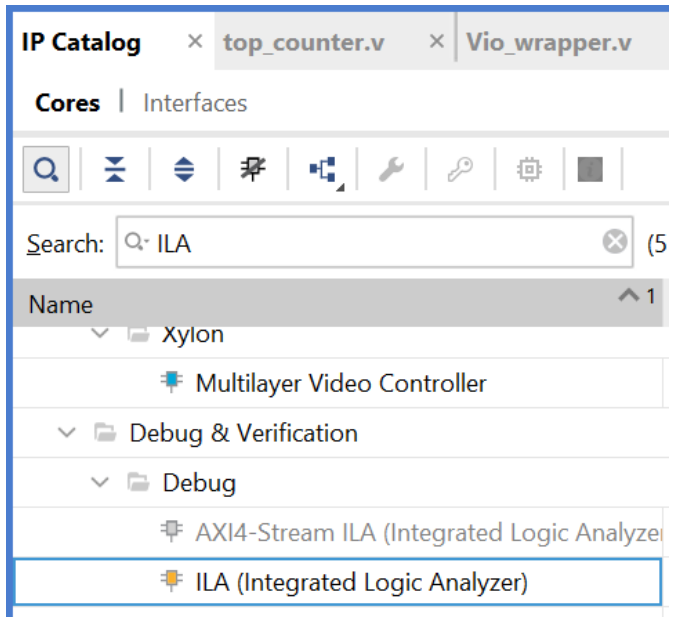
Digital Clock

```
module Dig_clock(
    input Clk_1Hz,
    input reset,
    output [5:0] Sec_Count,
    output [5:0] Min_Count
    );
```

```
reg [5:0] Sec_Count_next;
reg [5:0] Sec_Count_reg=0;
always@(posedge Clk_1Hz or posedge reset)
begin
    if(reset)
        Sec_Count_reg <= 0;
    else
        Sec_Count_reg <= Sec_Count_next;
end
always@(*)
begin
    if(Sec_Count_reg == 59)
        Sec_Count_next = 0;
    else
        Sec_Count_next = Sec_Count_reg + 1;
end
```

```
reg [5:0] Min_Count_next;
reg [5:0] Min_Count_reg=0;
always@(posedge Clk_1Hz or posedge reset)
begin
    if(reset)
        Min_Count_reg <= 0;
    else
        Min_Count_reg <= Min_Count_next;
end
always@(*)
begin
    if(Sec_Count_reg == 59)
        if(Min_Count_reg == 59)
            Min_Count_next = 0;
        else
            Min_Count_next = Min_Count_reg + 1;
    else
        Min_Count_next = Min_Count_reg;
end
assign Sec_Count = Sec_Count_reg;
assign Min_Count = Min_Count_reg;
```

ILA



Component Name: ILA_count

To configure more than 64 probe ports use Vivado Tcl

General Options | **Probe_Ports(0..2)**

Probe Port	Probe Width [1..4096]	Num
PROBE0	1	1
PROBE1	6	1
PROBE2	6	1

Component Name: ILA_count

To configure more than 64 probe ports use Vivado Tcl Console

General Options | Probe_Ports(0..2)

Monitor Type

(•) Native ( ) AXI

Number of Probes: 3 [1...1024]

Sample Data Depth: 1024

[x] Same Number of Comparators for All Probe Ports

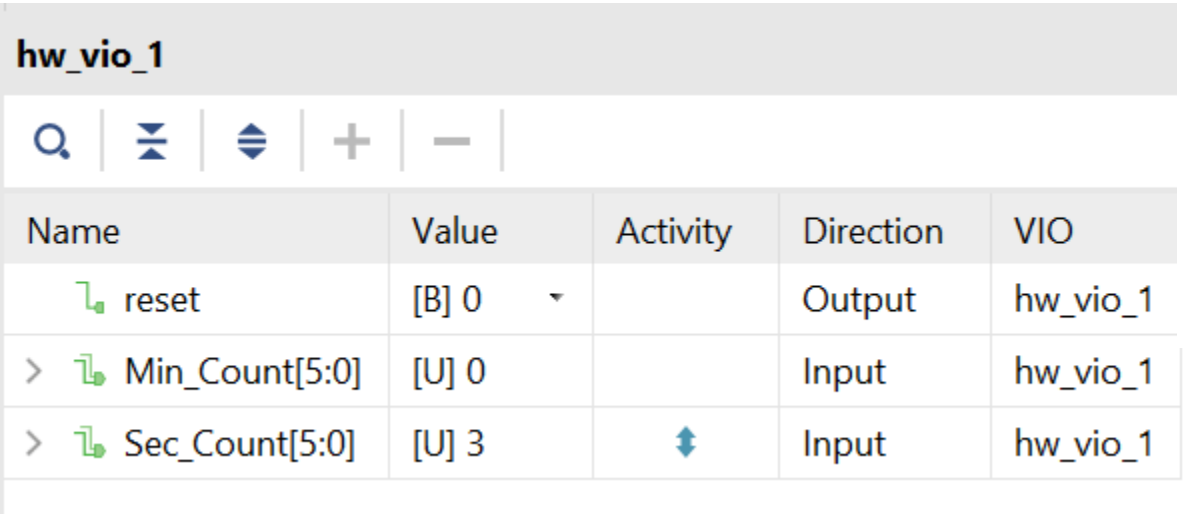
Number of Comparators: 1

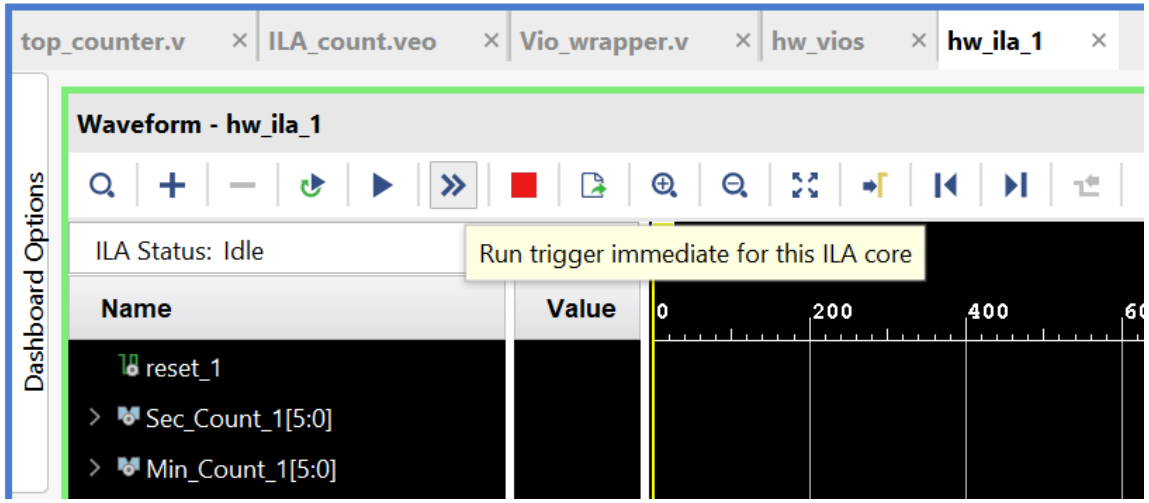
[ ] Trigger Out Port

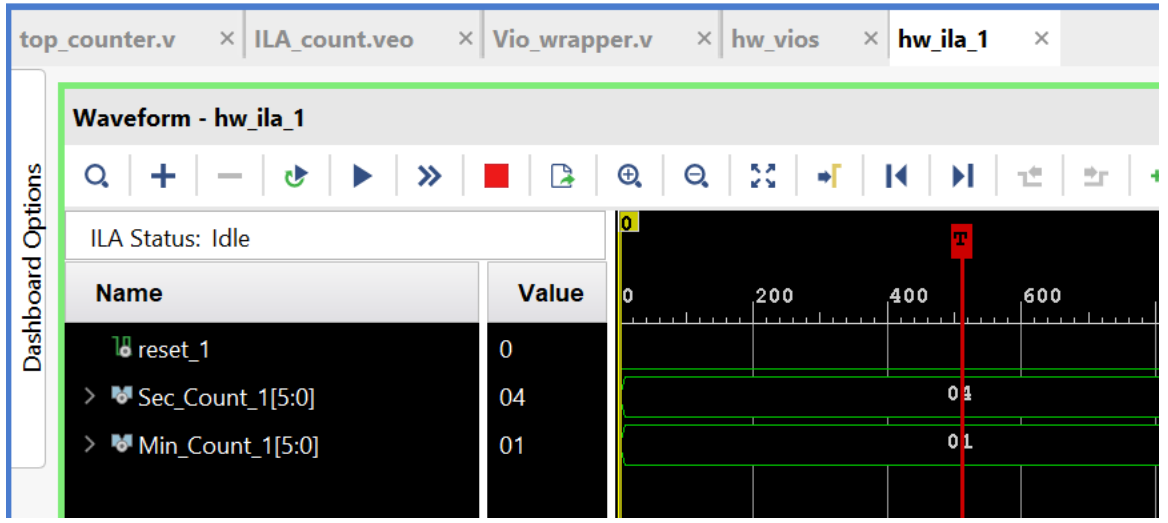
[ ] Trigger In Port

Input Pipe Stages: 0

Demo


hw_vio_1
Name
Value
Activity
Direction
VIO
reset
[B] 0
Output
hw_vio_1
Min_Count[5:0]
[U] 0
Input
hw_vio_1
Sec_Count[5:0]
[U] 3
Input
hw_vio_1


top_counter.v
ILA_count.veo
Vio_wrapper.v
hw_vios
hw_ila_1
Waveform - hw_ila_1
Dashboard Options
ILA Status: Idle
Run trigger immediate for this ILA core
Name
Value
reset_1
Sec_Count_1[5:0]
Min_Count_1[5:0]
0
200
400


top_counter.v
ILA_count.veo
Vio_wrapper.v
hw_vios
hw_ila_1
Waveform - hw_ila_1
Dashboard Options
ILA Status: Idle
Name
Value
reset_1
0
Sec_Count_1[5:0]
04
Min_Count_1[5:0]
01
0
200
400
600
T
04
01