ECE270: ELD: End-Sem Theory Exam B (30 Minutes)

Date: December 2, 2023

1. Explain the various tasks of snoop control unit in Zynq SoC. (3 Marks)
   - SCU is mainly responsible for data coherency between L1 cache, L2 cache and DDR memory.
   - The access and priority to L2 cache by the two cores of processor is controlled by SCU.
   - ACP accesses L1, L2, DDR and OCM via SCU.

   3 Marks for 3 relevant tasks

2. Discuss various steps involved in the boot process and configuration of Zynq SoC specifically highlighting the roles of BootROM, OCM and FSBL. (5 Marks)
   - The processors in the PS always boot first, allowing a software centric approach for PL configuration.
   - The boot process is multi-stage and minimally includes the boot ROM and the first-stage boot loader (FSBL). For example, Zynq-7000 AP SoC includes a factory-programmed boot ROM (stage 0 boot code) that is not user accessible.

   1 Marks

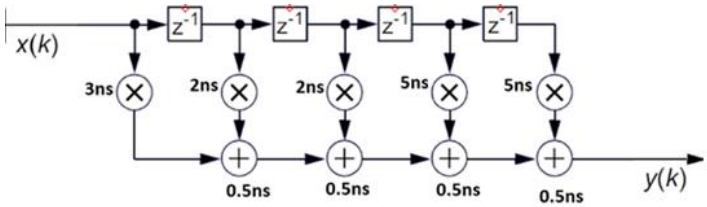
   - The main tasks of the BootROM (initialized at power-on) are to configure one of the ARM core, read the mode pins to determine the primary boot device, copy the Boot Image FSBL from the boot device to the on-chip memory (OCM), and then branch the code execution to the OCM. It finishes once it is satisfied that it can execute the FSBL.
   - PL is not configured by BootROM

   2 Marks

   - FSBL is typically stored in one of the flash memory or can be download through the JTAG
   - The FSBL/User code executes after the BootROM is finished.
   - The FSBL/User code reconfigures the PS as needed and optionally configures the PL.
   - The FSBL/User code operations:
     - Initialize the PS using the PS7 Init data that is generated by Vivado tools (MIO, DDR, etc.)
     - Program the PL using a bitstream (if provided).
     - Load the second stage bootloader or bare-metal application code into DDR memory.
     - Hand off system control to the second stage bootloader or bare-metal application.

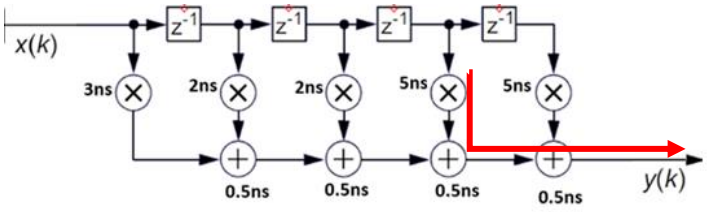
   2 Marks

3. Consider the circuit to realize finite impulse response (FIR) filter using convolution operation is shown below. The circuit has two arithmetic blocks: 1) Multiplier, and 2) Adder. Ignoring the internal delays of flip-flops as well as routing delays, find out the maximum clock frequency at which the circuit can be clocked? Then, pipeline the circuit **using minimum number of flip-flops.** Find out the maximum clock frequency at which the pipelined circuit can be clocked. Draw the architecture of the pipelined circuit (7 Marks)



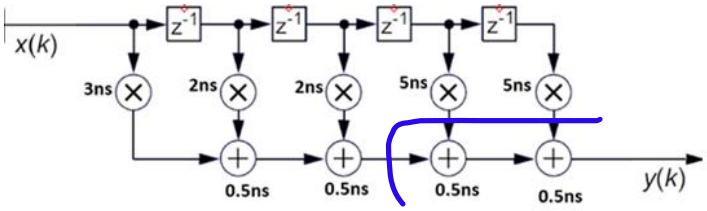
   - Maximum clock frequency depends on the critical path delay. For the critical path identified below, maximum clock frequency is 1/6 GHz.

1 Marks

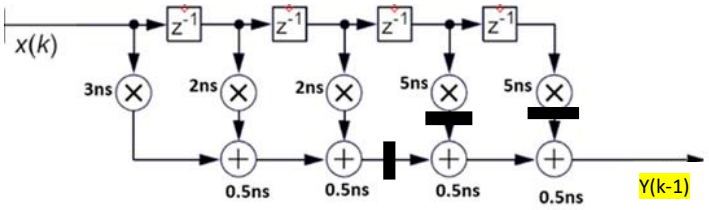


- The optimal pipelined circuit can be applied using following cutset retiming

3 Marks



- Newly pipelined circuit is given as



- New clock frequency is 1/5 GHz.

1 Marks

ECE270: ELD: End-Sem Lab Exam B (90 Minutes)

Date: December 2, 2023

1. Design an accelerator which performs square root operation followed by FFT on input data comprising of 32 complex samples of float data type.
    A. Implementation on processor and display the execution time (1 Marks)
    B. Implementation on PL, compare PS and PL outputs and display the execution time (6 marks)
    C. Demonstrate the outputs of logarithm and FFT on ILA (5 marks)
    D. Viva: Only if Part A and Part B is completed successfully. (2 marks)