ELD Lab 2
Verification of Full Adder on FPGA

Objective

- Implement a 4-bit adder for unsigned inputs using Full Adder on FPGA
- Verify using virtual input and output (VIO).
- **Lab Homework:** Verify 4-bit adder/subtractor circuit for signed numbers on FPGA using VIO

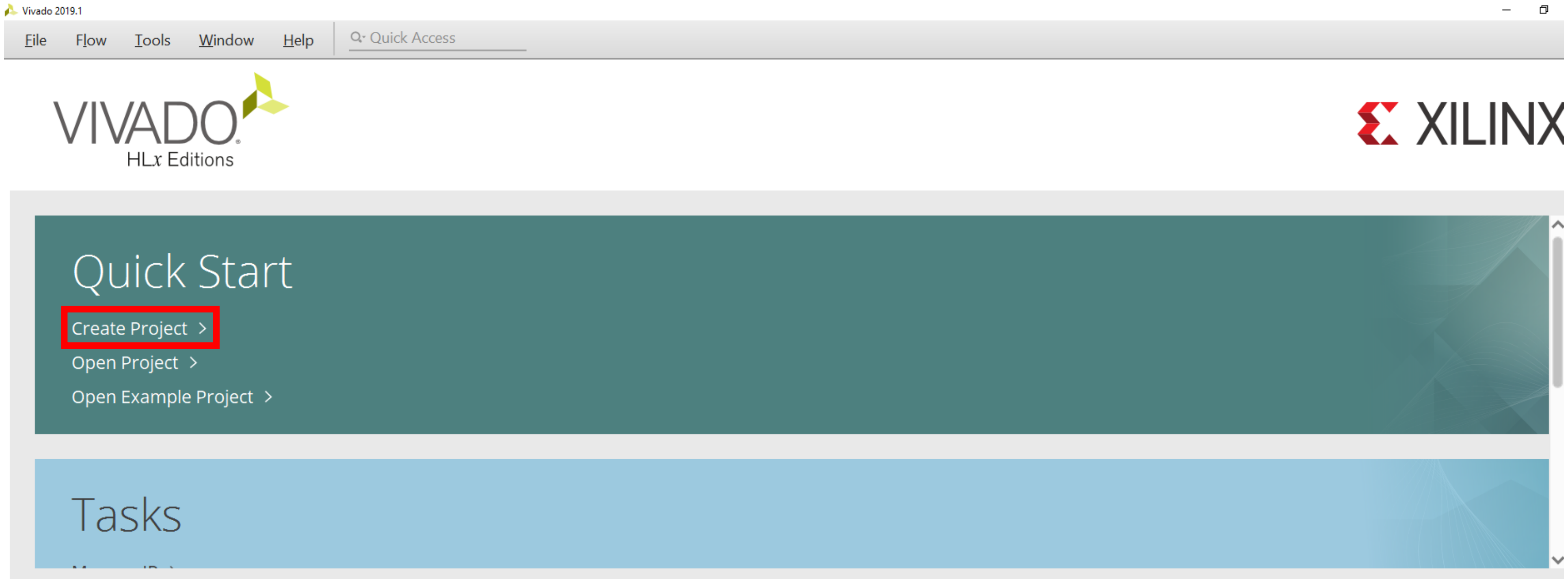
Verilog Revision

Lab

Proposed Approach

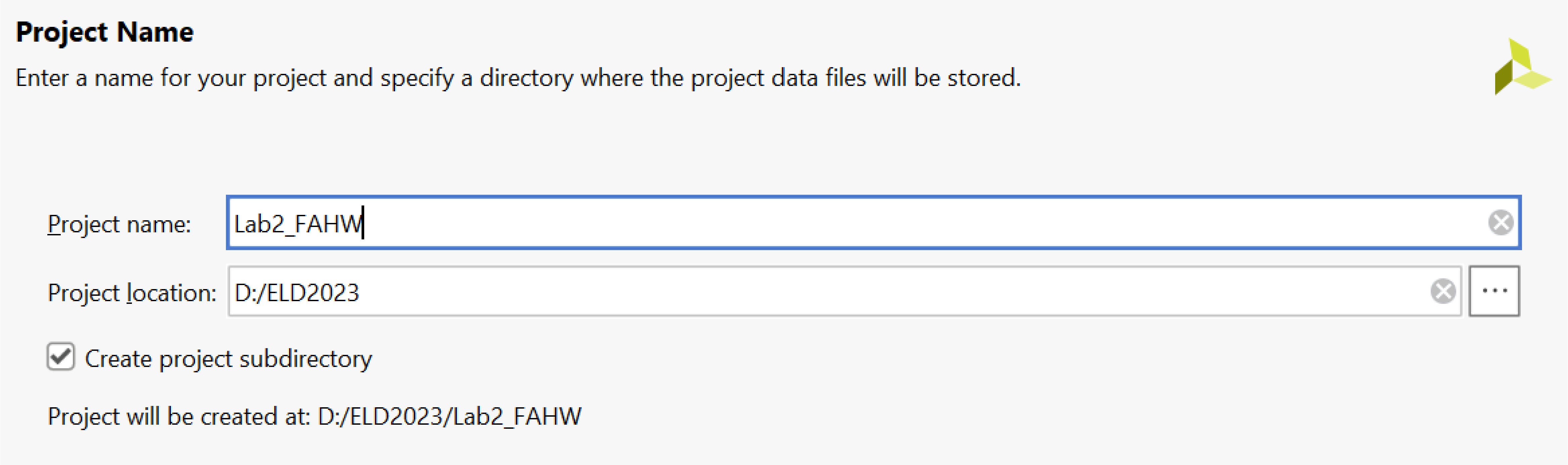
Open the Vivado

- Select Create Project and click on Next



Open the Vivado

- Select appropriate project folder.
- Avoid windows folder and space in address



Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

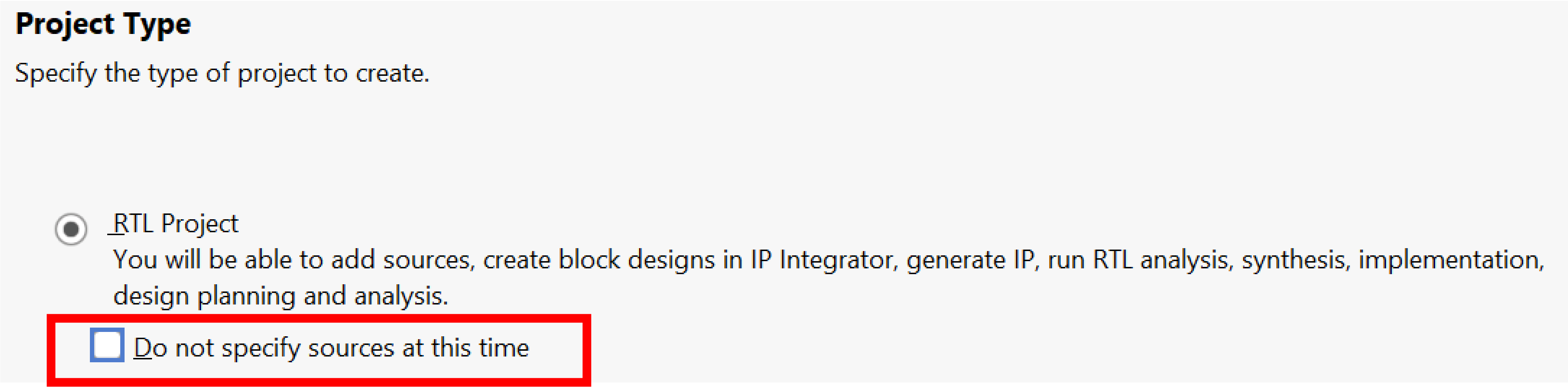
Project name: Lab2_FAHW

Project location: D:/ELD2023

☑ Create project subdirectory

Project will be created at: D:/ELD2023/Lab2_FAHW

Add Files Manually



Project Type

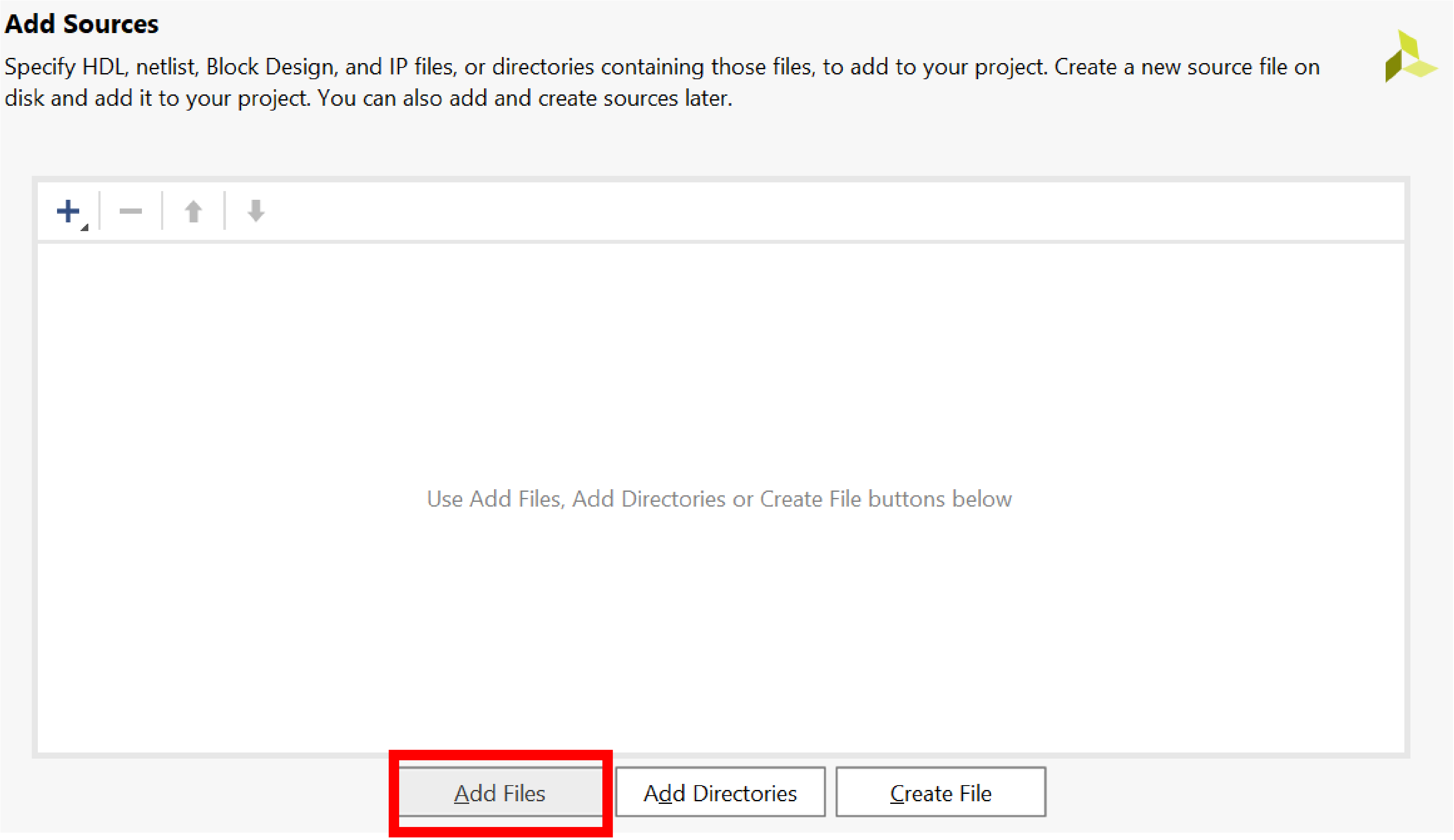
Specify the type of project to create.

● RTL Project

You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

□ Do not specify sources at this time

Add Files Manually

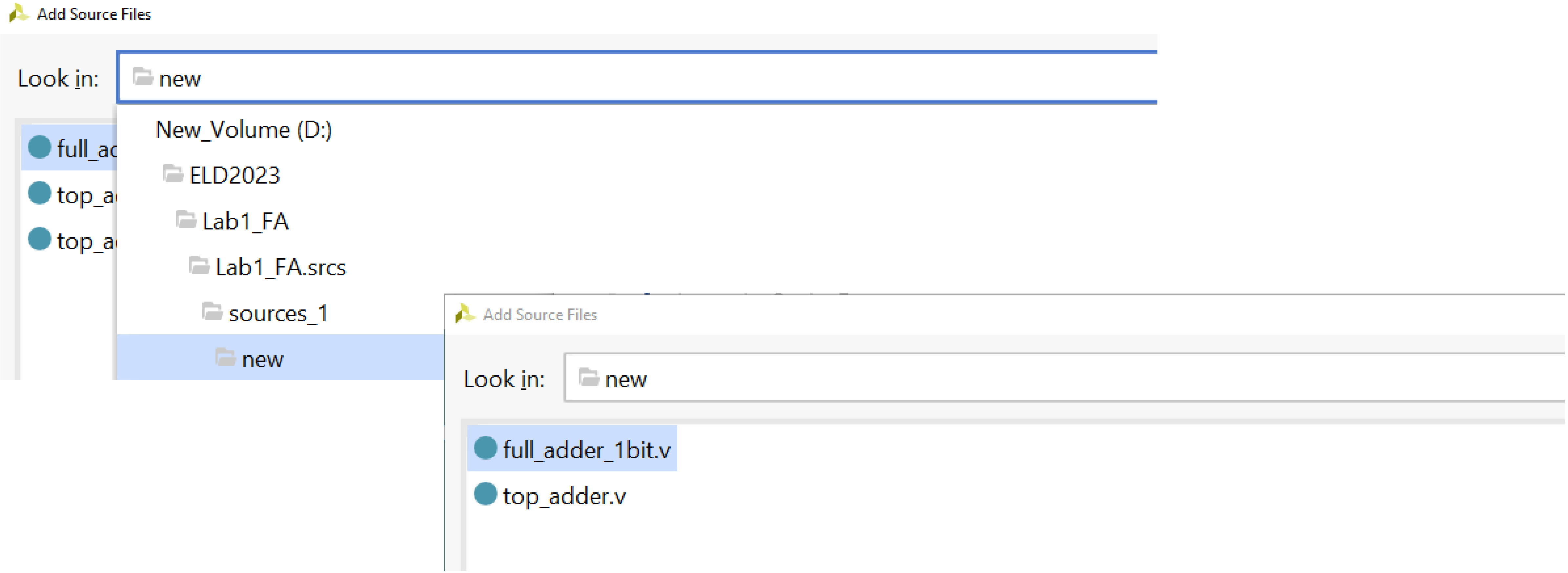


Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

Add Files Manually



Add Source Files

Look in: new

New_Volume (D:)
ELD2023
Lab1_FA
Lab1_FA.srcs
sources_1
new

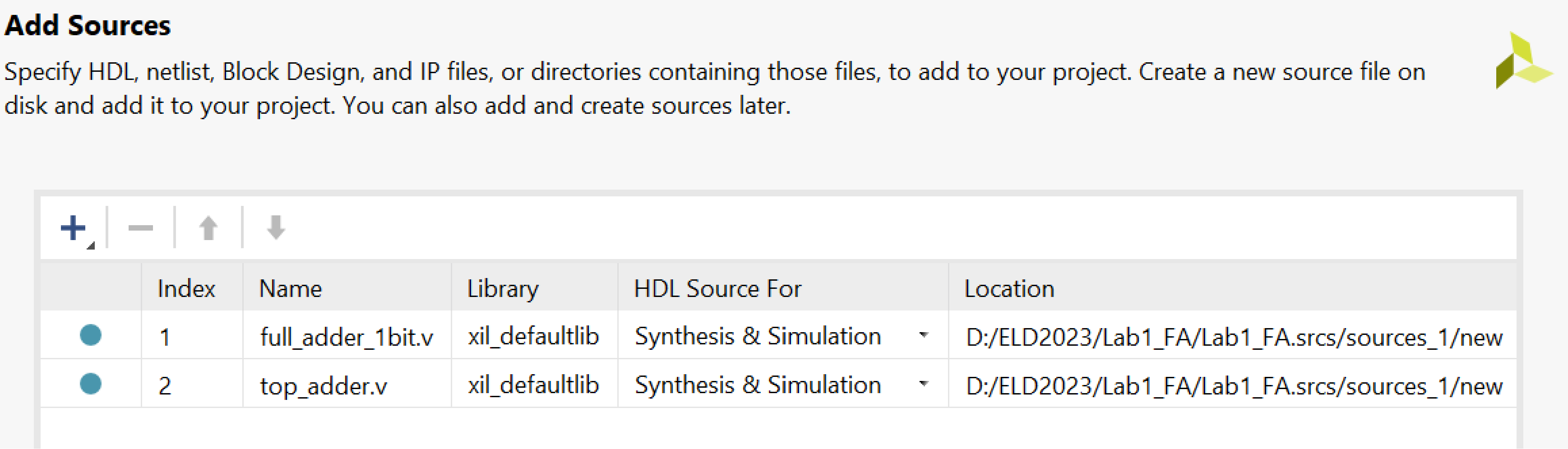
full_ac
top_a
top_a

Add Source Files

Look in: new

full_adder_1bit.v
top_adder.v

Add Files Manually

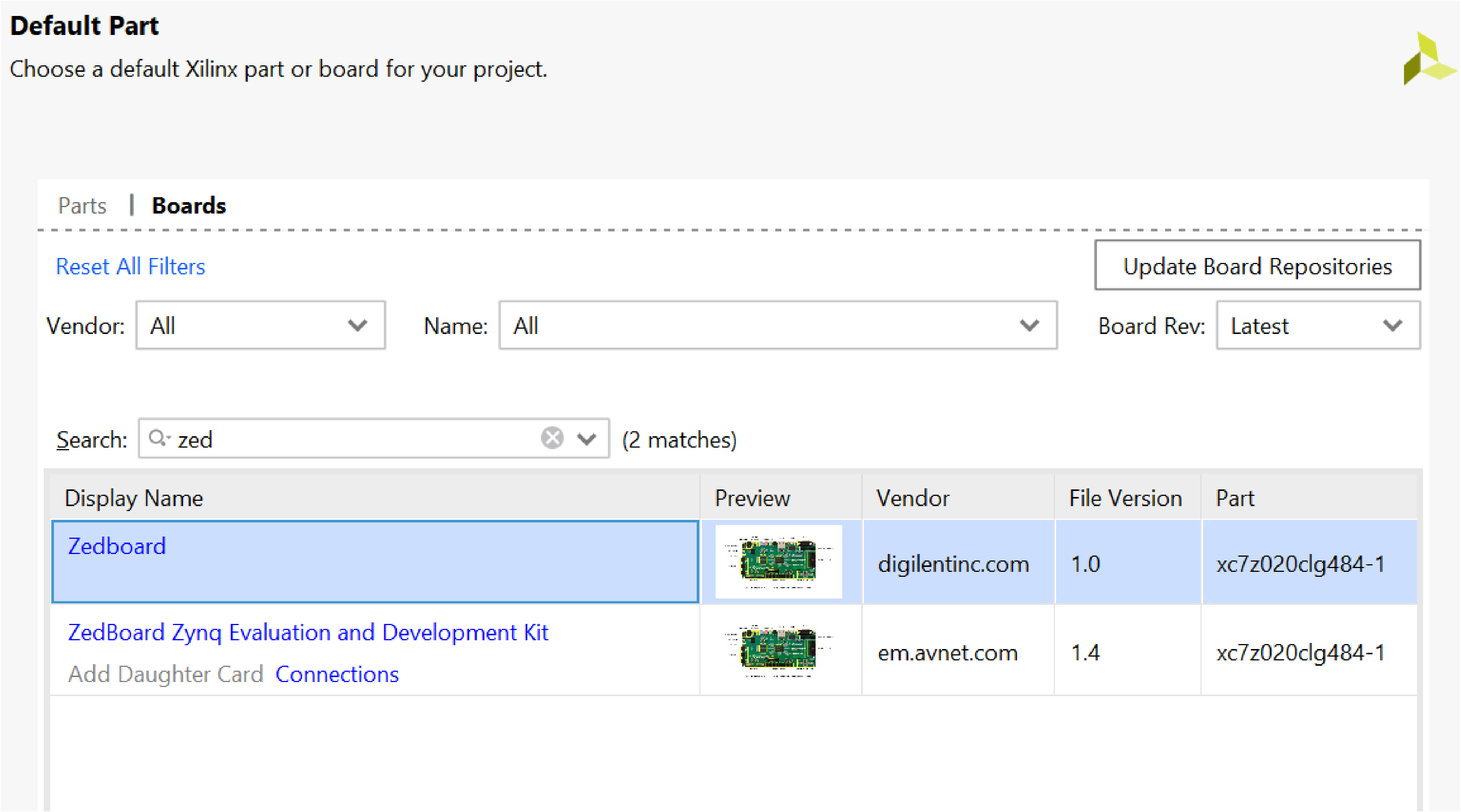


Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

	Index	Name	Library	HDL Source For	Location
●	1	full_adder_1bit.v	xil_defaultlib	Synthesis & Simulation	D:/ELD2023/Lab1_FA/Lab1_FA.srcs/sources_1/new
●	2	top_adder.v	xil_defaultlib	Synthesis & Simulation	D:/ELD2023/Lab1_FA/Lab1_FA.srcs/sources_1/new

Select Zedboard



Default Part

Choose a default Xilinx part or board for your project.

Vendor: All

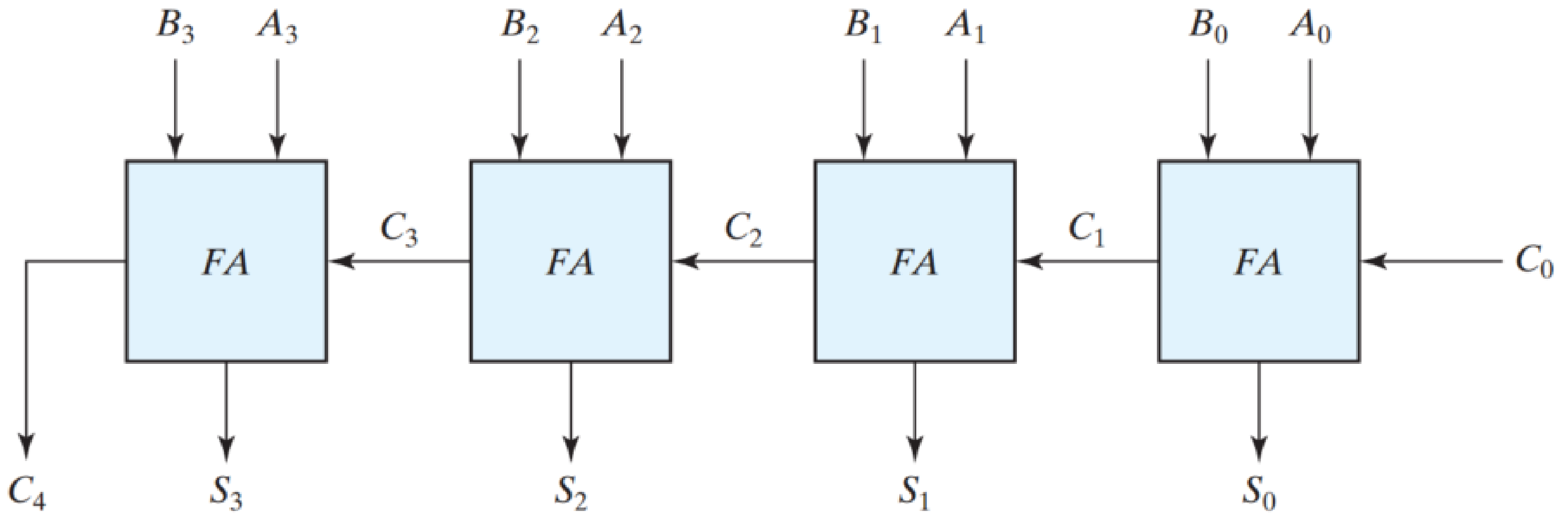
Name: All

Board Rev: Latest

Search: zed (2 matches)

Display Name	Preview	Vendor	File Version	Part
Zedboard		digilentinc.com	1.0	xc7z020clg484-1
ZedBoard Zynq Evaluation and Development Kit Add Daughter Card Connections		em.avnet.com	1.4	xc7z020clg484-1

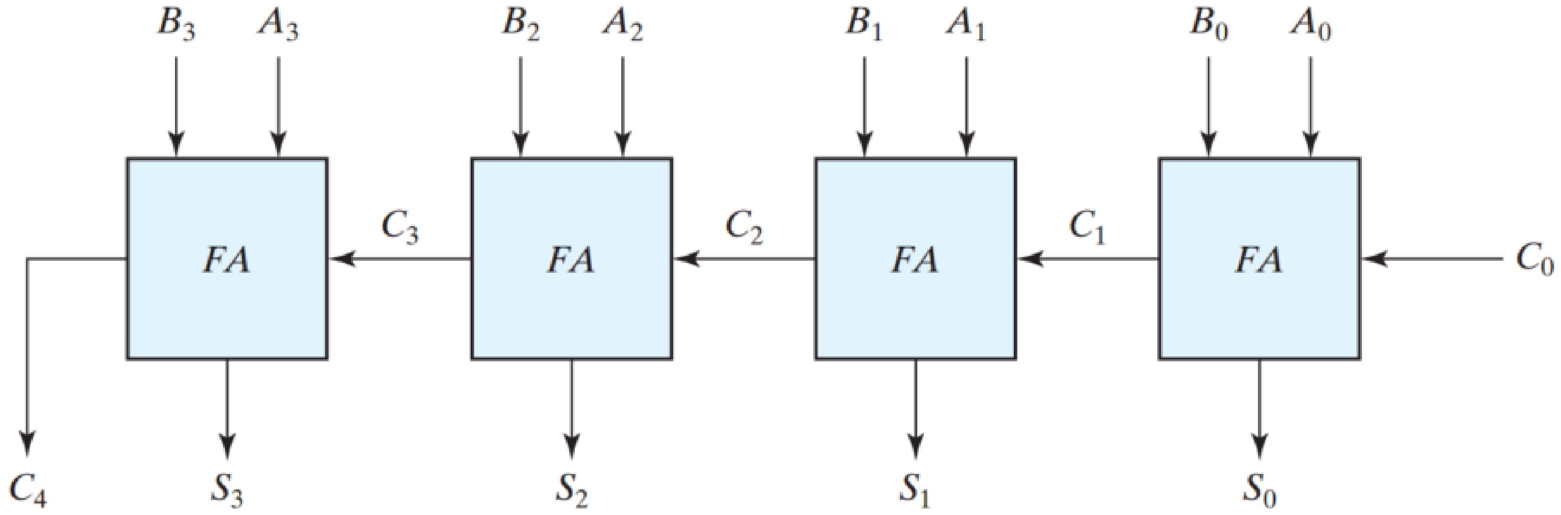
4-bit FA



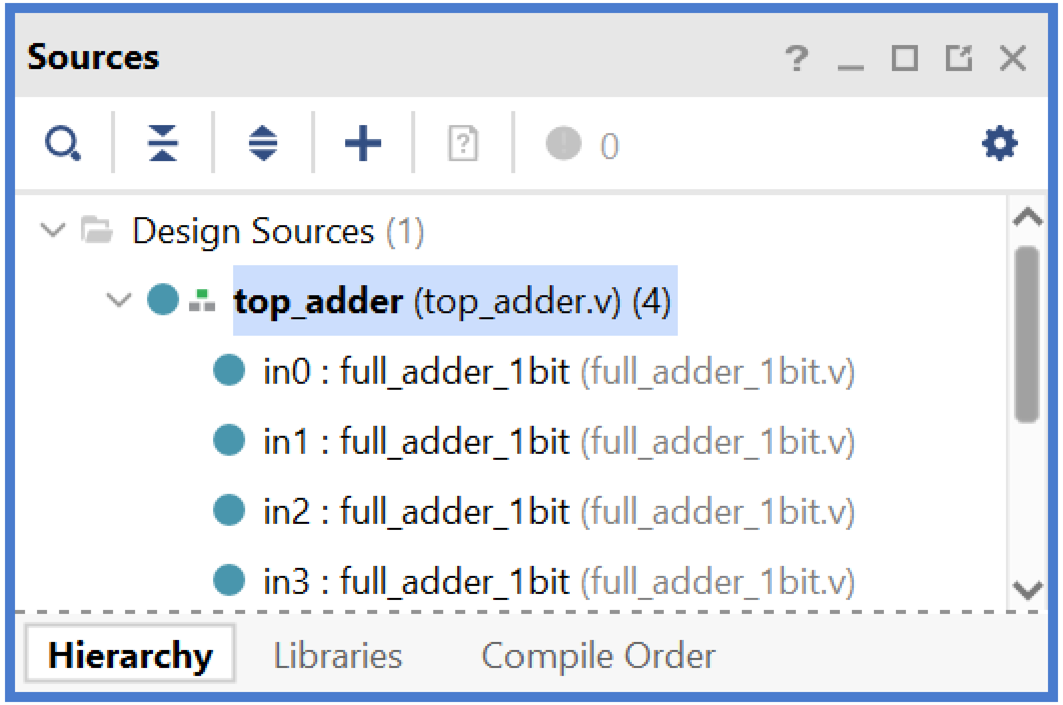
```
module top_adder(
    input [3:0] InA,
    input [3:0] InB,
    output [4:0] OutSum
    );
    
    wire carry1 , carry2, carry3;
    
    full_adder_1bit in0(.FA1_InA(InA[0]) , .FA1_InB(InB[0]) , .FA1_InC(1'b0) , .FA1_OutSum(OutSum[0]) , .FA1_OutC(carry1));
    full_adder_1bit in1(.FA1_InA(InA[1]) , .FA1_InB(InB[1]) , .FA1_InC(carry1) , .FA1_OutSum(OutSum[1]) , .FA1_OutC(carry2));
    full_adder_1bit in2(.FA1_InA(InA[2]) , .FA1_InB(InB[2]) , .FA1_InC(carry2) , .FA1_OutSum(OutSum[2]) , .FA1_OutC(carry3));
    full_adder_1bit in3(.FA1_InA(InA[3]) , .FA1_InB(InB[3]) , .FA1_InC(carry3) , .FA1_OutSum(OutSum[3]) , .FA1_OutC(OutSum[4]));

endmodule
```

4-bit FA



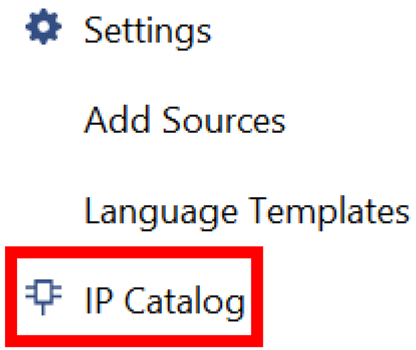
PROJECT MANAGER - Lab1_FA

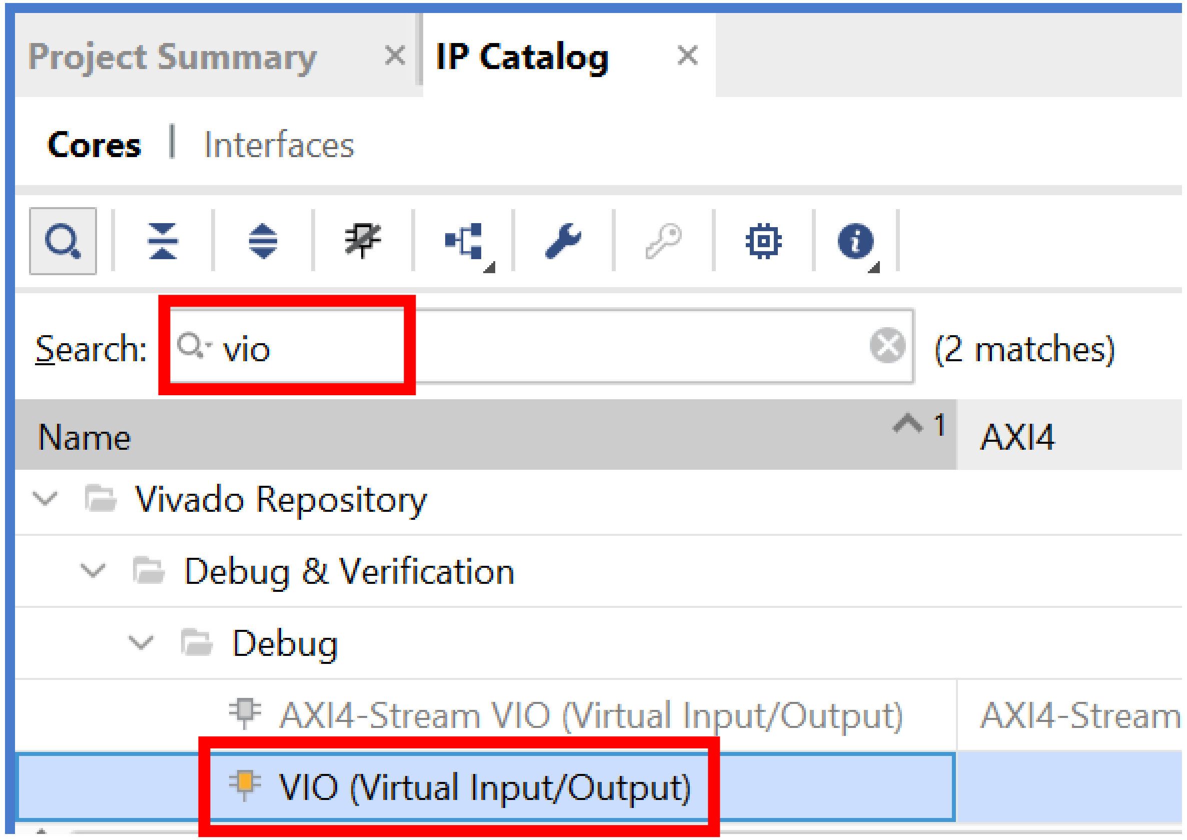


Design Sources (1)

- **top_adder** (top_adder.v) (4)
  - in0 : full_adder_1bit (full_adder_1bit.v)
  - in1 : full_adder_1bit (full_adder_1bit.v)
  - in2 : full_adder_1bit (full_adder_1bit.v)
  - in3 : full_adder_1bit (full_adder_1bit.v)

Select VIO

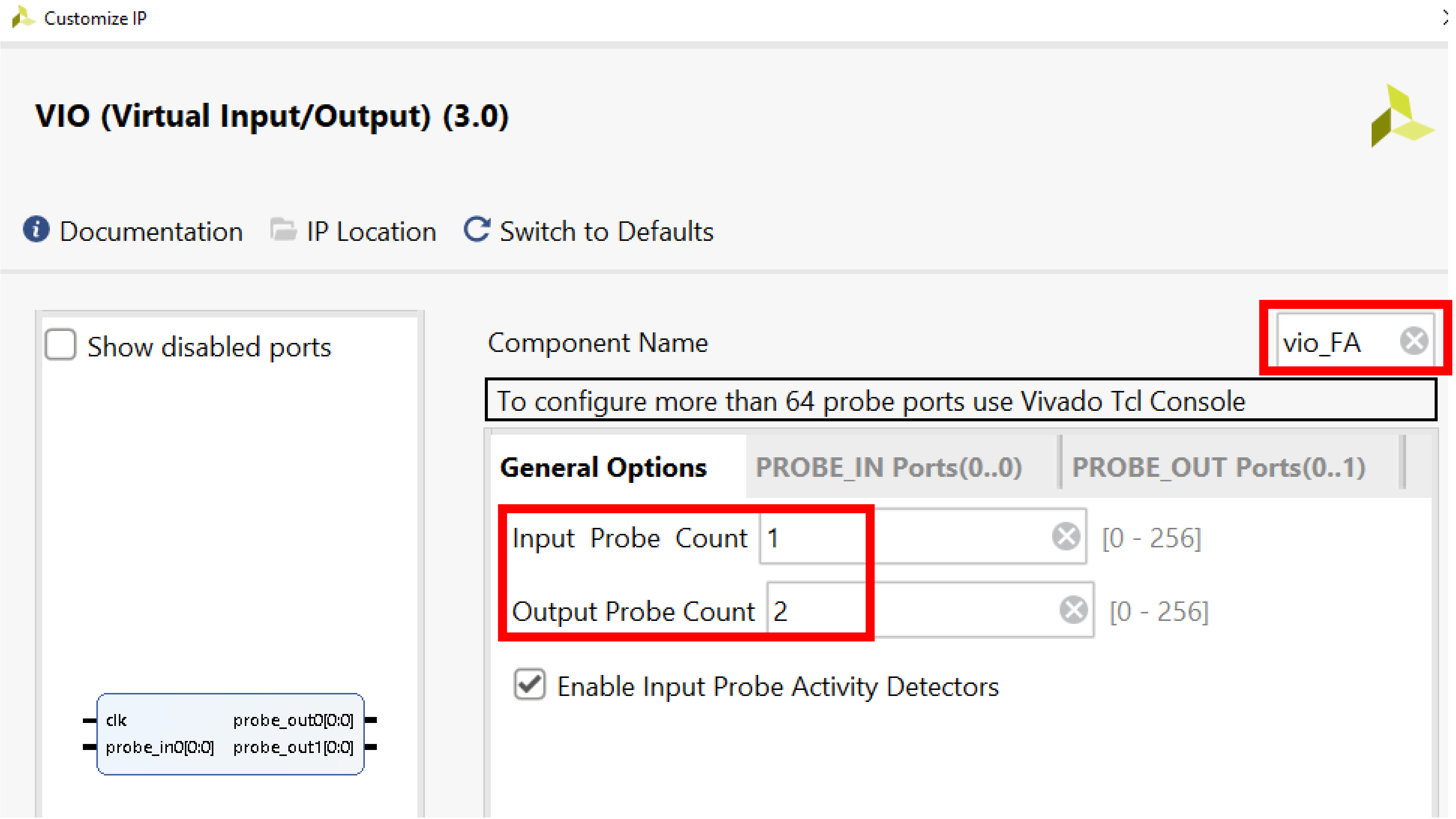




Search: vio (2 matches)

- Vivado Repository
  - Debug & Verification
    - Debug
      - AXI4-Stream VIO (Virtual Input/Output) | AXI4-Stream
      - VIO (Virtual Input/Output)

Select VIO



Customize IP

VIO (Virtual Input/Output) (3.0)

□ Show disabled ports

Component Name: vio_FA

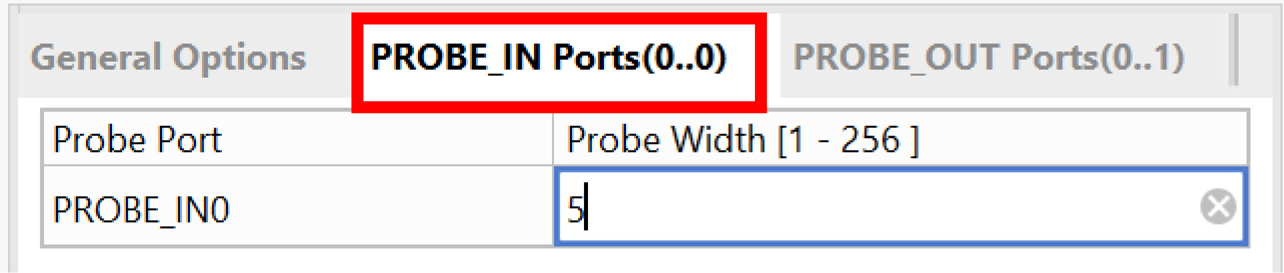
To configure more than 64 probe ports use Vivado Tcl Console

Input Probe Count: 1 [0 - 256]

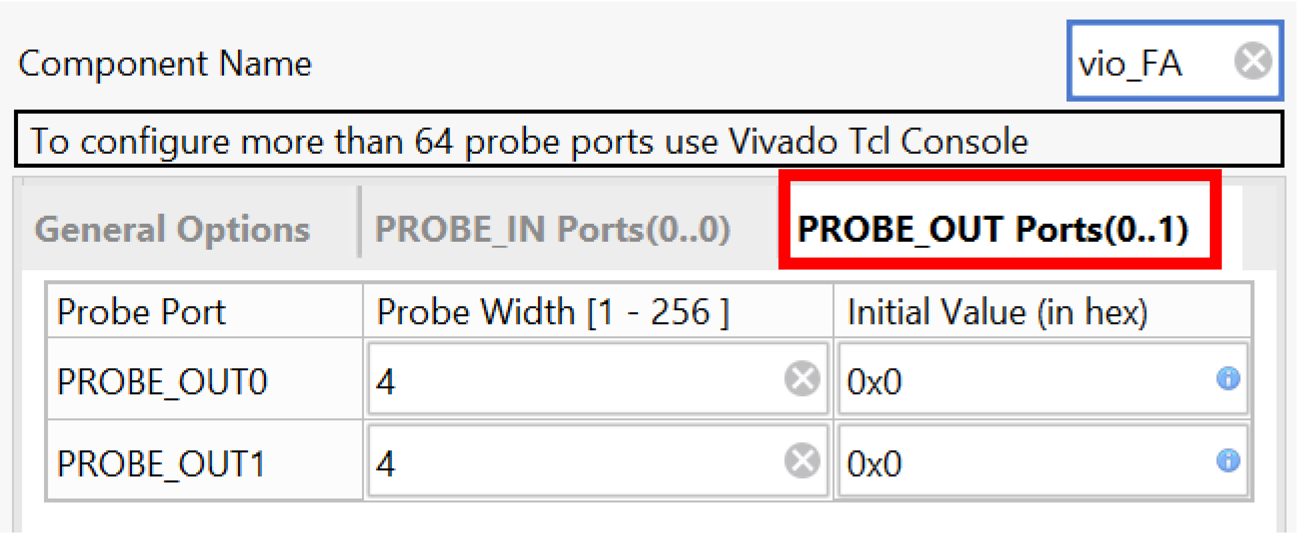
Output Probe Count: 2 [0 - 256]

☑ Enable Input Probe Activity Detectors

Select VIO



Probe Port	Probe Width [1 - 256]
PROBE_IN0	5


Component Name: vio_FA

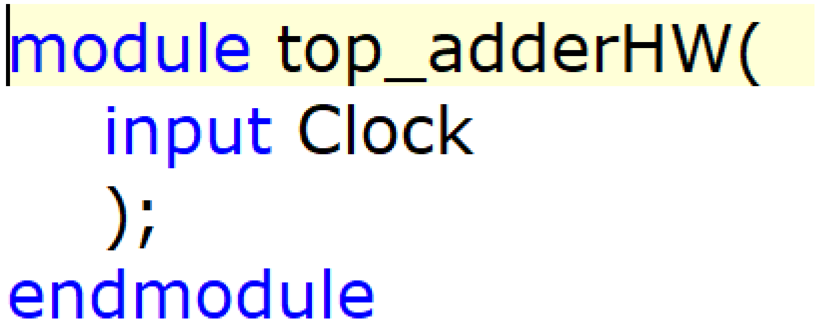
To configure more than 64 probe ports use Vivado Tcl Console

Probe Port	Probe Width [1 - 256]	Initial Value (in hex)
PROBE_OUT0	4	0x0
PROBE_OUT1	4	0x0

Proposed Approach

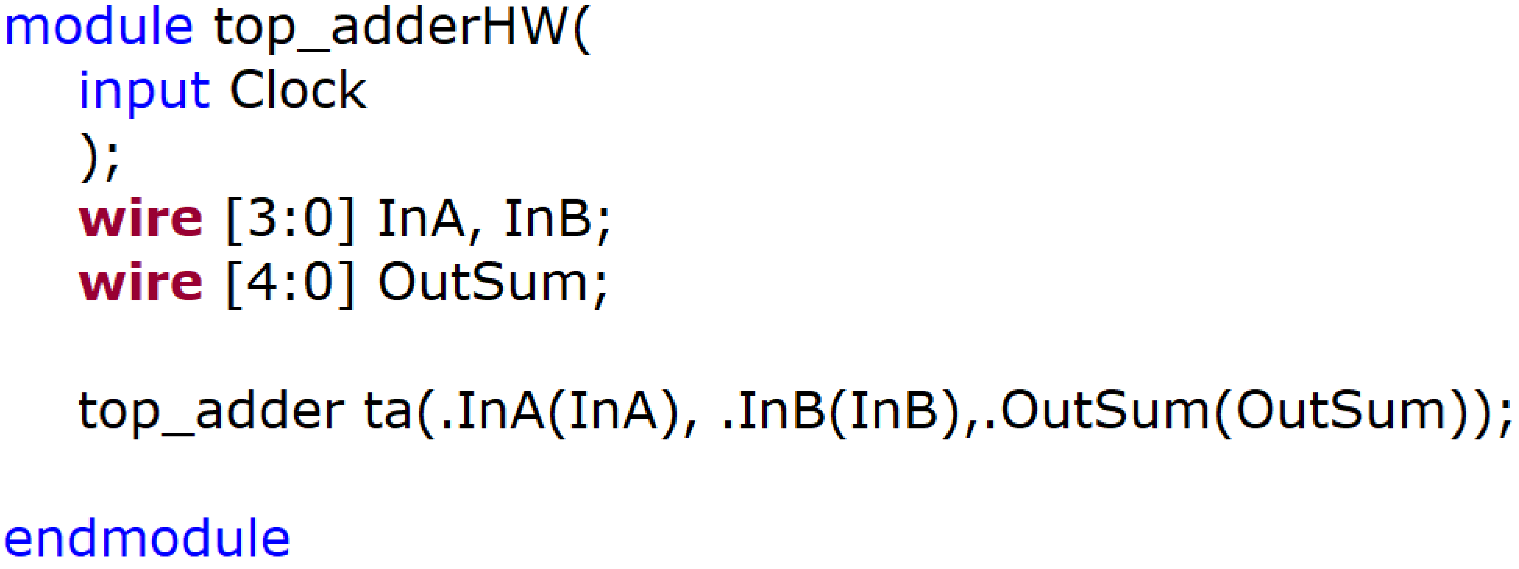
Add New File: top_adderHW

- Only Clock as interface



```
module top_adderHW(
    input Clock
    );
endmodule
```

- Instantiate top_adder

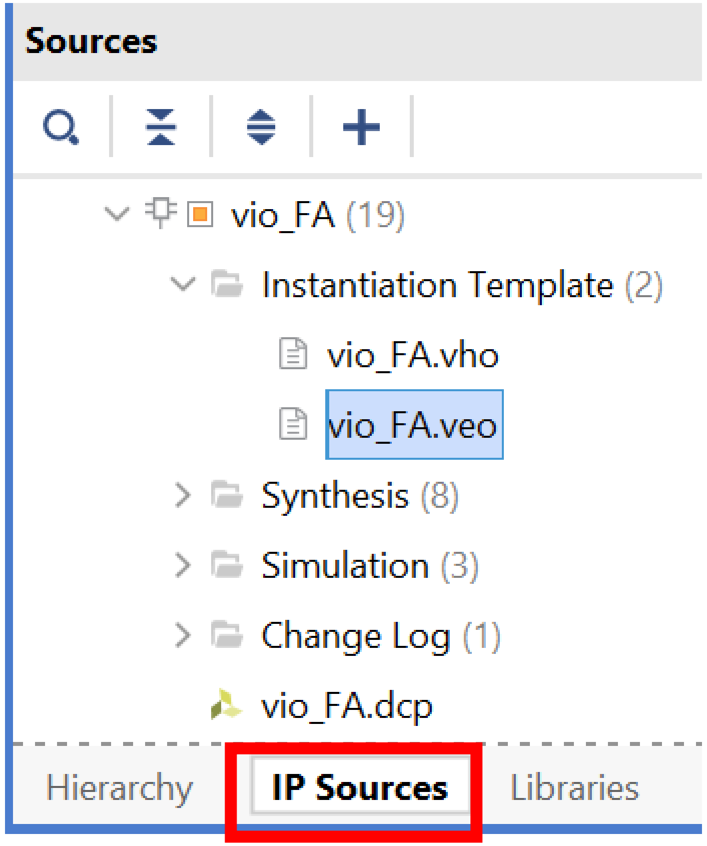


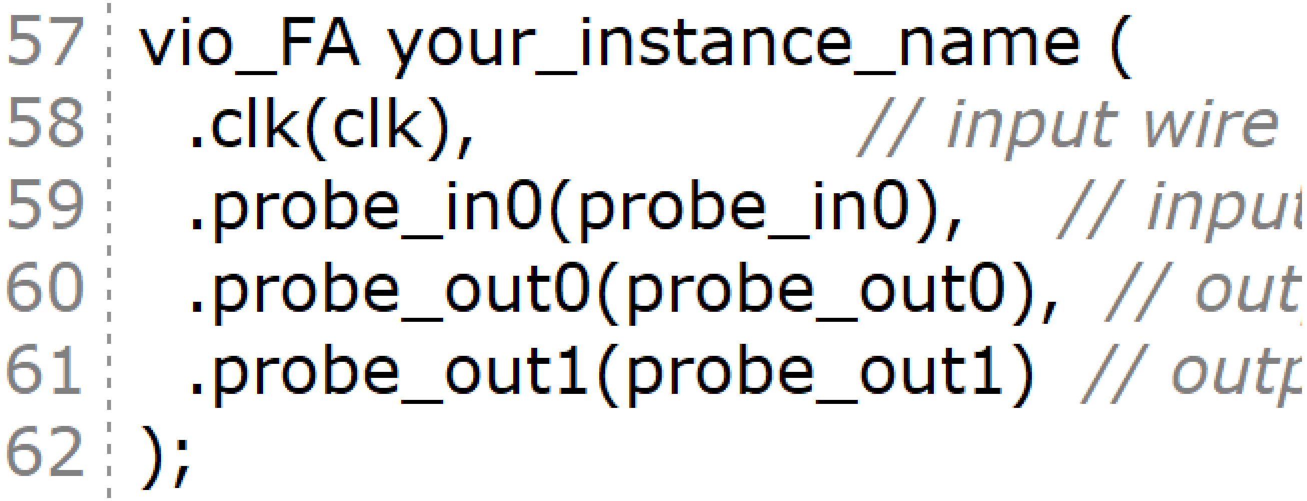
```
module top_adderHW(
    input Clock
    );
    wire [3:0] InA, InB;
    wire [4:0] OutSum;

    top_adder ta(.InA(InA), .InB(InB),.OutSum(OutSum));

endmodule
```

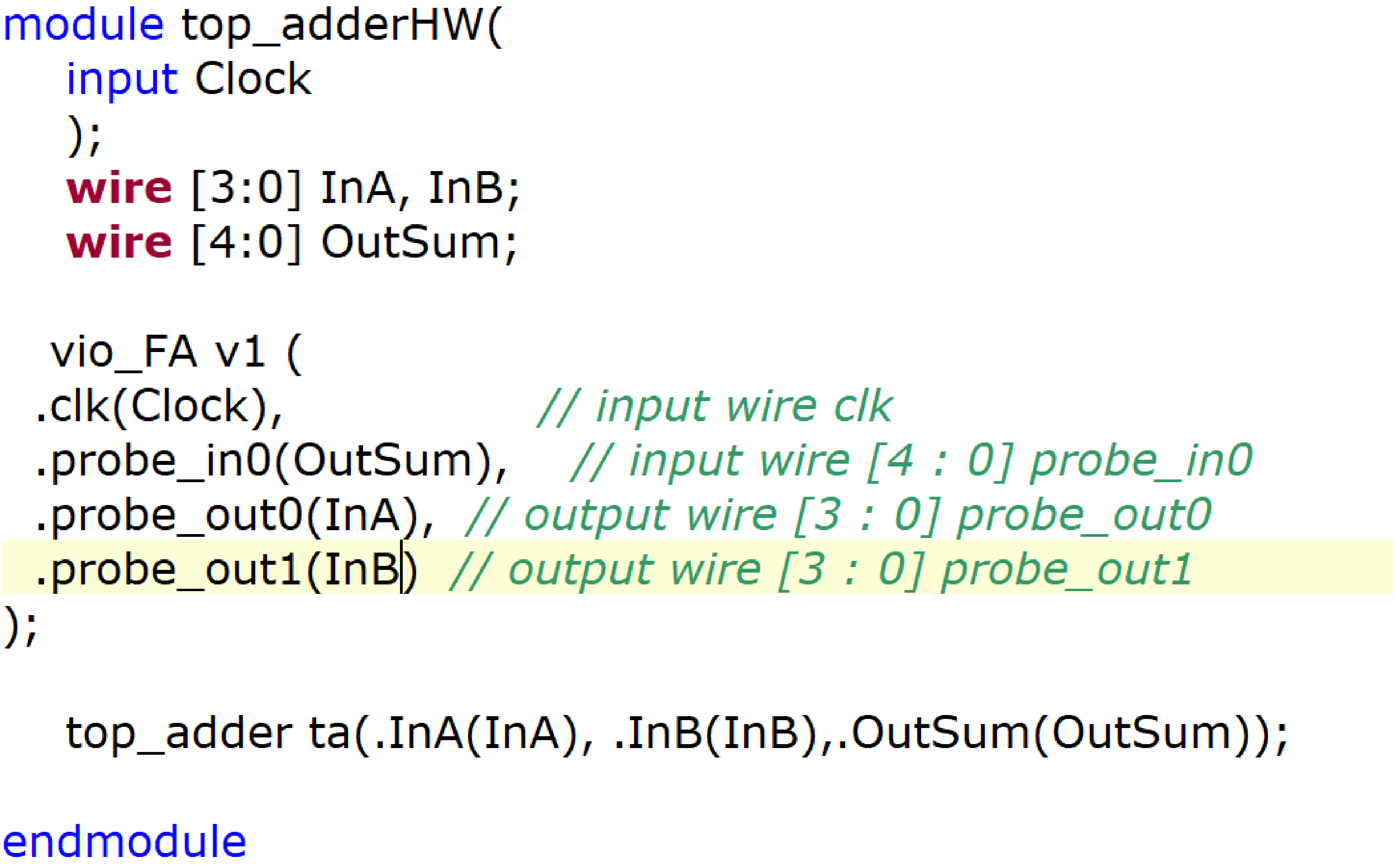
How to add VIO?





```
vio_FA your_instance_name (
  .clk(clk),                // input wire
  .probe_in0(probe_in0),    // input
  .probe_out0(probe_out0),  // out
  .probe_out1(probe_out1)  // outp
);
```

Final Code



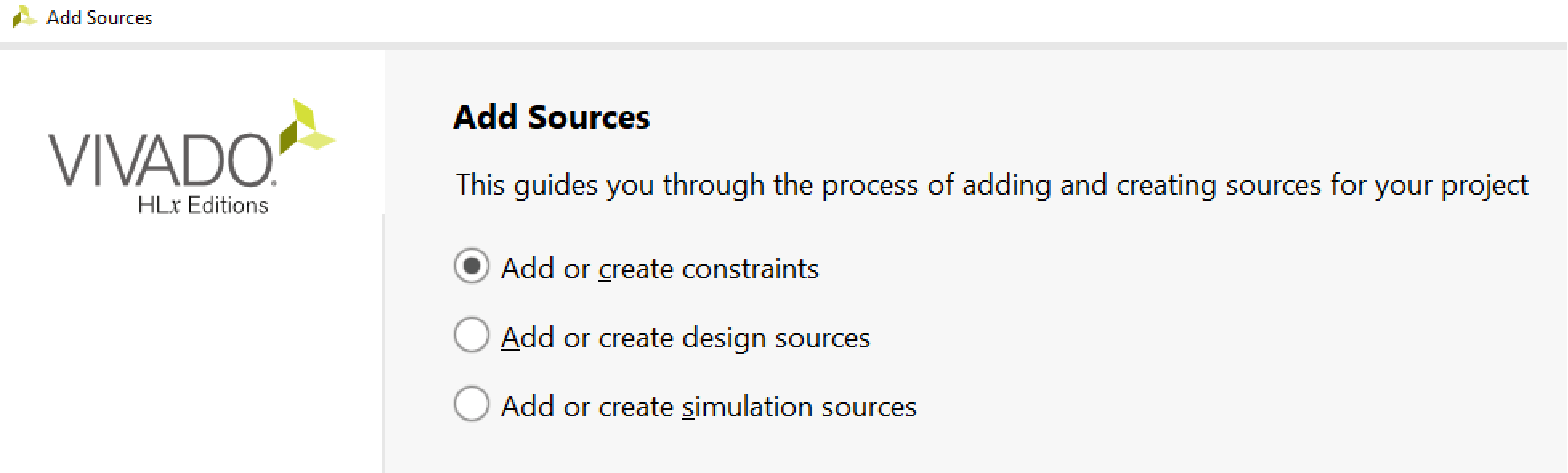
```
module top_adderHW(
    input Clock
    );
    wire [3:0] InA, InB;
    wire [4:0] OutSum;

   vio_FA v1 (
  .clk(Clock),                // input wire clk
  .probe_in0(OutSum),    // input wire [4 : 0] probe_in0
  .probe_out0(InA),  // output wire [3 : 0] probe_out0
  .probe_out1(InB)  // output wire [3 : 0] probe_out1
);

    top_adder ta(.InA(InA), .InB(InB),.OutSum(OutSum));

endmodule
```

How to input Clock?



Add Sources

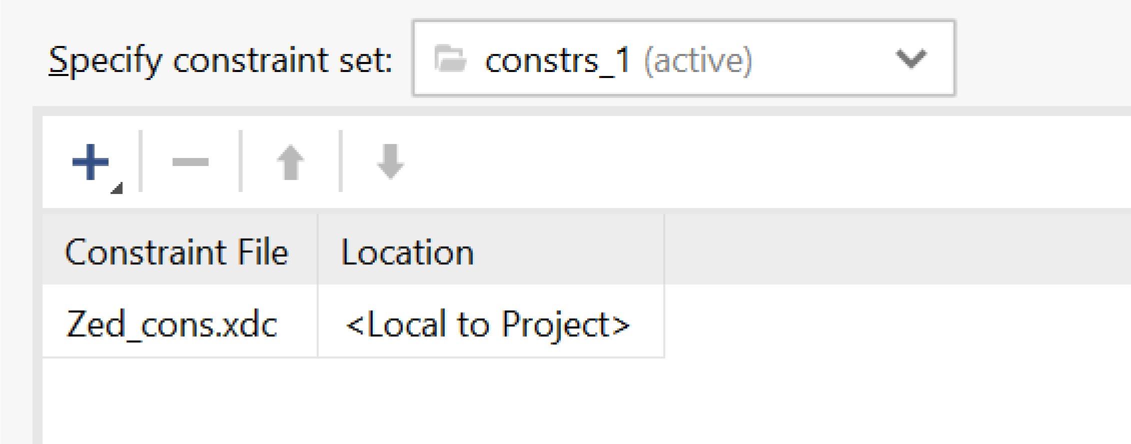
Add Sources

This guides you through the process of adding and creating sources for your project

● Add or create constraints

○ Add or create design sources

○ Add or create simulation sources

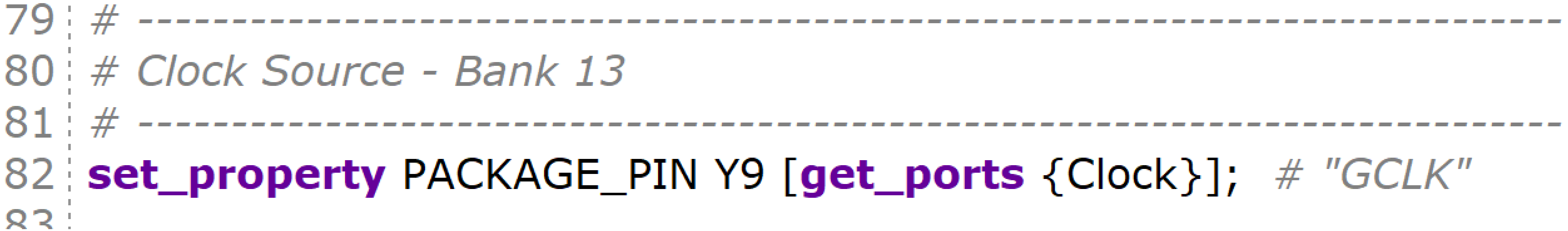


Specify constraint set: constrs_1 (active)

Constraint File	Location
Zed_cons.xdc	<Local to Project>

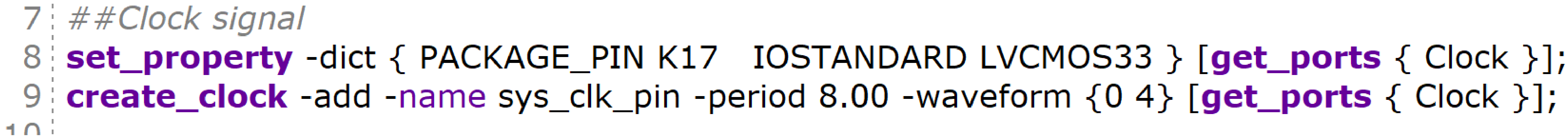
XDC File

- Zedboard



```
# ------------------------------------------------------------
# Clock Source - Bank 13
# ------------------------------------------------------------
set_property PACKAGE_PIN Y9 [get_ports {Clock}];  # "GCLK"
```

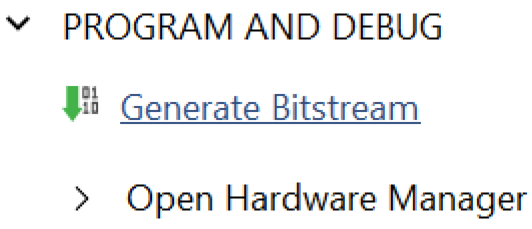
- Zybo



```
##Clock signal
set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports { Clock }];
create_clock -add -name sys_clk_pin -period 8.00 -waveform {0 4} [get_ports { Clock }];
```

Generate Bitstream

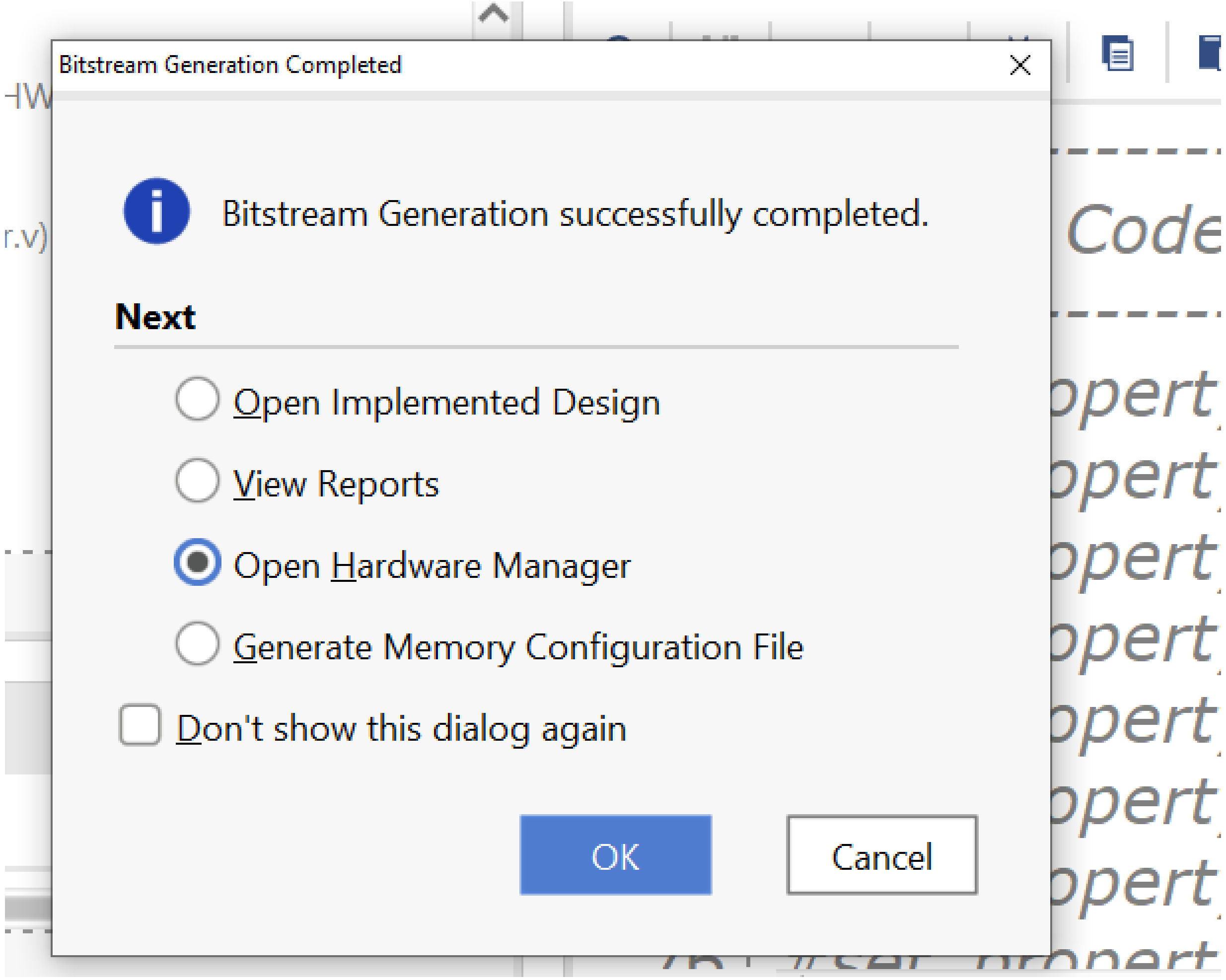
- Open hardware manager



PROGRAM AND DEBUG

Generate Bitstream

Open Hardware Manager



Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

○ Open Implemented Design

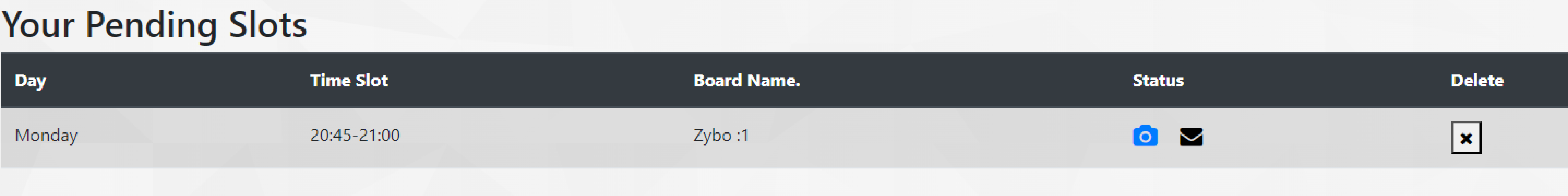
○ View Reports

● Open Hardware Manager

○ Generate Memory Configuration File

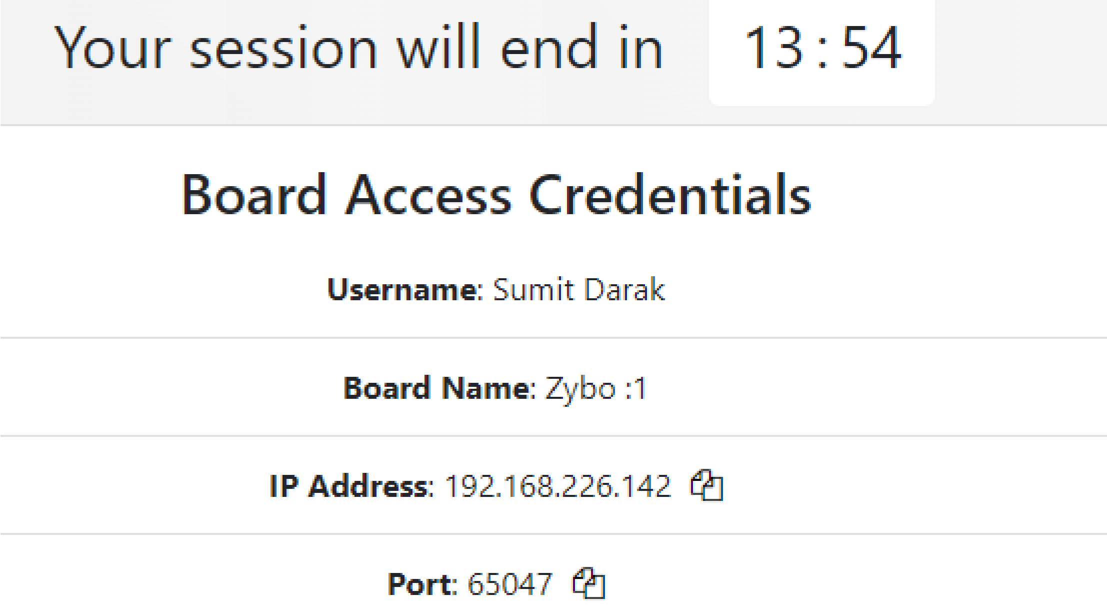
□ Don't show this dialog again

IP Address and Port from CloudLab



Your Pending Slots

Day	Time Slot	Board Name.	Status	Delete
Monday	20:45-21:00	Zybo :1	📷 ✉	☒



Your session will end in 13 : 54

Board Access Credentials

Username: Sumit Darak

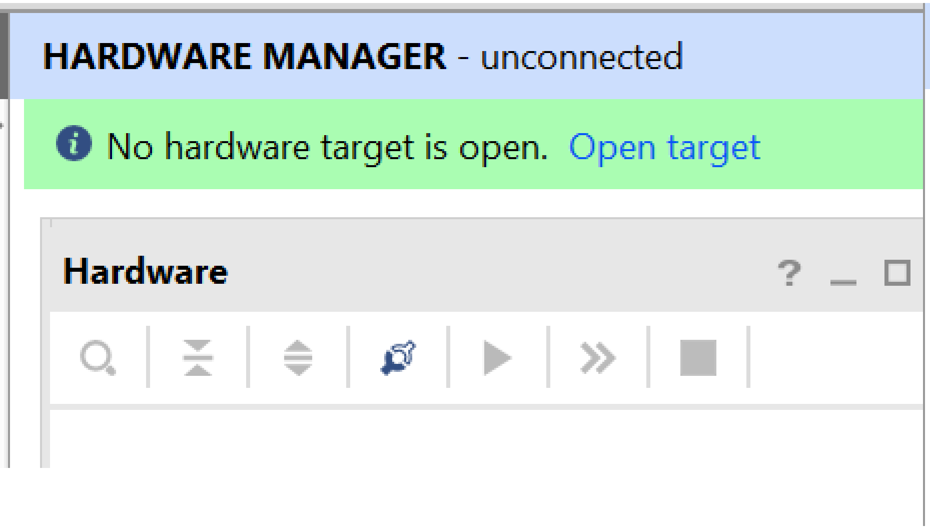
Board Name: Zybo :1

IP Address: 192.168.226.142

Port: 65047

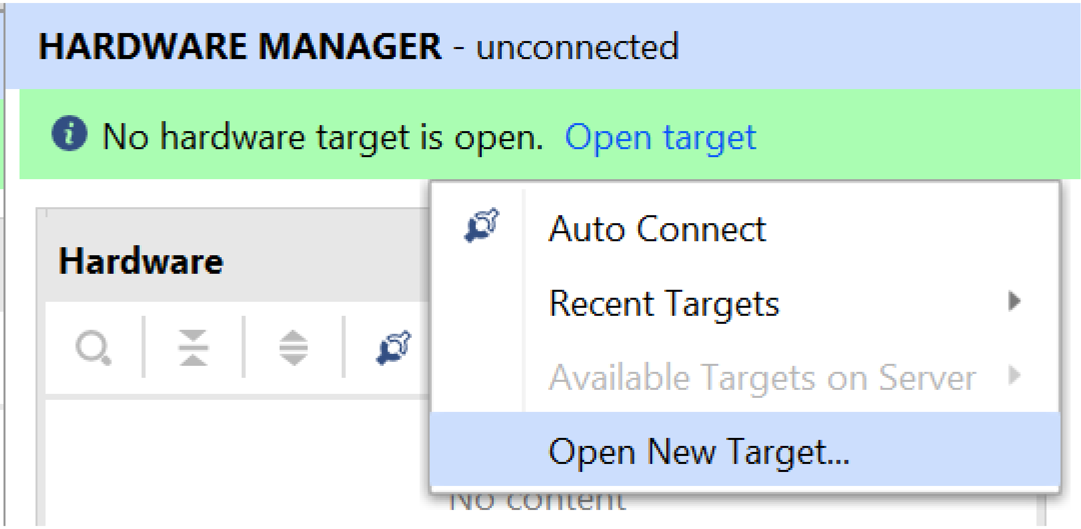
Connect to Hardware

- Click on Open target (after booking slot on CloudLab website)



HARDWARE MANAGER - unconnected

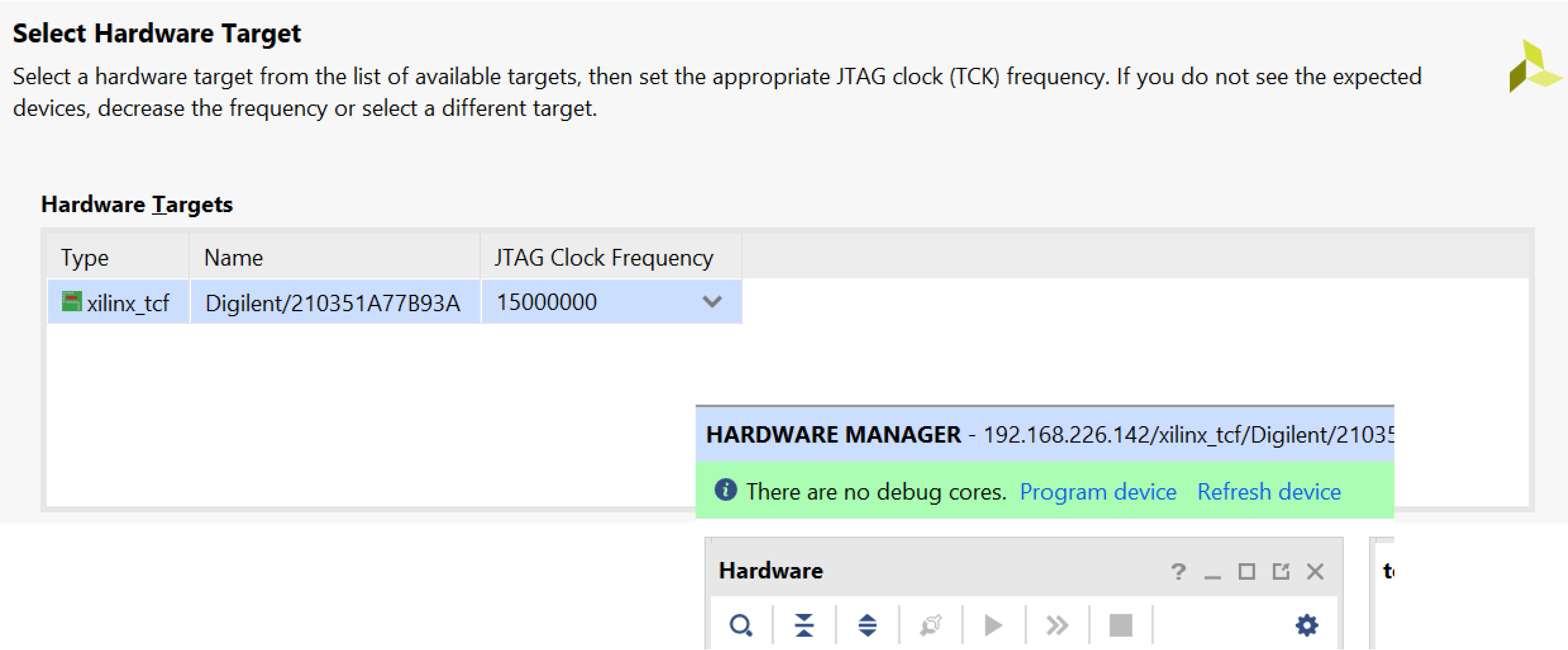
No hardware target is open. Open target



HARDWARE MANAGER - unconnected

No hardware target is open. Open target

Hardware Connection Successful



Select Hardware Target

Select a hardware target from the list of available targets, then set the appropriate JTAG clock (TCK) frequency. If you do not see the expected devices, decrease the frequency or select a different target.

Hardware Targets

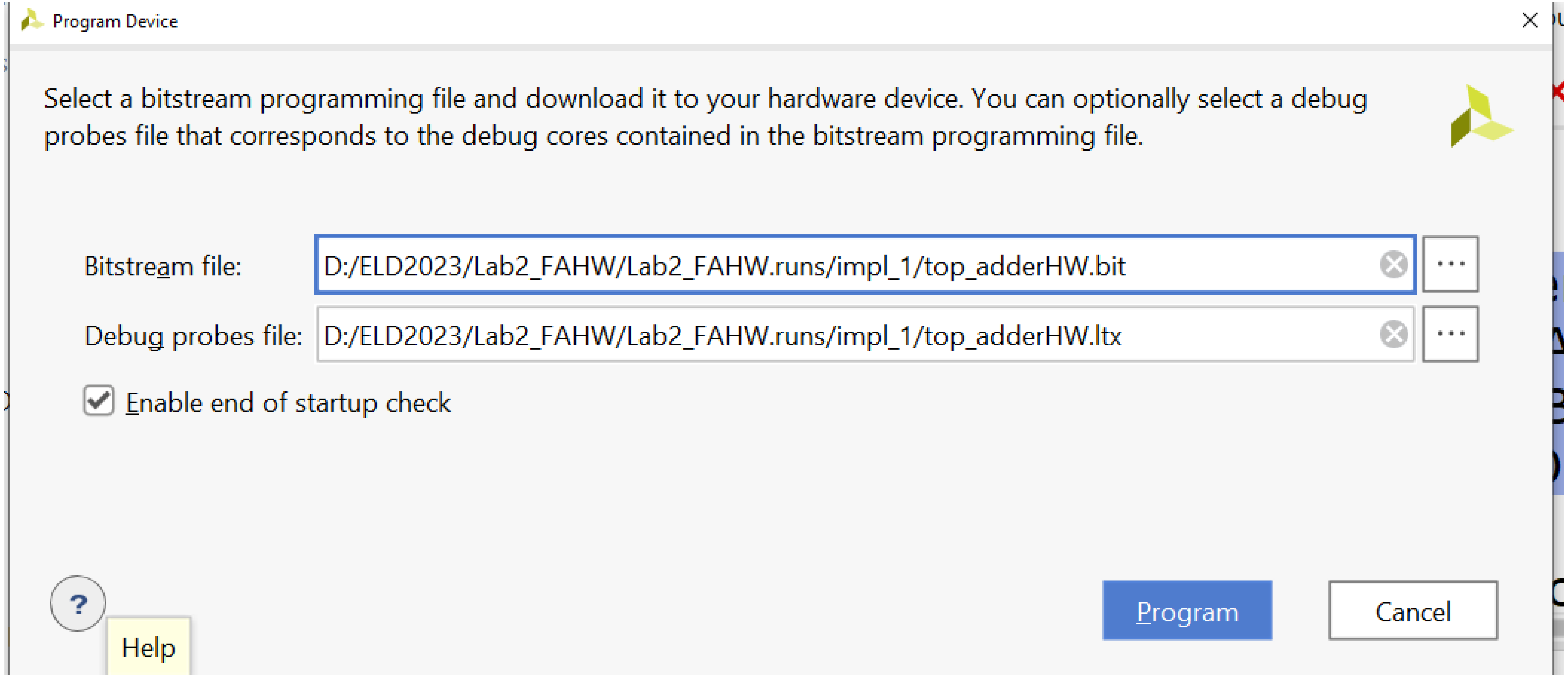
Type	Name	JTAG Clock Frequency
xilinx_tcf	Digilent/210351A77B93A	15000000

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/21035

There are no debug cores. Program device Refresh device

Hardware

Program FPGA



Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.

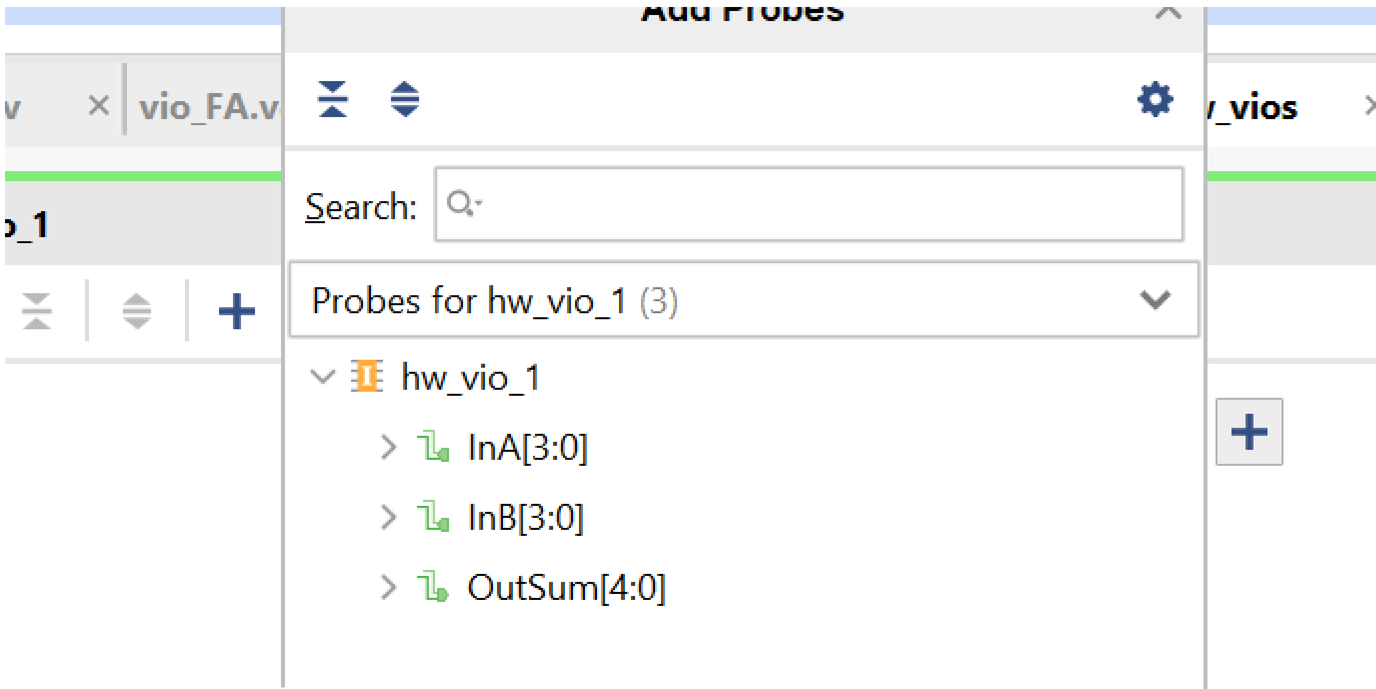
Bitstream file: D:/ELD2023/Lab2_FAHW/Lab2_FAHW.runs/impl_1/top_adderHW.bit

Debug probes file: D:/ELD2023/Lab2_FAHW/Lab2_FAHW.runs/impl_1/top_adderHW.ltx

☑ Enable end of startup check

VIO Probes

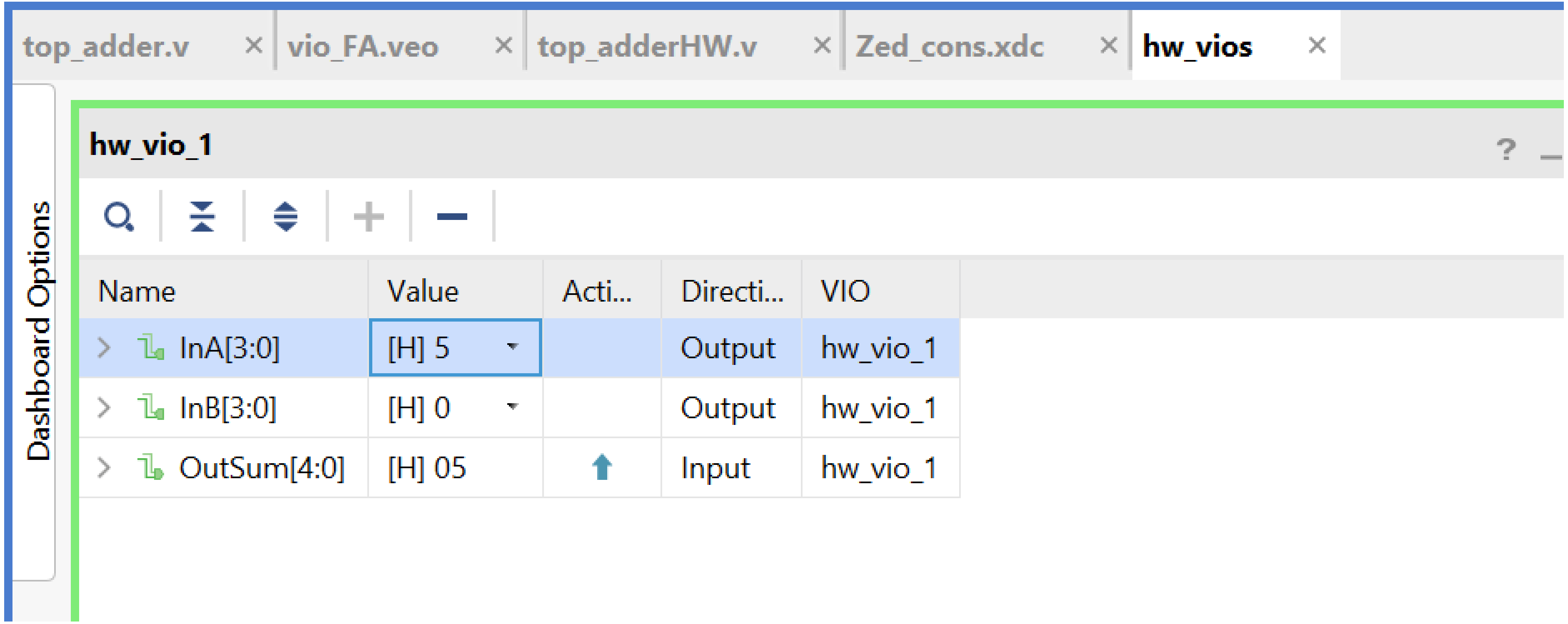
- Add all signals
- Set inputs and observe output



Search:

Probes for hw_vio_1 (3)

- hw_vio_1
  - InA[3:0]
  - InB[3:0]
  - OutSum[4:0]

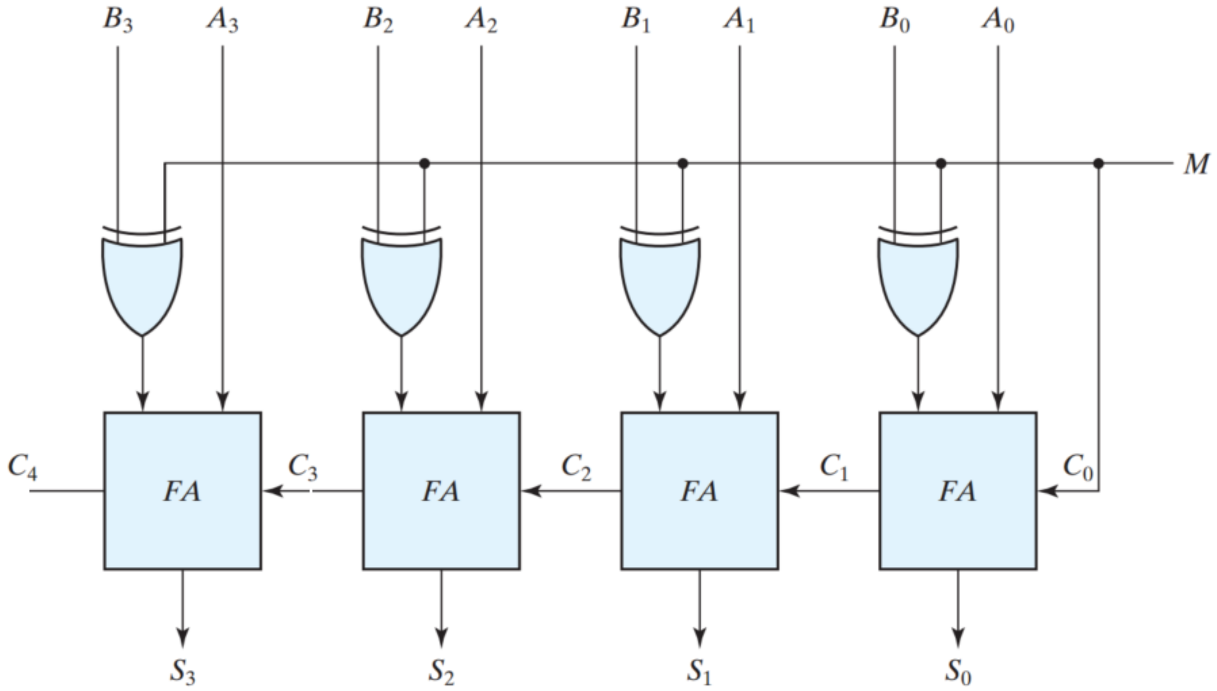


hw_vio_1

Name	Value	Acti...	Directi...	VIO
InA[3:0]	[H] 5		Output	hw_vio_1
InB[3:0]	[H] 0		Output	hw_vio_1
OutSum[4:0]	[H] 05	↑	Input	hw_vio_1

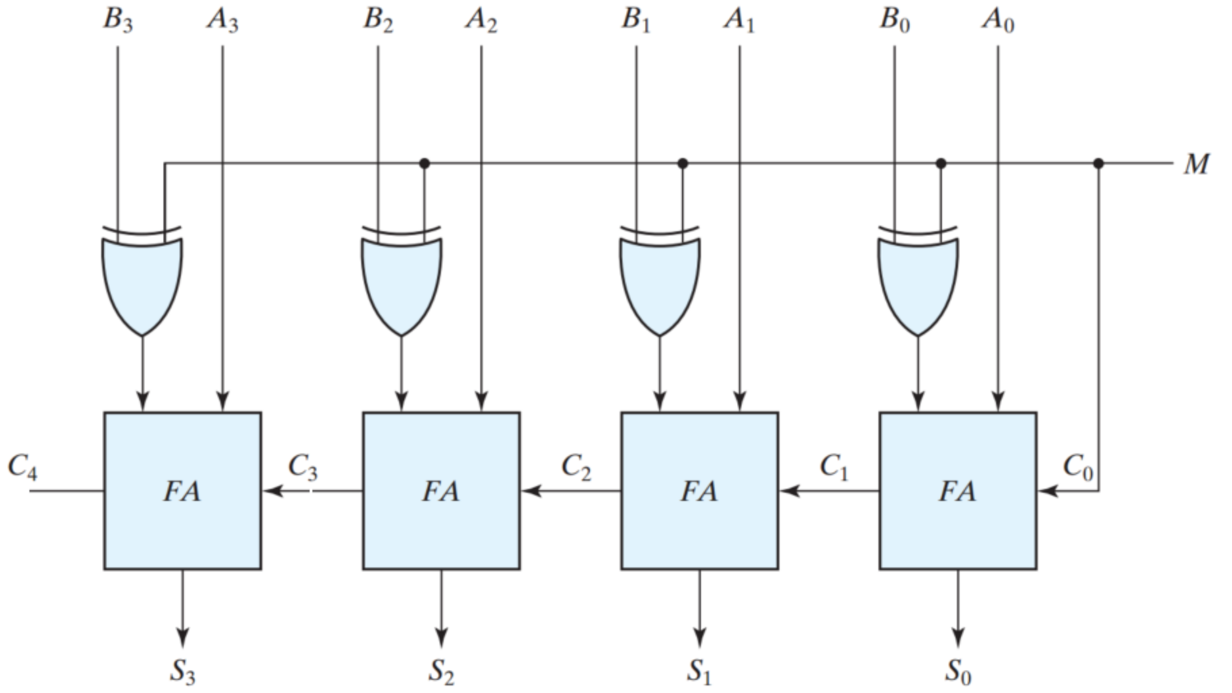
Homework

Adders



- For adder/subtractor with signed number inputs, add three independent output flags 1) First output flag goes high when overflow occurs, 2) Second output flag goes high when sum is negative, and 3) Third output flag goes high when sum is zero

Overflow



$$\begin{array}{rr} & (+7) \\ + & (-2) \\ \hline & (+5) \end{array} \qquad \begin{array}{rr} & 0111 \\ + & 1110 \\ \hline & 10101 \end{array}$$

$c_4 = 1$
$c_3 = 1$

$$\begin{array}{rr} & (-7) \\ + & (+2) \\ \hline & (-5) \end{array} \qquad \begin{array}{rr} & 1001 \\ + & 0010 \\ \hline & 1011 \end{array}$$

$c_4 = 0$
$c_3 = 0$

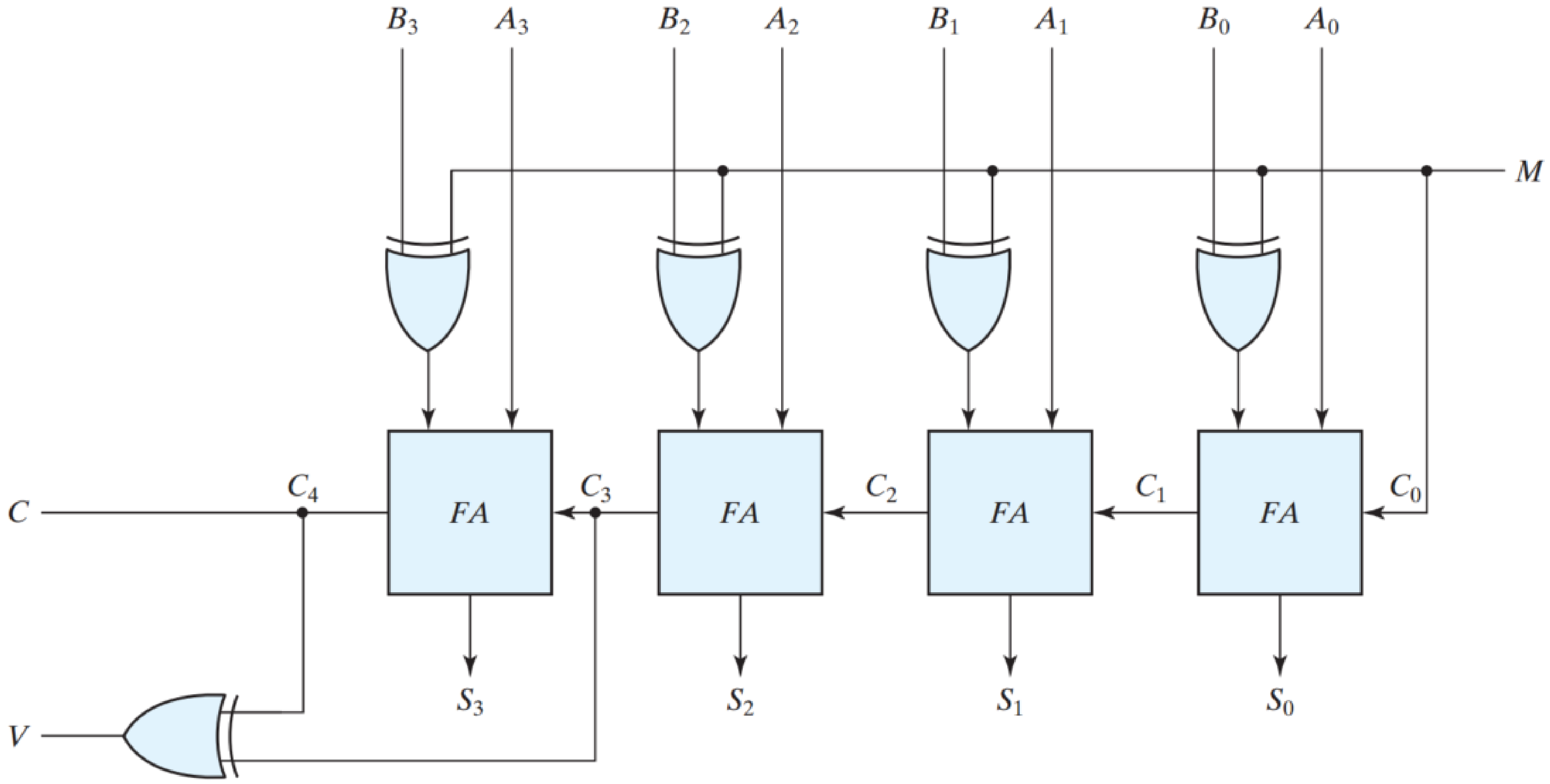
$$\begin{array}{rr} & (-7) \\ + & (-2) \\ \hline & (-9) \end{array} \qquad \begin{array}{rr} & 1001 \\ + & 1110 \\ \hline & 10111 \end{array}$$

$c_4 = 1$
$c_3 = 0$

$$\begin{array}{rr} & (+7) \\ + & (+2) \\ \hline & (+9) \end{array} \qquad \begin{array}{rr} & 0111 \\ + & 0010 \\ \hline & 1001 \end{array}$$

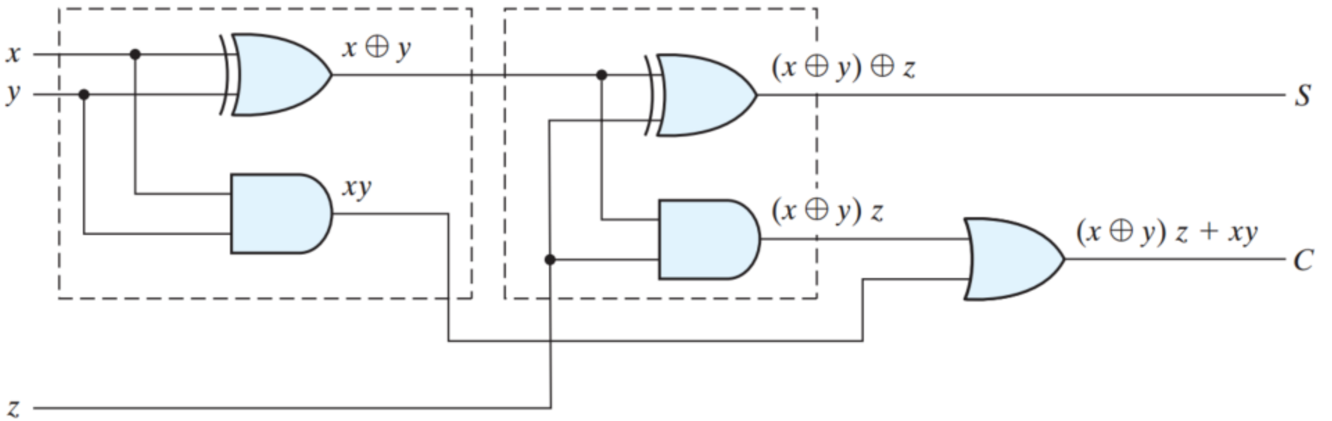
$c_4 = 0$
$c_3 = 1$

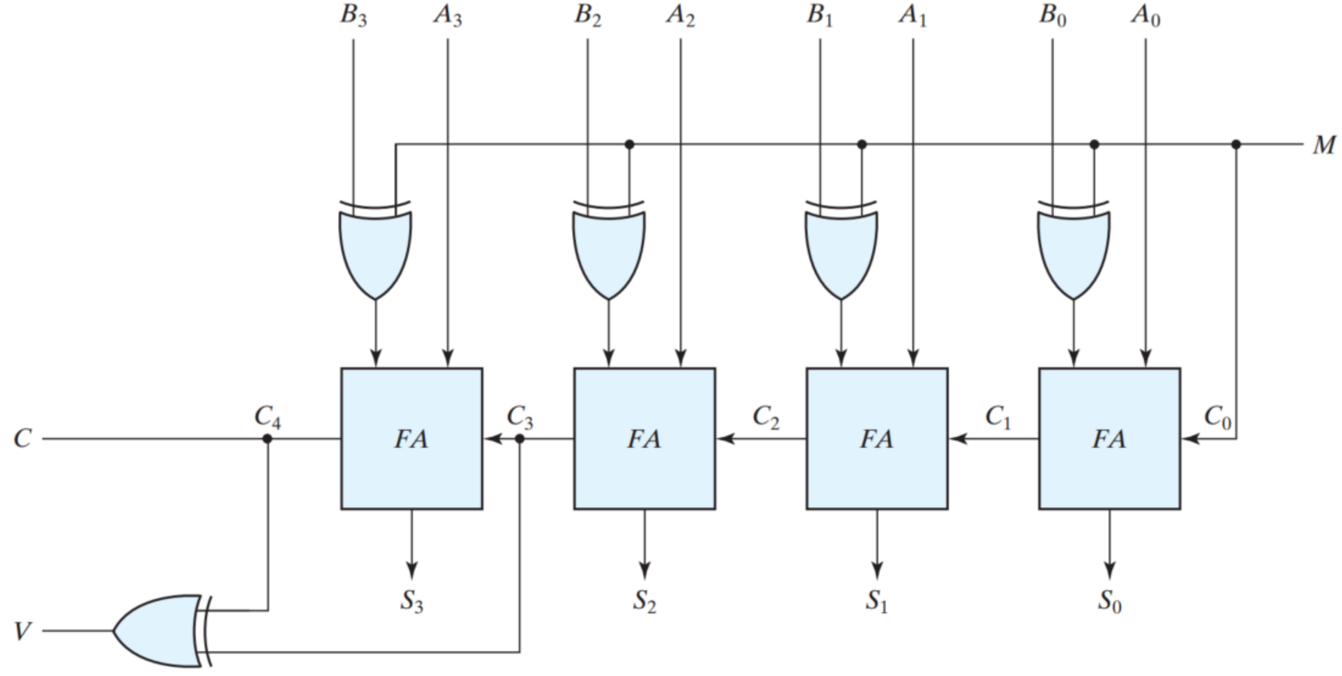
Overflow



Performance

- The longest propagation delay time in an adder is the time it takes the carry to propagate through the full adders.
- Inputs *A*3 and*B*3 are available as soon as input signals are applied to the adder. However, input carry *C*3 does not settle to its final value until *C*2 is available from the previous stage. Similarly, *C*2 has to wait for *C*1 and so on down to *C*0.

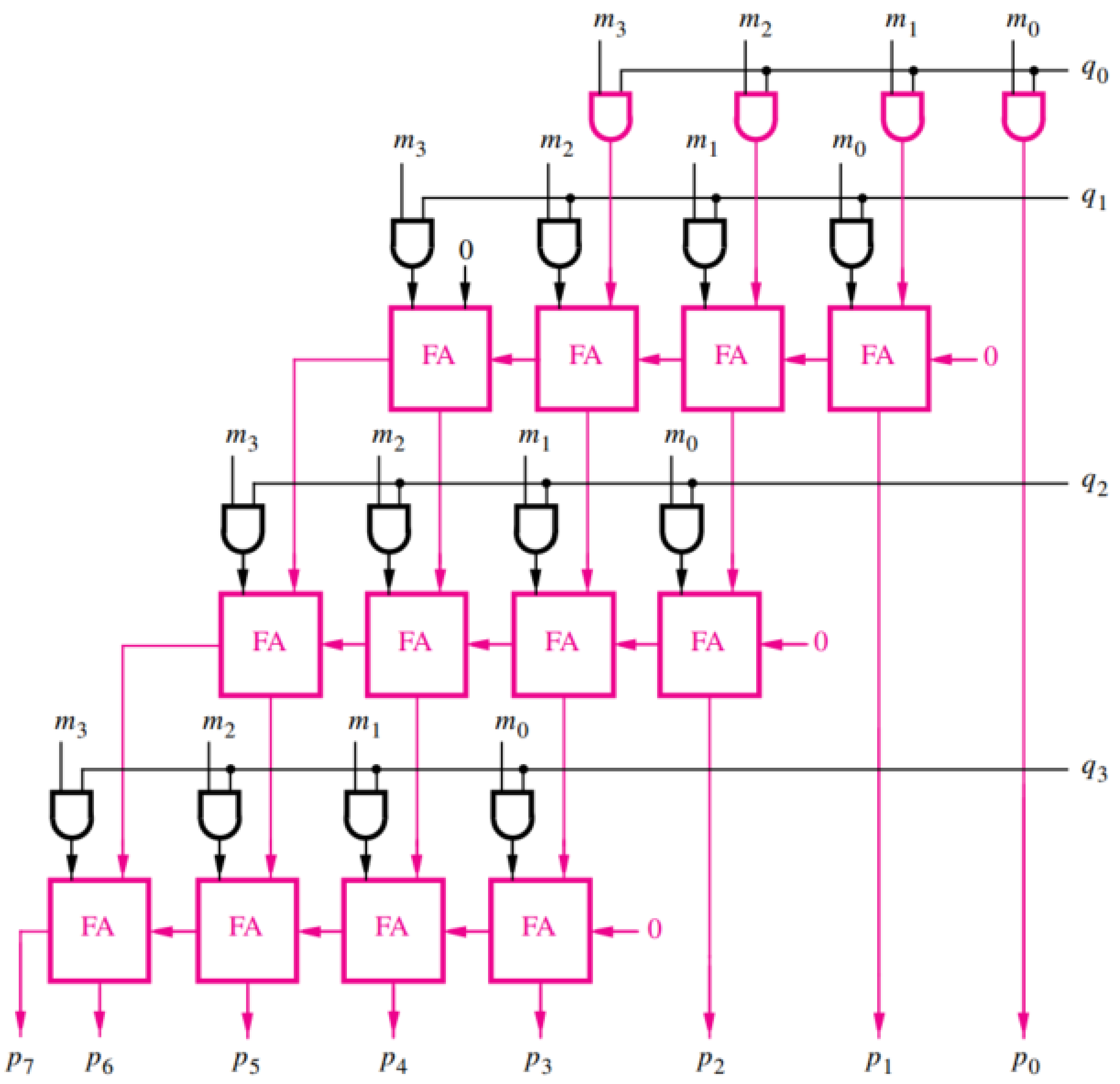




Self Study

Multiplication

$$\begin{array}{lcccccccc}
 & & & & & m_3 & m_2 & m_1 & m_0 \\
 & & & & \times & q_3 & q_2 & q_1 & q_0 \\ \cline{6-9}
\text{Partial product 0} & & & & & m_3q_0 & m_2q_0 & m_1q_0 & m_0q_0 \\
 & & & & +\ m_3q_1 & m_2q_1 & m_1q_1 & m_0q_1 & \downarrow \\ \cline{5-8}
\text{Partial product 1} & & & PP1_5 & PP1_4 & PP1_3 & PP1_2 & PP1_1 & \downarrow \\
 & & & +\ m_3q_2 & m_2q_2 & m_1q_2 & m_0q_2 & \downarrow & \downarrow \\ \cline{4-7}
\text{Partial product 2} & & PP2_6 & PP2_5 & PP2_4 & PP2_3 & PP2_2 & \downarrow & \downarrow \\
 & & +\ m_3q_3 & m_2q_3 & m_1q_3 & m_0q_3 & \downarrow & \downarrow & \downarrow \\ \cline{2-6}
\text{Product P} & p_7 & p_6 & p_5 & p_4 & p_3 & p_2 & p_1 & p_0
\end{array}$$


m_3
m_2
m_1
m_0
q_0
q_1
q_2
q_3
FA
0
p_7
p_6
p_5
p_4
p_3
p_2
p_1
p_0