Mid-Sem Paper
ECE214 - Integrated Electronics

- **INSTRUCTIONS:**

Total Marks = 100
Time Duration = 80 minutes for solving + 10 minutes uploading

1. **The duration of the exam is 80 mins, and 10 mins for scanning and uploading the solutions. No further extension of time will be given regarding this. Any late submission will be awarded 0 marks.**
2. **This paper contains four questions, with their respective subparts. Some questions may also utilize the elementary-level understanding of your previous courses.**
3. **The question paper will be uploaded to google classroom. Do not forget to turn it in. Solutions submitted by any other means (email etc.) won't be considered for evaluation.**
4. **Students are required to switch on their cameras and mute themselves. Make sure you are sitting in a well-lit room so that we are able to see your faces clearly. If you are not clearly visible, you will be awarded 0 marks.**
5. **The answers should be in your own handwriting and submission should be in PDF format only. No other mode of submissions will be accepted.**
6. **Write any assumption clearly, if any. Needless to say, only reasonable assumptions will be considered if any ambiguity is found in the question.**
7. **During the exam, if you have any queries, write them in the meet chatbox. It will be taken into notice by us. Don't unnecessarily unmute your mic for it creates a disturbance to others.**
8. **Calculators are NOT allowed during exam time. ONLY use pen and paper for writing the exam.**
9. **Students need to be present and visible for the whole exam duration (till the end of solution uploading time) even if they upload the solution before time.**
10. **NAMING CONVENTION - <Name>_<Roll No.>_Mid-Sem.pdf**
11. **Show your calculations and justifications in each question.**

Q1. It is given that the gain of the below given circuit in Fig. 1 is:

$$Av \approx \frac{-Rc}{\frac{1}{gm}+Re+\frac{Rb}{\beta+1}}$$

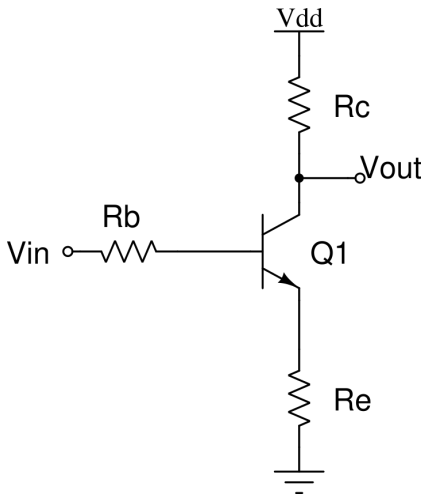

Fig. 1

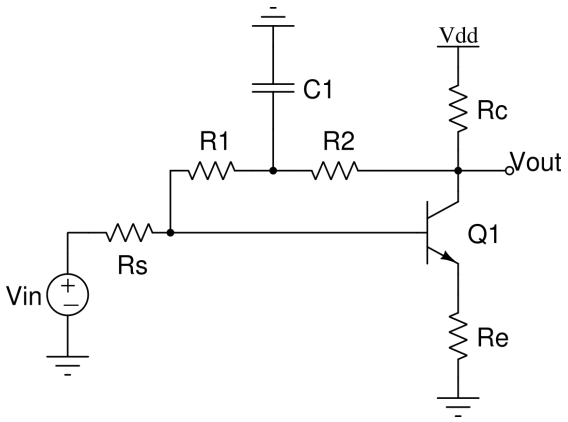

Fig. 2

a. Find the gain of the circuit given in Fig. 2. Where it is given that Rb = (Rs.R1)/(Rs+R1) and R2>>RC. Coupling capacitors are very large. [**15 Marks**]
[Hint: Try to simplify the circuit given in Fig. 2 to make it similar to the circuit given in Fig. 1.]

b. The β of different transistors of the same model and part number often comeout to will be different due to manufacturing variations. This poses a huge challenge in amplifier designs as β values for the same transistor design may be different, giving different amplifications. Thus we would want to reduce the dependence of gain on β. Can you suggest a way we can do that by looking at the Gain equation given obtained in Fig. 2? [Note that Rs or Rb is always non-zero because every signal source has some impedance.] [**10 Marks**]

Q2. In the circuit shown in Fig. 3 the diode is ideal (in FB the drop across diode is zero and in RB the diode behaves like a open circuit).

a. Plot the i_A vs. V_A characteristics for the nonlinear network shown in Fig. 3. [**10 Marks**]

b. The nonlinear network part (NLD) from Fig 1 is taken and connected in the circuit as shown in Fig. 4, Assuming no loading effect, draw the load line on your v-i characteristics from part a and find i_T. [**10 Marks**]

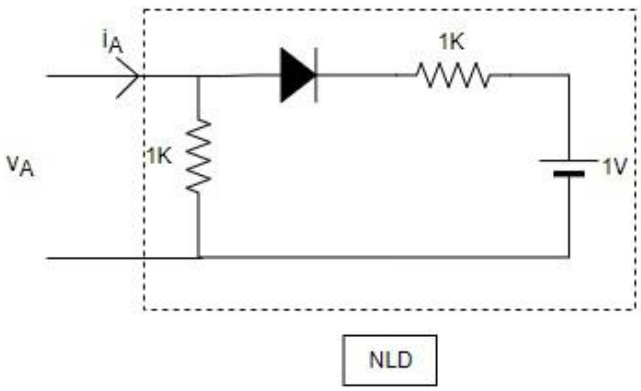

Fig. 3

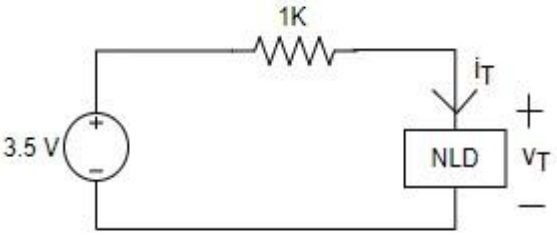

Fig. 4

Q3. For the n-MOS (M) shown in Fig. 5, μnCox = 100 μA/V2, where μn is the electron mobility in the channel and Cox is the oxide capacitance per unit area, threshold voltage V_{TH} = 0.2 V and aspect ratio (W/ L) = 10. Channel length modulation effects are negligible (λ = 0).

a. V_B = 0.7 V, find the transconductance gm in mA/V. [**10 Marks**]
b. At the bias point of V_B mentioned in part a, what would be the small-signal resistance offered by M. (Neglect body effect and channel length modulation effects). [**10 Marks**]
c. In the circuit indicated in Fig. 6, two such MOSFETs (M1 = M2 = M) are connected. Find the minimum bias voltage V_B, such that M2 will operate in the saturation region. [**15 Marks**]

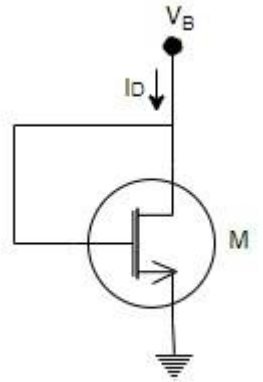

Fig. 5

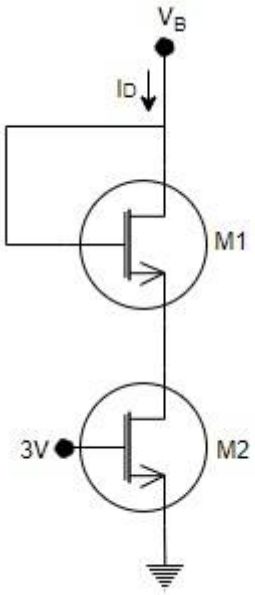

Fig. 6

Q4. For the circuit shown in Fig. 7 (CS amplifier), the PMOS transistor has Vtp = −0.8 V and a very large |VA|. Coupling capacitors are very large.

a. Select a value for R_S to bias the transistor at I_D = 0.3 mA and V_{OV} = 0.3 V. Assume Vsig to have a zero dc component. Where Vov is overdrive voltage. [**10 Marks**]
b. Select a value for R_D that results in the overall voltage gain (Gv) = −10 V/V. [**10 Marks**]

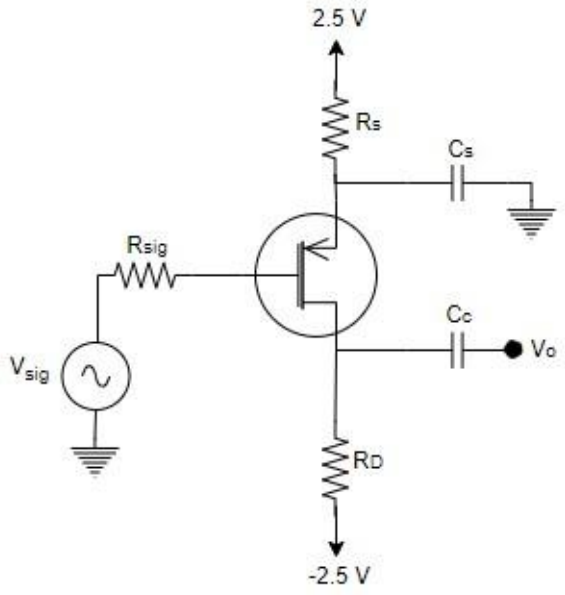

Fig. 7