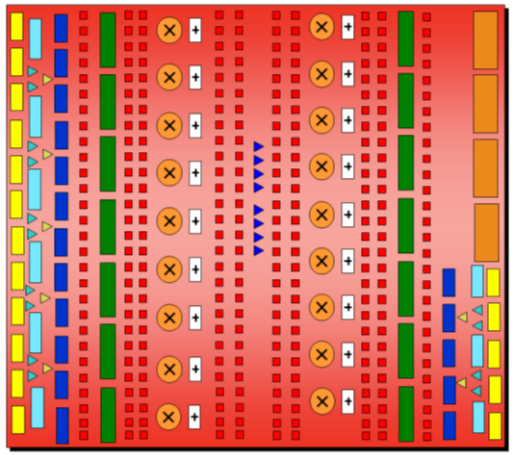
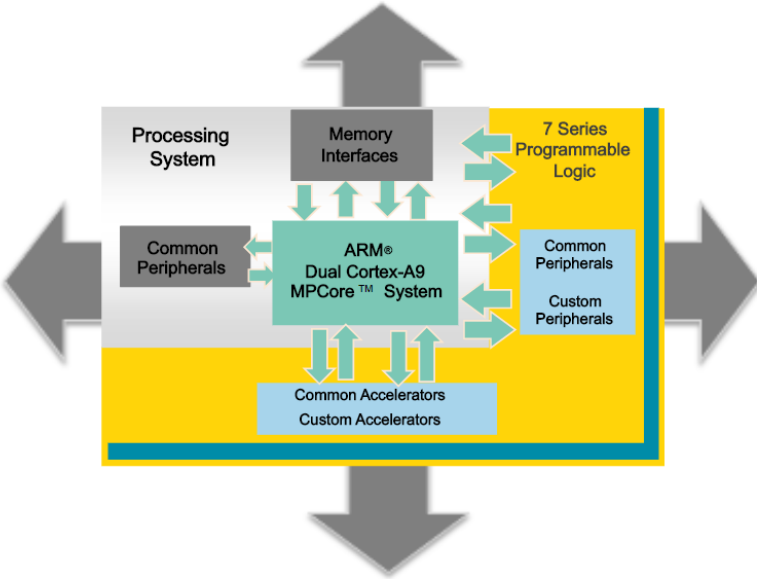
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

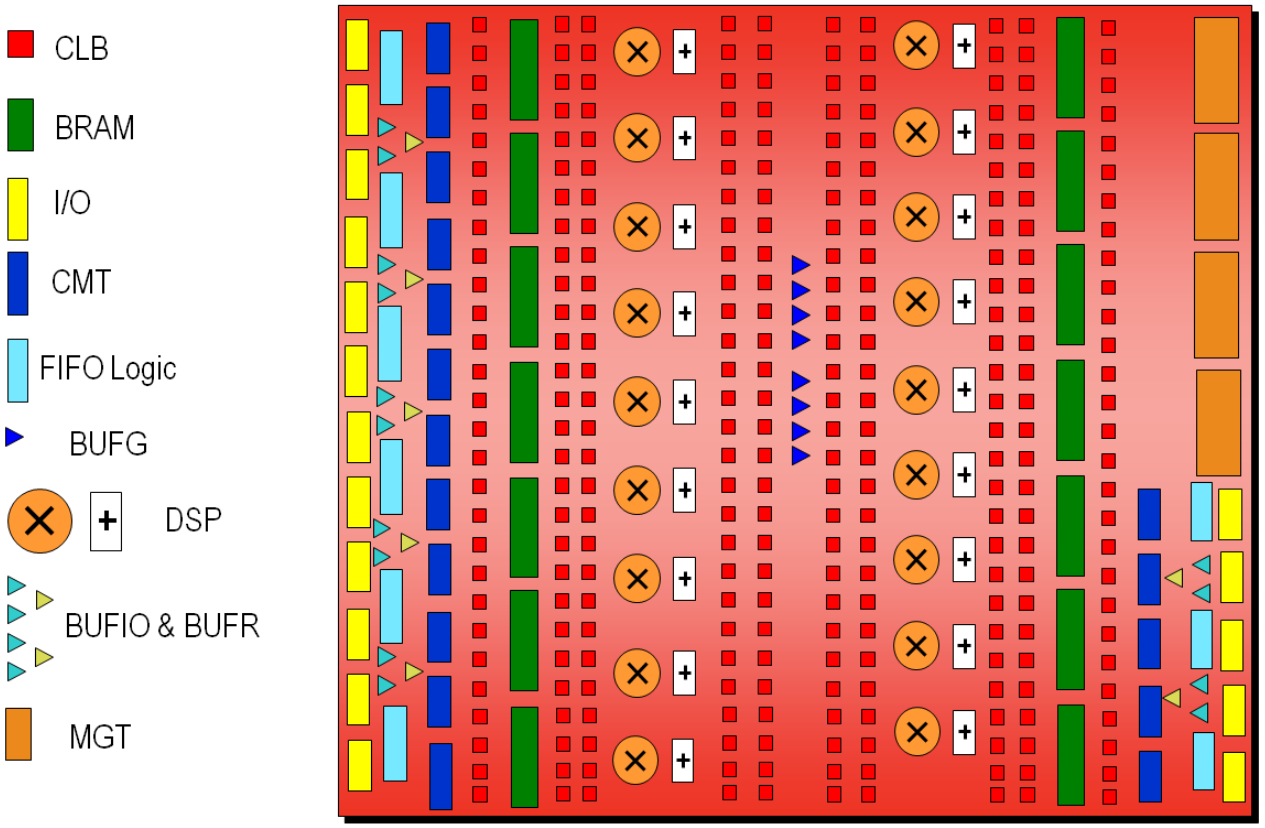
A2A
Algorithms to Architecture

ECE 270: Embedded Logic Design



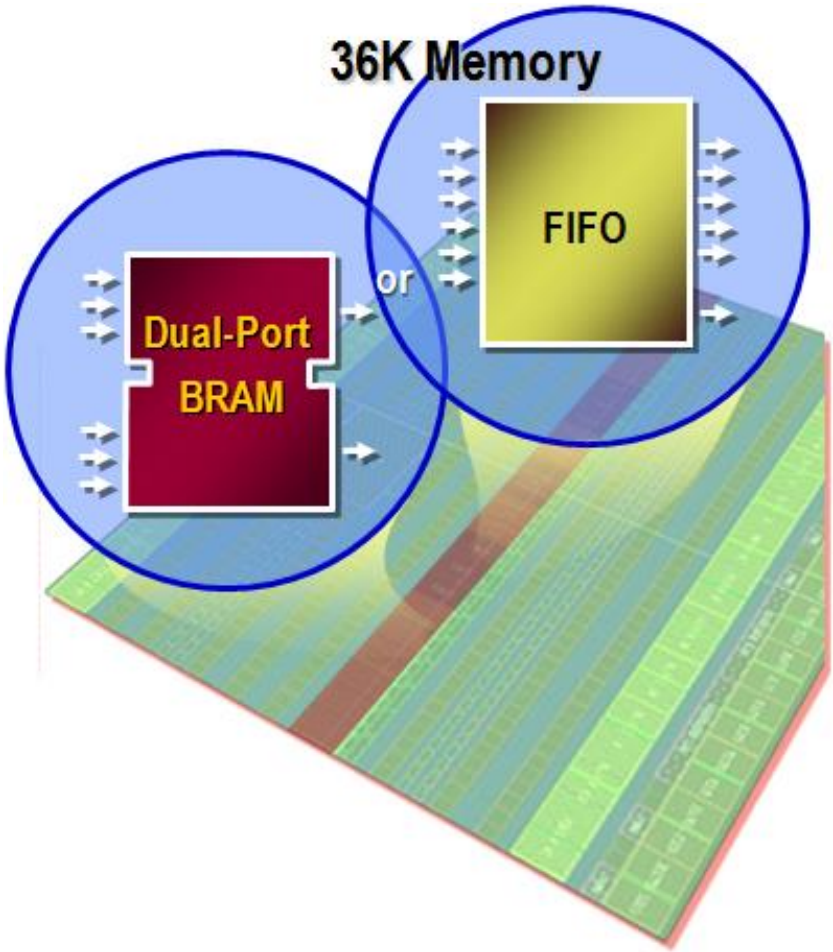


Block RAM



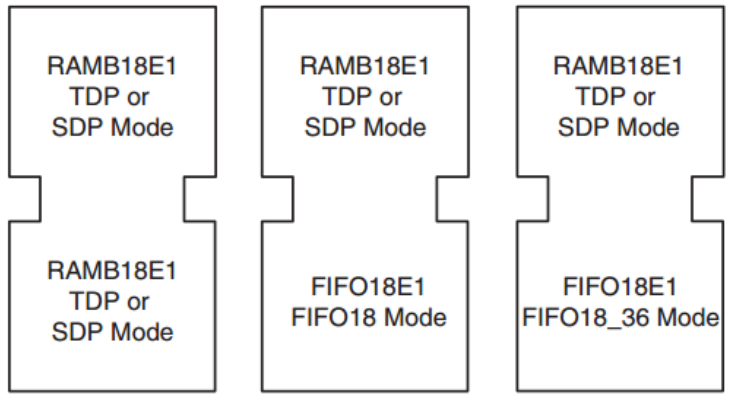
Block RAM

- All members of the 7-series families have dual-port 36 Kb block RAM with port widths of up to 72
- Fully synchronous operation
- Multiple configuration options: True dual port, simple dual port, single port

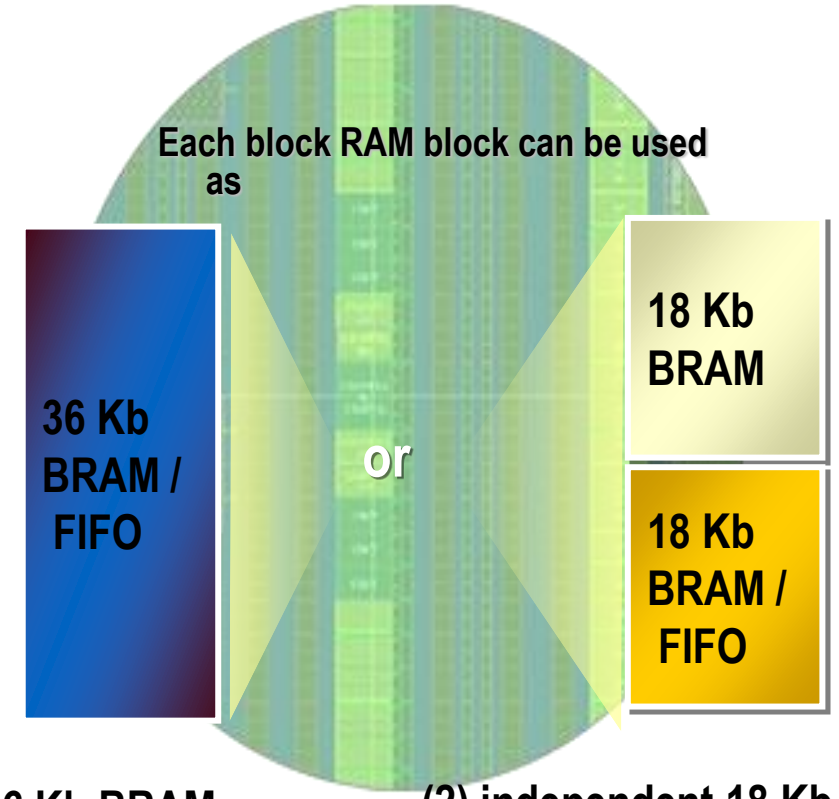


Block RAM

- Each BRAM can be segmented as:
  - 36 Kb BRAM
  - 36 Kb FIFO
  - Independent 18 Kb BRAMs
  - 18 Kb FIFO and 18 Kb BRAM



Legal Block RAM and FIFO Combinations

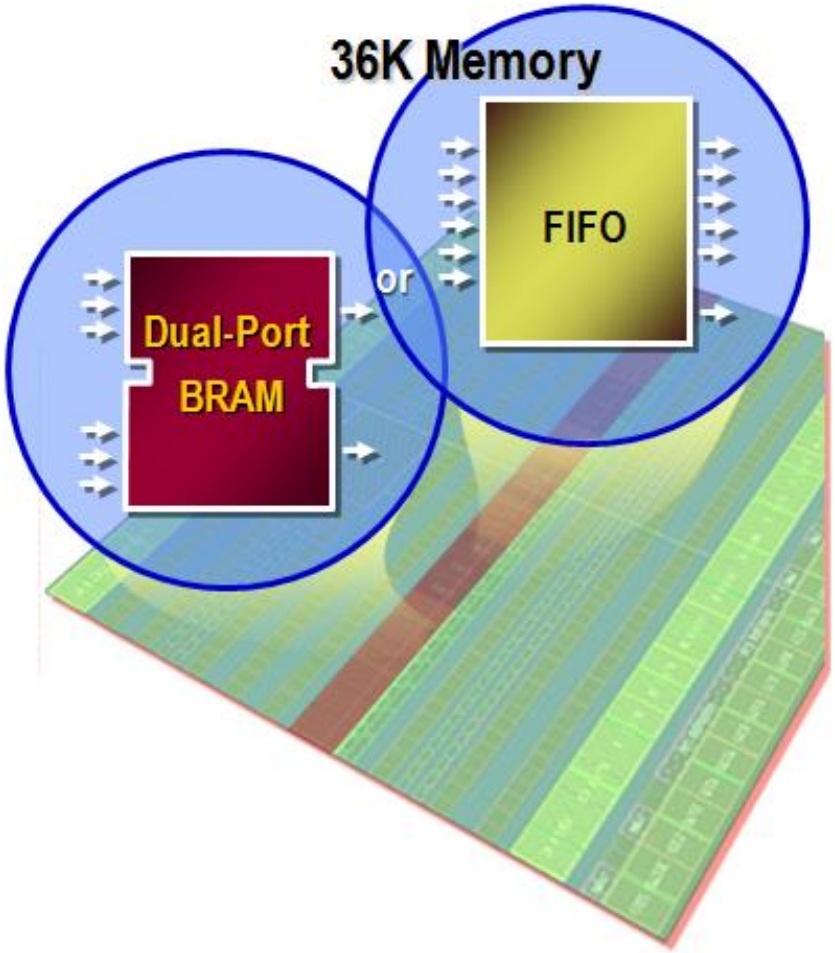


(1) 36 Kb BRAM OR (1) 36 Kb or FIFO

(2) independent 18 Kb block RAMs OR (1) 18 Kb FIFO + (1) 18 Kb block RAM

Block RAM

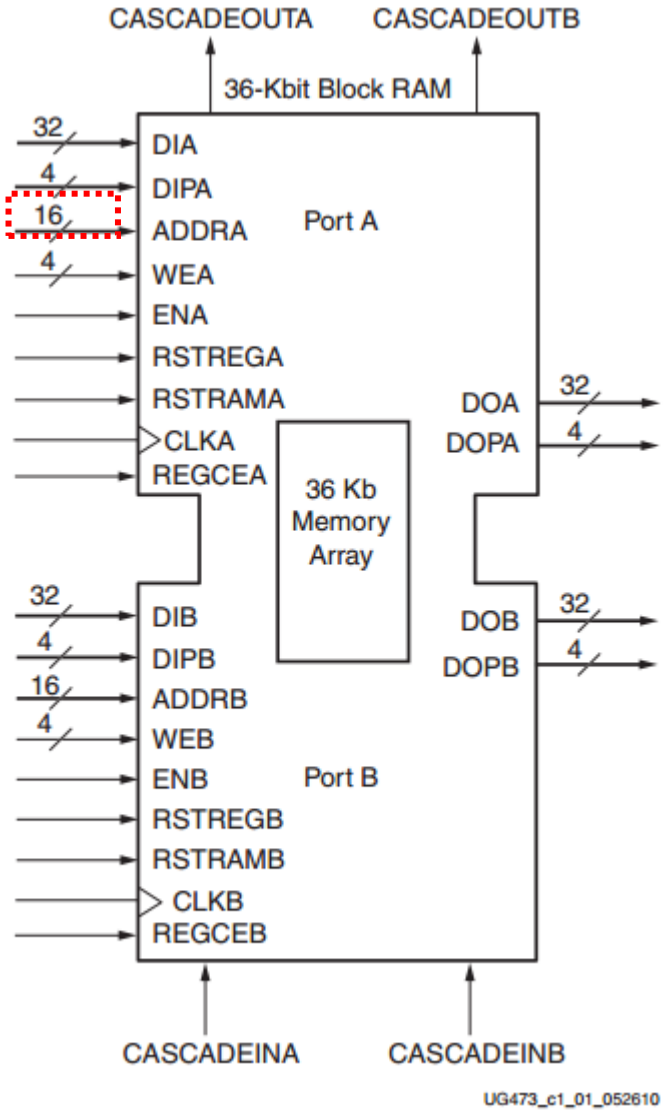
- Each BRAM can be segmented as:
  - 36 Kb BRAM
  - 36 Kb FIFO
  - Independent 18 Kb BRAMs
  - 18 Kb FIFO and 18 Kb BRAM
- Dedicated hardware to convert BRAM in to FIFO
- Integrated cascade logic to build larger memories
- Integrated error correction logic to fix bit errors*



Dual Port Block RAM

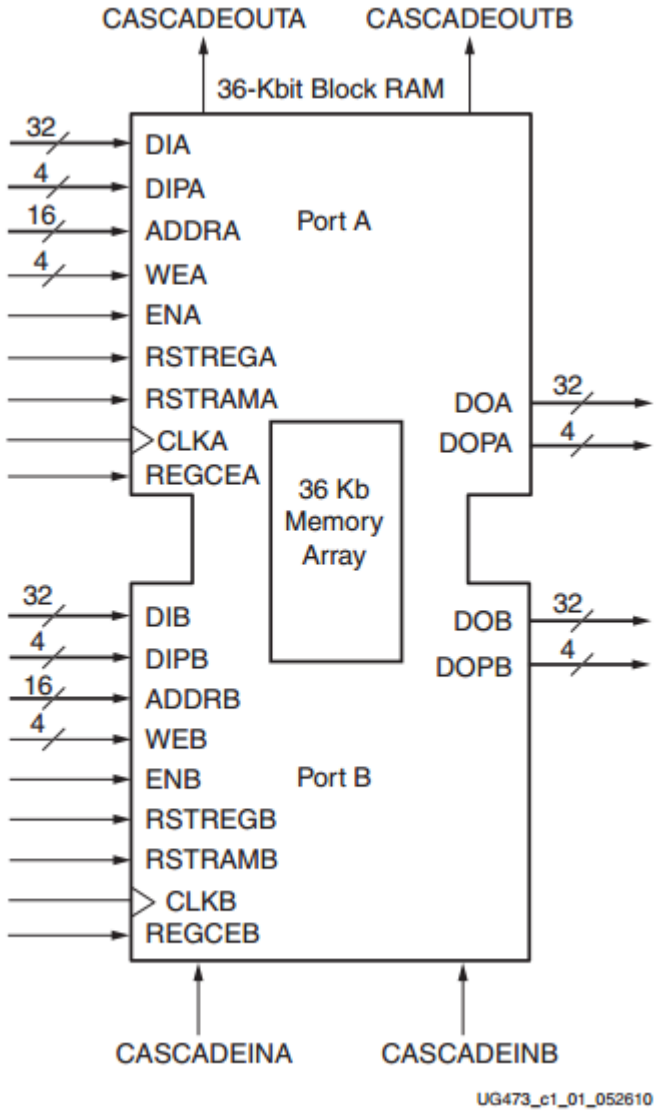
Dual-Port Block RAM

Port Function	Description
DI[A | B]	Data input bus.
DIP[A | B](1)	Data input parity bus. Can be used for additional data inputs.
ADDR[A | B]	Address bus.
WE[A | B]	Byte-wide write enable.
EN[A | B]	When inactive no data is written to the block RAM and the output bus remains in its previous state.
RSTREG[A | B]	Synchronous Set/Reset the output registers (DO_REG = 1). The RSTREG_PRIORITY attribute determines the priority over REGCE.
RSTRAM[A | B]	Synchronous Set/Reset the output data latches.
CLK[A | B]	Clock input.
DO[A | B]	Data output bus.
DOP[A | B](1)	Data output parity bus. Can be used for additional data outputs.
REGCE[A | B]	Output Register clock enable.
CASCADEIN[A | B]	Cascade input for 64K x 1 mode.
CASCADEOUT[A | B]	Cascade output for 64K x 1 mode.



Dual-Port Block RAM

- Two separate read/write ports
  - Each port has separate clock, address, data in, data out, write enable…
    - Clocks can be asynchronous to each other
  - The two ports can have different widths
  - The two ports can have different write modes
- Each block RAM can be divided into two completely independent 18 Kb block RAMs



Dual-Port Block RAM

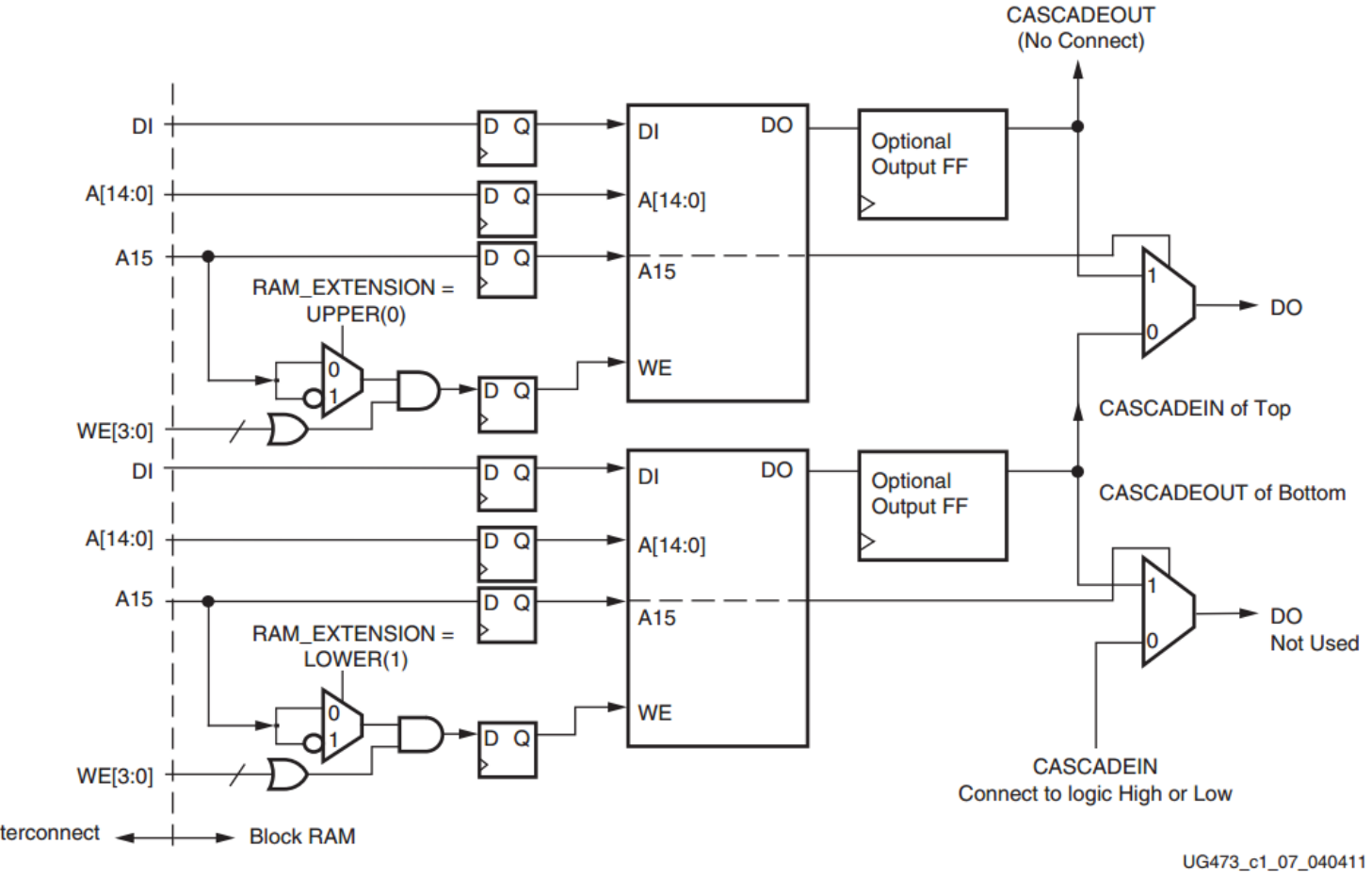
Configurations
32K x 1
16K x 2
8K x 4
4K x 8(or 9)
2K x 16(or 18)
1K x 32(or 36)

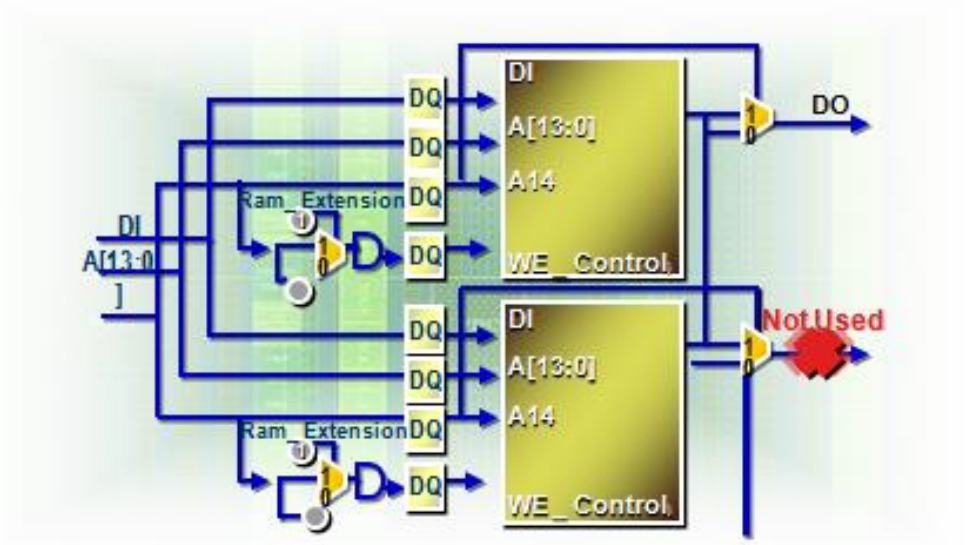
Primitive	Port A Width	Port B Width
RAMB16_S1_S1	1	1
RAMB16_S1_S2		2
RAMB16_S1_S4		4
RAMB16_S1_S9		(8+1)
RAMB16_S1_S18		(16+2)
RAMB16_S1_S36		(32+4)
RAMB16_S2_S2	2	2
RAMB16_S2_S4		4
RAMB16_S2_S9		(8+1)
RAMB16_S2_S18		(16+2)
RAMB16_S2_S36		(32+4)
RAMB16_S4_S4	4	4
RAMB16_S4_S9		(8+1)
RAMB16_S4_S18		(16+2)
RAMB16_S4_S36		(32+4)
RAMB16_S9_S9	(8+1)	(8+1)
RAMB16_S9_S18		(16+2)
RAMB16_S9_S36		(32+4)
RAMB16_S18_S18	(16+2)	(16+2)
RAMB16_S18_S36		(32+4)
RAMB16_S36_S36	(32+4)	(32+4)

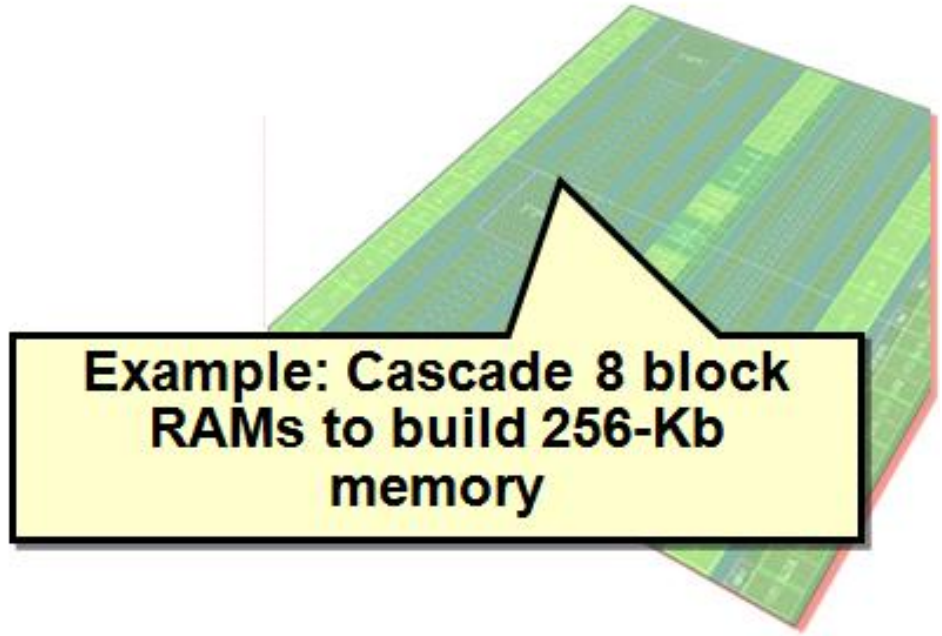
Block RAM Cascading

- Built-in cascade logic for 64Kx1
  - Cascade *two* vertically adjacent 32Kx1 block RAMs without using external CLB logic or compromising performance

Block RAM Cascading

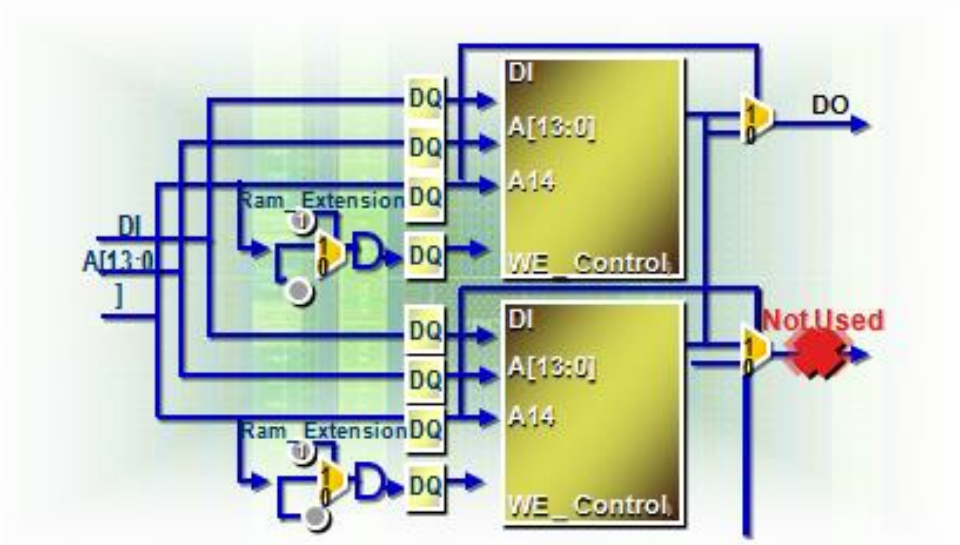


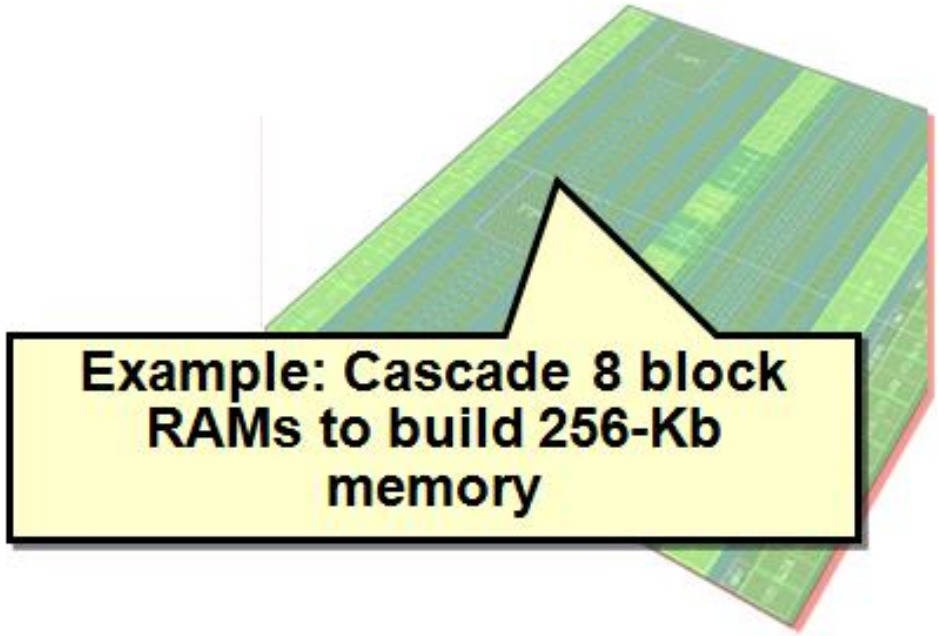




Block RAM Cascading

- Built-in cascade logic for 64Kx1
  - Cascade *two* vertically adjacent 32Kx1 block RAMs without using external CLB logic or compromising performance
  - Saves resources and improves speed of larger memories
- Cascade option for larger arrays
  - 128Kb, 256Kb, 512Kb, 1 Mb, …
  - Using external CLB logic for depth expansion
    - Not quite as fast as cascaded block RAMs
  - Width expansion uses parallel block RAMs





Verilog Codes for Memory

- Dual-Port RAM with Asynchronous Read (Distributed RAM)

```
module rams_dist (clk, we, a, dpra, di, spo, dpo);

input clk;
input we;
input [5:0] a;
input [5:0] dpra;
input [15:0] di;
output [15:0] spo;
output [15:0] dpo;
reg  [15:0] ram [63:0];

always @(posedge clk)
begin
 if (we)
   ram[a] <= di;
end

assign spo = ram[a];
assign dpo = ram[dpra];

endmodule
```

128x2 Dual Port LUT

reg [1:0] LUT [127:0];