ELD Lab 11

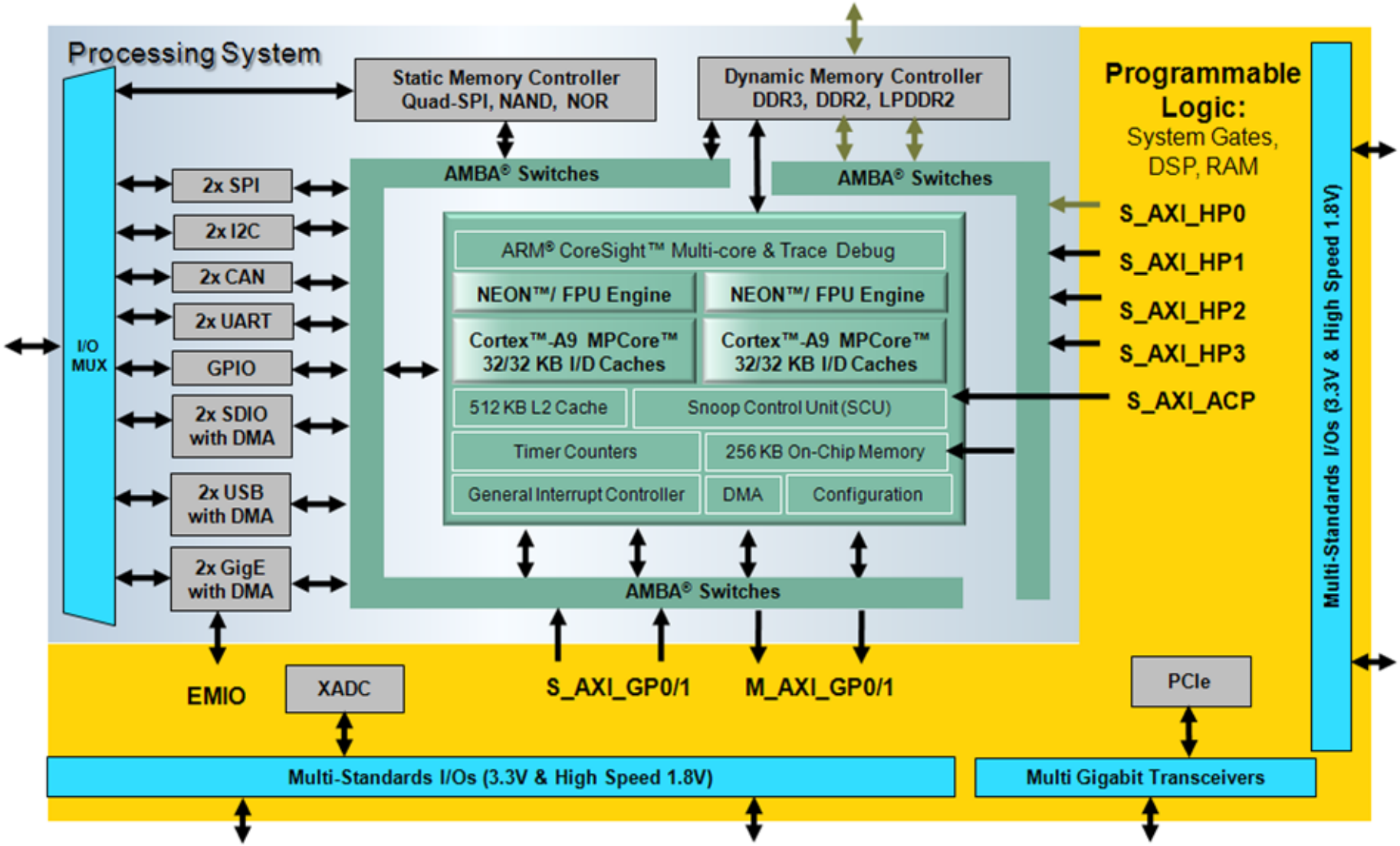
Multi-Stream IP based Accelerator Using FPGA and Comparison with ARM Processor

Objective

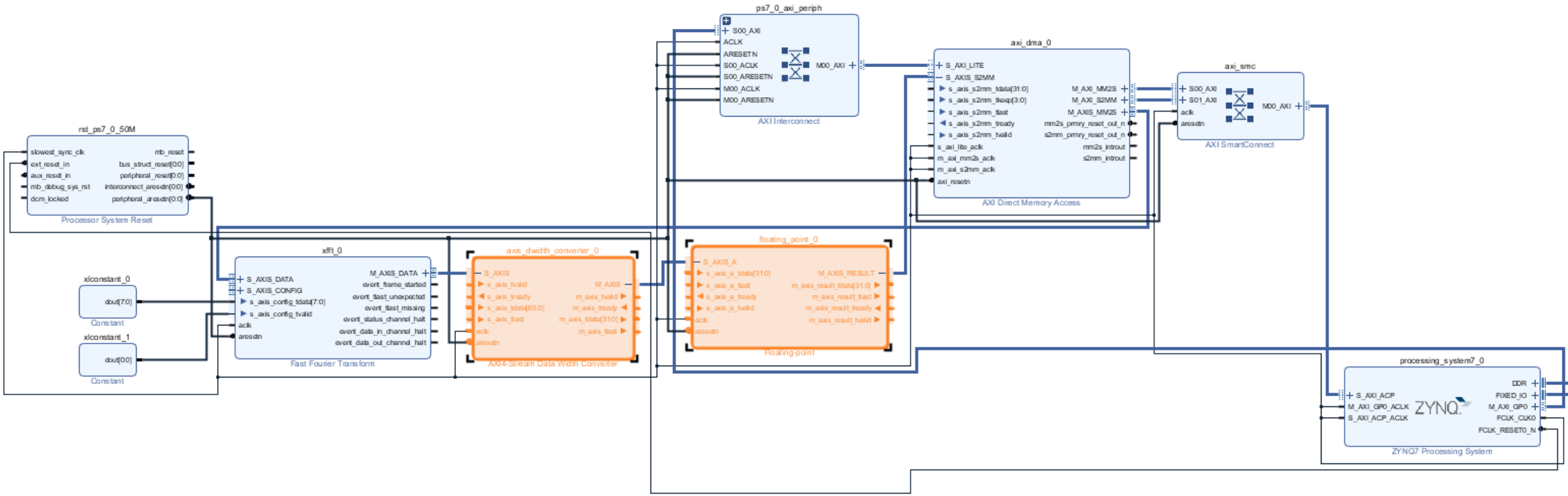
- Implement 8-point FFT followed by inverse on FPGA and ARM Cortex A9 processor of Zynq SoC and compare their execution time.
- Verify AXI transaction using ILA
- **Homework 1:** Implement 64-point FFT followed by inverse on FPGA and ARM Cortex A9 processor of Zynq SoC and compare their execution time.

Theory & Lab

Zynq Architecture: PS and PL



FFT Accelerator



Show disabled ports

Component Name: axi_dma_0

- [ ] Enable Asynchronous Clocks (Auto)
- [ ] Enable Scatter Gather Engine
- [ ] Enable Micro DMA
- [ ] Enable Multi Channel Support
- [ ] Enable Control / Status Stream

Width of Buffer Length Register (8-26): 23 bits

Address Width (32-64): 32 bits

Enable Read Channel

Number of Channels	1
Memory Map Data Width	64
Stream Data Width	64
Max Burst Size	64

- [x] Allow Unaligned Transfers

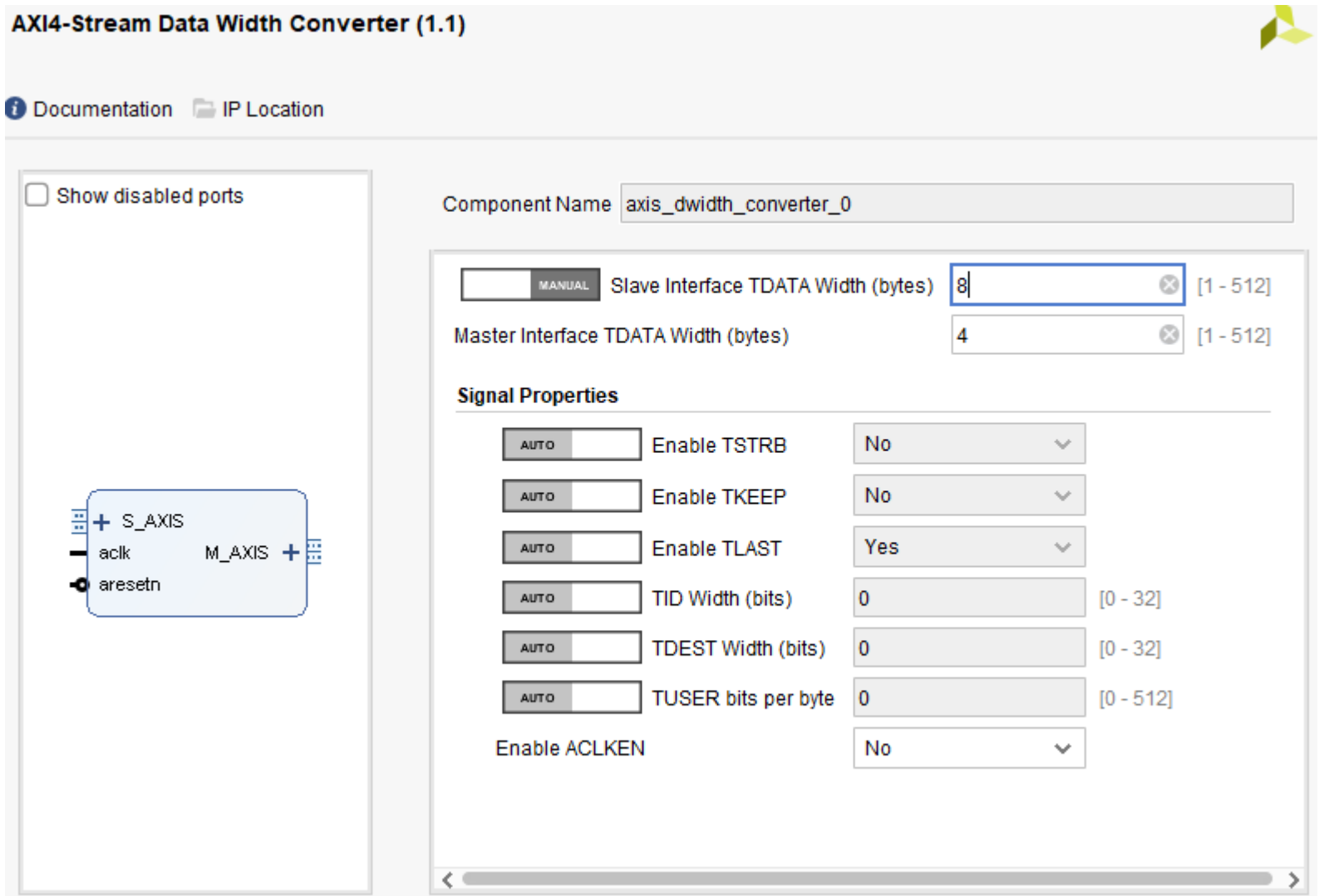
Enable Write Channel

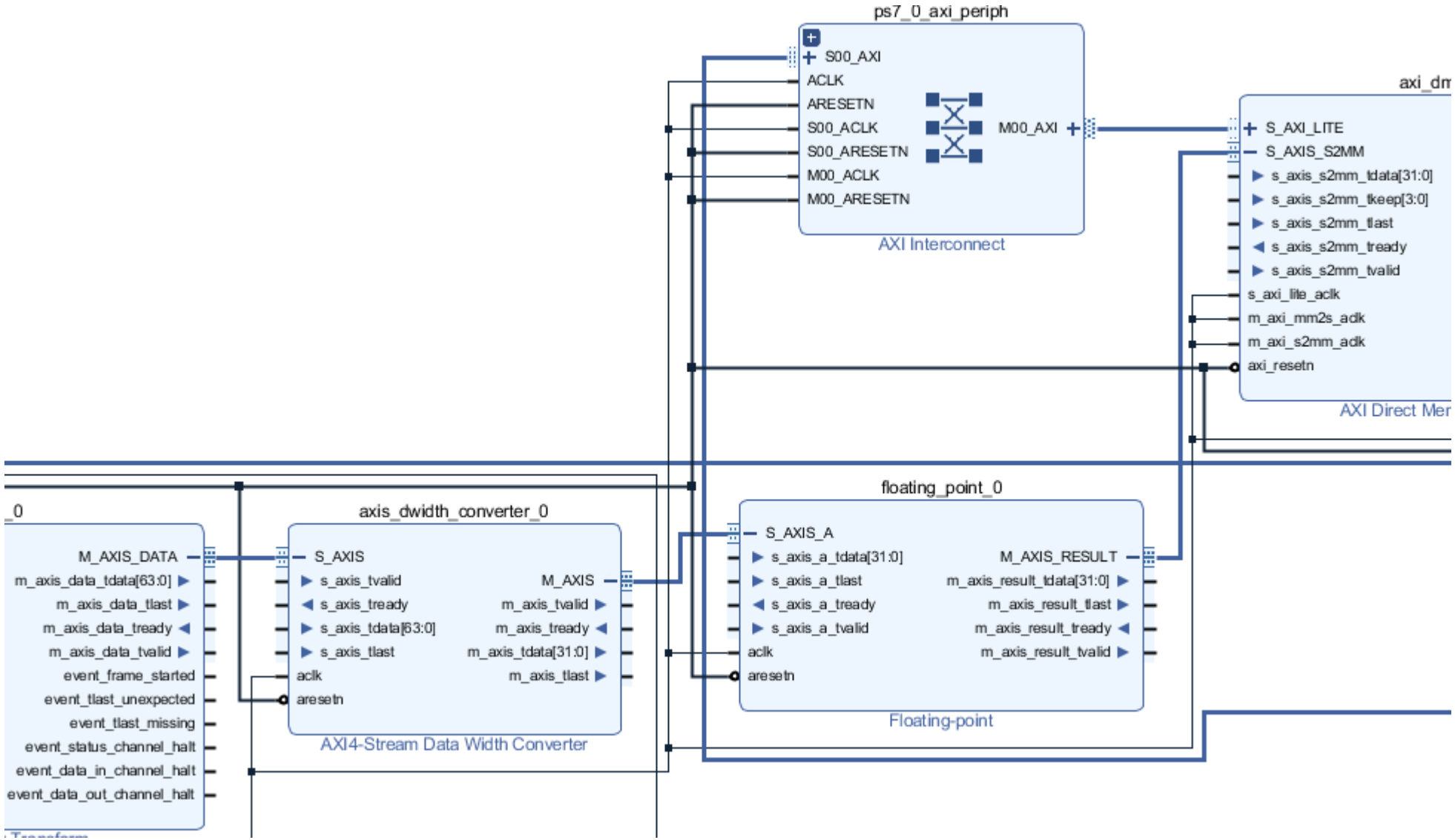
Number of Channels	1
MANUAL Memory Map Data Width	64
Stream Data Width (Auto)	32
Max Burst Size	64

- [x] Allow Unaligned Transfers
- [ ] Use Rxlength In Status Stream

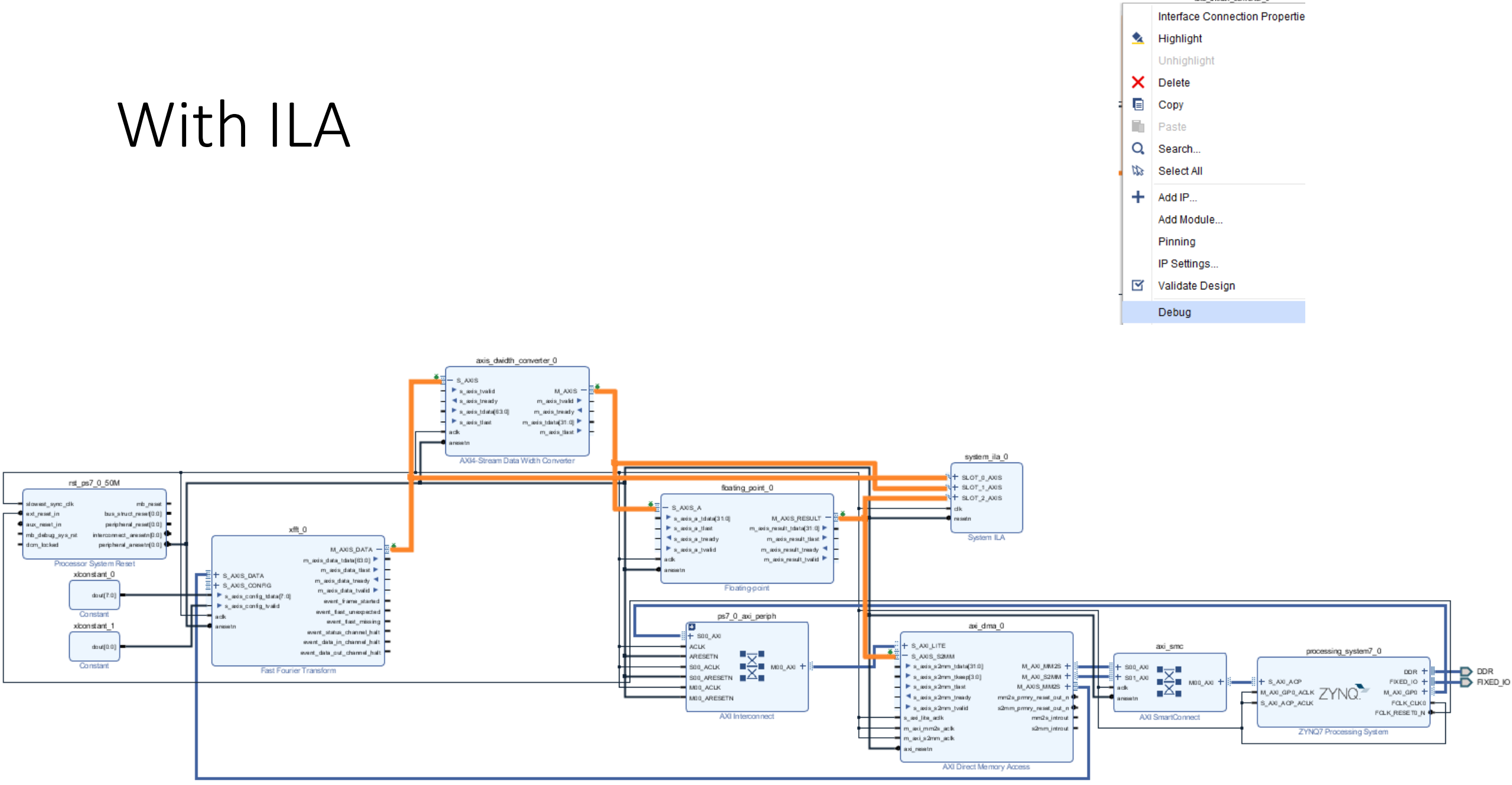
AUTO

- [ ] Enable Single AXI4 Data Interface


AXI4-Stream Data Width Converter (1.1)
Documentation
IP Location
Show disabled ports
S_AXIS
aclk
aresetn
M_AXIS
Component Name
axis_dwidth_converter_0
MANUAL
Slave Interface TDATA Width (bytes)
8
[1 - 512]
Master Interface TDATA Width (bytes)
4
[1 - 512]
Signal Properties
AUTO
Enable TSTRB
No
AUTO
Enable TKEEP
No
AUTO
Enable TLAST
Yes
AUTO
TID Width (bits)
0
[0 - 32]
AUTO
TDEST Width (bits)
0
[0 - 32]
AUTO
TUSER bits per byte
0
[0 - 512]
Enable ACLKEN
No


ps7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
axi_dm
S_AXI_LITE
S_AXIS_S2MM
s_axis_s2mm_tdata[31:0]
s_axis_s2mm_tkeep[3:0]
s_axis_s2mm_tlast
s_axis_s2mm_tready
s_axis_s2mm_tvalid
s_axi_lite_aclk
m_axi_mm2s_aclk
m_axi_s2mm_aclk
axi_resetn
AXI Direct Mer
floating_point_0
S_AXIS_A
s_axis_a_tdata[31:0]
s_axis_a_tlast
s_axis_a_tready
s_axis_a_tvalid
aclk
aresetn
M_AXIS_RESULT
m_axis_result_tdata[31:0]
m_axis_result_tlast
m_axis_result_tready
m_axis_result_tvalid
Floating-point
axis_dwidth_converter_0
S_AXIS
s_axis_tvalid
s_axis_tready
s_axis_tdata[63:0]
s_axis_tlast
aclk
aresetn
M_AXIS
m_axis_tvalid
m_axis_tready
m_axis_tdata[31:0]
m_axis_tlast
AXI4-Stream Data Width Converter
_0
M_AXIS_DATA
m_axis_data_tdata[63:0]
m_axis_data_tlast
m_axis_data_tready
m_axis_data_tvalid
event_frame_started
event_tlast_unexpected
event_tlast_missing
event_status_channel_halt
event_data_in_channel_halt
event_data_out_channel_halt

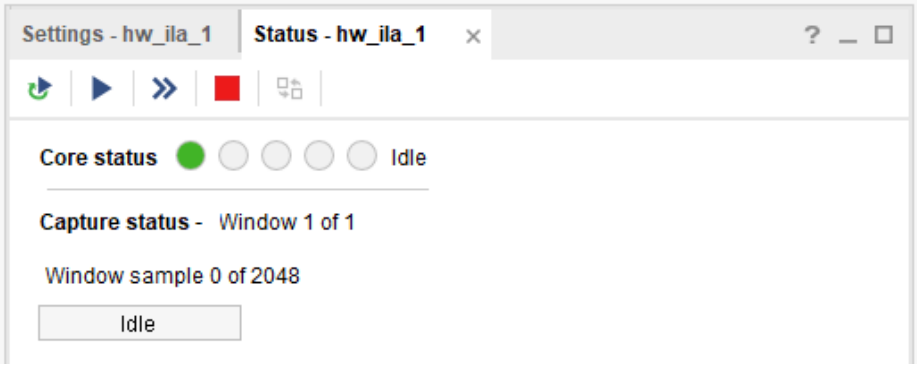
With ILA

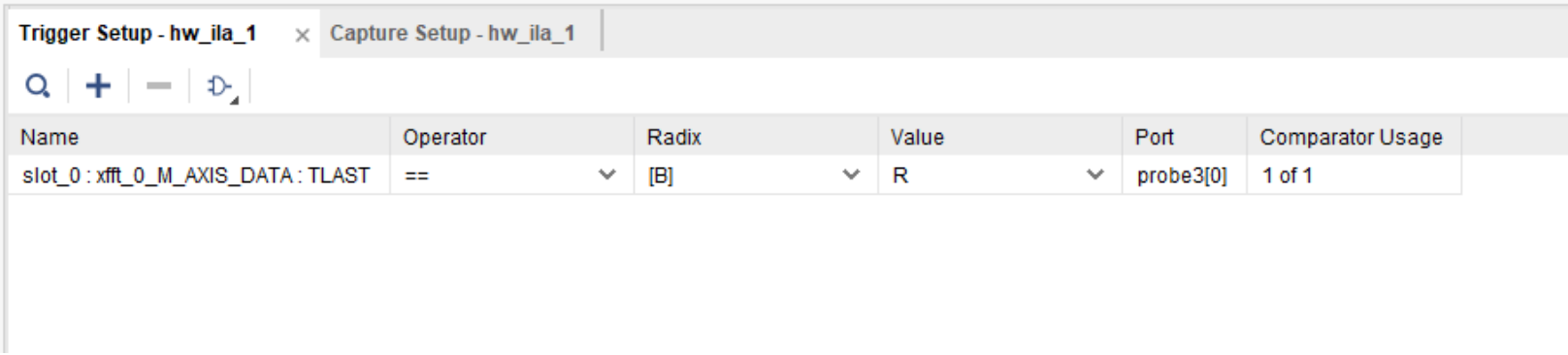

Interface Connection Propertie
Highlight
Unhighlight
Delete
Copy
Paste
Search...
Select All
Add IP...
Add Module...
Pinning
IP Settings...
Validate Design
Debug
axis_dwidth_converter_0
AXI4-Stream Data Width Converter
rst_ps7_0_50M
Processor System Reset
xfft_0
Fast Fourier Transform
xlconstant_0
Constant
xlconstant_1
Constant
floating_point_0
Floating-point
system_ila_0
System ILA
ps7_0_axi_periph
AXI Interconnect
axi_dma_0
AXI Direct Memory Access
axi_smc
AXI SmartConnect
processing_system7_0
ZYNQ7 Processing System
DDR
FIXED_IO

Execution Time Using Timer

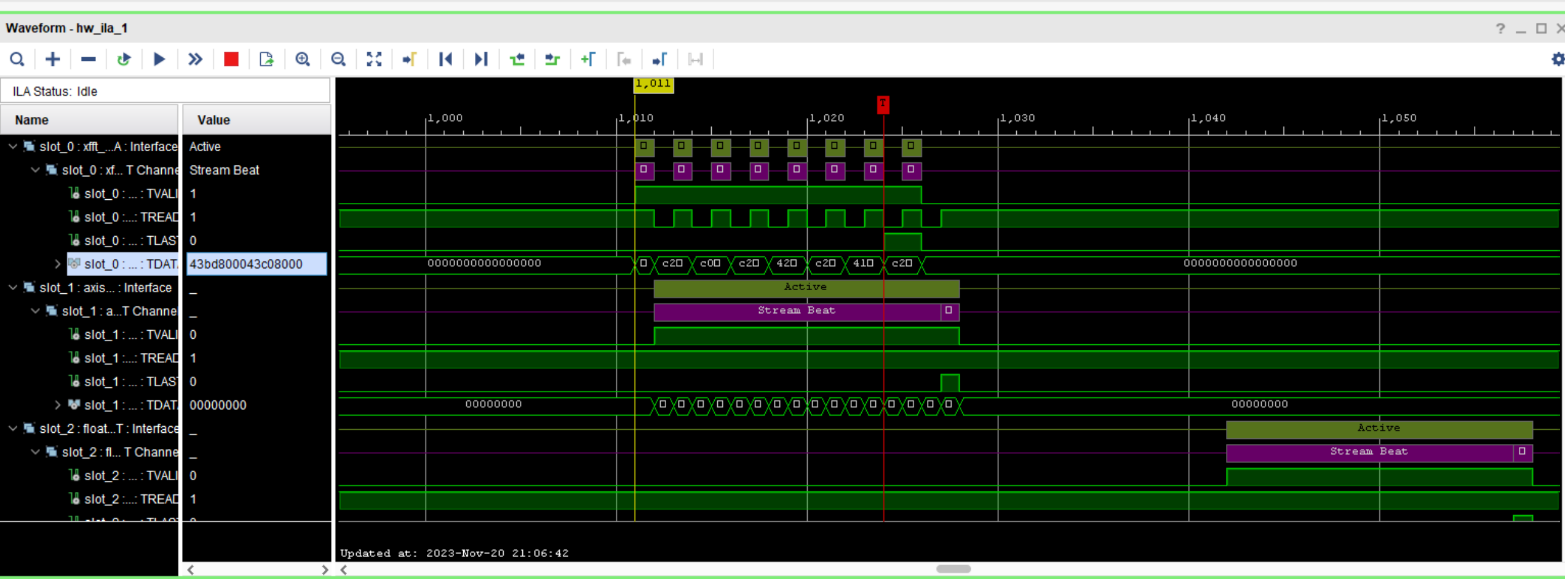
```
PS Output- 0.002597+0.002639I, PL Output- 0.002597+0.002639IDMA Transfer Successful!

PS Output- 0.015893+-0.022389I, PL Output- 0.015893+-0.022389IDMA Transfer Successful!

PS Output- -0.004274+-0.250000I, PL Output- -0.004274+-0.250000IDMA Transfer Successful!

PS Output- -0.008184+-0.027563I, PL Output- -0.008184+-0.027563IDMA Transfer Successful!

PS Output- 0.009524+0.012346I, PL Output- 0.009524+0.012346IDMA Transfer Successful!

PS Output- 0.052412+-0.010949I, PL Output- 0.052412+-0.010949IDMA Transfer Successful!

PS Output- -0.041667+0.050000I, PL Output- -0.041667+0.050000IDMA Transfer Successful!

PS Output- -0.009633+-0.008353I, PL Output- -0.009633+-0.008353IDMA Transfer Successful!

------- Execution Time Comparison --------

Execution time for PS in Micro-seconds: 5.291291

Execution time for PL in Micro-seconds: 8.759760
```

Vivado ILA


Settings - hw_ila_1
Status - hw_ila_1
Core status
Idle
Capture status - Window 1 of 1
Window sample 0 of 2048
Idle


Trigger Setup - hw_ila_1
Capture Setup - hw_ila_1
Name
Operator
Radix
Value
Port
Comparator Usage
slot_0 : xfft_0_M_AXIS_DATA : TLAST
==
[B]
R
probe3[0]
1 of 1

Vivado ILA


Waveform - hw_ila_1
ILA Status: Idle
Name
Value
slot_0 : xfft_...A : Interface
Active
slot_0 : xf... T Channe
Stream Beat
slot_0 : ... : TVALI
1
slot_0 :...: TREAD
1
slot_0 : ... : TLAST
0
slot_0 : ... : TDAT
43bd800043c08000
slot_1 : axis... : Interface
slot_1 : a...T Channe
slot_1 : ... : TVALI
0
slot_1 :...: TREAD
1
slot_1 : ... : TLAST
0
slot_1 : ... : TDAT
00000000
slot_2 : float...T : Interface
slot_2 : fl... T Channe
slot_2 : ... : TVALI
0
slot_2 :...: TREAD
1
1,011
T
1,000
1,010
1,020
1,030
1,040
1,050
0000000000000000
c2
c0
c2
42
c2
41
c2
0000000000000000
Active
Stream Beat
00000000
00000000
Active
Stream Beat
Updated at: 2023-Nov-20 21:06:42