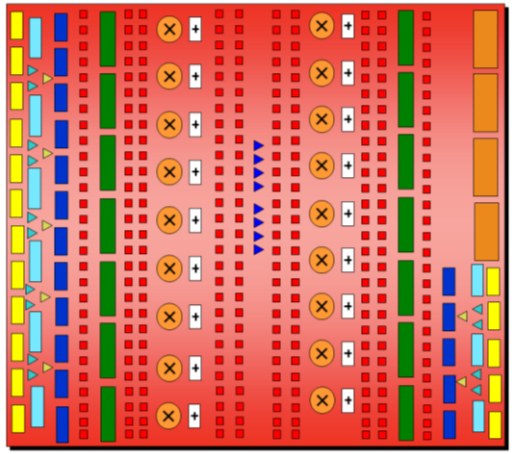
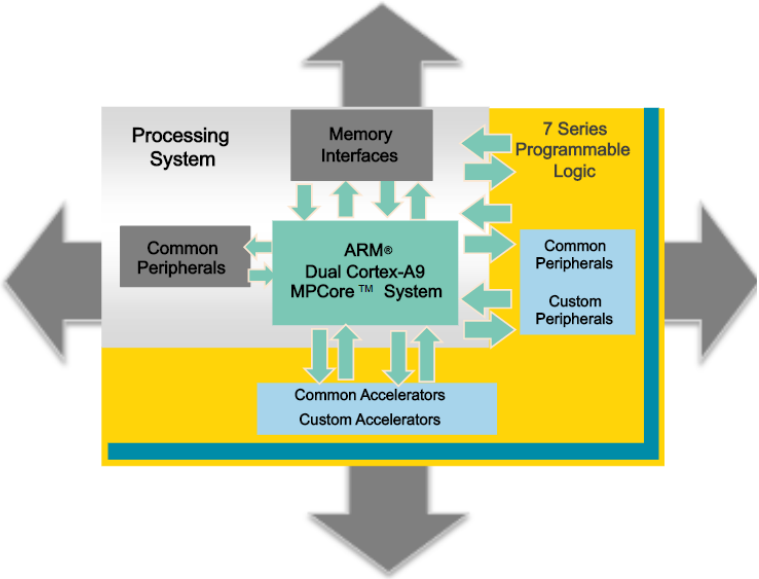
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

A2A
Algorithms to Architecture

ECE 270: Embedded Logic Design





Dr. Sumit J Darak
Algorithms to Architectures Lab
Associate Professor, ECE, IIIT Delhi
http://faculty.iiitd.ac.in/~sumit/

Instructor

- **Teaching Experience (UG):** DC (3 years) and ELD (6 years): avg. feedback 3.9+/5
- **Teaching Experience (PG):** DHD (4 years) and AELD (4 years): avg. feedback 4.5+/5
- **Consultant:** VVDN Tech. (2.5 years), Apexplus Tech. (1 year)
- **Research projects:** Reconfigurable and intelligent architectures for wireless/radar/satellite, light-weight AI/ML on hardware (CPU, GPU, Microcontrollers)
- Gain good enough knowledge in digital system design

What you (should) know ☺

- **Binary number representation:** Signed, unsigned
- **Combinational circuits:** logic gates, multiplexers, encoder, decoder, adder, subtractor, multipliers, BCD adder
- **Sequential circuits:** latch, flip-flops, counter (synchronous and asynchronous), registers, frequency divider, mod-counter with desired duty-cycle and phase
- **Finite state machines (FSM):** Moore and mealy, pattern generation and detection
- **Timing*:** Setup and hold time, Critical path delay, pipelining

What you *don't* know ☺☺

- **Binary number representation:** Signed, unsigned (Impact on hardware)
- **Combinational circuits** -> logic gates, multiplexers, encoder, decoder, adder, subtractor, multipliers, BCD adder (Prototype on hardware)
- **Sequential circuits** -> latch, flip-flops, counter (synchronous and asynchronous), registers, frequency divider, mod-counter with desired duty-cycle and phase (Prototype on hardware)
- **Finite state machines (FSM)** -> Moore and mealy, pattern generation and detection: (Prototype on hardware)
- **Timing:** Setup and hold time, Critical path delay, pipelining (Use it to optimize your prototypes on hardware)
- Embedded Systems, heterogenous platforms and many more…

What you will learn by December-end?

- Design and implement any algorithm on software (ARM Processor) and hardware (FPGA)
- Compare the execution time between software and hardware
- First baby step towards hardware-software co-design
- **Philosophy:** I hear and I forget. I see and I remember. I do and I understand: Confucius/Xunzi

Textbooks and Online Resources

- *“Verilog HDL” by Samir Palnitkar*
- https://hdlbits.01xz.net/wiki/Main_Page (VIMP)
- *Datasheets and reference manuals from Xilinx (will be shared on Google classroom)*
- *D. Harris and S. Harris, “Digital Design and Computer Architecture”, Morgan Kauffmann, 2012.*
- Online resources*
  1. https://www.youtube.com/c/AlgorithmstoArchitectureIIITDelhi/playlists
  2. http://www.asic-world.com/verilog/veritut.html
  3. https://www.youtube.com/playlist?list=PL7kkolCtIBKLukrBsEDwKRTE64JvaJDhM
  4. https://www.youtube.com/user/LBEbooks/videos
  5. https://www.youtube.com/playlist?list=PLoVsjlwzzlUQqPluXn-XWRP5t0G1jqamj

Lectures

- Monday and Thursday: 11 am –12.30 pm
- FPGA and System-on-Chip architectures
- Verilog/C programming
- Refer to previous year’s video lectures on YouTube channel.
- Discussions during lecture and lab sessions will NOT be recorded
- **Lectures:** Not mandatory*

Labs

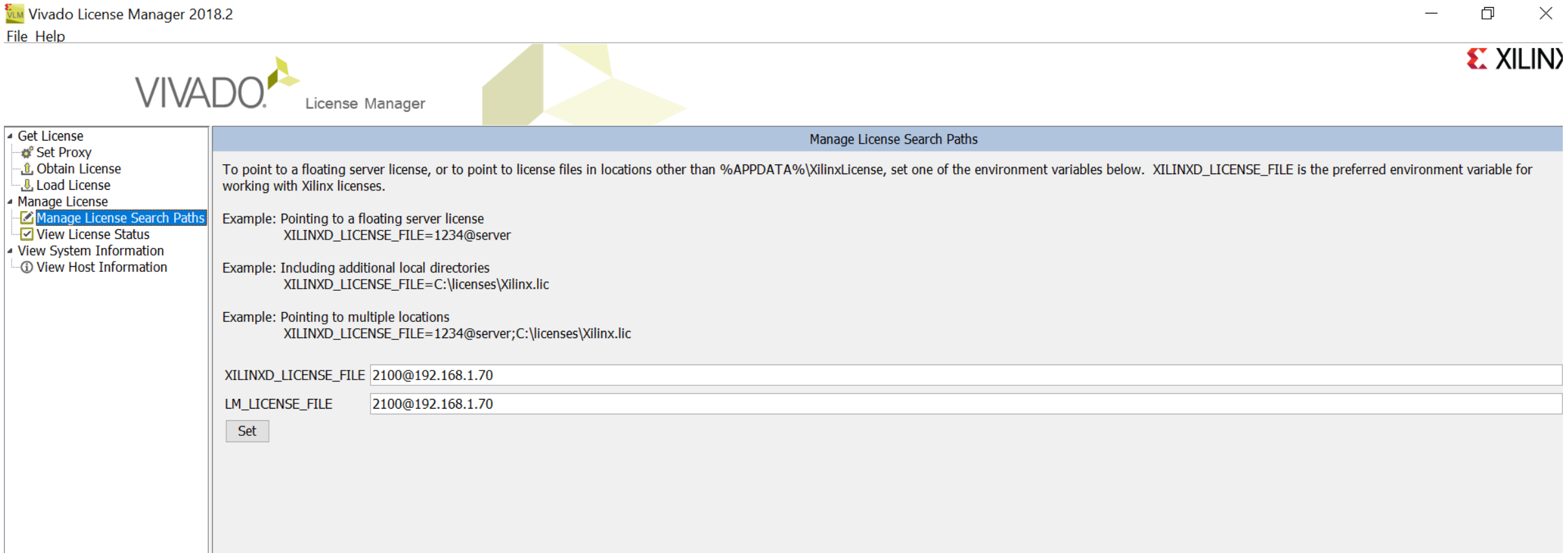
- **Philosophy:** I hear and I forget. I see and I remember. I do and I understand: Confucius/Xunzi
- Opportunity to consolidate your learning through a series of interesting design examples
- Lab attendance should be 100%. Most of the materials are design from scratch and are based on datasheets (100+ pages for each sub-module). Three labs hours are equivalent to 20 hours of self-study.
- Weekly lab homework are extensions of lab exercises
- Install Vivado 2019.1 (**with SDK**) on your laptops before first lab. Installation manual is shared on Classroom. Use Laptop with at least 4/8 GB RAM.
- We will share the policy for accessing desktop and FPGA /SoC boards remotely.

Labs

- Labs will be conducted by Instructor* and will start sharp at 8.30 am. Late comers will not be allowed (Same for lectures as well).
- You need to complete the lab homework and pass the viva. Total 10 out of 12 labs will be considered and there are 1.5 marks for each Viva.
- Lab grades are given only if you attend the lab and complete all the tasks.
- If you skip the viva (conducted in subsequent week) without informing before the submission deadline, there will be penalty of 1 mark.
- Lab sessions will not be recorded (Refer to YouTube channel for previous year's videos)
- Please follow the lab and lecture discipline

Lab requirements

- Install Vivado 2019.1 and SDK
- Check google classroom for lab handouts



Evaluation

- Assignments: 0%
- Mid-term Exam (Theory and Lab): 30%
- Final Exam (Theory and Lab): 30%
- Surprise Quizzes: 25% (Two optional quizzes, No re-quiz)
- Lab Homework: 15%

Plagiarism: Zero tolerance!

https://www.iiitd.ac.in/sites/default/files/docs/education/AcademicDishonesty.pdf

1) **One letter grade reduction for first instance during entire stay at IIITD and report to academic department**
2) **F grade for each subsequent instances**

***In case of habitual offenders in multiple courses or past history, stringent action will be taken.**

Evaluation (A+ Grade)

- If you would like to be considered for A+ grade, you should have at least 60% in all quizzes/exams/assignments (till mid-semester)

and

- Minor project after mid-semester
- For A+ grade,

  1) Complete the project

  2) Score at least 90% in rest of the course

Grades are important 😐

- For good internship
- For good research project
- For scholarship/TA'ship during BTech
- For BTP
- For recommendation letters
- For placements in "good" companies
- For admission and scholarship for MS/PhD

Grade	Lowest	Highest	No. of students
A+	91	103	4
A	91	103	7
A-	79	89	13
B	70	77	10
B-	63	68	5
C	53	60	10
C-	44	50	8
D	20	40	18
F	0	16	16

Grade	Lowest	Highest	No. of students
A+	90	100	2
A	77	86	10
A-	70	76	12
B	56	68	21
B-	46	55	14
C	36	44	15
C-	25	34	10
D	16	23	2
F	-2	11	6

Grade	Lowest	Highest	No. of students
A	93	95.5	2
A-	76.8	87.5	7
B	64.2	72.8	15
B-	55.7	61.6	4
C	40.5	53.2	29
C-	29.2	38.3	15
D	20.8	27.6	10
F	18	0	20
Total			102

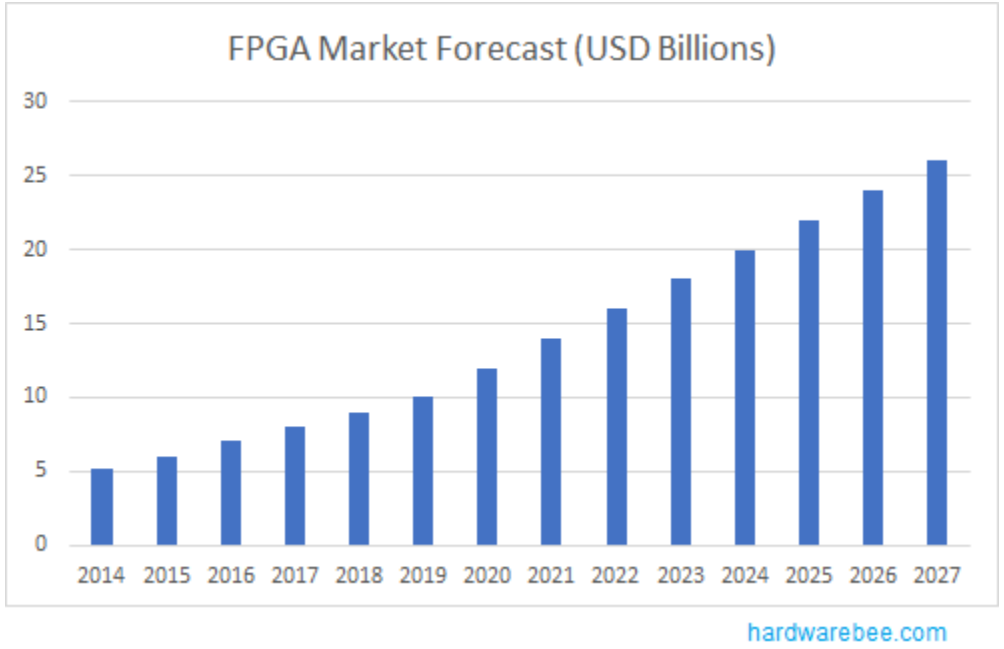
Grade	Lowest	Highest	No. of students
A+	87	87	1
A	83.55	88	3
A-	74	81	8
B	63.5	71.7	10
B-	55.25	61.1	9
C	38.1	51.5	26
C-	26.3	36.8	23
D	17	25	12
F	0	15	10
Total			102

In Monsoon 2023, anyone scoring 30 or below will directly receive F grade.
Relative grading above 30.

Why ELD?

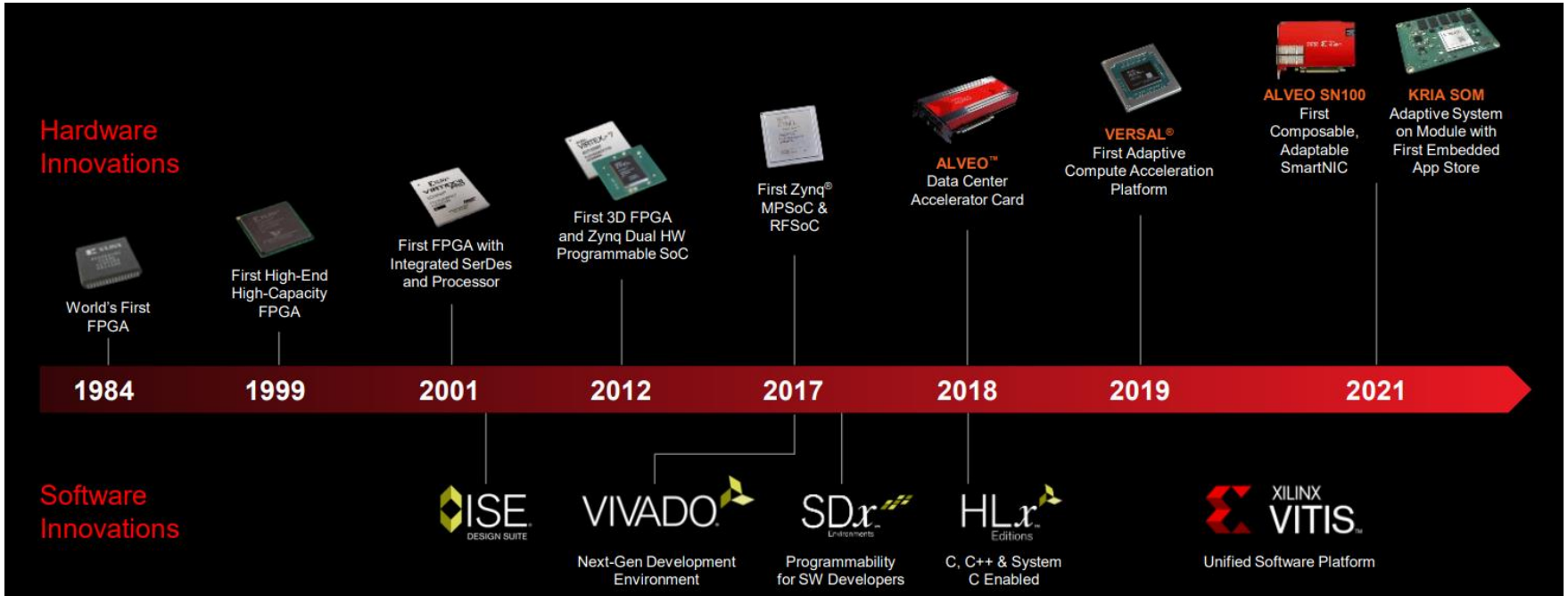
- Focus on FPGA as well as System on Chip architecture
- State-of-the-art labs, software and hardware
- Skill sets relevant for other VLSI domains

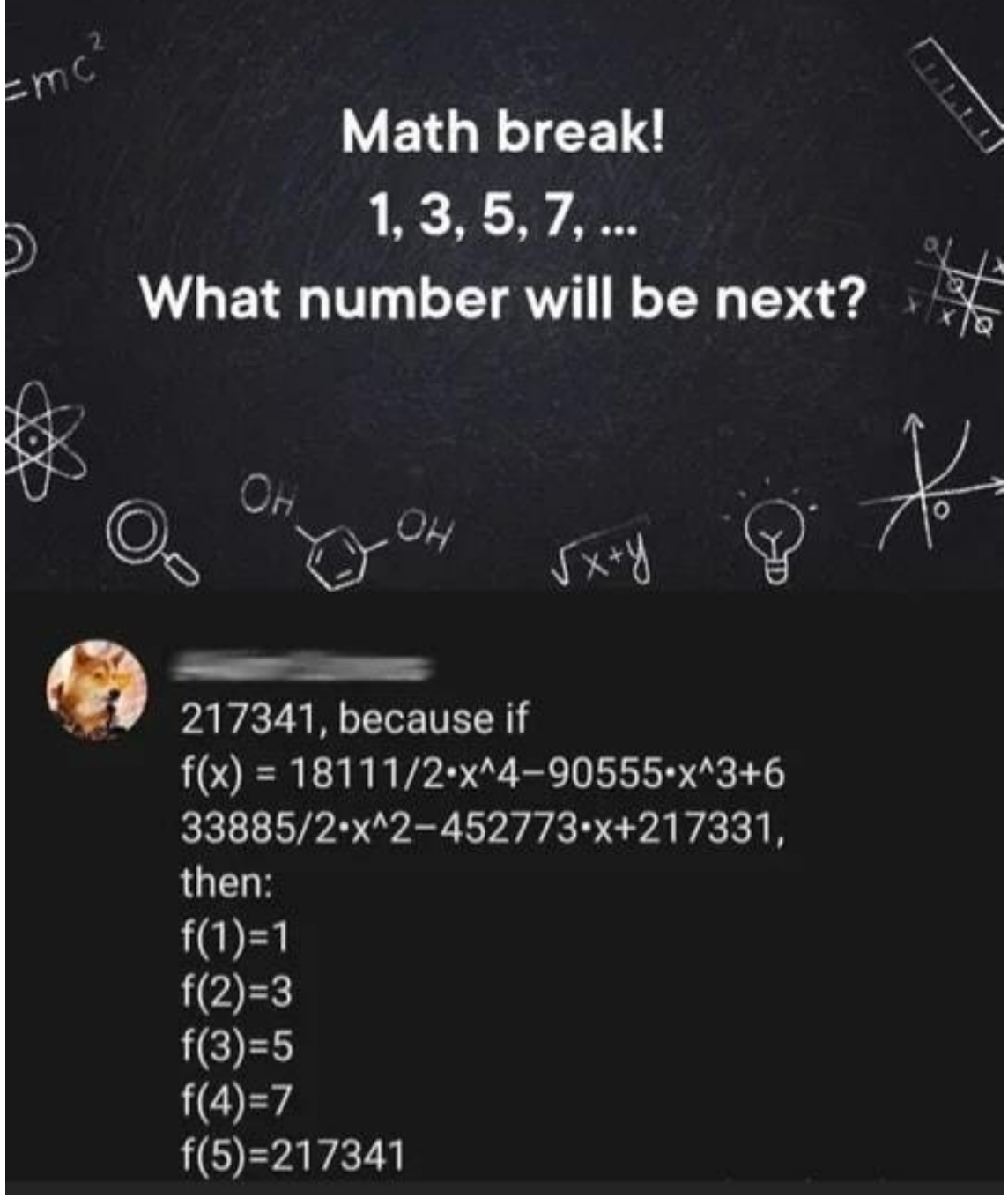
FPGAs are getting more popular!



Why ELD?

- Wide range of applications: Data center, wired and wireless communications, smarter vision, automotive, defense, aerospace, IoT, medical and audio etc.
- Significant change in SoC architectures in last 3-4 years to make them suitable for above applications.




Math break!
1, 3, 5, 7, ...
What number will be next?
OH
OH
√x+y
[redacted]
217341, because if
f(x) = 18111/2•x^4−90555•x^3+6
33885/2•x^2−452773•x+217331,
then:
f(1)=1
f(2)=3
f(3)=5
f(4)=7
f(5)=217341

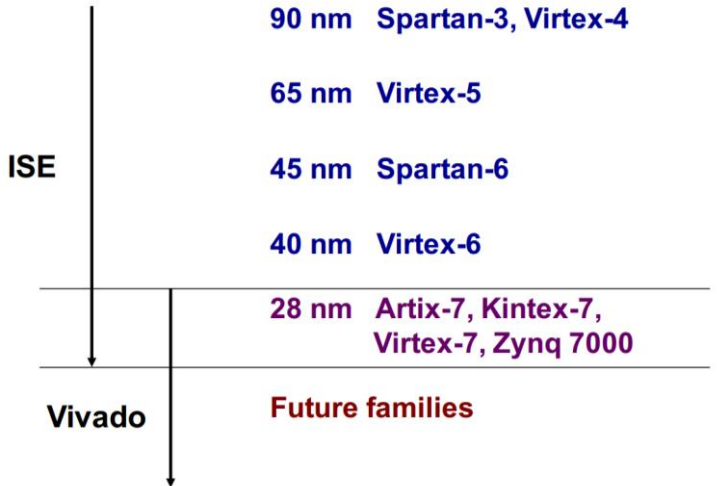
Why ELD?

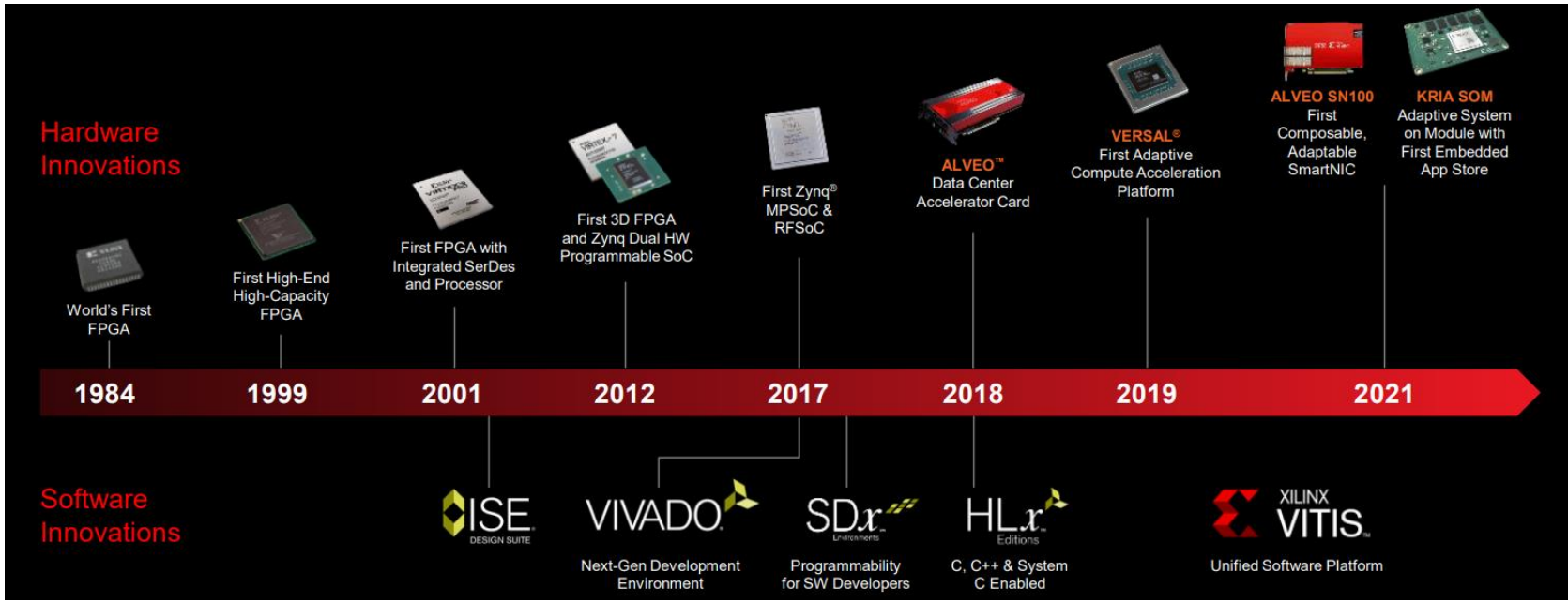
- Wide range of SoC applications: Data center, wired and wireless communications, smarter vision, medical and audio applications etc.
- Significant change in SoC architectures in last 3-4 years to make them suitable for above applications.
- **HDL for synthesis:** one of the most sought-after skills
- Knowledge of **state-of-the-art tools and modern SoC technologies** used in the R&D industry

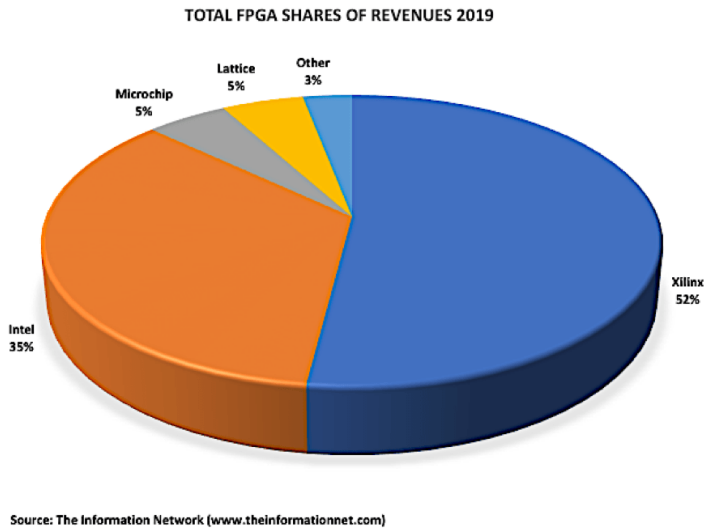
Why ELD?

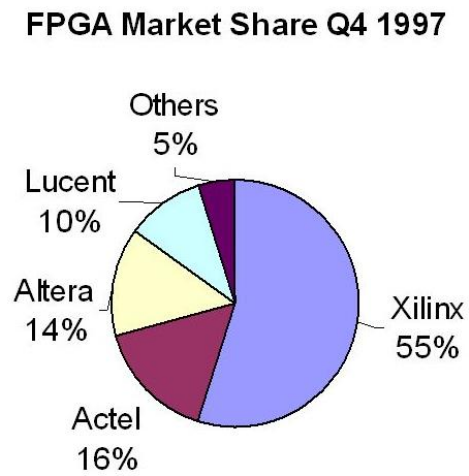
Xilinx FPGA Families

Technology	Low-cost	Mid-range	High-performance
220 nm			Virtex
180 nm	Spartan-II, Spartan-IIE		
120/150 nm			Virtex-II, Virtex-II Pro
90 nm	Spartan-3		Virtex-4
65 nm			Virtex-5
45 nm	Spartan-6		
40 nm			Virtex-6
28 nm	**Artix-7**	Kintex-7	Virtex-7
20 nm		Kintex UltraSCALE	Virtex UltraSCALE
16 nm		Kintex UltraSCALE+	Virtex UltraSCALE+

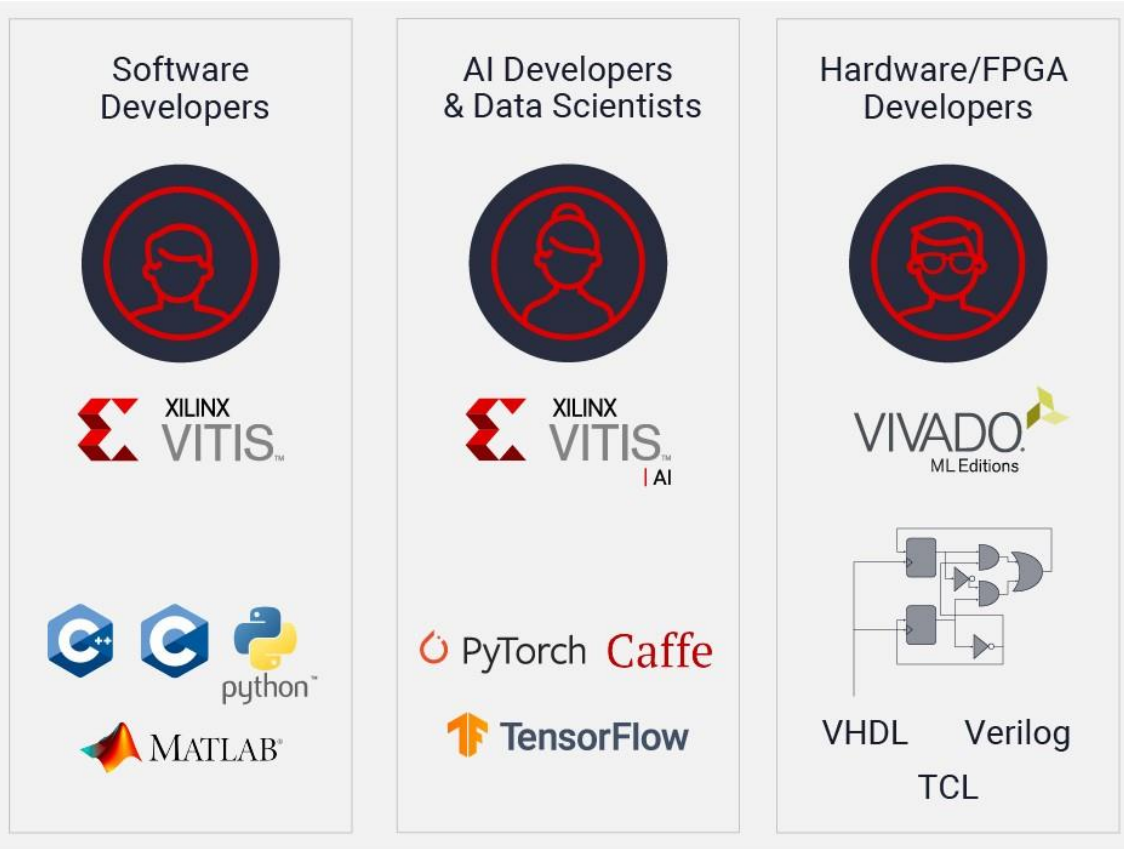


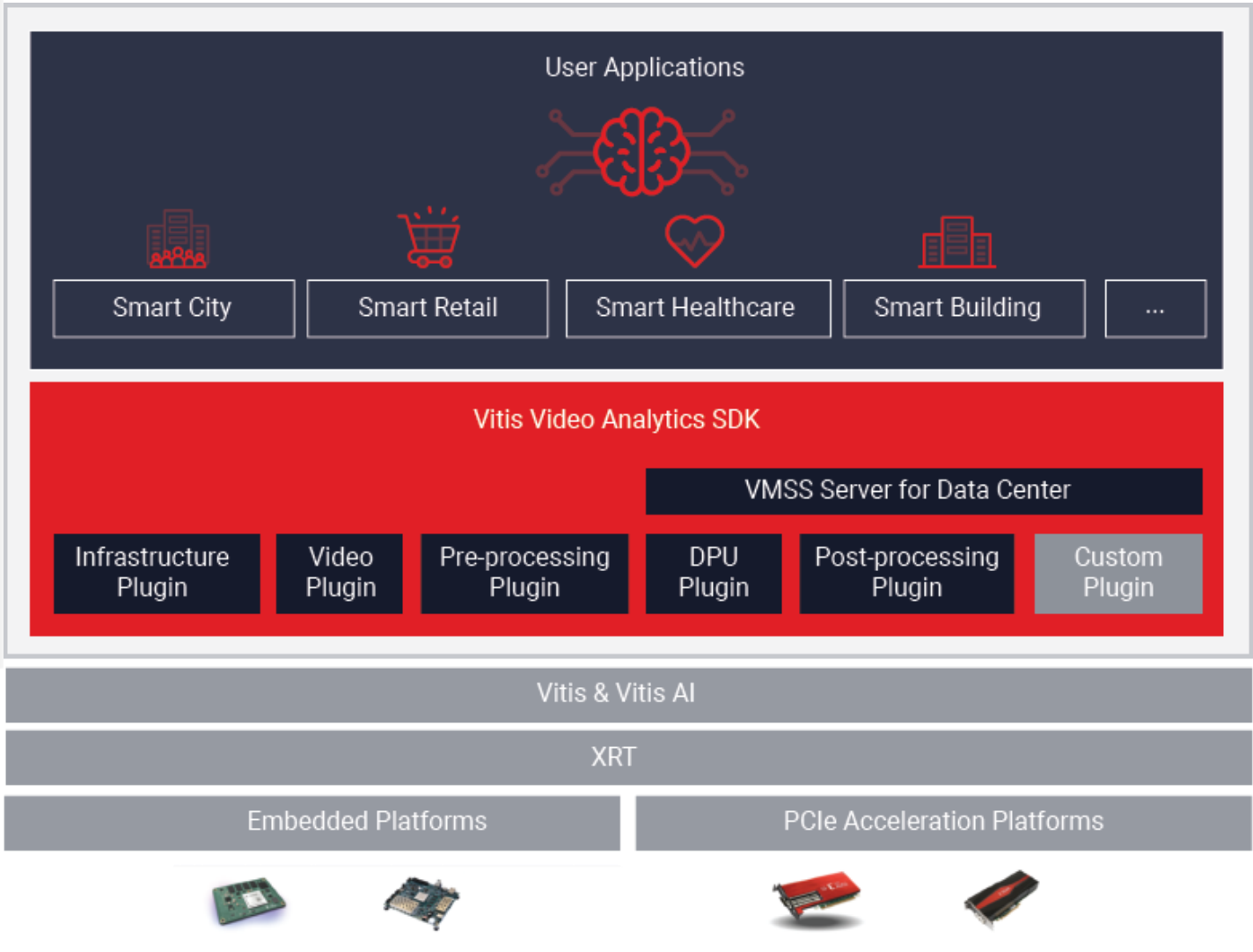






Why ELD?


Software Developers
XILINX VITIS
python
MATLAB
AI Developers & Data Scientists
XILINX VITIS AI
PyTorch
Caffe
TensorFlow
Hardware/FPGA Developers
VIVADO ML Editions
VHDL
Verilog
TCL


User Applications
Smart City
Smart Retail
Smart Healthcare
Smart Building
...
Vitis Video Analytics SDK
VMSS Server for Data Center
Infrastructure Plugin
Video Plugin
Pre-processing Plugin
DPU Plugin
Post-processing Plugin
Custom Plugin
Vitis & Vitis AI
XRT
Embedded Platforms
PCIe Acceleration Platforms

Why This Course?

Location / *City*	Class Title (Click to Register)	Price
AL *Huntsville*	Vivado Design Suite for ISE Project Navigator Users (1 day)	800 USD
MA *Burlington*	Designing with Verilog (3 days)	2100 USD
MN *Minneapolis*	Designing with 7 Series (2 days)	1400 USD
GA *Duluth*	Essentials of FPGA Design (2 days)	1500 USD

Designing with Verilog

Add to Cart

USD Price = 300
Training Credit Price = 3 TC
Show Detailed Course Description

Overview

Provides a thorough introduction to the Verilog language.
The emphasis is on:

- Writing efficient hardware designs
- Performing high-level HDL simulations
- Employing structural,register transfer level (RTL), and behavioral coding styles
- Targeting Xilinx devices specifically and FPGA devices in general
- Utilizing best coding practices

View the course description PDF for more details.

What's new for 2019.1:

- Mealy Finite State Machines: New state diagram for detecting a non-overlapping sequence added
- Moore Finite State Machines: New state diagram for detecting an overlapping sequence added

Questions?

- Email Us
- Frequently Asked Questions

Embedded Systems Design

Add to Cart

USD Price = 200
Training Credit Price = 2 TC
Show Detailed Course Description

Overview

Highlights the general embedded concepts, tools, and techniques using the Vivado Design Suite.
The emphasis is on:

- Designing, expanding,and modifying embedded systems utilizing the features and capabilities of the Zynq® System on a Chip (SoC), Zynq UltraScale+™ MPSoC, or MicroBlaze™ soft processor
- Adding and simulating AXI-based peripherals using bus functional model (BFM) simulation

Questions?

- Email Us
- Frequently Asked Questions

C-based Design - High-Level Synthesis with the Vivado HLx Tool

Add to Cart

USD Price = 200
Training Credit Price = 2 TC
Show Detailed Course Descripti

Overview

This content provides a thorough introduction to the Vivado® High-Level Synthesis (HLS) tool.
The focus is on:

- Covering synthesis strategies and features
- Improving through put, area, interface creation, latency, testbench coding, and coding tips
- Utilizing the Vivado HLS tool to optimize code for high-speed performance in an embedded environment
- Downloading for in-circuit validation

View the course description PDF for more details.
What's new for 2019.2:

- Introduction to High-Level Synthesis: Added the RTL black-box feature, which enables the integration of a pre-existing RTL IP into an HLS design
- Introduction to I/O Interfaces: Updated the graphics to make sure they point to proper block-level or port-level interfaces
- Vivado HLS Tool C Libraries - Arbitrary Precision: Added more information on floating-point cores
- HLS Design Flow - System Integration: Added Zynq® UltraScale+™ ZCU104 board support to the lab
- Accelerating OpenCV Applications Using Vivado HLS Video Libraries: Added more information on using OpenCV in FPGA designs

Questions?

- Email Us
- Frequently Asked Questions

Why ELD?

- https://www.youtube.com/watch?v=p3KYmsTUj_0
- https://www.youtube.com/watch?v=Ksm8xzSWrko&list=PLRr5m7hDN9TJbNEs3LWbk0N9iI4wcyzU5&index=2
- https://www.youtube.com/watch?v=CTrG-iLGCOw
- https://www.youtube.com/watch?v=AcmAOBaMblk&list=PLRr5m7hDN9TJbNEs3LWbk0N9iI4wcyzU5&index=18
- https://www.youtube.com/playlist?list=PLPbeWYWLwPjBZnGLtcGu-Brst7LBIUf9f
- https://www.youtube.com/watch?v=8pCeZvHnR6I&ab_channel=Yu-ChienChung
- https://www.youtube.com/watch?v=7pdFxzoWy-Y&ab_channel=XilinxInc
- https://www.youtube.com/watch?v=63hfjQJsCb8&ab_channel=XilinxInc
- https://www.youtube.com/watch?v=1WOpdyr7cTU&list=PL579fbjB-a0vAr1L90KnYSxhAKEbRVI5g&index=3&ab_channel=AlgorithmstoArchitectureIIITDelhi
- https://www.youtube.com/watch?v=RSxh13s0FgQ&list=PL579fbjB-a0vAr1L90KnYSxhAKEbRVI5g&index=11&ab_channel=AlgorithmstoArchitectureIIITDelhi

CloudLab: Physical Lab Experiments in Online Mode

Motivation

- Delivery of hardware based courses has been challenging task in offline mode.
- Example: FPGA, System-on-Chip, Robotics, IoT
- During pandemic, over 95% of the universities have dropped such courses due to lack of remote access systems.
- Online and hybrid course delivery will be a requirement even after pandemic is over.
- Lack of hardware based system design exposure leads to significant compromise on course objectives and impact the availability of trained manpower in academia as well as industry.
- Poor utilization of hardware resources available in resource-rich universities.

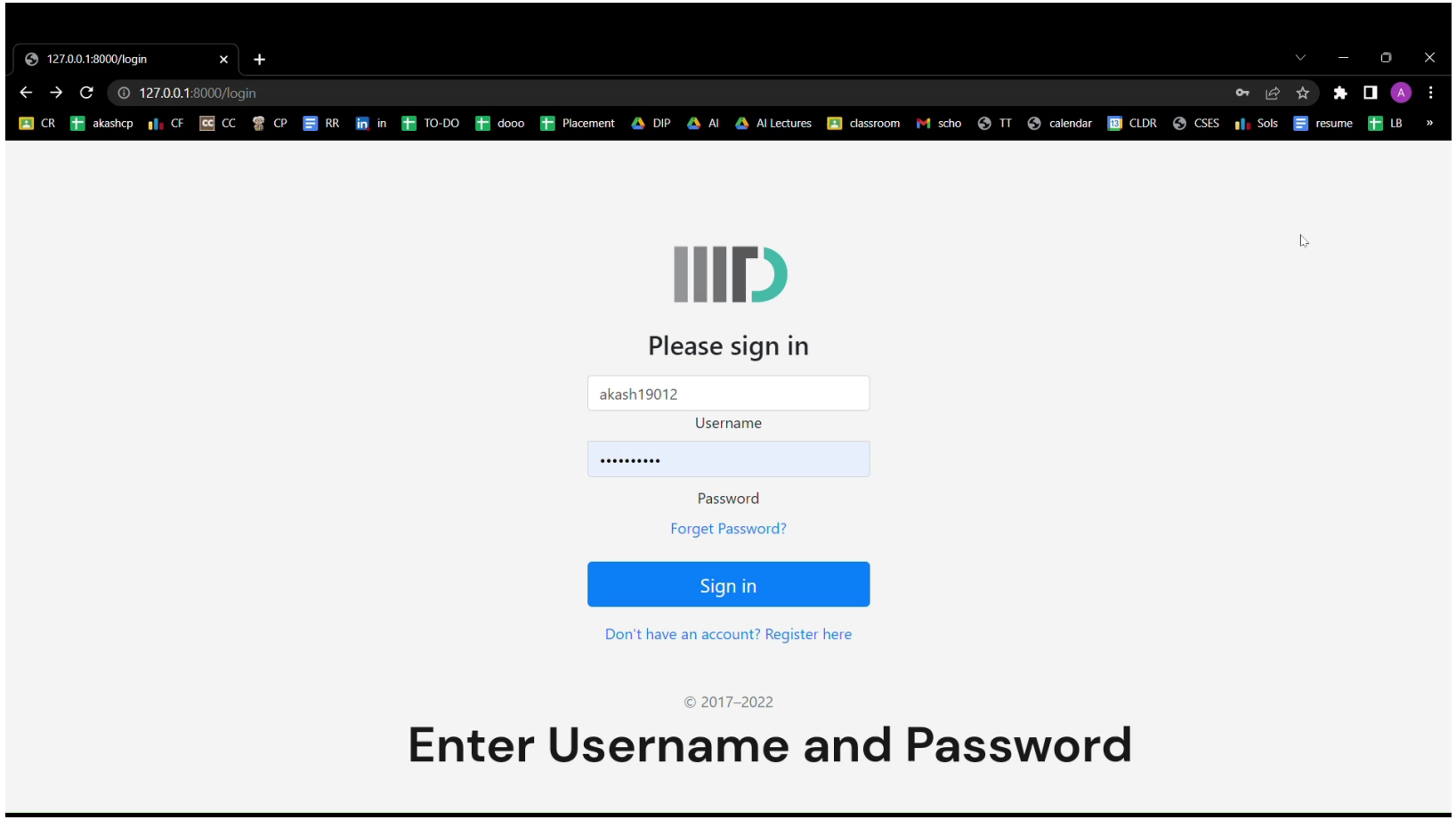
Problem Statement and Objectives

Enable Hardware Based Labs in Remote Environment and Develop Self-paced Learning Modules

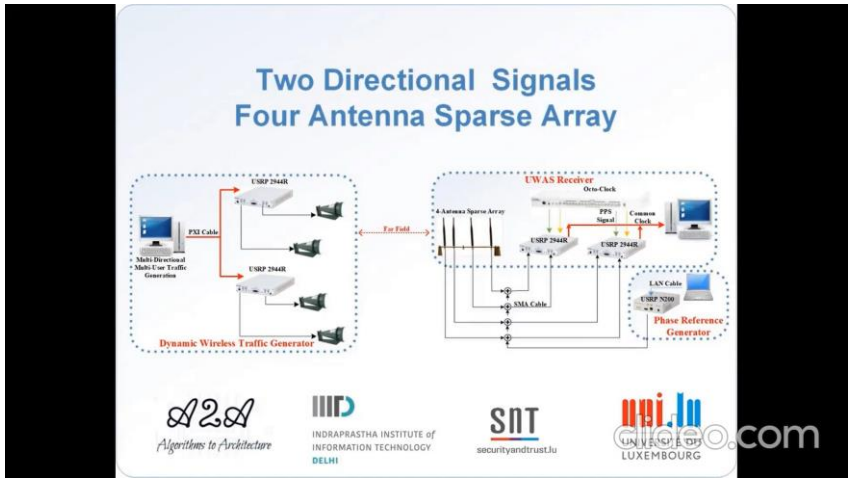
- Develop integrated hardware and software solutions which enables remote access to hardware resources to anyone at anytime from anywhere.
- Offer live-streaming of hardware as well as remote controls of hardware peripheral enabling physical lab experience
- Self-spaced learning module of duration ranging from 2-8 weeks.
- Generalised solutions for different types of hardware to cater domains such as Embedded Systems, Digital System Design, Internet of Things (IoT), Robotics, Mechatronics, AI Accelerators, Edge-AI and many more.

Proposed System

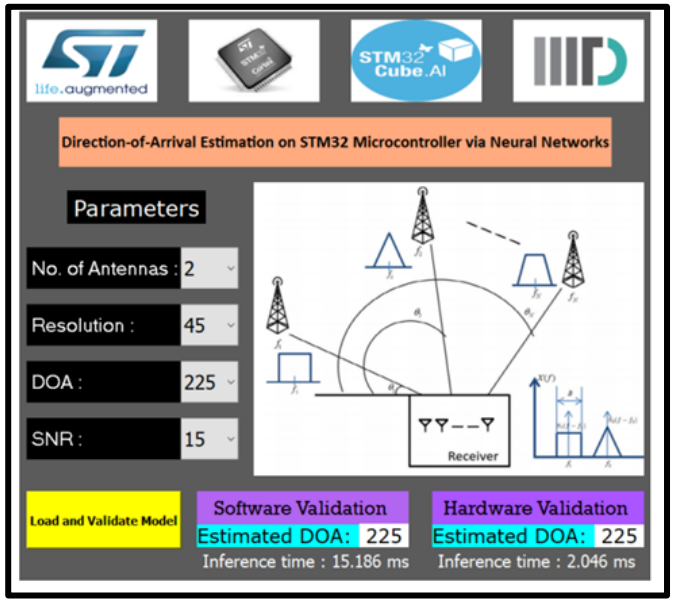
- Deployed since June 2020
- More than 25K bookings
- Supported by DST-Prayas



Algorithms to Architecture Lab

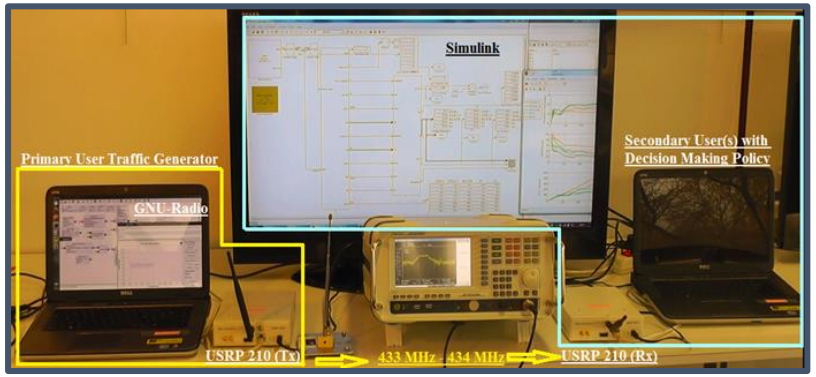


COMSNETS 2022 Best Thesis Award
IIIT Delhi 2022 Best Thesis Award

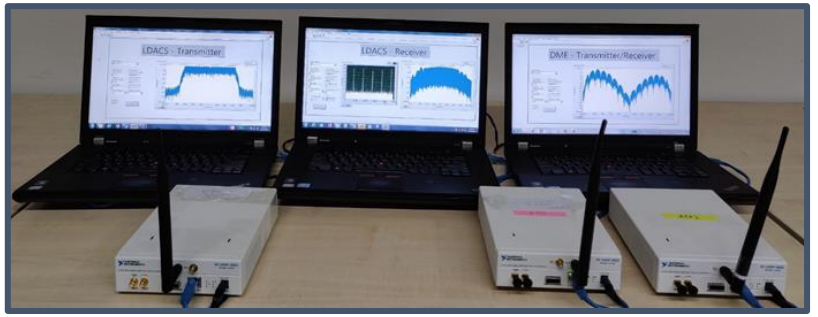


Best Paper Award in AIML Systems 2021

CloudLab: Remote Hardware Access



Distributed Learning in Wireless Networks:
Best Demo Award at CROWNCOM 2016



Air-to-Ground Communication in L Band:
Second Best Paper Award, IEEE DASC 2017

Other Awards: Qualcomm Innovation Fellowship (2023), VLSID 2023 Design Contest Runner-up, Qualcomm Innovation Fellowship (2022), VLSID 2022 Design Contest Winner, 2021 IIITD Research Excellence Award, Second-Best Poster Award in COMSNETS 2019, Young Scientist Paper Award in URSI 2017, National Instruments (NI) Academic Research Grant (2017, 2018)

FPGA: Field Programmable Gate Array

- **Array** of generic logic gates
- **Gates** where logic function can be programmed
- **Programmable** interconnection between gates
- **Field**: System can be reprogrammed in the field (After fabrication)