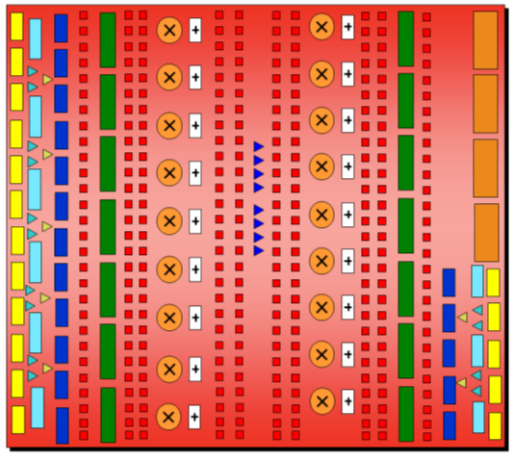
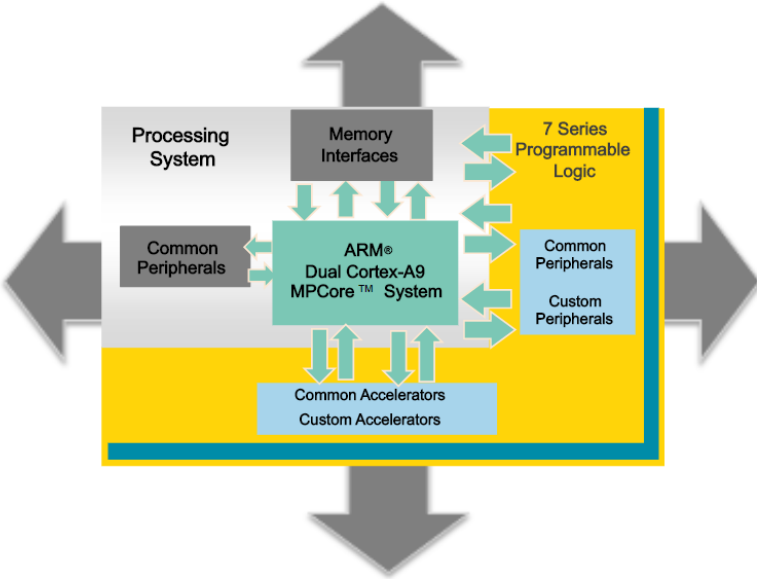
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

A2A
Algorithms to Architecture

ECE 270: Embedded Logic Design

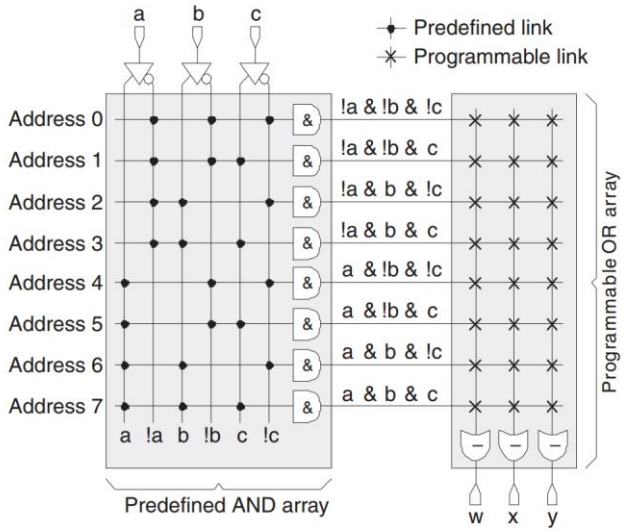


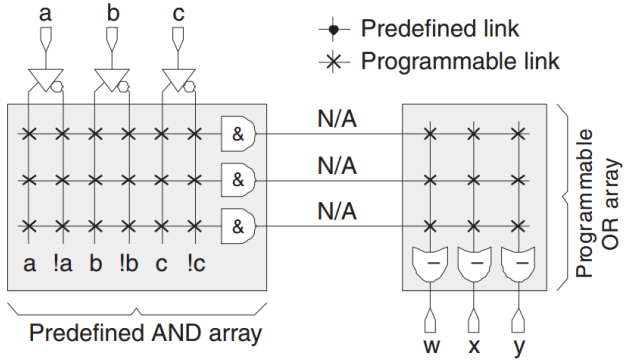


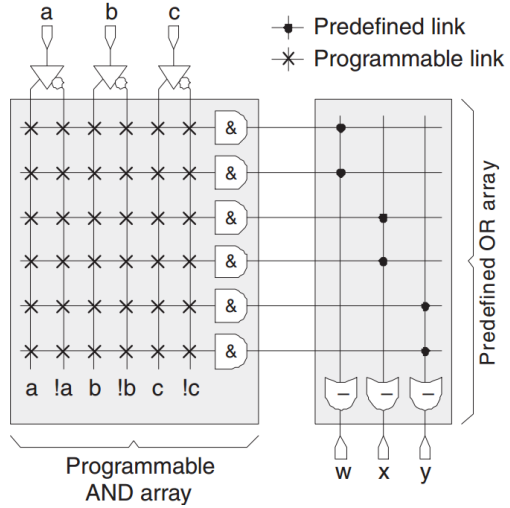
Evolution of Programmable Logic Device (PLD)

PLD

- **Programmable logic devices (PLD)**: Devices whose internal architecture is predetermined by manufacturer but which are created in such a way that they can be configured in the field to perform variety of functions

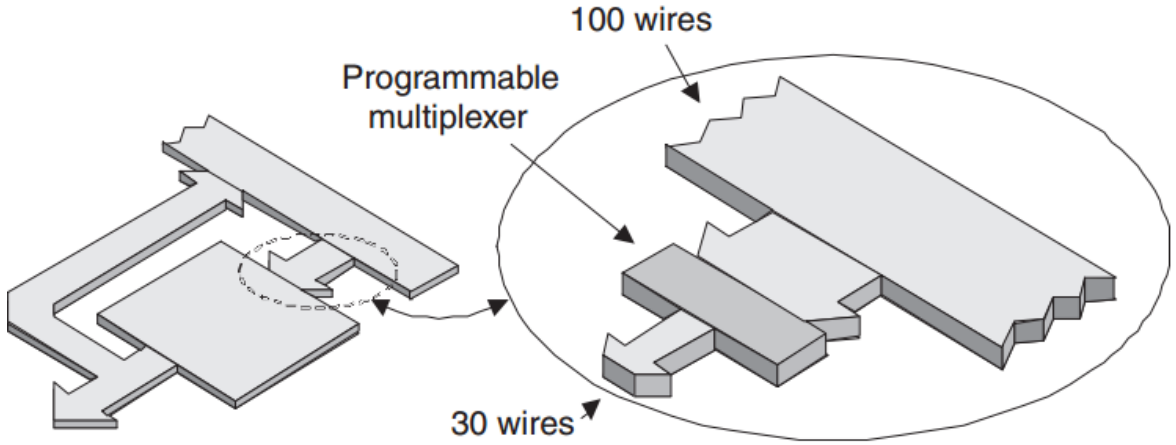


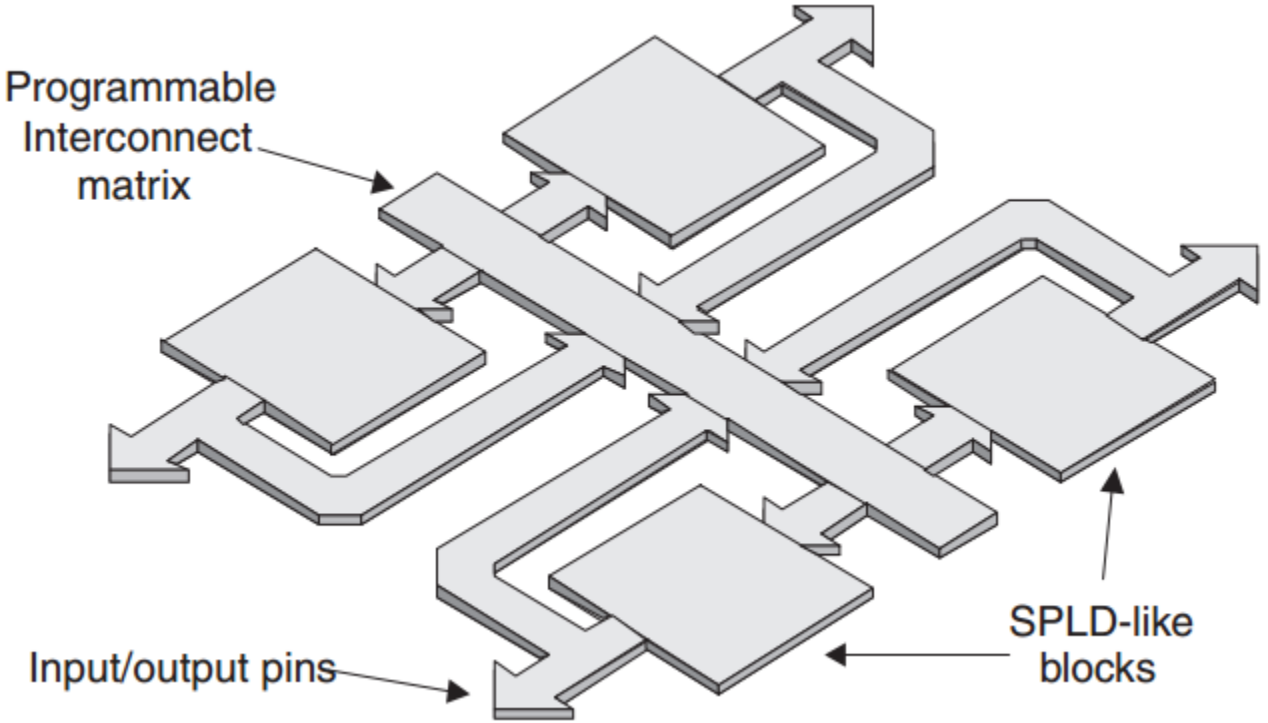




PAL: Complex PLDs

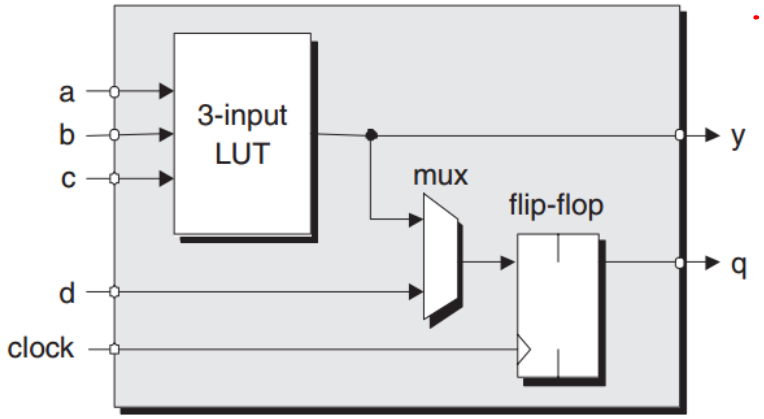
- Novelty: Central interconnect
- In addition to programming SPLD (PAL), connections can also be programmed using programmable interconnect matrix
- This leads to increase in the complexity of software tools

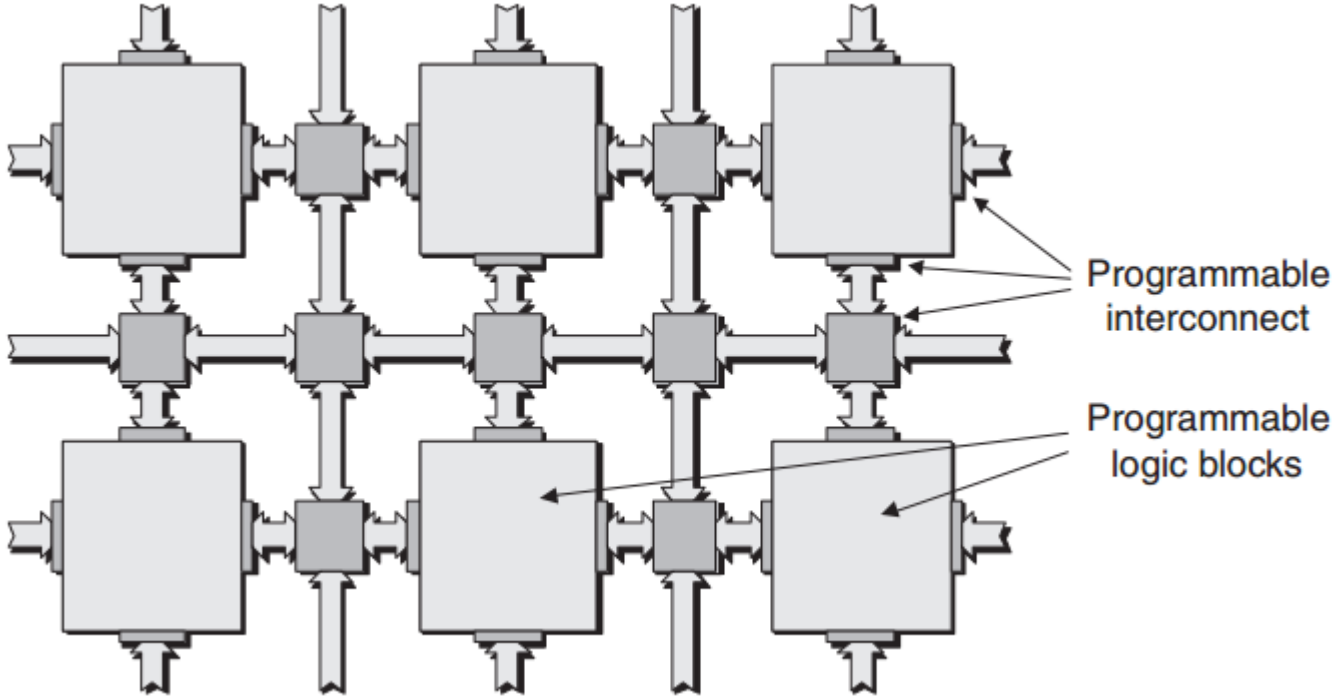




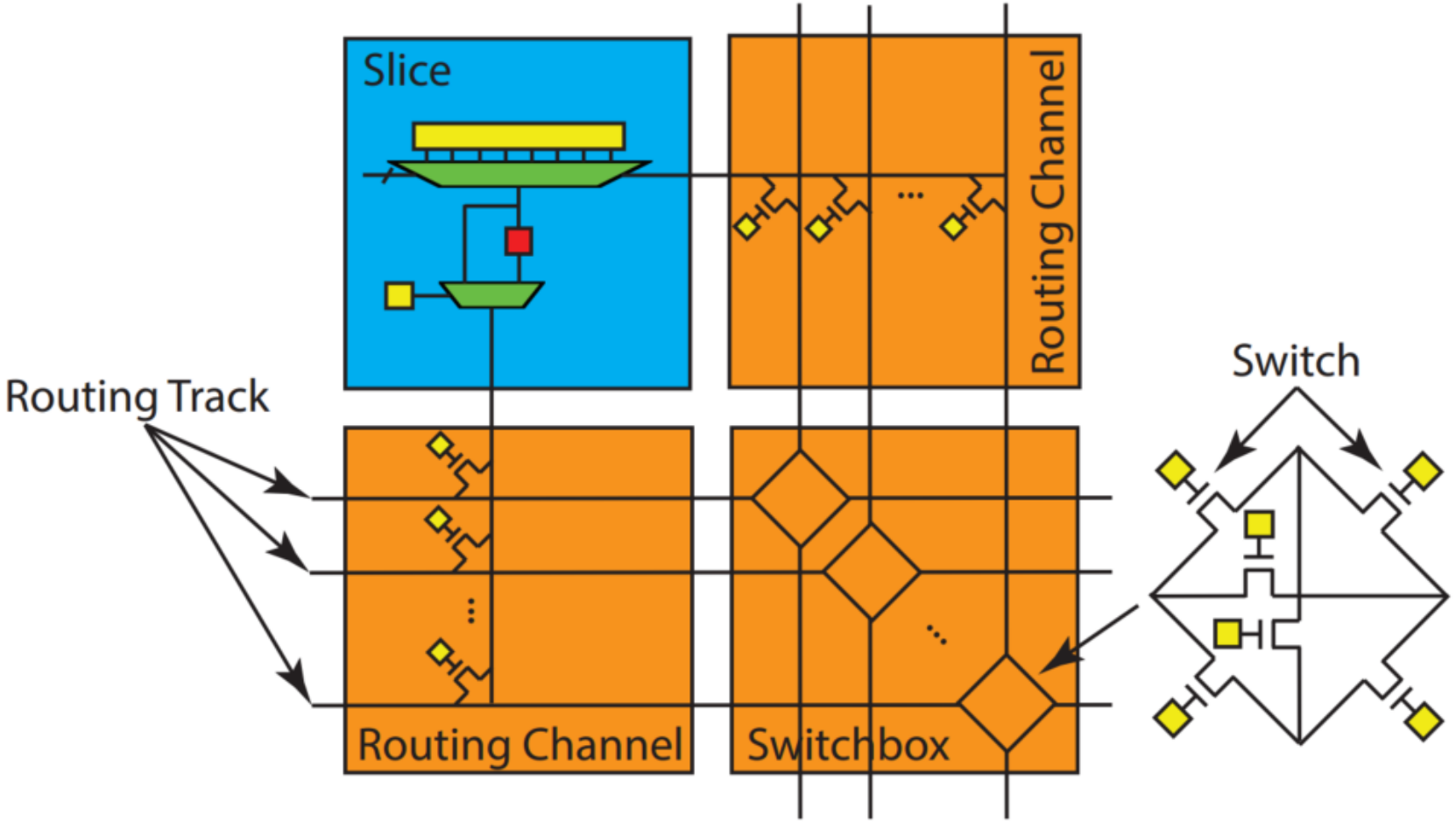
FPGA Architecture

FPGA (1984)

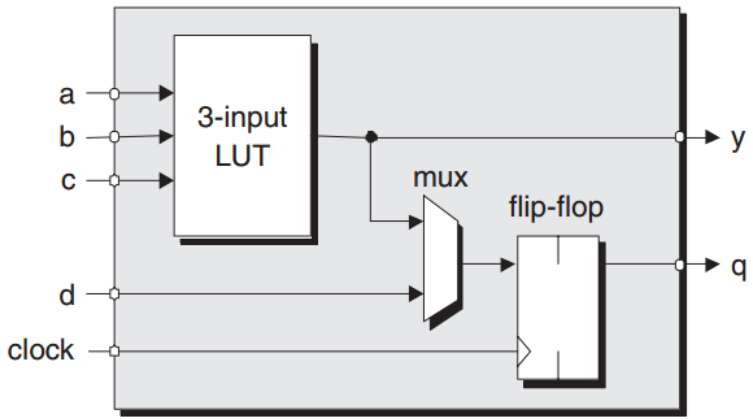

a
b
c
d
clock
3-input
LUT
mux
flip-flop
y
q

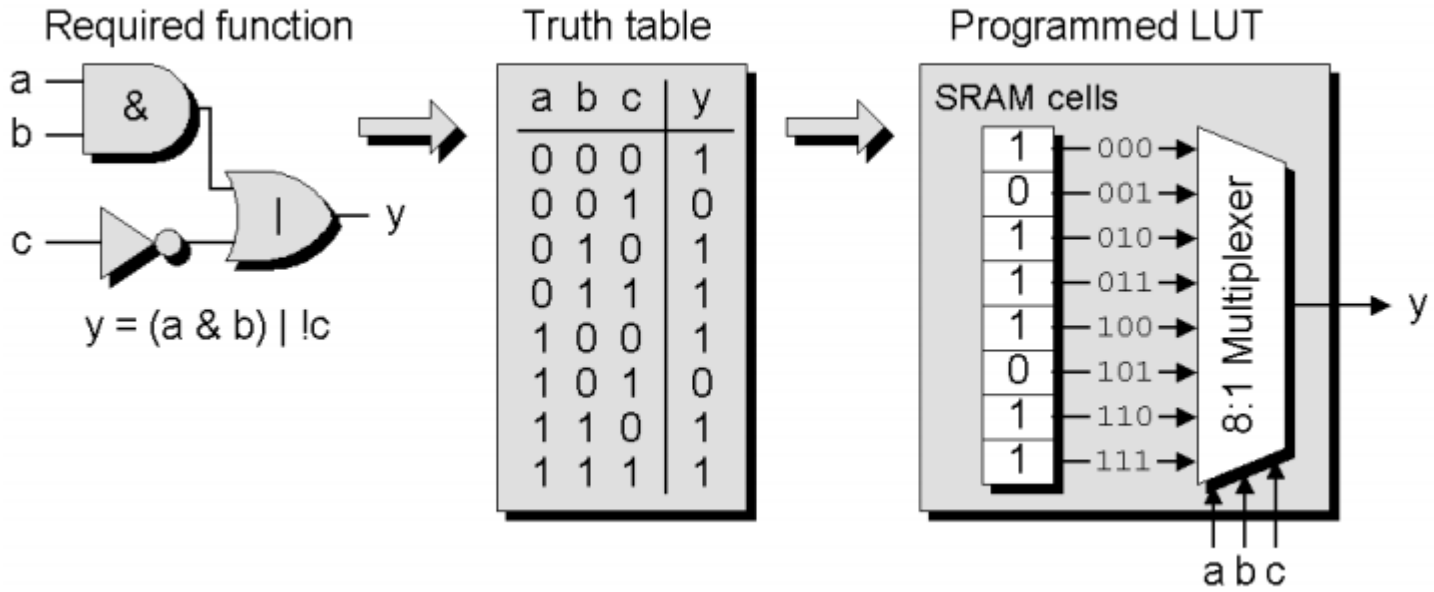

Programmable
interconnect
Programmable
logic blocks

FPGA: Interconnect

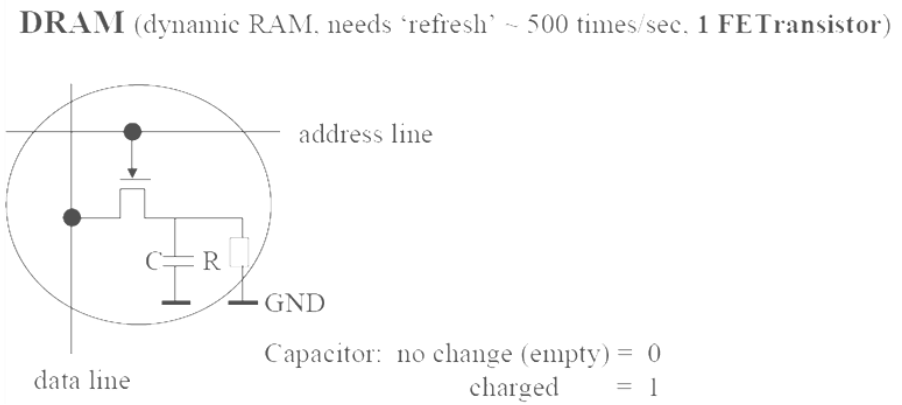


FPGA (1984)


a
b
c
3-input
LUT
mux
flip-flop
y
d
q
clock


Required function
a
b
&
|
c
y
y = (a & b) | !c
Truth table
a b c | y
0 0 0 | 1
0 0 1 | 0
0 1 0 | 1
0 1 1 | 1
1 0 0 | 1
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1
Programmed LUT
SRAM cells
1
0
1
1
1
0
1
1
000
001
010
011
100
101
110
111
8:1 Multiplexer
y
a b c

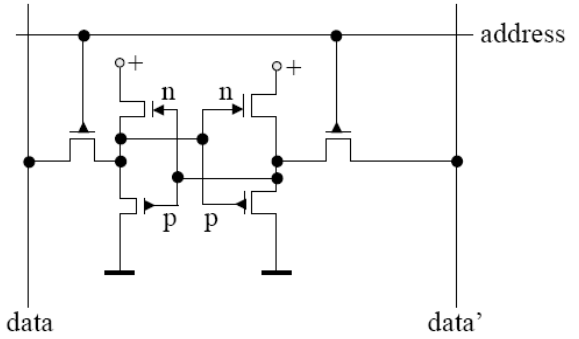
Memory



- DRAM: Dynamic RAM
- A DRAM chip consists of a number of memory cells which can each hold 1-bit of data, stored in a capacitor.
- Due to the fact that capacitors leak electric charge, the state of the bit of information held by each memory cell will eventually fade unless the charge of the capacitor is periodically refreshed by the memory controller.
- The memory controller does this by reading the state of each memory cell and then writing the state back again.
- This is where dynamic RAM gets its name.

Memory

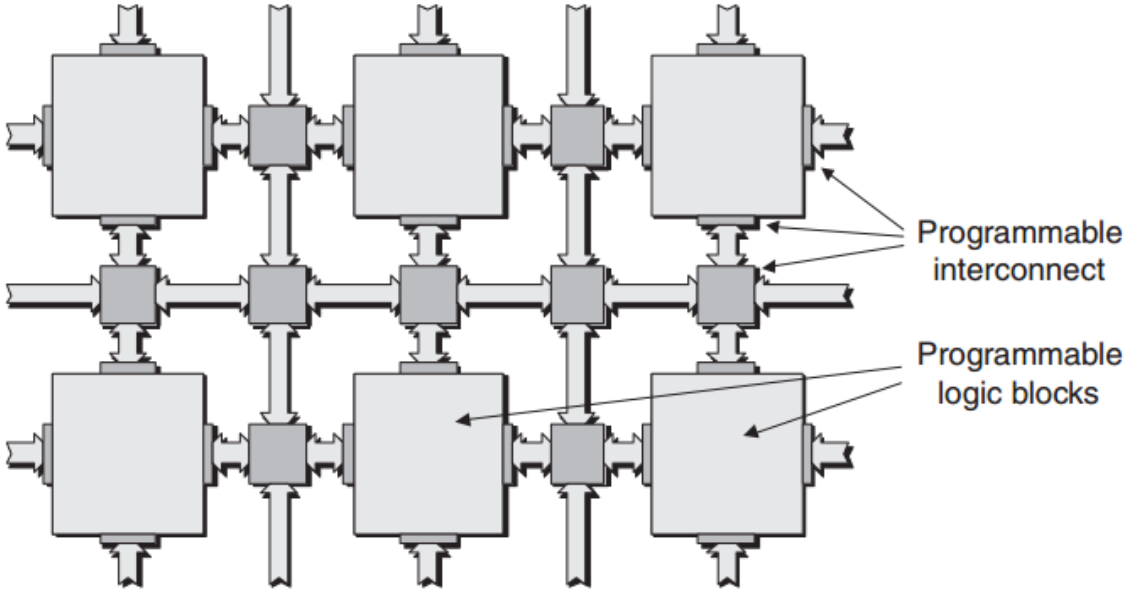
SRAM (static RAM, no 'refresh' required, **6 FETransistors**)
CMOS = complementary metal oxide silicon



- SRAM: Static RAM
- Whereas each bit of memory in DRAM is stored in a capacitor, SRAM uses **latches** to store the data.
- More space than DRAM and expensive
- No refreshing and hence, faster than DRAM
- Used in high-speed, low-capacity memory chips (L1 Cache)

FPGA

- Islands of PLD surrounded by sea of programmable interconnects
- Based on CMOS and SRAM (EPROM or EEPROM in CPLD)
- FPGA Logic Blocks are implemented as LUTs (Look Up Tables) which are RAM based, while CPLDs implement sum-of-product style logic
- SRAM is mature technology and hence, efficient
- Easy and fast to program
- Less delay in data communication from one logic block to another



FPGA

Feature	SRAM	Antifuse	E2PROM / FLASH
Technology node	State-of-the-art	One or more generations behind	One or more generations behind
Reprogrammable	Yes (in system)	No	Yes (in-system or offline)
Reprogramming speed (inc. erasing)	Fast	----	3x slower than SRAM
Volatile (must be programmed on power-up)	Yes	No	No (but can be if required)
Requires external configuration file	Yes	No	No
Good for prototyping	Yes (very good)	No	Yes (reasonable)
Instant-on	No	Yes	Yes
IP Security	Acceptable (especially when using bitstream encryption)	Very Good	Very Good
Size of configuration cell	Large (six transistors)	Very small	Medium-small (two transistors)
Power consumption	Medium	Low	Medium
Rad Hard	No	Yes	Not really

FPGA Architecture

- All 7-series families share the same basic building blocks.
- The mixture and number of these resources varies across families