ECE270: ELD: Quiz 3-4 A (40 Minutes)

Date: October 23, 2023

1. Explain the concept of memory mapped IO.

3 Marks

In SoC, processor can communicate with other components or IOs only when they are memory mapped.

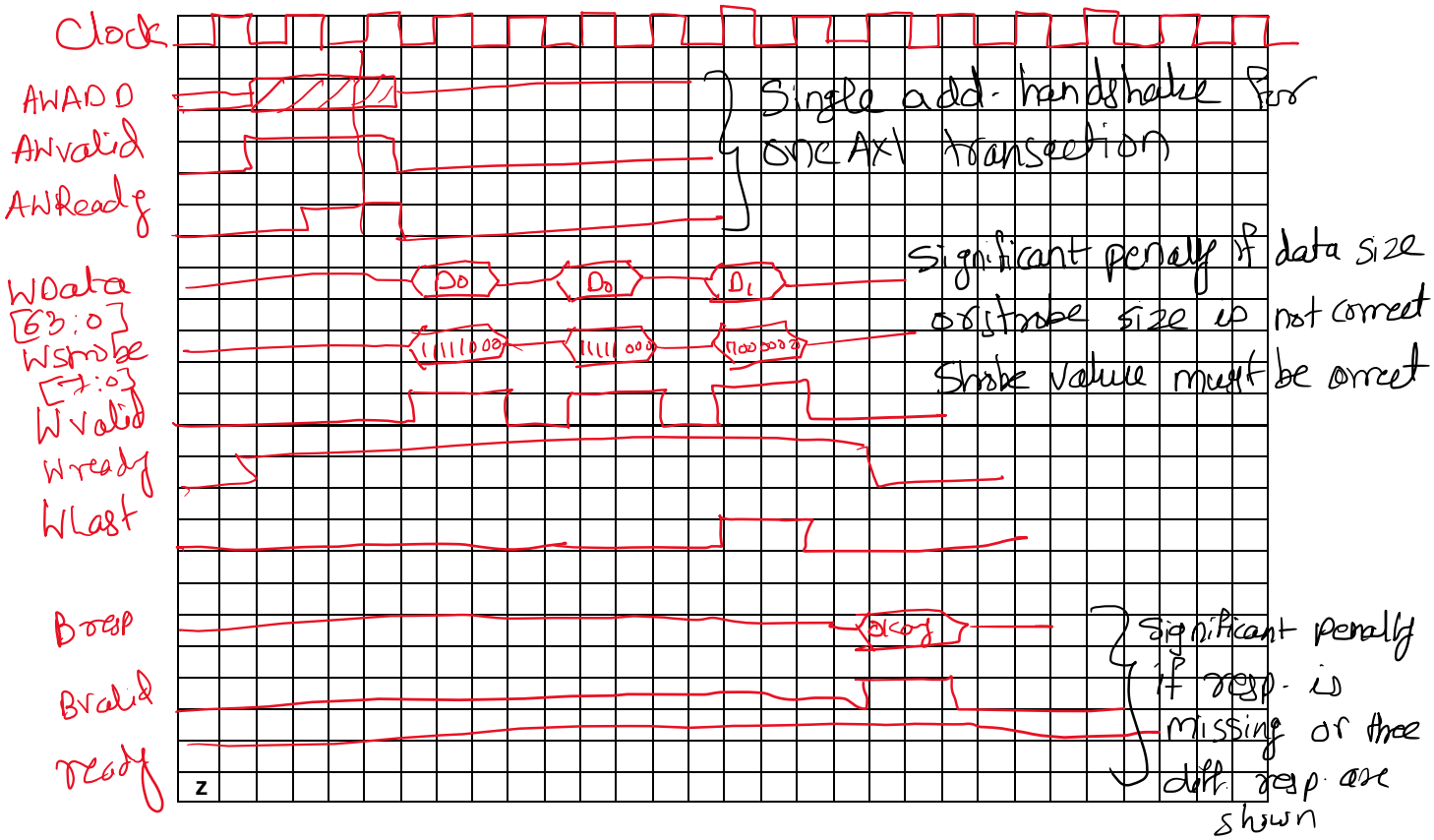
Each of the memory mapped IO has dedicated memory space with unique starting address. Processor use this starting address to read and write the data with IOs using any of the AMBA protocol.

The number of memory mapped IOs depend on the address space of the processor.

AXI Memory Mapped and AXI Lite are based on the memory mapped IOs.

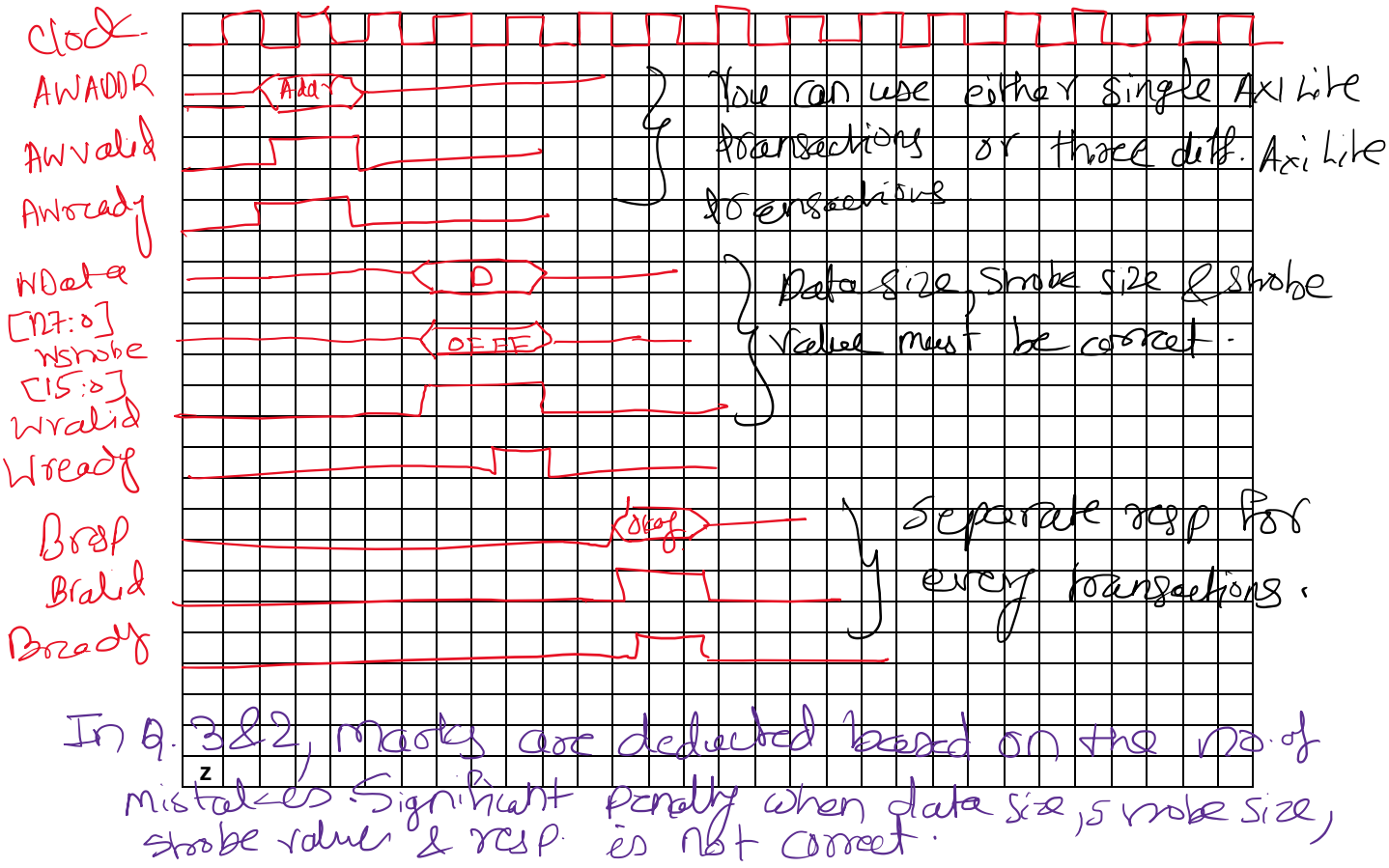
2. Draw the timing diagram explaining write transaction on the AXI memory mapped interface. One transaction consists of X number of transfers and the size of each transfer is Y bytes. Assume Y=5 i.e. 5 bytes must be transmitted in a single transfer. If master needs to transfer total 12 bytes of data using single transaction, identify X and using appropriate signals, explain the complete transaction via suitable timing diagram.

10 Marks



3. Modify the timing diagram in the above question to AXI Lite.

5 Marks



4. Explain the difference between assertion of ready and valid signals.

2 Marks

Ready signal is controlled by destination and valid signal is controlled by source.

Source asserts the valid signal when information is on information bus.

Destination asserts the ready signal when it is ready to accept the data.

Handshake happens when ready and valid is high on the positive edge of the clock.

Ready can be asserted without waiting for valid signal or after the valid signal is asserted. Ready can be deasserted if valid is not asserted. Ready cannot be deasserted if valid is already asserted.

Source should not wait for ready signal before asserting the valid signal for transfer of information.

5. Explain in detail the meaning and significance of the following signals of AXI protocol.

10 Marks

ARBURST[1:0] AWBURST[1:0]	Burst type
b00	FIXED
b01	INCR
b10	WRAP
b11	Reserved

AxSIZE[2:0]	Bytes in transfer
0b000	1
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	64
0b111	128

AxSize:

This signal is used in AXI Memory Mapped protocol to indicate the size of each transfer in the burst.

The number of bytes that can be transferred in a single transfer of the burst should be power of two.

AxSize also determines the size of the strobe signal.

AxSize is fixed for a given burst.

By controlling AxSize and strobe signal, source can control or inform the destination about the number of valid bytes in a given transfer.

4 Marks

AxBurst:

This signal determines the type of burst in the AXI Memory Mapped Protocol. Using this signal, source informs the destination about how to read or write the data to be received in the burst consisting of more than one transfers.

In FIXED mode, the data received from various transfers in a burst is stored at the same address. This means data received in first transfer will be overwritten with the data received in the second transfer in the burst. One application is FIFO in memory mapped IO mode where only the address of the FIFO is needed since the FIFO internally calculates the address of subsequent data received in a burst.

In INCR mode, the data received from various transfers in a burst is stored at the different address. This means data received in the first transfer will be

stored at the initial address. Thereafter, address is incremented for every new received data.

In WRAP mode, the data received from various transfers in a burst is stored at the different address. This is similar to INCR mode except that the address is wrapped back to initial address once it reaches certain predefined threshold.

ECE270: ELD: Quiz 3-4 B (40 Minutes)

Date: October 23, 2023

1. Explain the difference between read and write transaction.

2 Marks

Read transaction allows transfer of data from slave to master while write transaction allows transfer of data from master to slave.

Read transaction consists of two AXI channels, Read Address and Read Data. Write transaction consists of three AXI channels, Write Address, Write Data and Write Response.

2. Draw the timing diagram explaining write transaction on the AXI memory mapped interface. One transaction consists of X number of transfers and the size of each transfer is Y bytes. Assume Y=3 i.e. 3 bytes must be transmitted in a single transfer. If master needs to transfer total 5 bytes of data using single transaction, identify X and using appropriate signals, explain the complete transaction via suitable timing diagram.

10 Marks

Refer to Section A Solution. Here, the burst consists of 2 transfers instead of 3. Size of WDATA is [31:0] and size of strobe is [3:0].

3. Modify the timing diagram in the above question to AXI Lite.

5 Marks

Refer to Section A Solution.

4. Explain the concept of memory mapped IO.

3 Marks

Refer to Section A Solution.

5. Explain in detail the meaning and significance of the following signals of AXI protocol.

10 Marks

ARBURST[1:0] AWBURST[1:0]	Burst type
b00	FIXED
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AxSIZE[2:0]	Bytes in transfer
0b000	1
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	64
0b111	128

Refer to Section A Solution.