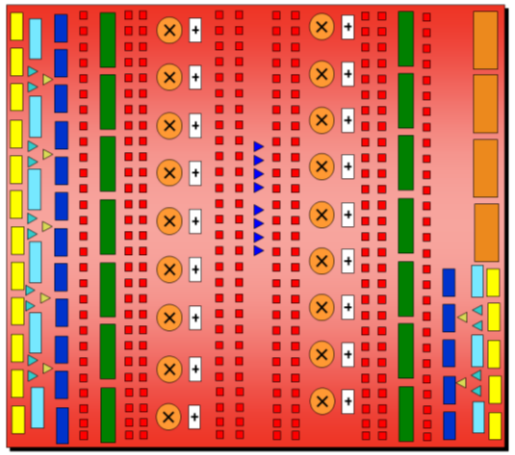
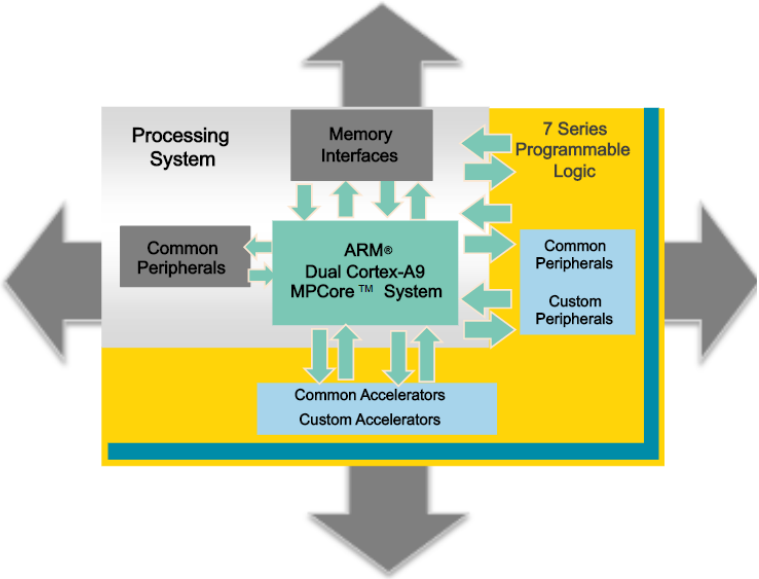
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

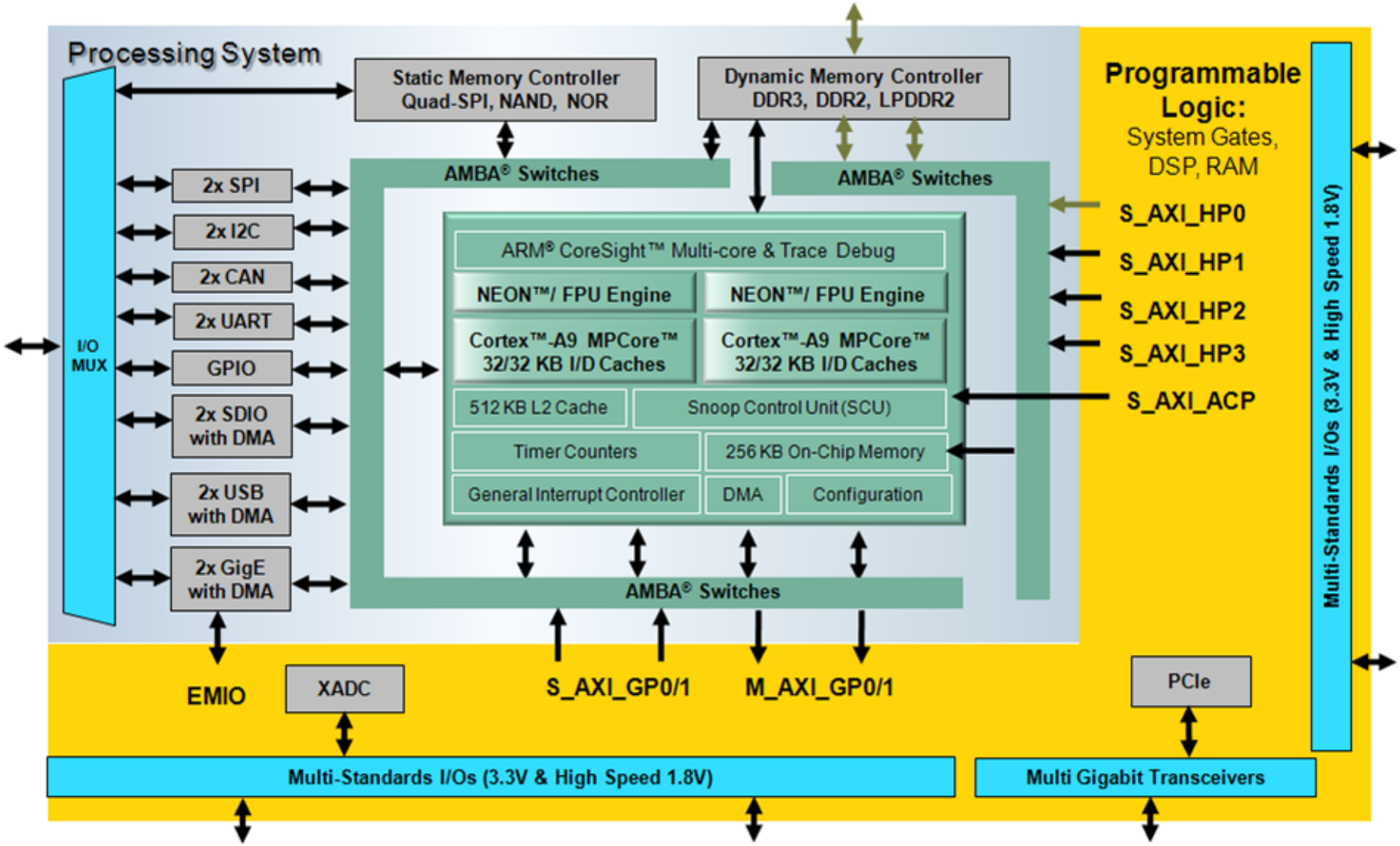
A2A
Algorithms to Architecture

ECE 270: Embedded Logic Design



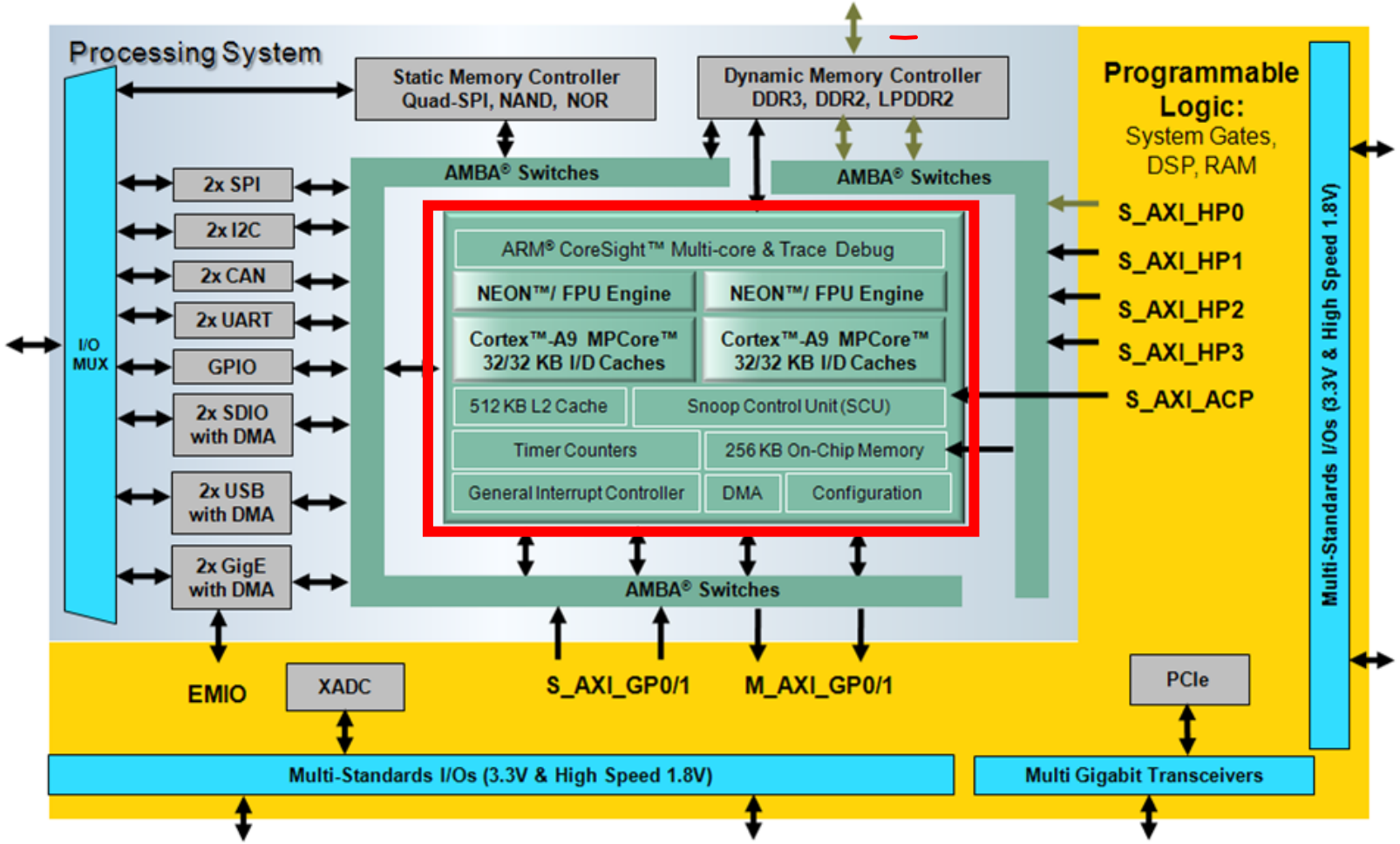


Zynq Architecture: PS and PL



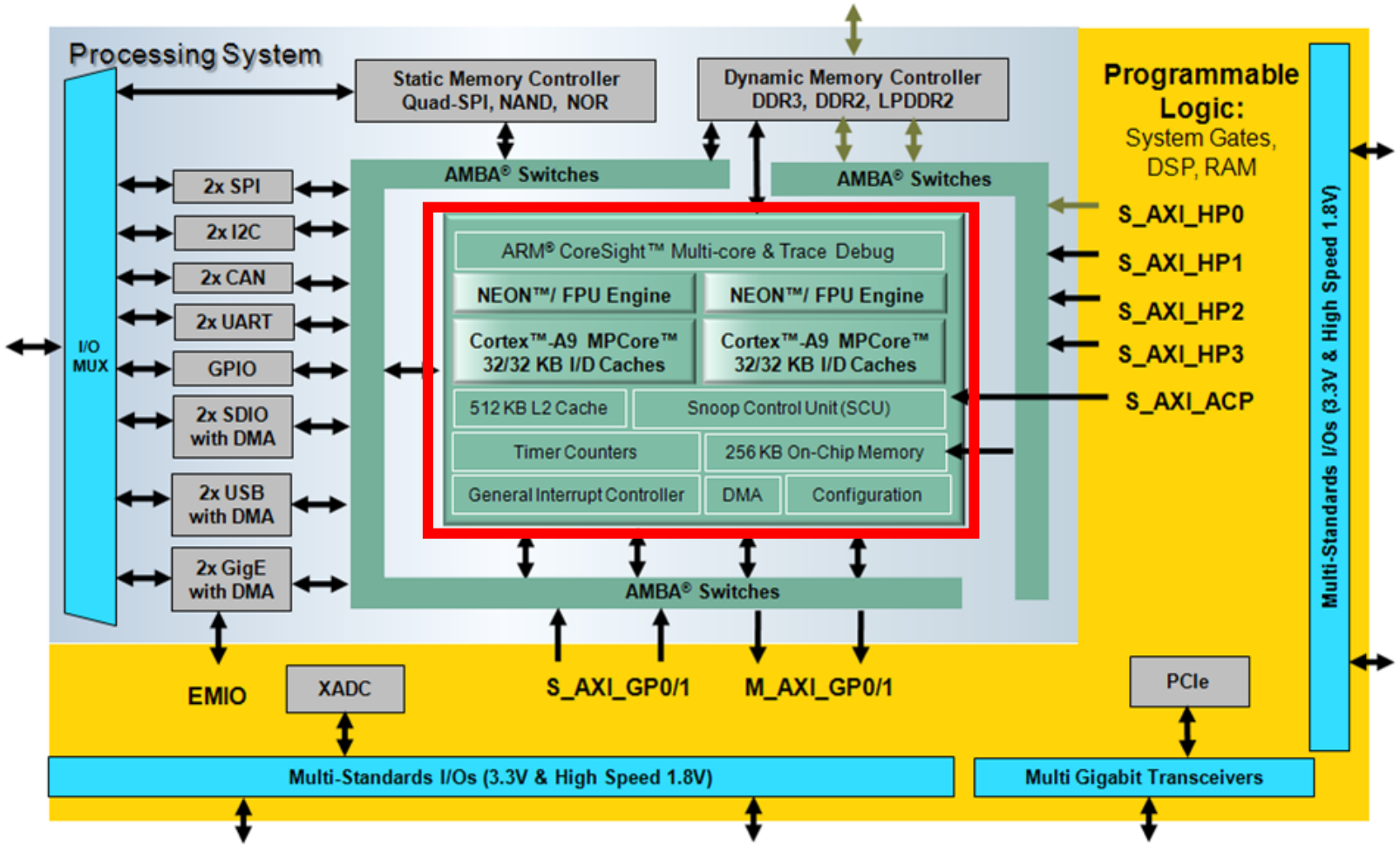
Zynq Architecture: PS and PL

- ARM: Advanced RISC Machine
- AMBA: Advanced Microcontroller Bus Architecture (AMBA)



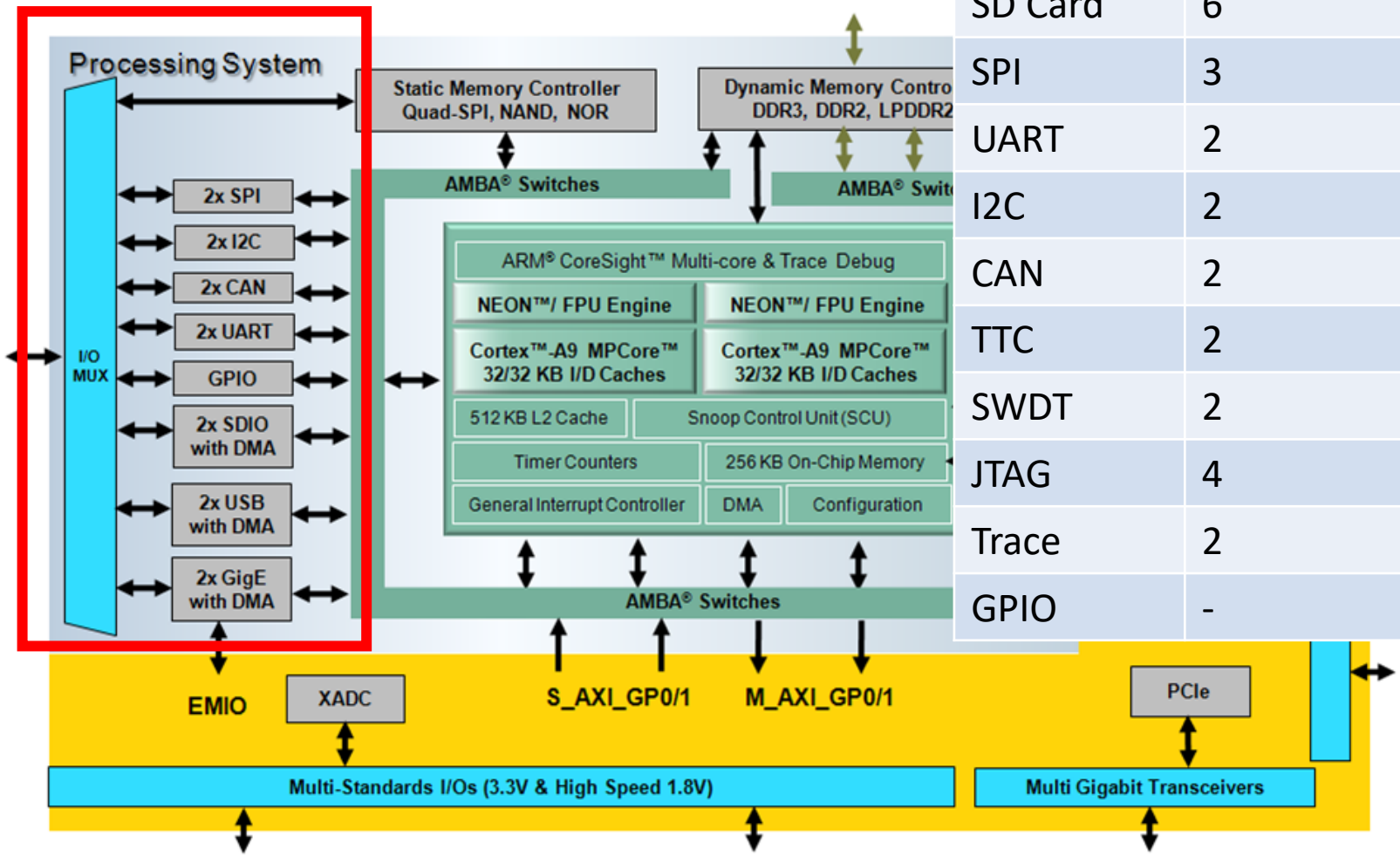
Zynq Architecture: PS and PL

- ARM: Advanced RISC Machine
- AMBA: Advanced Microcontroller Bus Architecture (AMBA)
- 130 PS IO out of which 76 for DDR and 54 MIO for processor



Zynq Architecture: PS and PL

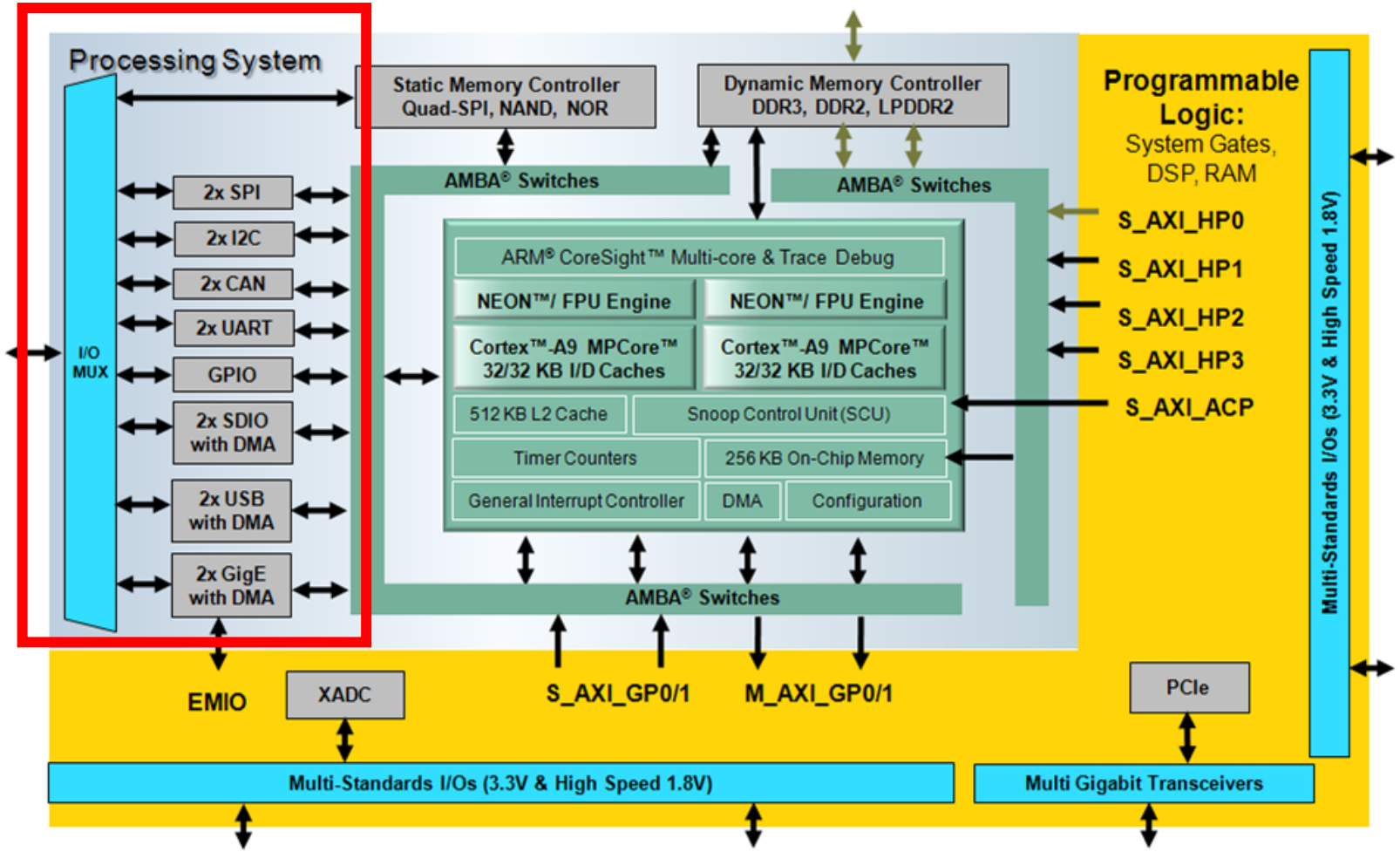
- Communication between the PS and external interfaces is achieved primarily via the Multiplexed Input/Output (MIO)
- MIO provides 54 pins of flexible connectivity, meaning that the mapping between peripherals and pins can be defined as required.

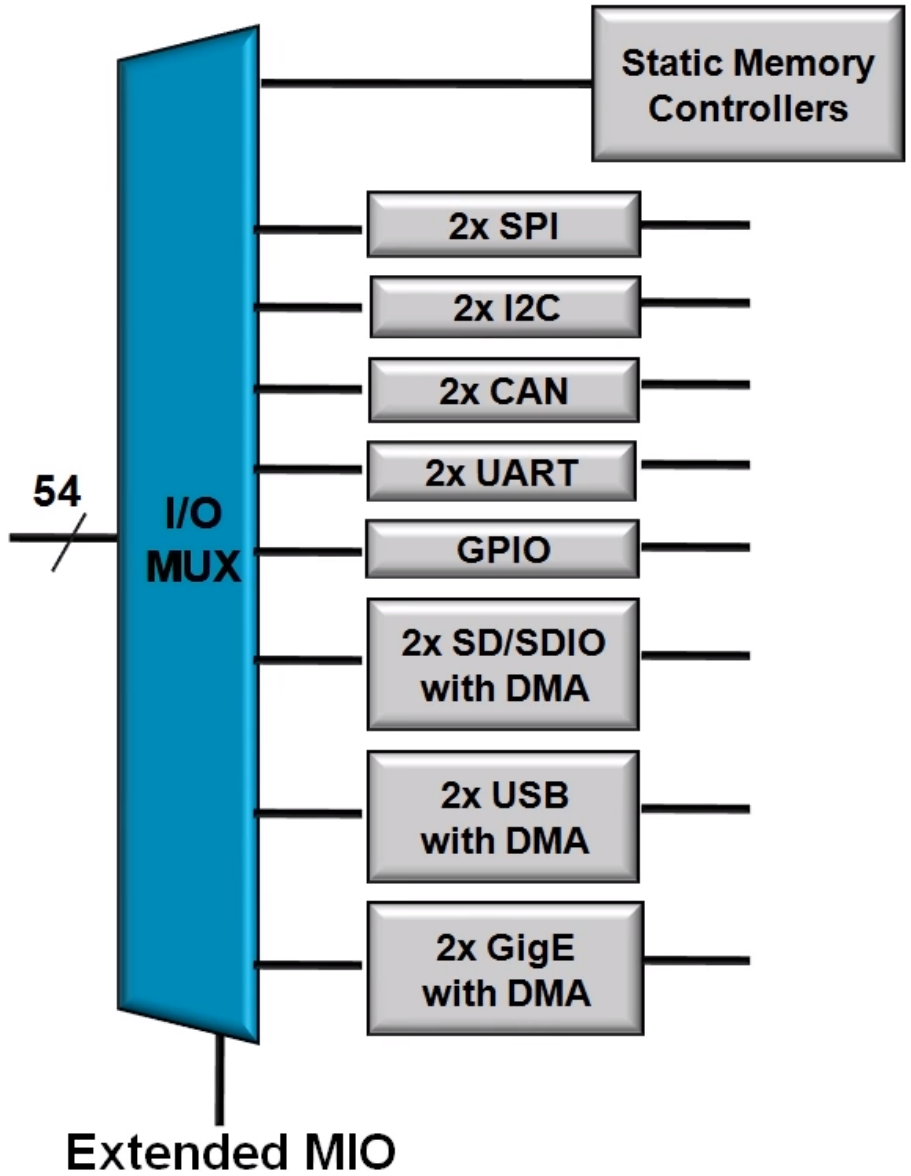


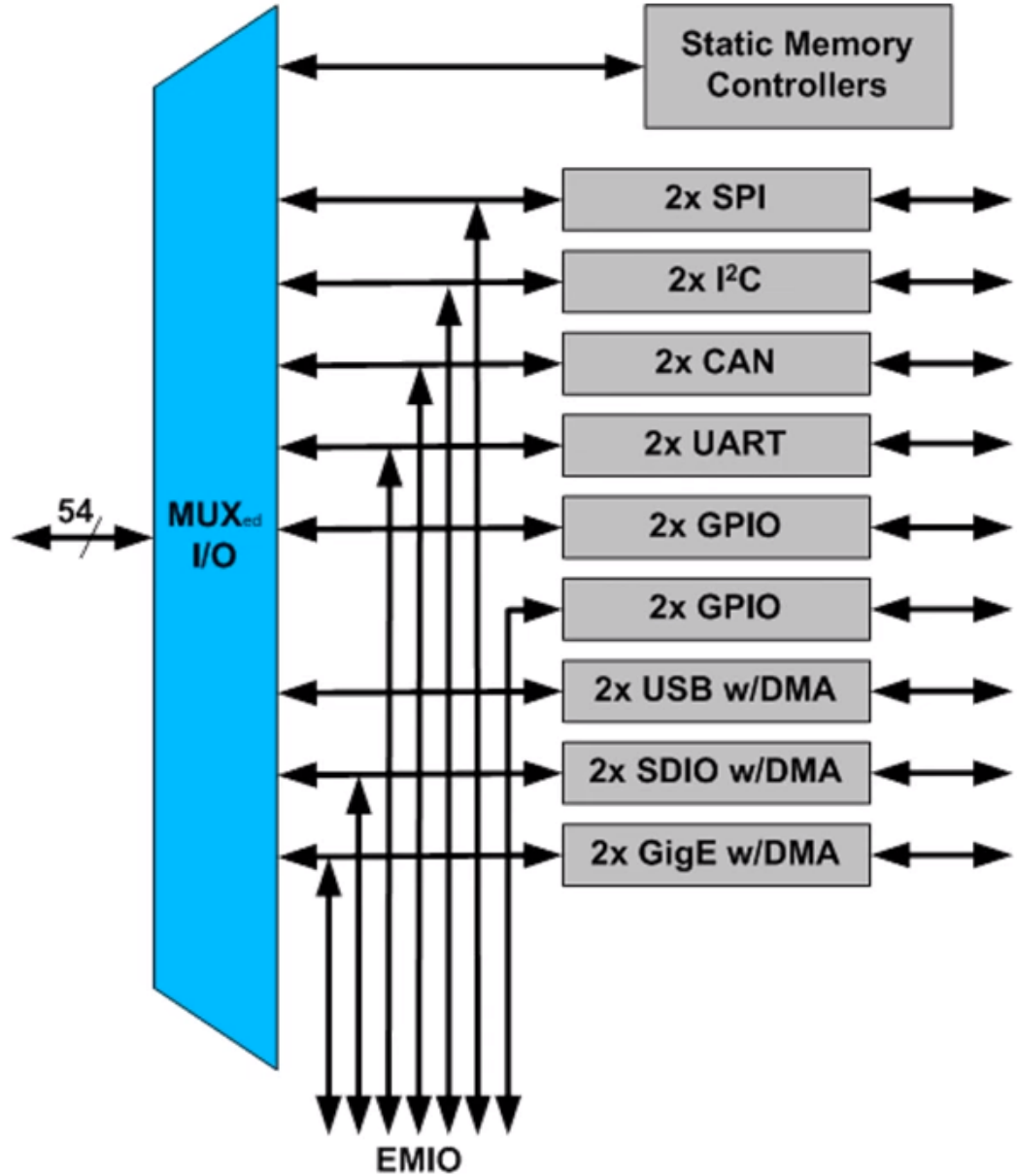
Peripheral	# of Pins
Flash	24
Ethernet	12
USB	12
SD Card	6
SPI	3
UART	2
I2C	2
CAN	2
TTC	2
SWDT	2
JTAG	4
Trace	2
GPIO	-

Zynq Architecture: PS and PL

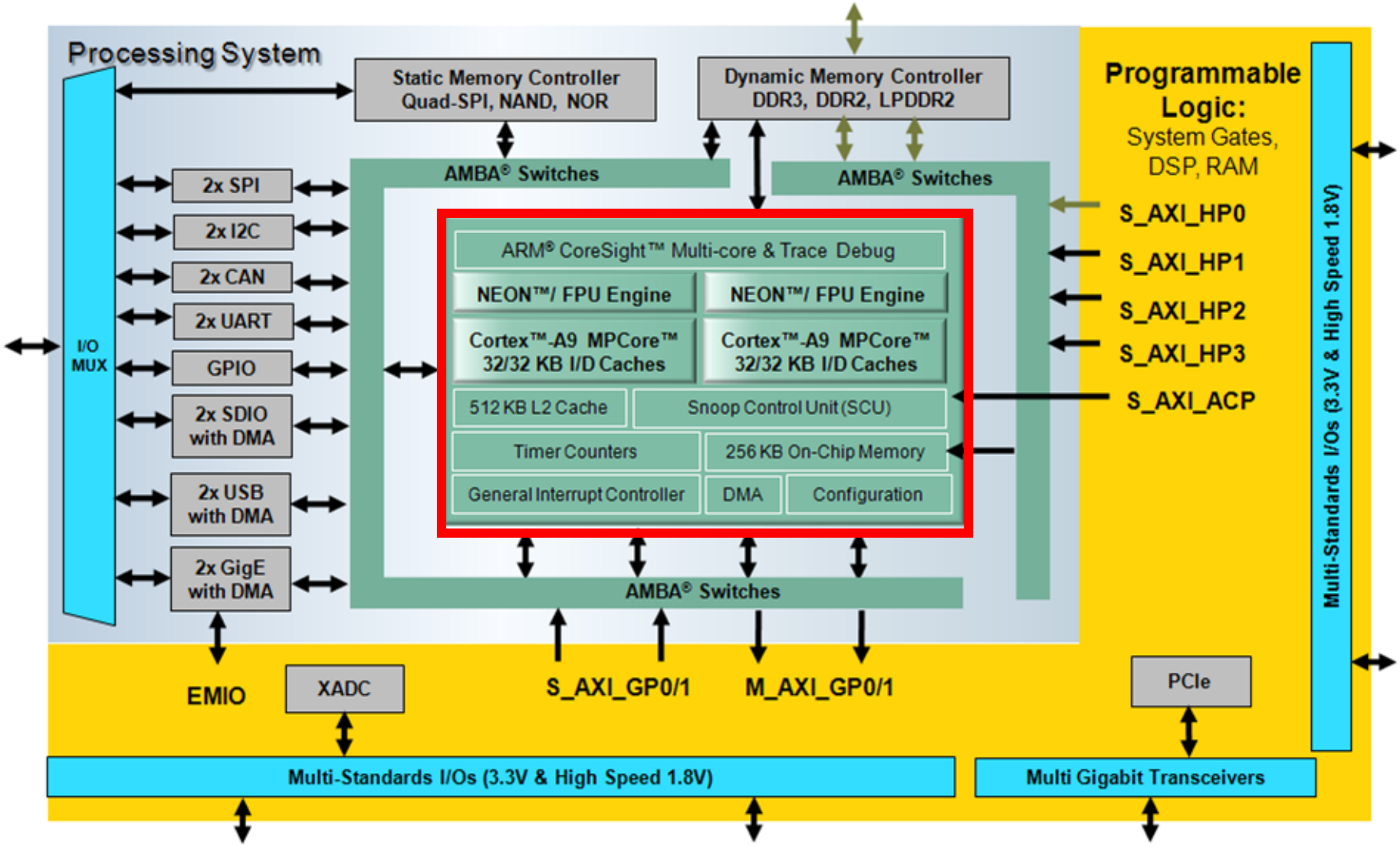
- Certain connections can also be made via the Extended MIO (EMIO), which is not a direct path from the PS to external connections, but instead passes through and shares the I/O resources of the PL.
- 192 EMIOs

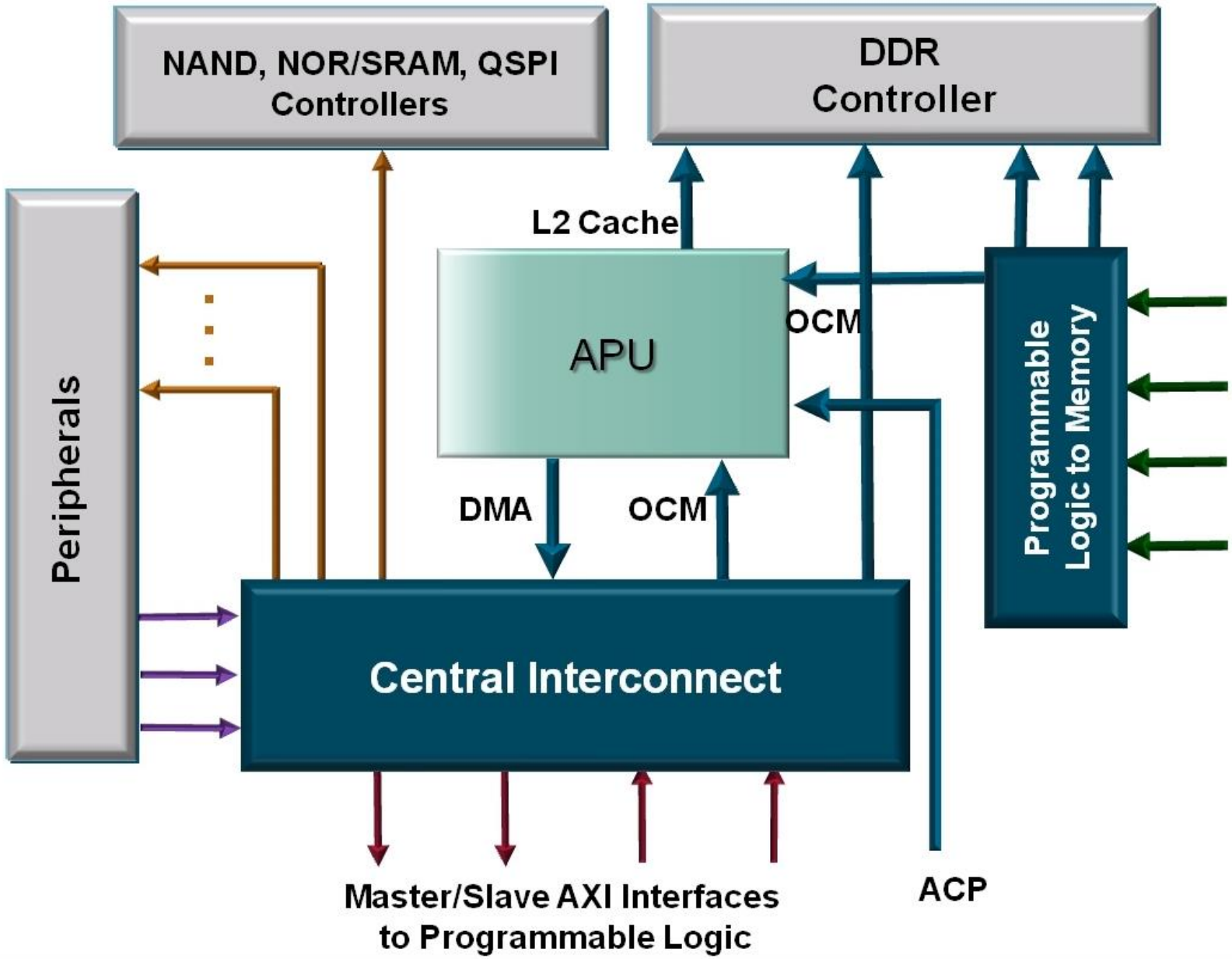


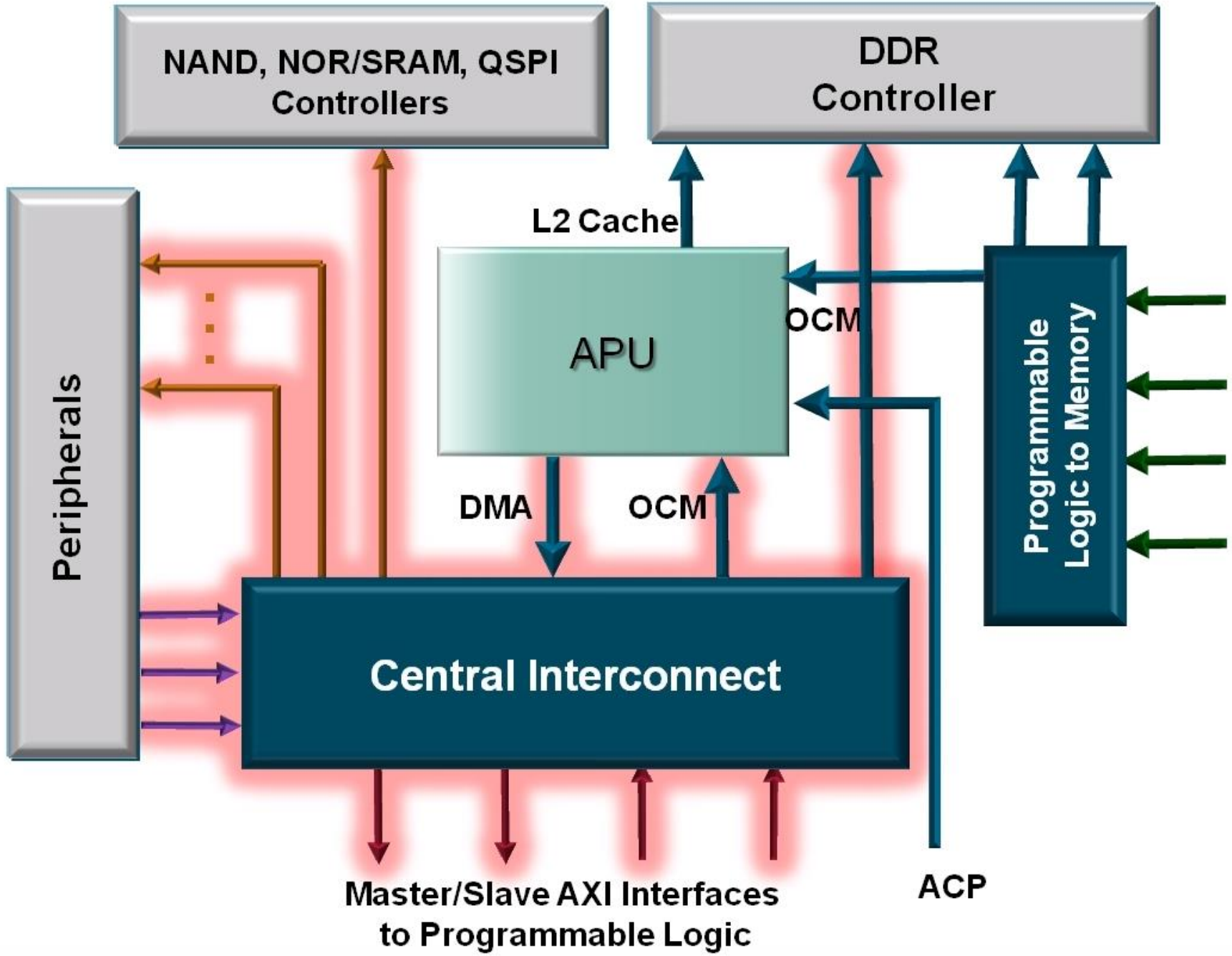

Static Memory Controllers
2x SPI
2x I2C
2x CAN
2x UART
GPIO
2x SD/SDIO with DMA
2x USB with DMA
2x GigE with DMA
54
I/O MUX
Extended MIO


Static Memory Controllers
2x SPI
2x I²C
2x CAN
2x UART
2x GPIO
2x GPIO
2x USB w/DMA
2x SDIO w/DMA
2x GigE w/DMA
54
MUXed I/O
EMIO

Zynq Architecture: PS and PL




NAND, NOR/SRAM, QSPI Controllers
DDR Controller
L2 Cache
APU
OCM
Programmable Logic to Memory
Peripherals
DMA
OCM
Central Interconnect
Master/Slave AXI Interfaces to Programmable Logic
ACP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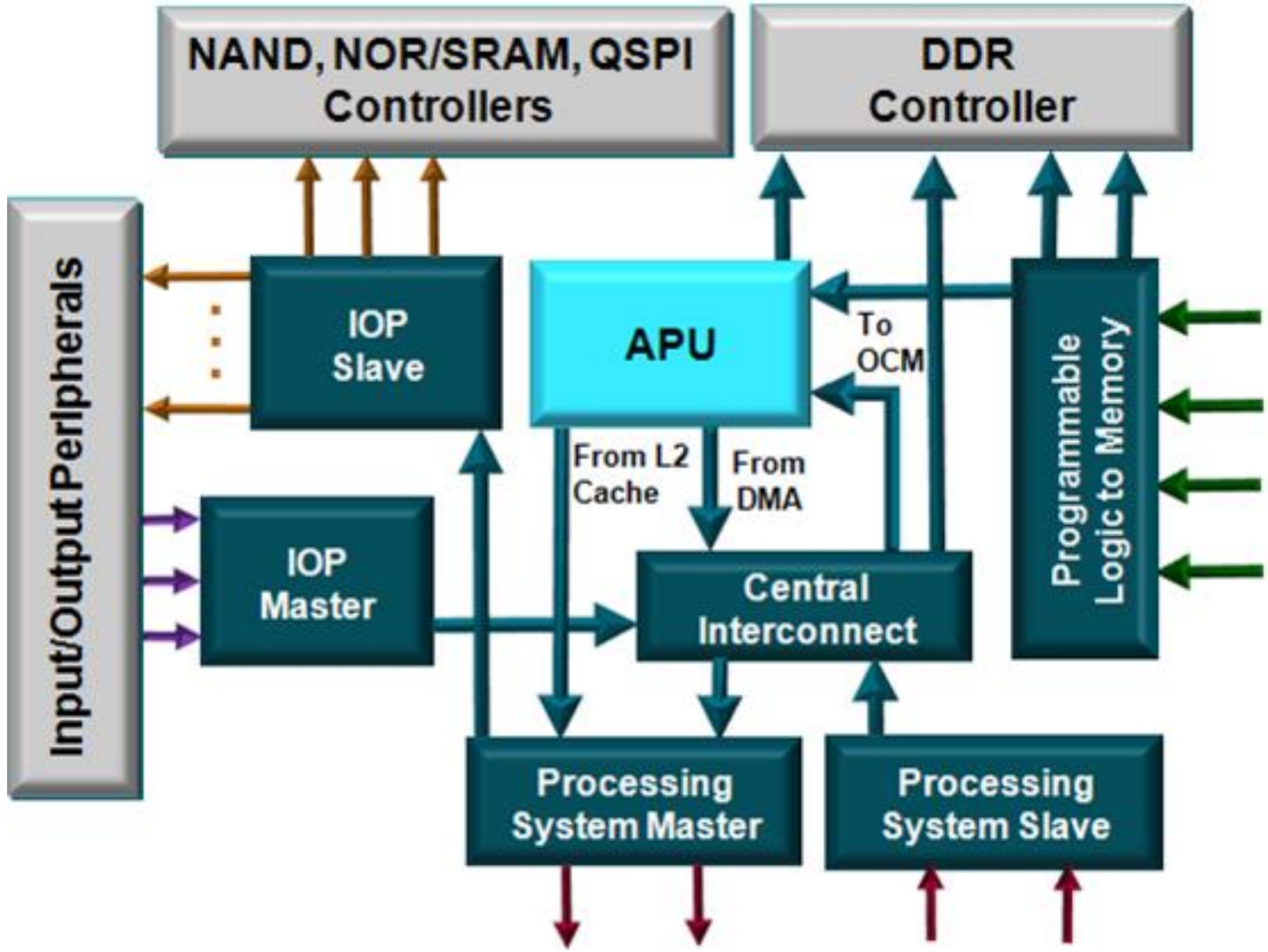
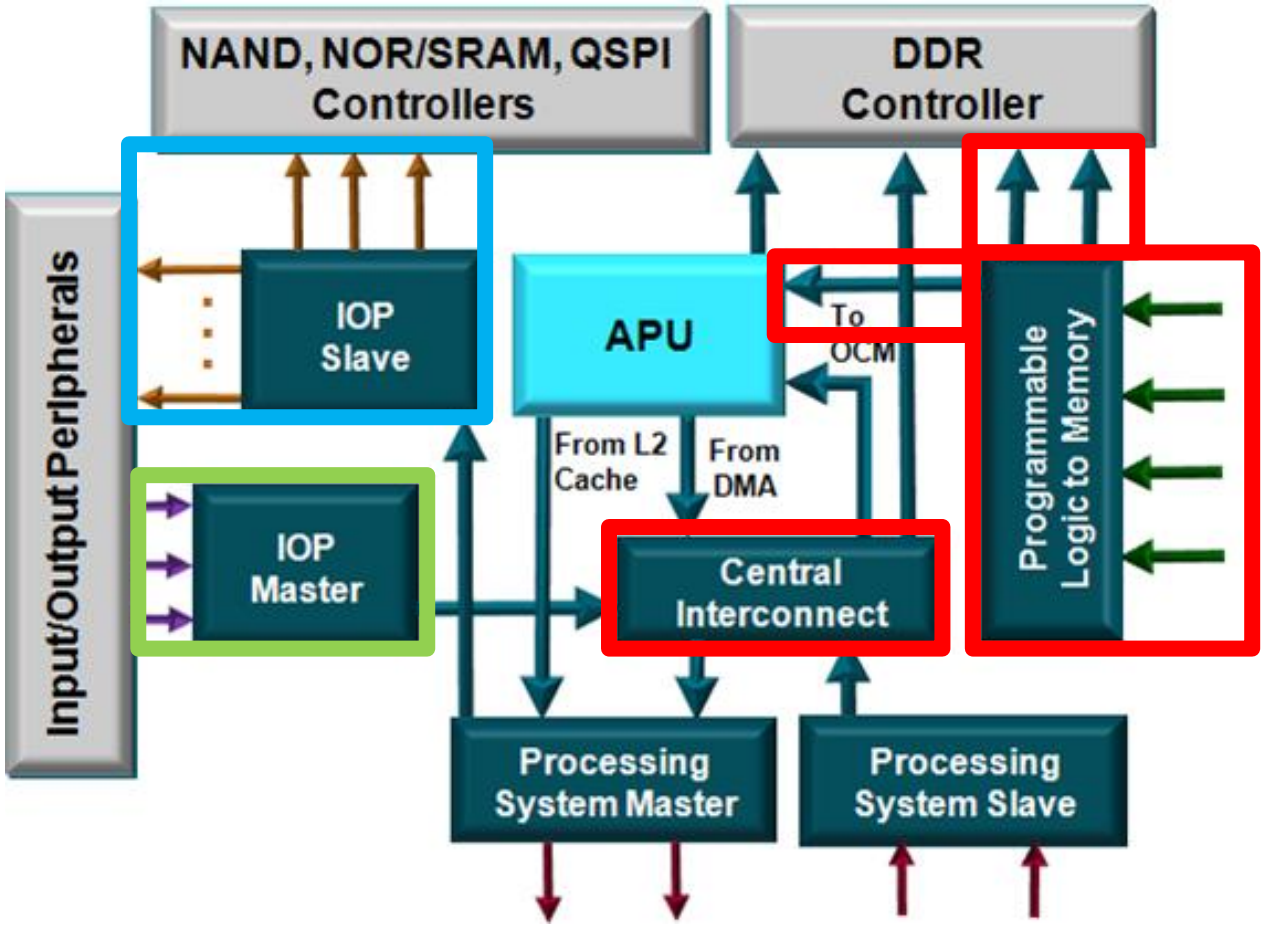

NAND, NOR/SRAM, QSPI Controllers
DDR Controller
Input/Output Perlpherals
IOP Slave
APU
To OCM
Programmable Logic to Memory
From L2 Cache
From DMA
IOP Master
Central Interconnect
Processing System Master
Processing System Slave

Processing System Interconnect

- Programmable logic to memory
  - Two ports to DDR
  - One port to OCM
- Central interconnect
  - Enables other interconnects to communicate
- Peripheral master
  - USB, GigE, SDIO connects to DDR and PL via the central interconnect
- Peripheral slave
  - CPU/APU, DMA, and PL access to IOP peripherals



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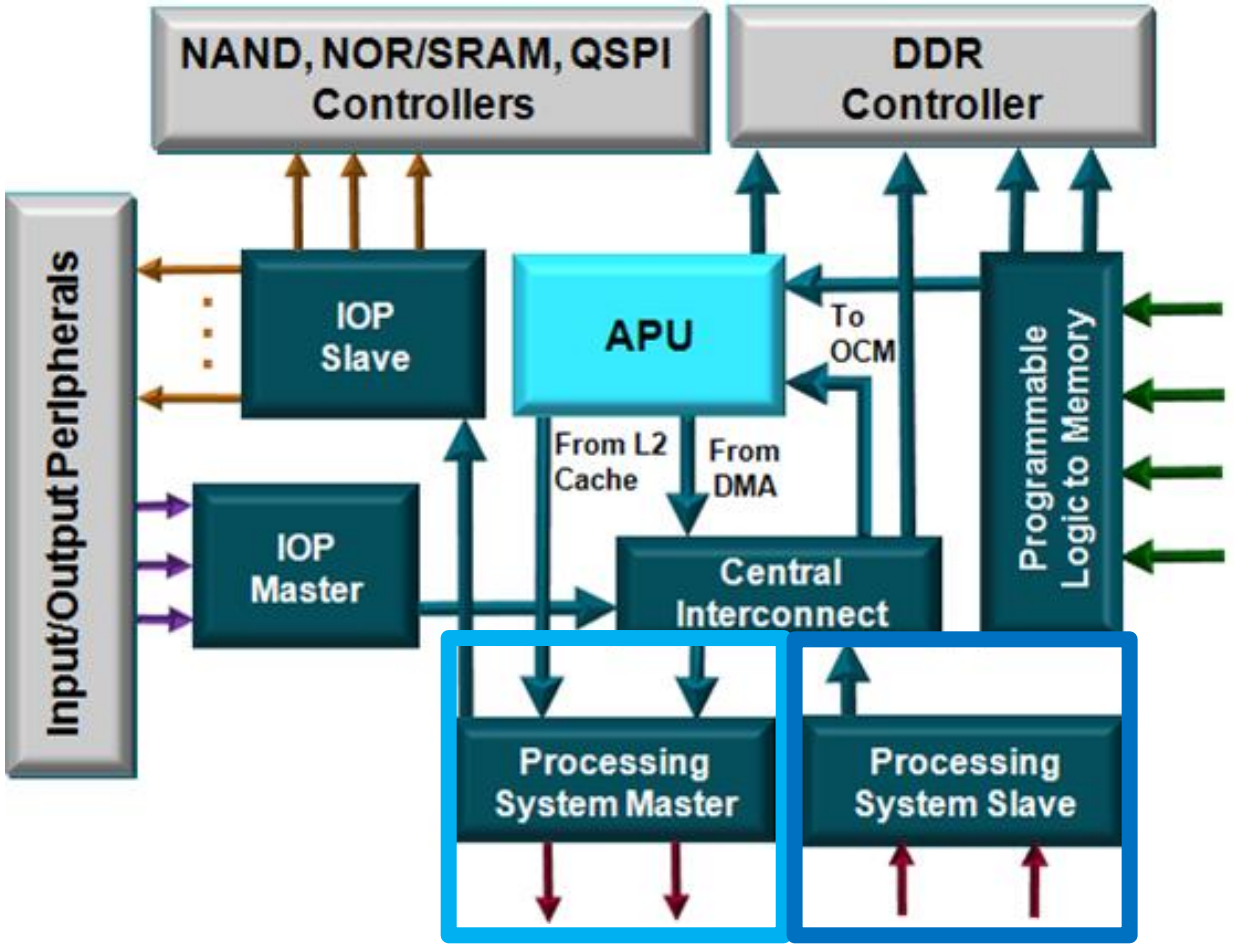
Processing System Interconnect

- Processing system master
  - Two ports from the processing system to programmable logic
  - Connects the CPU block to common peripherals through the central interconnect
- Processing system slave
  - Two ports from programmable logic to the processing system



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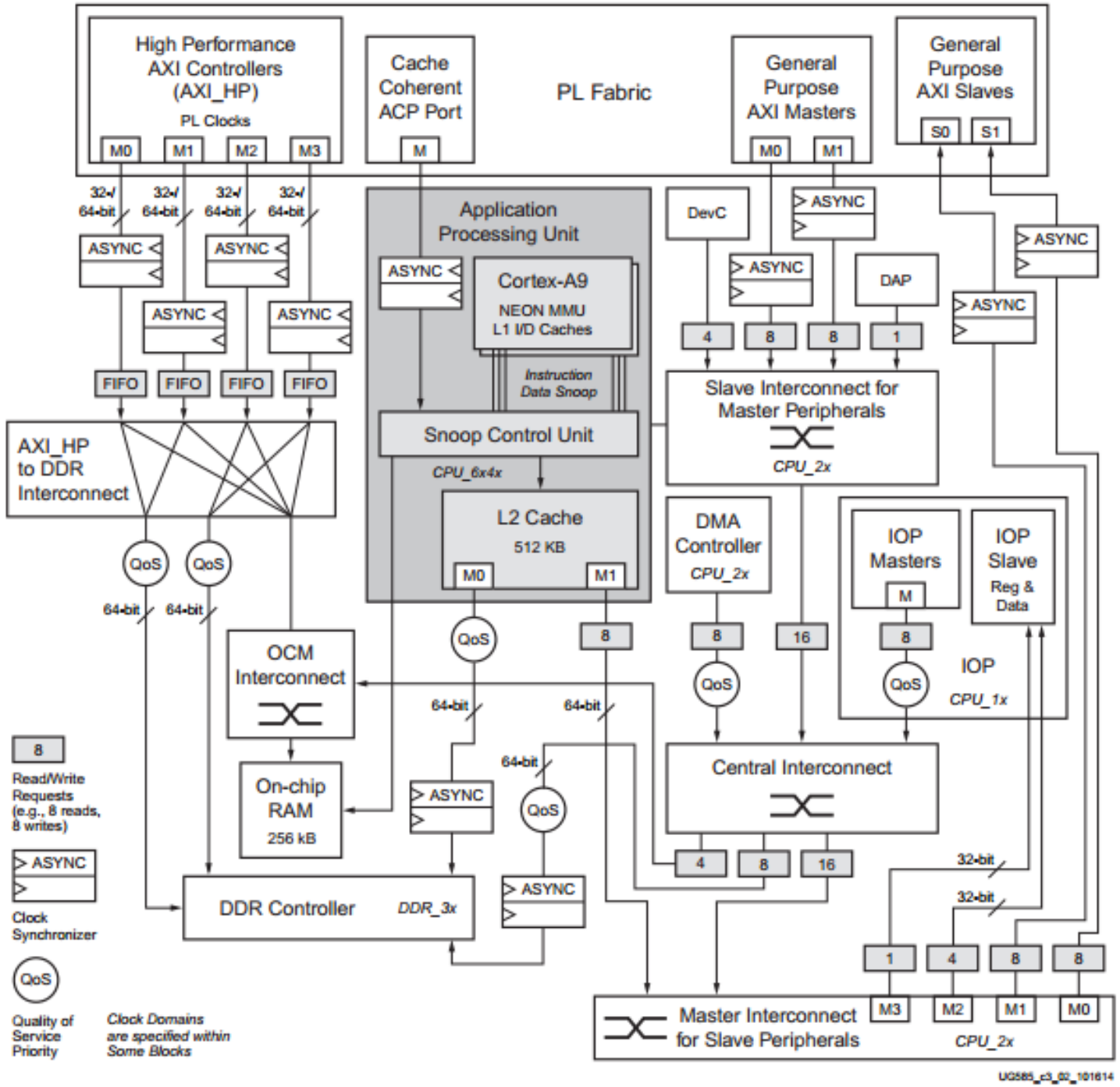
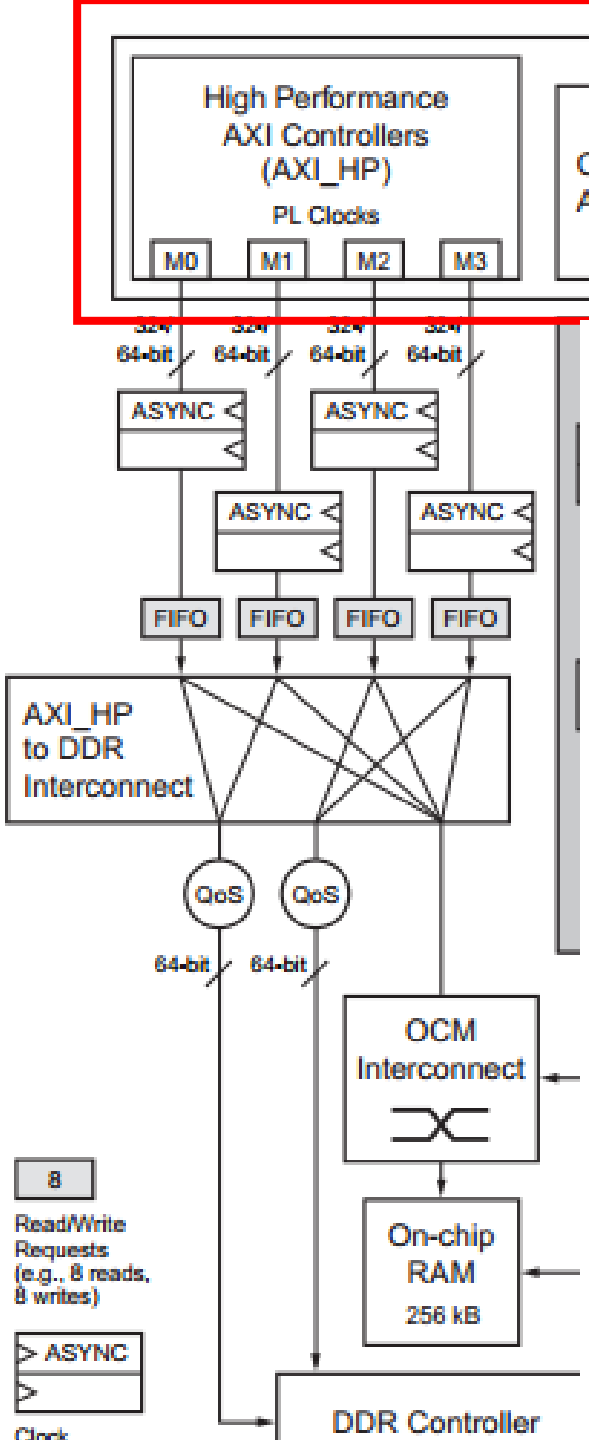
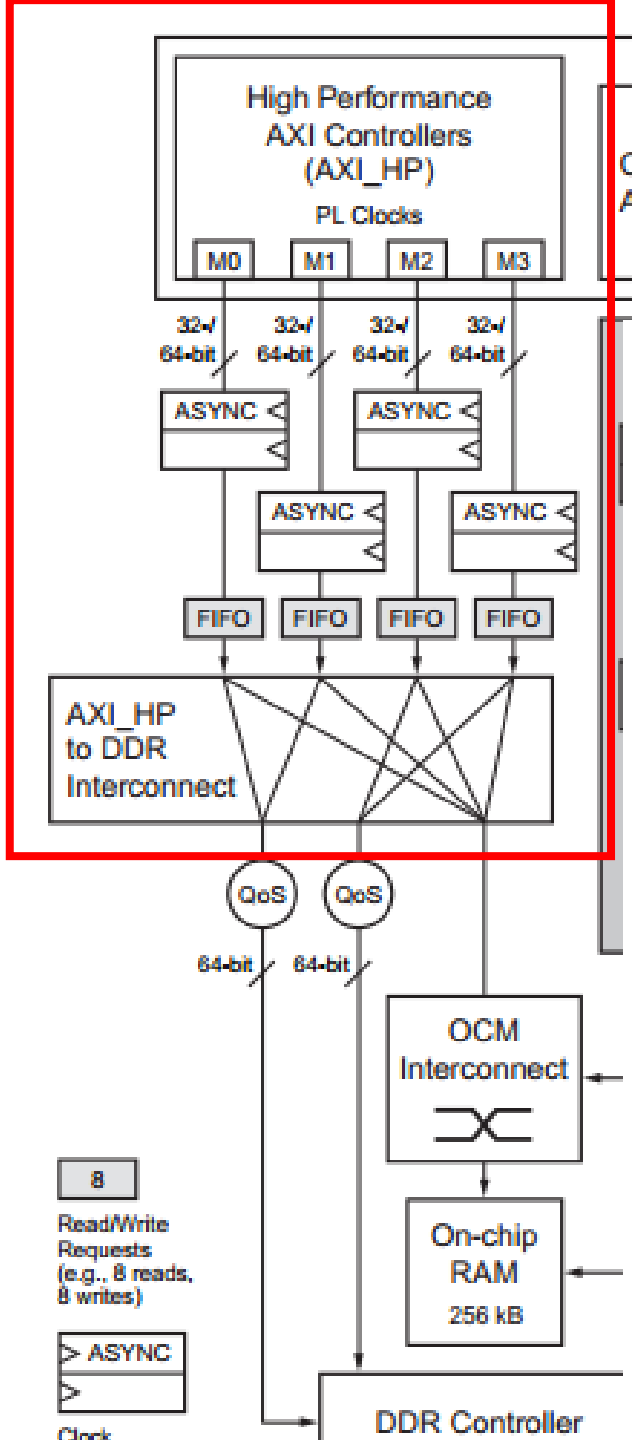
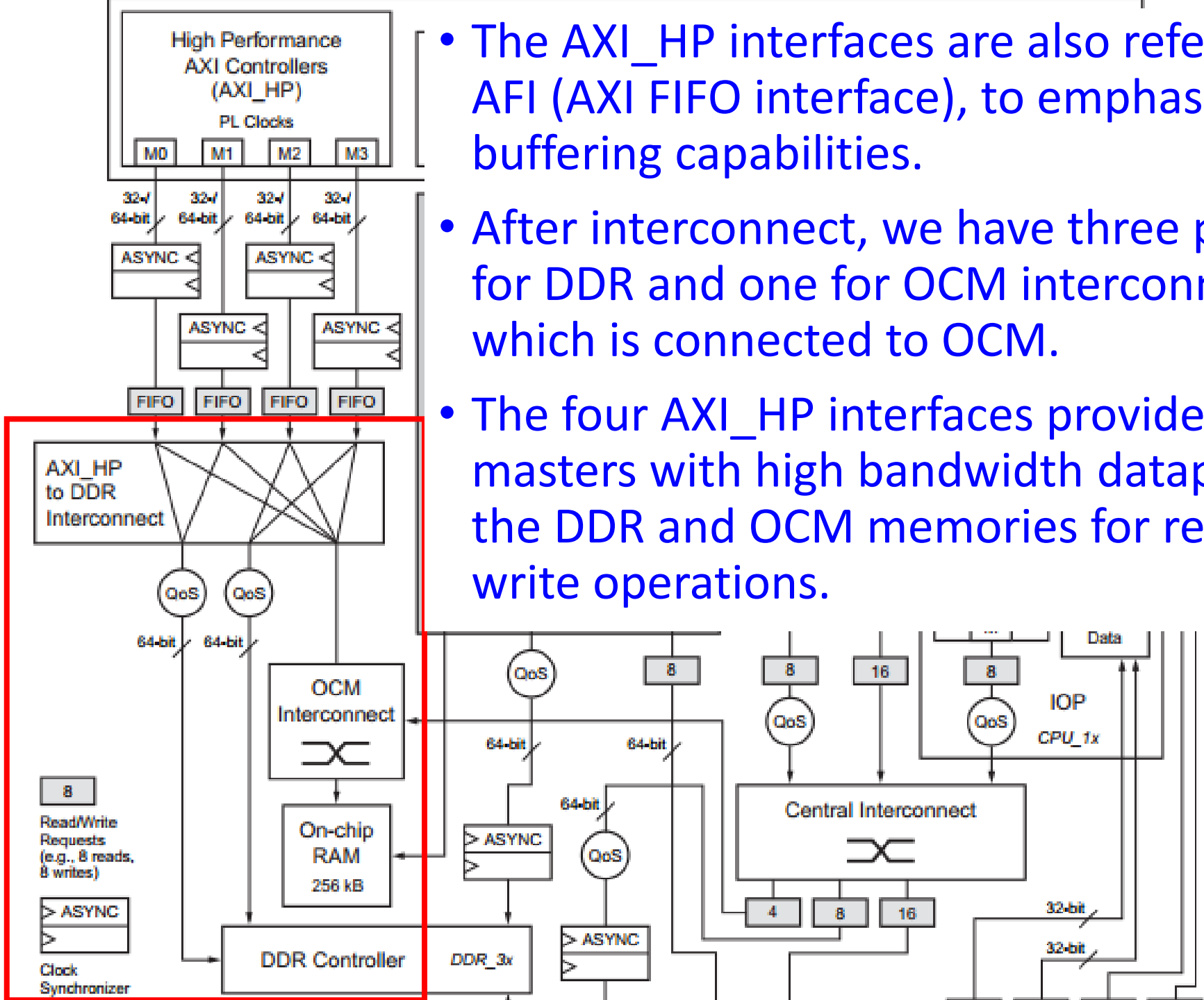

High Performance AXI Controllers (AXI_HP)
PL Clocks
M0
M1
M2
M3
Cache Coherent ACP Port
M
PL Fabric
General Purpose AXI Masters
M0
M1
General Purpose AXI Slaves
S0
S1
32-/64-bit
ASYNC
FIFO
AXI_HP to DDR Interconnect
QoS
64-bit
Application Processing Unit
Cortex-A9
NEON MMU
L1 I/D Caches
Instruction
Data Snoop
Snoop Control Unit
CPU_6x4x
L2 Cache
512 KB
DevC
DAP
4
8
1
Slave Interconnect for Master Peripherals
CPU_2x
DMA Controller
CPU_2x
16
IOP Masters
M
IOP Slave
Reg & Data
IOP
CPU_1x
OCM Interconnect
On-chip RAM
256 kB
Central Interconnect
DDR Controller
DDR_3x
32-bit
Master Interconnect for Slave Peripherals
CPU_2x
M3
M2
M1
M0
Read/Write Requests (e.g., 8 reads, 8 writes)
Clock Synchronizer
Quality of Service Priority
Clock Domains are specified within Some Blocks
UG585_c3_02_101614



- At the top, we have PL fabric where we have HP port, ACP port, GP AXI master and slave ports



- AXI-HP M0-M3 ports are implemented inside the PL i.e. FPGA.
- ASYNC block allows clock domain change so rest of logic in PS can operate at different clock than PL.
- FIFO is used to buffer the data if needed



- The AXI_HP interfaces are also referred as AFI (AXI FIFO interface), to emphasize their buffering capabilities.
- After interconnect, we have three ports: 2 for DDR and one for OCM interconnect which is connected to OCM.
- The four AXI_HP interfaces provide PL bus masters with high bandwidth datapaths to the DDR and OCM memories for read and write operations.

Zynq Architecture: PS and PL