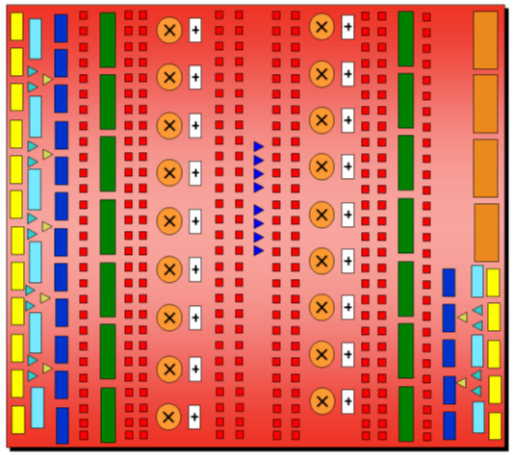
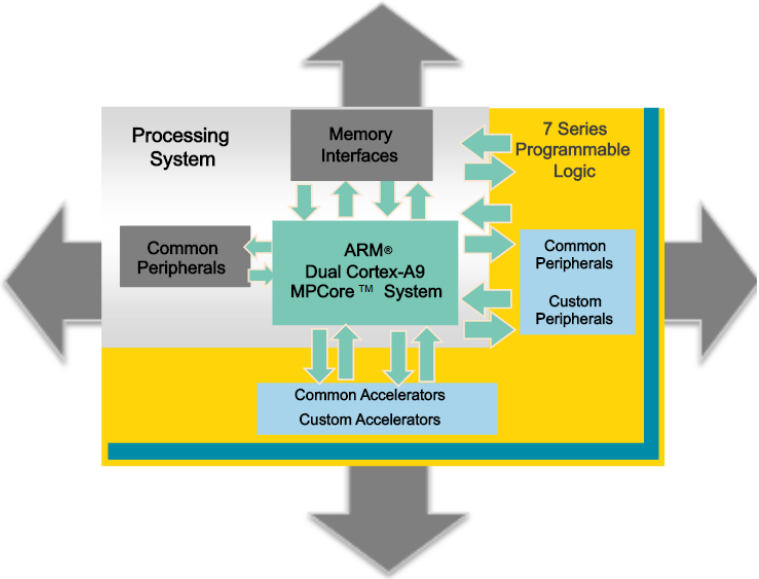
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

A2A
Algorithms to Architecture

ECE 270: Embedded Logic Design

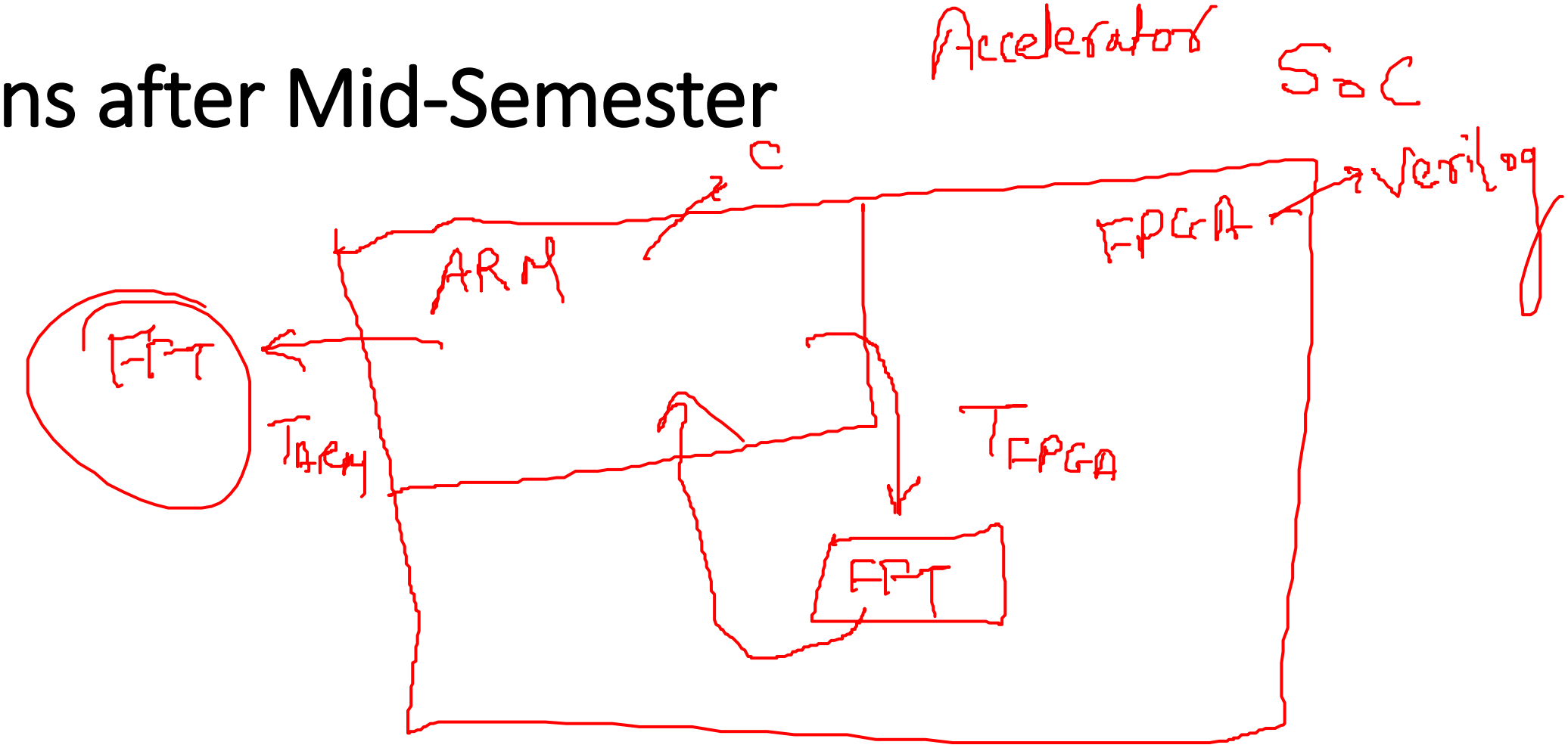




Mid-Semester Performance

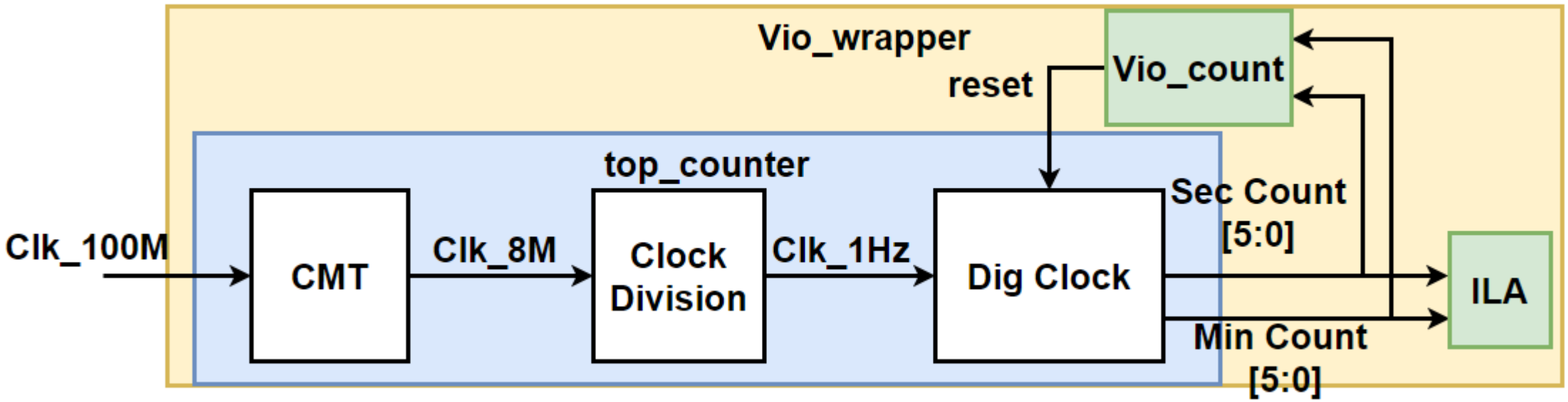
- 35 students with 10+ marks (27 with 15 marks)
- 75 students with 0 marks (even after open book test with ChatGPT)
- Theory performance is nearly same as lab performance

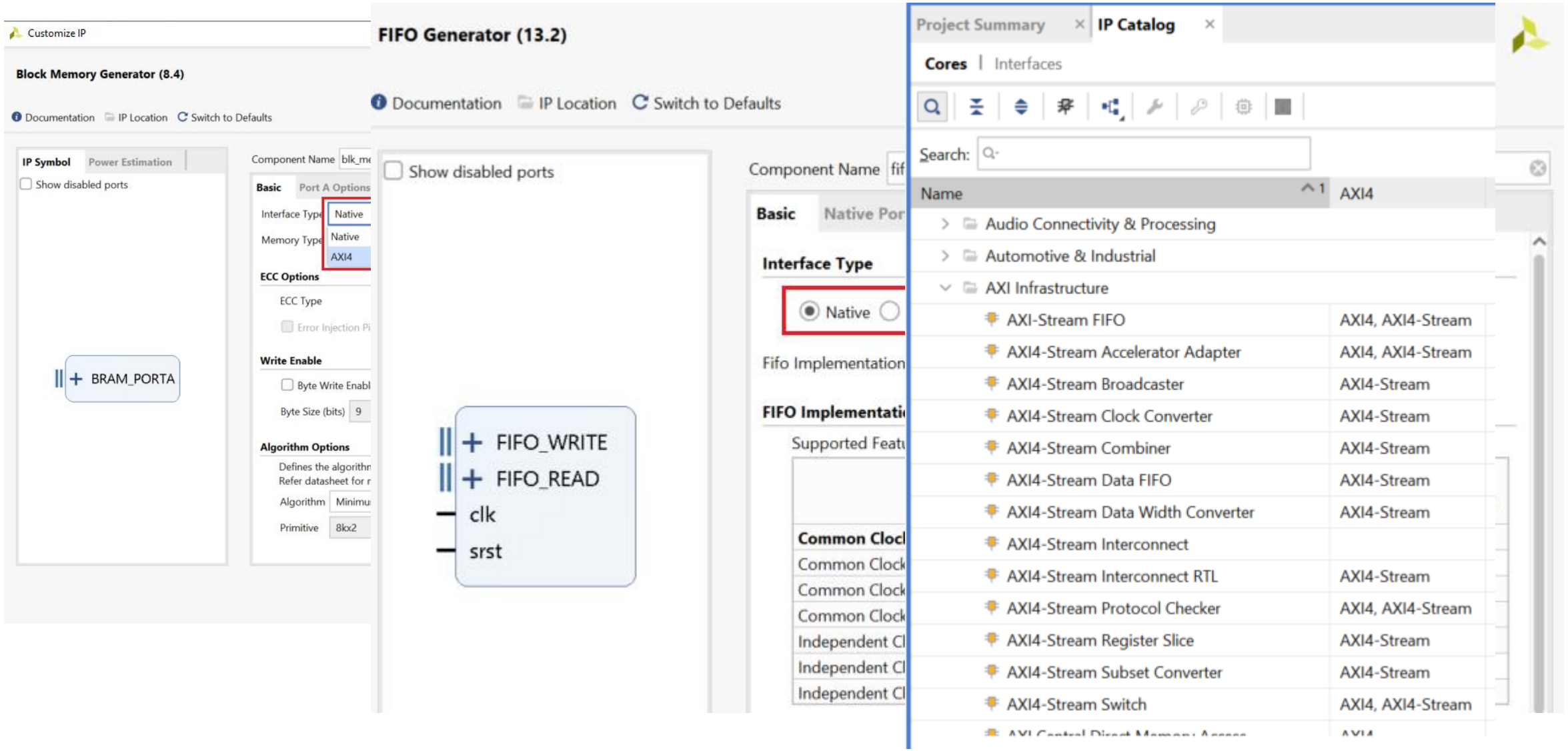
Plans after Mid-Semester

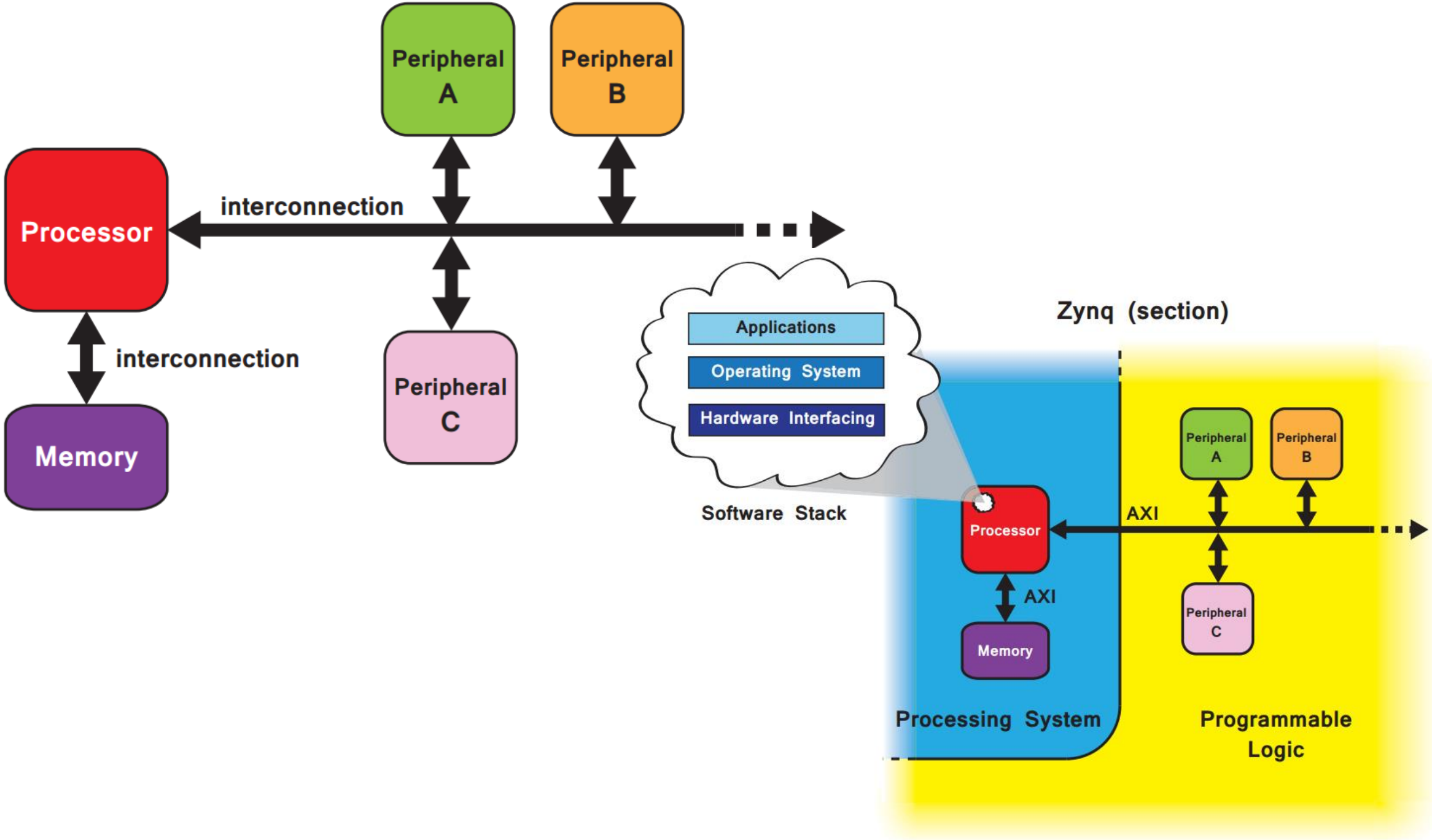


Advanced eXtensible Interface (AXI)

Native Interface

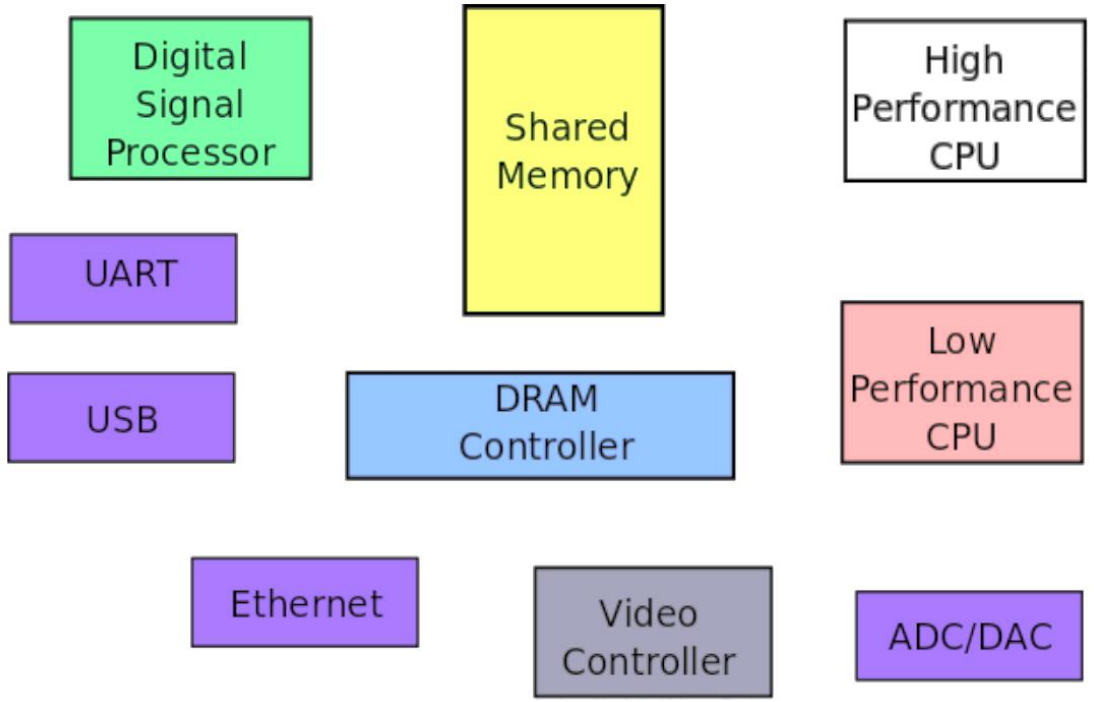


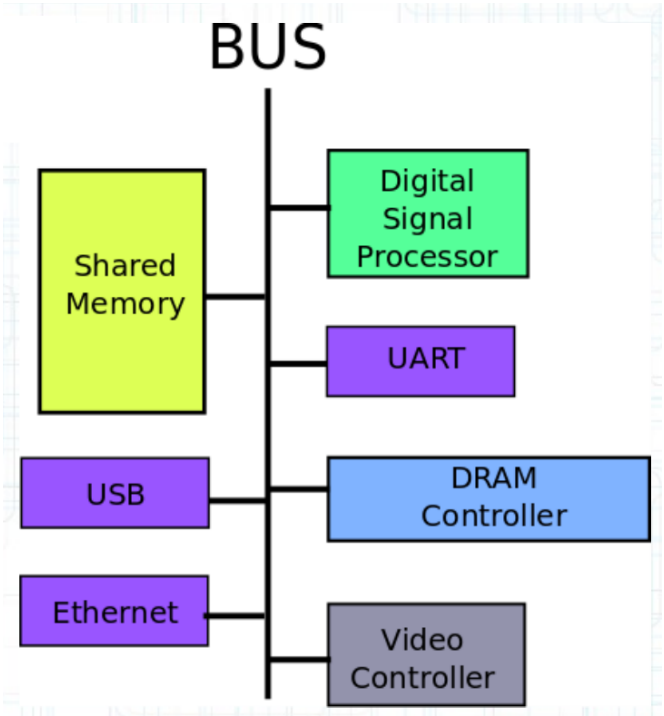

Customize IP
Block Memory Generator (8.4)
Documentation
IP Location
Switch to Defaults
IP Symbol
Power Estimation
Show disabled ports
BRAM_PORTA
Component Name
Basic
Port A Options
Interface Type
Native
Memory Type
Native
AXI4
ECC Options
ECC Type
Write Enable
Byte Write Enabl
Byte Size (bits)
9
Algorithm Options
Algorithm
Primitive
8kx2
FIFO Generator (13.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
FIFO_WRITE
FIFO_READ
clk
srst
Component Name
Basic
Native Por
Interface Type
Native
Fifo Implementation
FIFO Implementati
Supported Featu
Common Clock
Common Clock
Common Clock
Common Clock
Independent Cl
Independent Cl
Independent Cl
Project Summary
IP Catalog
Cores
Interfaces
Search:
Name
AXI4
Audio Connectivity & Processing
Automotive & Industrial
AXI Infrastructure
AXI-Stream FIFO
AXI4, AXI4-Stream
AXI4-Stream Accelerator Adapter
AXI4, AXI4-Stream
AXI4-Stream Broadcaster
AXI4-Stream
AXI4-Stream Clock Converter
AXI4-Stream
AXI4-Stream Combiner
AXI4-Stream
AXI4-Stream Data FIFO
AXI4-Stream
AXI4-Stream Data Width Converter
AXI4-Stream
AXI4-Stream Interconnect
AXI4-Stream Interconnect RTL
AXI4-Stream
AXI4-Stream Protocol Checker
AXI4, AXI4-Stream
AXI4-Stream Register Slice
AXI4-Stream
AXI4-Stream Subset Converter
AXI4-Stream
AXI4-Stream Switch
AXI4, AXI4-Stream


Peripheral A
Peripheral B
Processor
interconnection
interconnection
Memory
Peripheral C
Applications
Operating System
Hardware Interfacing
Software Stack
Zynq (section)
Peripheral A
Peripheral B
AXI
Processor
AXI
Memory
Peripheral C
Processing System
Programmable Logic

Interface

- Modern day design consists of large number of IP blocks, each one designed to efficiently perform assigned task.
- In order to talk with each other and share data, communication standard or protocol is necessary.

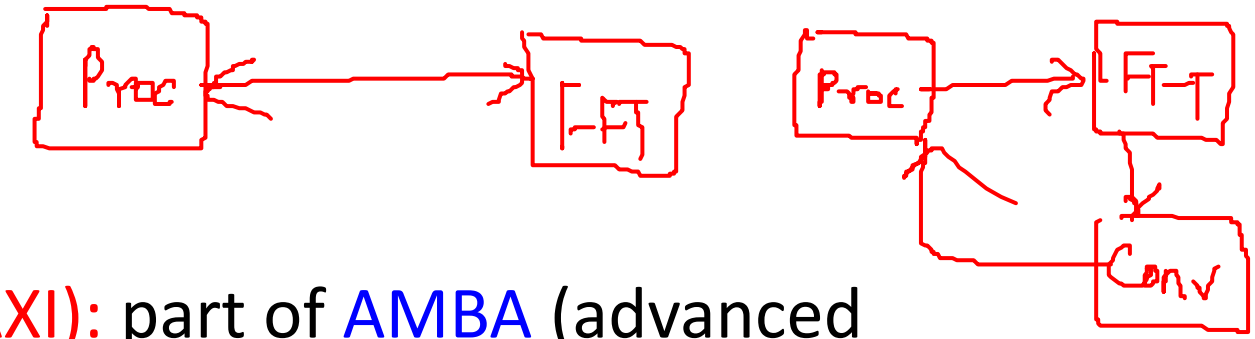




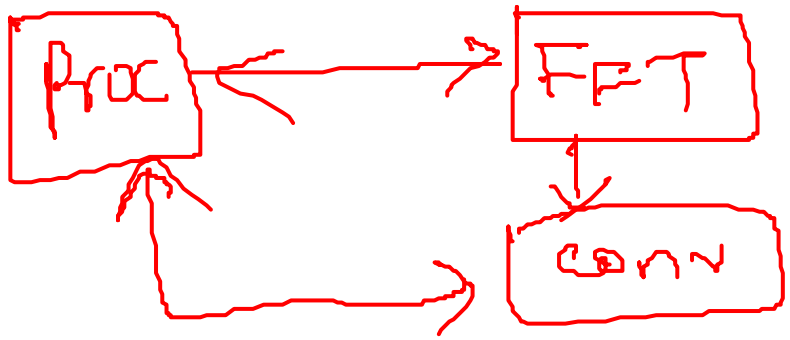
Interface

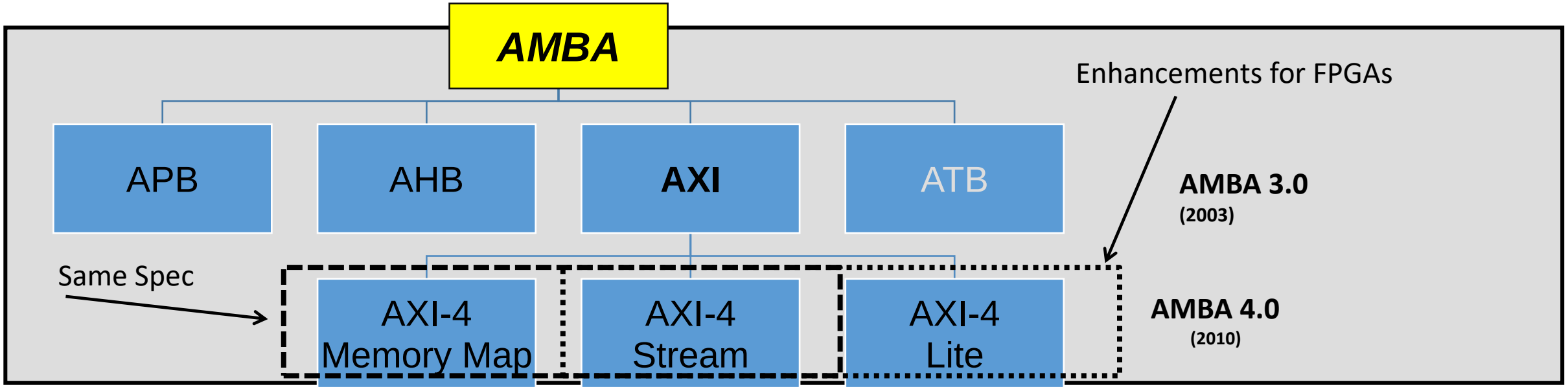
- **Advanced eXtensible Interface (AXI)** is one of the several standards developed by ARM and adopted by Xilinx for Zynq architecture (Others are IBM core connect and WishBone).
- **Availability**: By moving to an industry-standard, you have access not only to the Vivado IP Catalog, but also to a worldwide community of ARM partners.
- **Productivity**: By standardizing on the AXI interface, developers need to learn only a single protocol for IP
- **Flexibility**: Providing the right protocol for the application

AXI



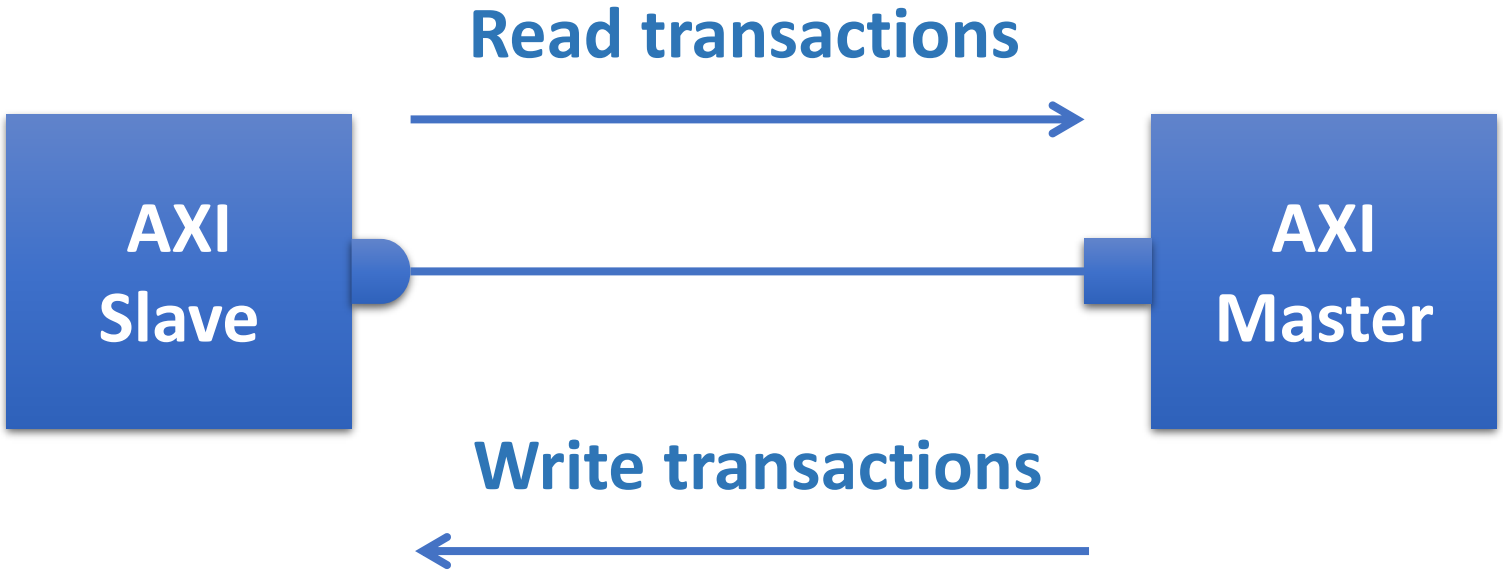
❖ Advanced eXtensible Interface (AXI): part of AMBA (advanced microcontroller bus architecture)





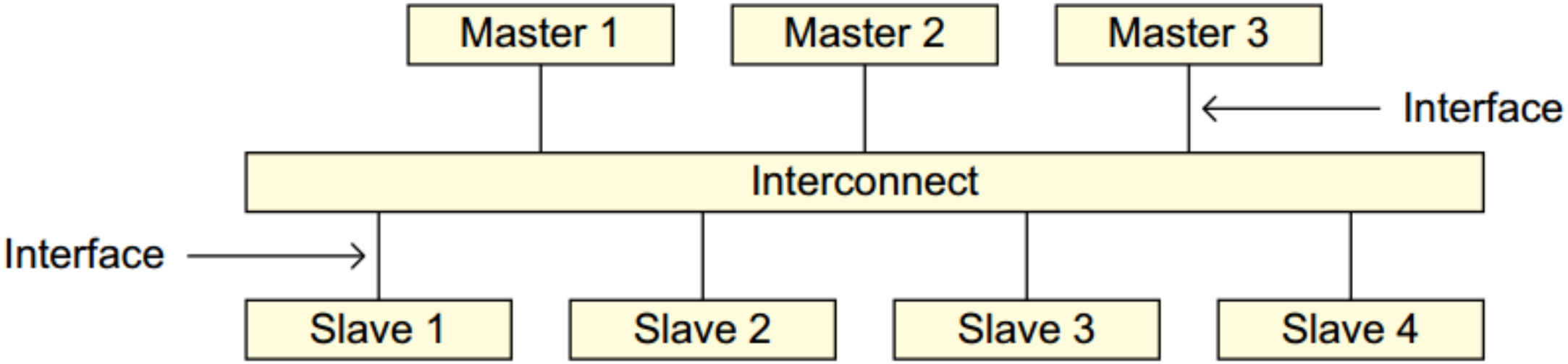
AXI

- Every AXI link contains two part: AXI master and AXI slave.
- AXI master initializes the transactions such as read and write. AXI slave is the one who responds to AXI master transactions.
- **Transaction:** Transfer of data from one point to another point



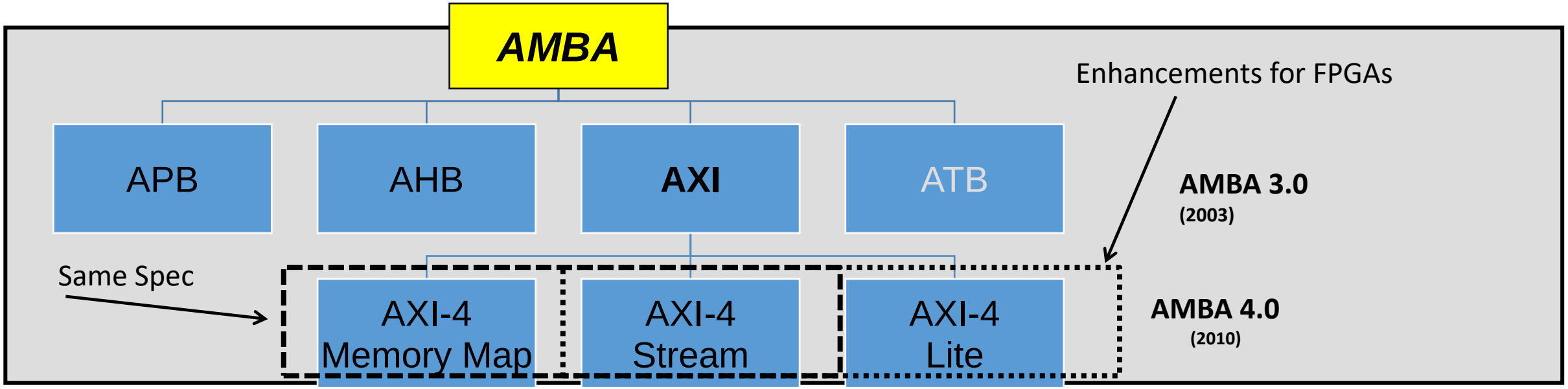
The AXI protocol provides a single interface definition, for the interfaces:

- between a master and the interconnect
- between a slave and the interconnect
- between a master and a slave.



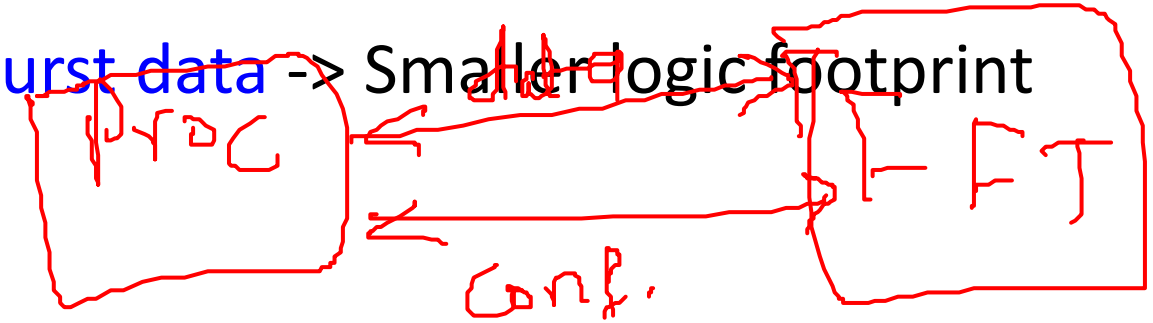
AXI

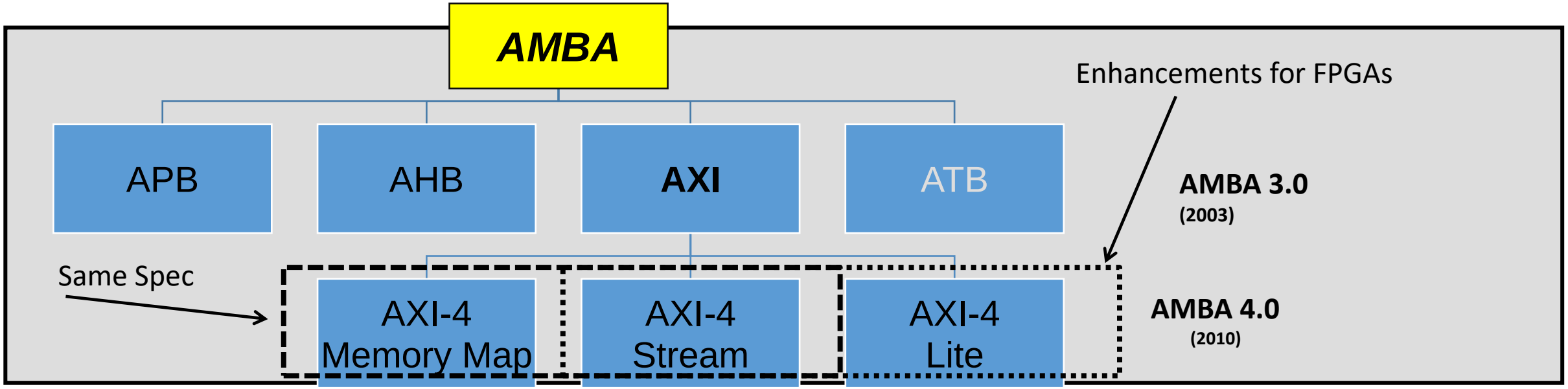
- **AXI4-memory mapped:**
  - Single address, multiple data
  - High-performance interface
  - Suited for memory mapped communication allowing bursts of up to 256 data transfer cycles per address phase



AXI

- **AXI4-Lite:**
  - Single address, single data: memory mapped single transactions
  - Does not support burst data -> Smaller logic footprint





AXI

- **AXI4-Stream:**
  - No address phase means this is not memory mapped
  - Unlimited* data burst size