Universidad del Valle de Guatemala
Curso Arquitectura de computadores
Sección 11

Procesador

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=== Ciclo 0 === Tiempo 10 ===
PC = 0 | Instruccion = 00101000000000010000000000001111
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001010
Operacion:
write_reg = 1 | ALU_Result = 15 | write_data = 15
----------------------------------------

=== Ciclo 1 === Tiempo 20 ===
PC = 4 | Instruccion = 00101000000000010000000000010100
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001010
Operacion:
write_reg = 2 | ALU_Result = 20 | write_data = 20
----------------------------------------

=== Ciclo 2 === Tiempo 30 ===
PC = 8 | Instruccion = 00101000000000011000000000110010
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001010
Operacion:
write_reg = 3 | ALU_Result = 50 | write_data = 50
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=== Ciclo 3 === Tiempo 40 ===
PC = 12 | Instruccion = 00101000000001000000000000000101
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001010
Operacion:
write_reg = 4 | ALU_Result = 5 | write_data = 5
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=== Ciclo 4 === Tiempo 50 ===
PC = 16 | Instruccion = 00101000000001010000000000000010
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001010
Operacion:
write_reg = 5 | ALU_Result = 2 | write_data = 2
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=== Ciclo 5 === Tiempo 60 ===
PC = 20 | Instruccion = 00000000001000100011000000100000
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 6 | ALU_Result = 35 | write_data = 35
----------------------------------------

=== Ciclo 6 === Tiempo 70 ===
PC = 24 | Instruccion = 00000000011000010011100000100010
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 7 | ALU_Result = 35 | write_data = 35
----------------------------------------

=== Ciclo 7 === Tiempo 80 ===
PC = 28 | Instruccion = 00000000010000110100000000011000
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 8 | ALU_Result = 1000 | write_data = 1000
----------------------------------------

=== Ciclo 8 === Tiempo 90 ===
PC = 32 | Instruccion = 00000000011000100100100000011010
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 9 | ALU_Result = 2 | write_data = 2
----------------------------------------

=== Ciclo 9 === Tiempo 100 ===
PC = 36 | Instruccion = 00100000001000010000000000001010
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001000
Operacion:
write_reg = 1 | ALU_Result = 25 | write_data = 25
----------------------------------------
```

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=== Ciclo 10 === Tiempo 110 ===
PC = 40 | Instruccion = 00100100010000100000000000000100
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001001
Operacion:
write_reg = 2 | ALU_Result = 16 | write_data = 16
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=== Ciclo 11 === Tiempo 120 ===
PC = 44 | Instruccion = 00000000110001000101000000100000
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 10 | ALU_Result = 40 | write_data = 40
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=== Ciclo 12 === Tiempo 130 ===
PC = 48 | Instruccion = 00000000110001010101100000011000
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 11 | ALU_Result = 70 | write_data = 70
---------------------------------------

=== Ciclo 13 === Tiempo 140 ===
PC = 52 | Instruccion = 00000001010001010110000000011010
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 12 | ALU_Result = 20 | write_data = 20
---------------------------------------

=== Ciclo 14 === Tiempo 150 ===
PC = 56 | Instruccion = 00100000100001000000000000010100
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001000
Operacion:
write_reg = 4 | ALU_Result = 25 | write_data = 25
---------------------------------------

=== Ciclo 15 === Tiempo 160 ===
PC = 60 | Instruccion = 00000000100000110110100000100010
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 13 | ALU_Result = -25 | write_data = -25
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=== Ciclo 16 === Tiempo 170 ===
PC = 64 | Instruccion = 00101000000011100000000001100100
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001010
Operacion:
write_reg = 14 | ALU_Result = 100 | write_data = 100
----------------------------------------

=== Ciclo 17 === Tiempo 180 ===
PC = 68 | Instruccion = 00000001110000010111100000100000
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 15 | ALU_Result = 125 | write_data = 125
----------------------------------------

=== Ciclo 18 === Tiempo 190 ===
PC = 72 | Instruccion = 00100100011000110000000000000101
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001001
Operacion:
write_reg = 3 | ALU_Result = 45 | write_data = 45
----------------------------------------

=== Ciclo 19 === Tiempo 200 ===
PC = 76 | Instruccion = 00000001111000101000000000011000
Senales de Control:
RegWrite = 1 | ALUSrc = 0 | RegDst = 1 | Opcode = 000000
Operacion:
write_reg = 16 | ALU_Result = 2000 | write_data = 2000
----------------------------------------

=== Ciclo 20 === Tiempo 210 ===
PC = 80 | Instruccion = 00100000001100010000000000000001
Senales de Control:
RegWrite = 1 | ALUSrc = 1 | RegDst = 0 | Opcode = 001000
Operacion:
write_reg = 17 | ALU_Result = 26 | write_data = 26
----------------------------------------

=== Ciclo 21 === Tiempo 220 ===
PC = 84 | Instruccion = 00001000000000000000010000000000
Senales de Control:
RegWrite = 0 | ALUSrc = 0 | RegDst = 0 | Opcode = 000010
Operacion:
write_reg = 0 | ALU_Result = 0 | write_data = 0
----------------------------------------
```

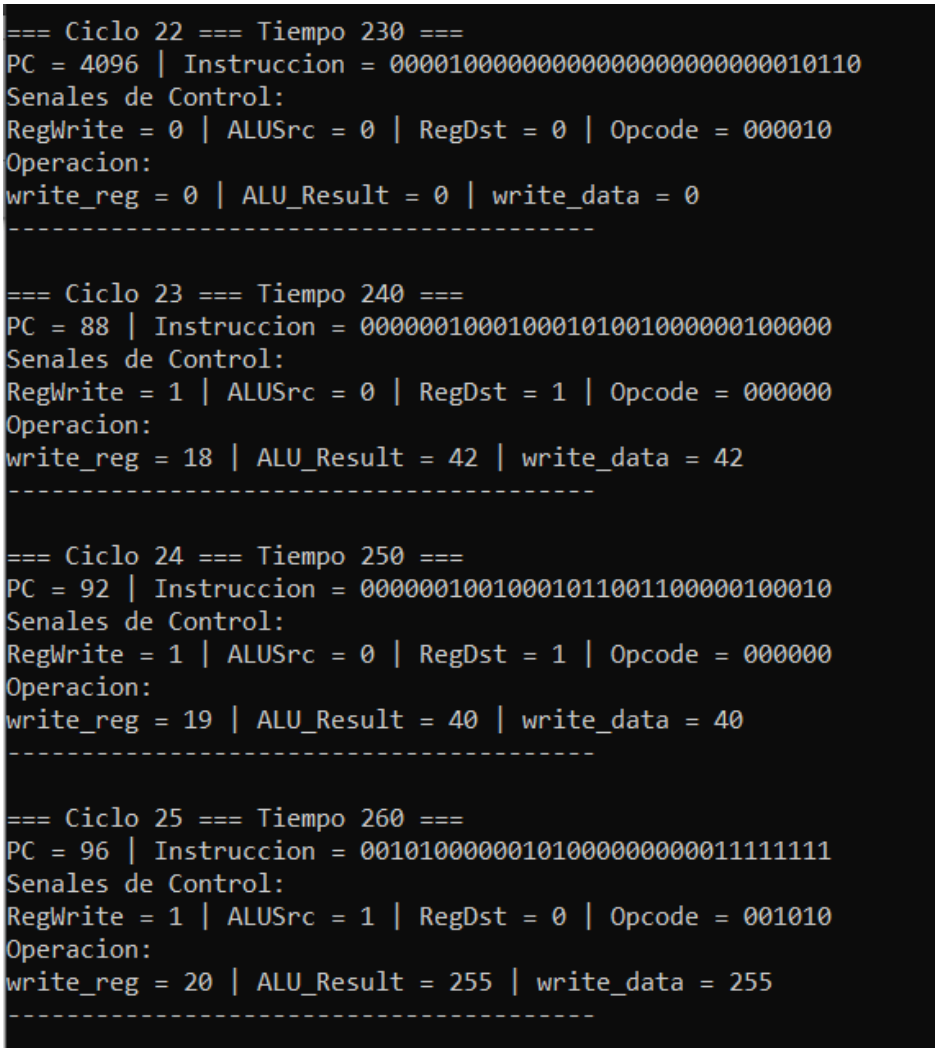

Figura 1. Ciclos, cambios, registros y resultados

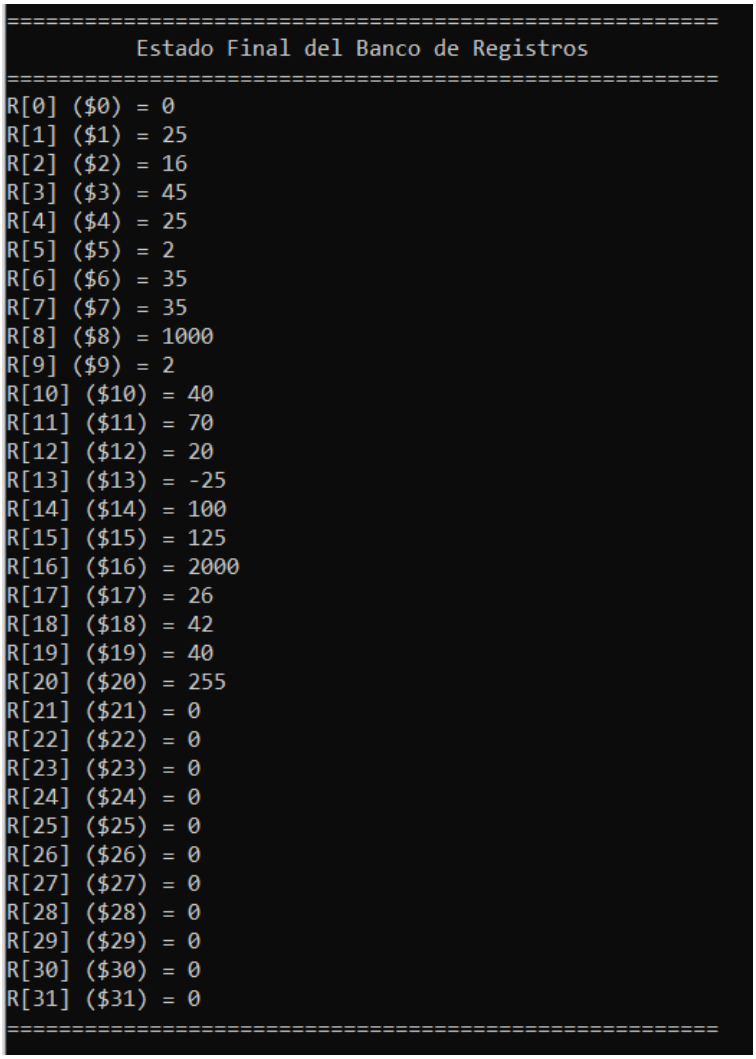

Figura 2. Estado final de registro

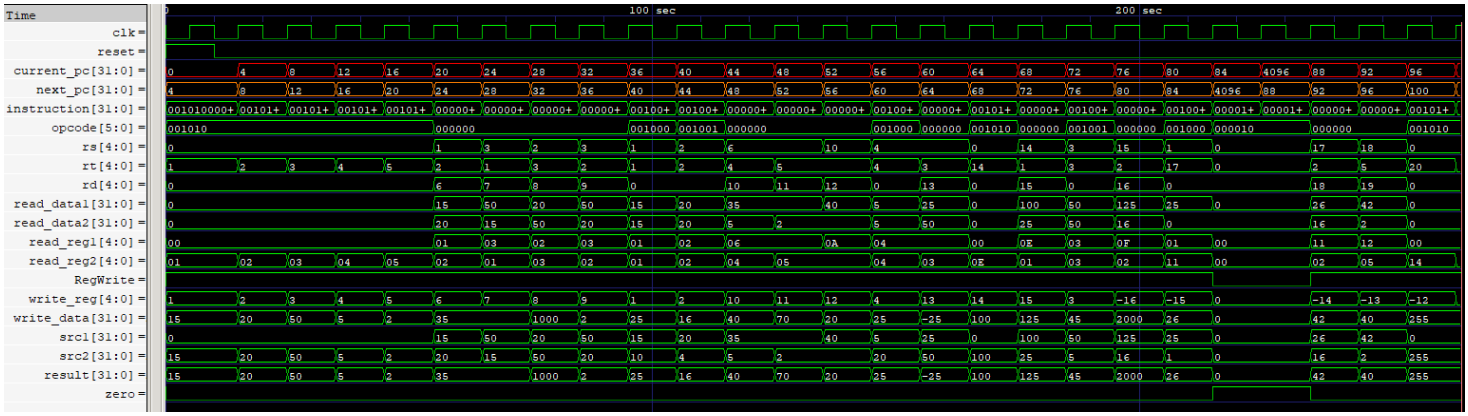

Figura 3. Resultados correctos en GTKWAVE