











AMC1301



SBAS667C -APRIL 2016-REVISED SEPTEMBER 2016

AMC1301 Precision, ±250-mV Input, 3-µs Delay, Reinforced Isolated Amplifier

1 Features

- ±250-mV Input Voltage Range Optimized for Current Measurement Using Shunt Resistors
- Low Offset Error and Drift: ±200 μV at 25°C, ± 3 μV/°C
- Fixed Gain: 8.2
- Very Low Gain Error and Drift: ±0.3% at 25°C, ± 50 ppm/°C
- Very Low Nonlinearity and Drift: 0.03%, 1 ppm/°C
- · 3.3-V Operation on High-Side and Low-Side
- · System-Level Diagnostic Features
- · Safety-Related Certifications:
 - 7000-V_{PK} Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
 - 5000-V_{RMS} Isolation for 1 Minute per UL1577
 - CAN/CSA No. 5A-Component Acceptance Service Notice, IEC 60950-1, and IEC 60065 End Equipment Standards
- Fully Specified Over the Extended Industrial Temperature Range

2 Applications

- Shunt-Resistor-Based Current Sensing In:
 - Motor Drives
 - Frequency Inverters
 - Uninterruptible Power Supplies
- Isolated Voltage Sensing

3 Description

The AMC1301 device is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV_{PEAK} according to VDE V 0884-10 and UL1577. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry.

The input of the AMC1301 device is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The excellent performance of the device supports accurate current control resulting in system-level power savings and, especially in motor control applications, lower torque ripple. The integrated common-mode overvoltage and missing high-side supply voltage detection features of the AMC1301 device simplify system-level design and diagnostics.

The AMC1301 device is fully specified over the extended industrial temperature range of -40°C to +125°C and is available in a wide-body 8-pin SOIC (DWV) package.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1301	SOIC (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

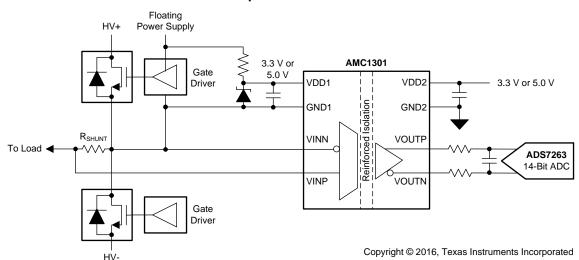




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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision B (June 2016) to Revision C	Page
•	Changed 12-Bit ADC to 14-Bit ADC in Simplified Schematic figure	1
•	Changed maximum specification of Supply voltage row in Absolute Maximum Ratings table	5
•	Changed 12-Bit ADC to 14-Bit ADC in Zener-Diode Based, High Side Power Supply figure in Power Supply Recommendations section	25

Cł	hanges from Revision A (April 2016) to Revision B	Page
•	Changed Features bullet from "Safety and Regulatory Approvals" to "Safety-Related Certifications"	1
•	Changed Simplified Schematic figure in Device Information table	1
•	Changed section title from "Regulatory Information" to "Safety-Related Certifications"	<mark>7</mark>
•	Changed V _{CM} test conditions in <i>Electrical Characteristics</i> table	<mark>7</mark>
•	Added V _{IN} footnote to <i>Electrical Characteristics</i> table	<mark>7</mark>
•	Changed V _{IN} test conditions in <i>Electrical Characteristics</i> table	
•	Changed V _{IN} units in <i>Electrical Characteristics</i> table	
•	Changed common-mode rejection ratio test condition in <i>Electrical Characteristics</i> table	
•	Changed R _{IN} parameter information in <i>Electrical Characteristics</i> table	
•	Changed output noise equation in Electrical Characteristics table	
•	Deleted "Safety and" from Insulation Characteristics Curves section title	
•	Changed Using the AMC1301 Device for Current Sensing in Frequency Inverters figure in Application Information	
•	Changed Zener-Diode Based, High Side Power Supply figure in Power Supply Recommendations	
•	Changed wording in the Receiving Notification of Documentation Updates section	
•	Added a paragraph and changed the formatting of the <i>Related Documentation</i> section	

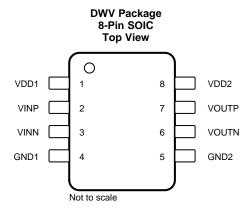




Cł	hanges from Original (April 2016) to Revision A	Pag
•	Released to production	



5 Pin Configuration and Functions



Pin Functions

P	PIN	1/0	DECORPORTION	
NAME	NO.	1/0	DESCRIPTION	
GND1	4	_	High-side analog ground	
GND2	5	_	Low-side analog ground	
VDD1	1	_	gh-side power supply, 3.0 V to 5.5 V. ee the <i>Power Supply Recommendations</i> section for decoupling recommendations.	
VDD2	8	_	Low-side power supply, 3.0 V to 5.5 V. See the <i>Power Supply Recommendations</i> section for decoupling recommendations.	
VINN	3	I	Inverting analog input	
VINP	2	1	Noninverting analog input	
VOUTN	6	0	erting analog output	
VOUTP	7	0	Noninverting analog output	



6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, VDD1 to GND1 or VDD2 to GND2	-0.3	7	V
Analog input voltage at VINP, VINN	GND1 – 6	VDD1 + 0.5	V
Input current to any pin except supply pins	-10	10	mA
Junction temperature, T _J		150	°C
Storage temperature, T _{stg}	-65	150	°C

¹⁾ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
.,	Electroptetic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD1	High-side supply voltage (VDD1 to GND1)	3.0	5.0	5.5	V
VDD2	Low-side supply voltage (VDD2 to GND2)	3.0	3.3	5.5	V
T _A	Operating ambient temperature	-40		125	ů

6.4 Thermal Information

		AMC1301	
	THERMAL METRIC ⁽¹⁾	DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	16.0	°C/W
ΨЈВ	Junction-to-board characterization parameter	64.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics, SPRA953.

6.5 Power Ratings

	PARAMETER	TEST CONDITIONS	VALUE	UNIT
P_{D}	Maximum power dissipation (both sides)		81.4	mW
P_{D1}	Maximum power dissipation (high-side supply)	VDD1 = VDD2 = 5.5 V	45.65	mW
P_{D2}	Maximum power dissipation (low-side supply)		35.75	mW



6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	VALUE	UNIT
GENERA	L			
CLR	External clearance ⁽¹⁾	Shortest pin-to-pin distance through air	≥ 9	mm
CPG	External creepage ⁽¹⁾	Shortest pin-to-pin distance across the package surface	≥ 9	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0135 mm)	≥ 0.027	mm
СТІ	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
		Rated mains voltage ≤ 300 V _{RMS}	I-IV	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V _{RMS}	1-111	
		Rated mains voltage ≤ 1000 V _{RMS}	1-11	
DIN V VD	E V 0884-10 (VDE V 0884-10): 2006-12 ⁽²⁾		<u> </u>	
V _{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar)	1500	V_{PK}
.,	Maximum-rated isolation working	At ac voltage (sine wave)	1000	V_{RMS}
V _{IOWM}	voltage	At dc voltage	1500	V_{DC}
		V _{TEST} = V _{IOTM} , t = 60 s (qualification test)	7000	
V_{IOTM}	Maximum transient isolation voltage	V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test)	8400	V_{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50- μ s waveform, V _{TEST} = 1.6 × V _{IOSM} = 10000 V _{PK} (qualification)	6250	V_{PK}
		Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s, $V_{pd(m)} = 1.2 \times V_{IORM} = 1800$ V_{PK} , $t_m = 10$ s	≤ 5	
q _{pd}	Apparent charge ⁽⁴⁾	Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}, t_{ini} = 60 \text{ s}, \\ V_{pd(m)} = 1.6 \times V_{IORM} = 2400 V_{PK}, t_m = 10 \text{ s}$	≤ 5	рС
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini} = 1$ s, $V_{pd(m)} = 1.875 \times V_{IORM} = 2812.5 V_{PK}$, $t_m = 1$ s	≤ 5	
C _{IO}	Barrier capacitance, input to output (5)	$V_{IO} = 0.5 V_{PP}$ at 1 MHz	1.2	pF
R _{IO}	Insulation resistance, input to output (5)	$V_{IO} = 500 \text{ V at T}_{S} = 150^{\circ}\text{C}$	> 10 ⁹	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577			.	
V _{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000 \ V_{RMS} \ or 7000 \ V_{DC}, \ t = 60 \ s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000 \ V_{RMS}, \ t = 1 \ s$ (100% production test)	5000	V_{RMS}

⁽¹⁾ Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.

⁽²⁾ This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

⁽³⁾ Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

⁽⁴⁾ Apparent charge is electrical discharge caused by a partial discharge (pd).

⁽⁵⁾ All pins on each side of the barrier are tied together, creating a two-pin device.



6.7 Safety-Related Certifications

VDE	UL			
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs			
Reinforced insulation	Single protection			
Certificate number: 40040142	File number: E181974			

6.8 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O may allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

	PARAMETER	TEST CONDITIONS	MIN	TYP MA	X	UNIT
	Safety input, output, or supply current	$\theta_{JA} = 110.1$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C		2	06	A
IS		$\theta_{JA} = 110.1^{\circ}\text{C/W}, \ V_{I} = 3.6 \ \text{V}, \ T_{J} = 150^{\circ}\text{C}, \ T_{A} = 25^{\circ}\text{C}$		3	15	mA
Ps	Safety input, output, or total power	θ _{JA} = 110.1°C/W, T _J = 150°C, T _A = 25°C		1135	(1)	mW
T_S	Maximum safety temperature			1:	50	°C

⁽¹⁾ Input, output, or the sum of input and output power must not exceed this value.

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

Minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VINP = -250 mV to +250 mV, and VINN = 0 V. Typical specifications are at $T_A = 25^{\circ}\text{C}$, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG	INPUT					
$V_{Clipping}$	Differential input voltage before clipping output	VINP – VINN		±302.7		mV
V_{FSR}	Specified linear differential full-scale	VINP – VINN	-250		250	mV
V_{CM}	Specified common-mode input voltage	(VINP + VINN) / 2 to GND1	-0.16	VDE	01 – 2.1	V
	Absolute common-mode input voltage ⁽¹⁾	(VINN + VINP) / 2 to GND1	-2		VDD1	V
V_{CMov}	Common-mode overvoltage detection level		VDD1 – 2			V
Vos	Input offset voltage	Initial, at T _A = 25°C, VINP = VINN = GND1	-200	±50	200	μV
TCV _{OS}	Input offset drift		-3	±1	3	μV/°C
CMRR	Common mode valuation vatio	$f_{IN} = 0 \text{ Hz}, V_{CM \text{ min}} \le V_{CM} \le V_{CM \text{ max}}$		-93		dB
CIVIKK	Common-mode rejection ratio	f _{IN} = 10 kHz, V _{CM min} ≤ V _{CM} ≤ V _{CM max}		-93		uБ
C _{IND}	Differential input capacitance			1		pF
R _{IN}	Single-ended input resistance	VINN = GND1		18		kΩ
R _{IND}	Differential input resistance			22		kΩ
I _{IB}	Input bias current	VINP = VINN = GND1	-82	-60	-48	μΑ
TCI _{IB}	Input bias current drift			1		nA/°C
BW _{IN}	Input bandwidth			1000		kHz

⁽¹⁾ Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in *Absolute Maximum Ratings*.



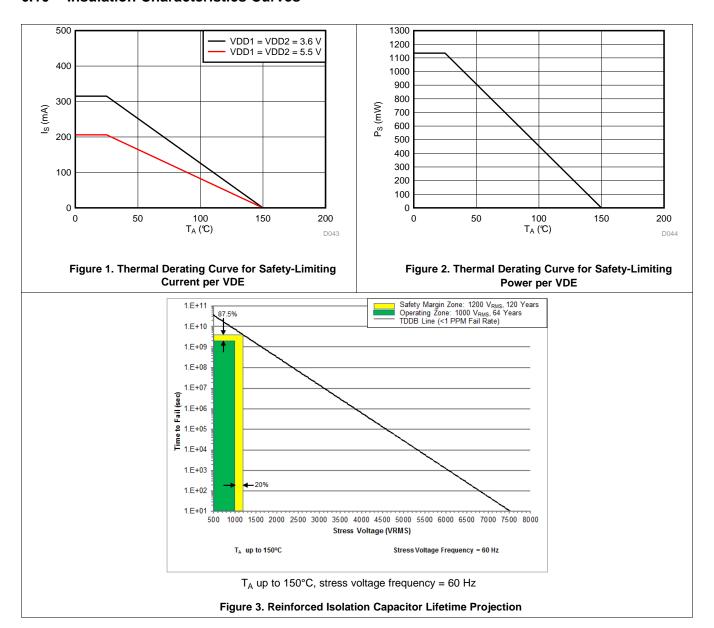
Electrical Characteristics (continued)

Minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VINP = -250 mV to +250 mV, and VINN = 0 V. Typical specifications are at $T_A = 25^{\circ}\text{C}$, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
ANALOG	OUTPUT						
	Nominal gain			8.2			
E _G	Gain error	Initial, at T _A = 25°C	-0.3%	±0.05%	0.3%		
TCE _G	Gain error drift		-50	±15	50	ppm/°C	
	Nonlinearity		-0.03%	±0.01%	0.03%		
	Nonlinearity drift			1		ppm/°C	
THD	Total harmonic distortion	f _{IN} = 10 kHz		-87		dB	
	Output noise	VINP = VINN = GND1, f _{IN} = 0 Hz, BW = 100 kHz		220		μV_{RMS}	
CNID	Cignal to paige ratio	$f_{IN} = 1 \text{ kHz}, BW = 10 \text{ kHz}$	80	84		٩D	
SNR	Signal-to-noise ratio	f _{IN} = 10 kHz, BW = 100 kHz		71		dB	
		vs VDD1, at dc		-94			
PSRR	Power-supply rejection ratio	vs VDD1, 100-mV and 10-kHz ripple		-90		-10	
PSKK		vs VDD2, at dc		-100		dB	
		vs VDD2, 100-mV and 10-kHz ripple		-94			
t _r	Rise time	See Figure 45		2.0		μs	
t _f	Fall time	See Figure 45		2.0		μs	
	V _{IN} to V _{OUT} signal delay (50% – 10%)	See Figure 46, unfiltered output		0.7	2.0	μs	
	V _{IN} to V _{OUT} signal delay (50% – 50%)	See Figure 46, unfiltered output		1.6	2.6	μs	
	V _{IN} to V _{OUT} signal delay (50% – 90%)	See Figure 46, unfiltered output		2.5	3.0	μs	
CMTI	Common-mode transient immunity	GND1 – GND2 = 1 kV	15			kV/µs	
V _{CMout}	Common-mode output voltage		1.39	1.44	1.49	V	
	Output short-circuit current			±13		mA	
R _{OUT}	Output resistance	on VOUTP or VOUTN		< 0.2		Ω	
BW	Output bandwidth		190	210		kHz	
V _{FAILSAFE}	Failsafe differential output voltage	V _{CM} ≥ V _{CMov} , or VDD1 missing		-2.563	-2.545	V	
POWER S	SUPPLY		•				
	High aids according accorde	3.0 V ≤ VDD1 ≤ 3.6 V		5.0	6.9	A	
I _{DD1}	High-side supply current	4.5 V ≤ VDD1 ≤ 5.5 V		5.9	8.3	mA	
	Law aida ayaab ayeest	3.0 V ≤ VDD1 ≤ 3.6 V		4.4	5.6	mA	
I _{DD2}	Low-side supply current	4.5 V ≤ VDD1 ≤ 5.5 V		4.8	8 6.5		
D	Llieb side pourer distinction	3.0 V ≤ VDD1 ≤ 3.6 V		16.5	24.84		
P_{DD1}	High-side power dissipation	4.5 V ≤ VDD1 ≤ 5.5 V		29.5 45.65		mW	
D	Low side newer disciplation	3.0 V ≤ VDD1 ≤ 3.6 V		14.52	20.16	mW	
P_{DD2}	Low-side power dissipation	4.5 V ≤ VDD1 ≤ 5.5 V		24 3			



6.10 Insulation Characteristics Curves

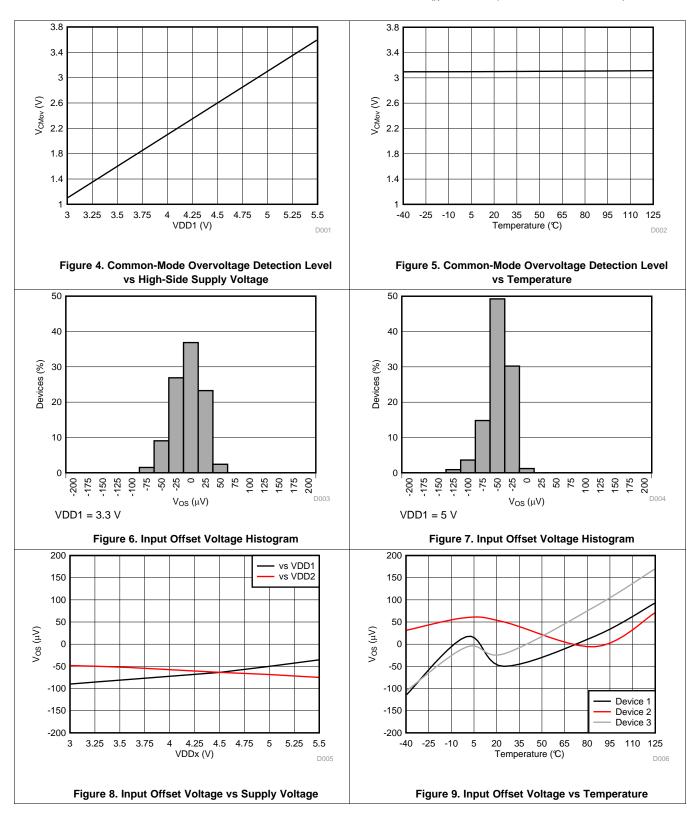


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TEXAS INSTRUMENTS

6.11 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = -250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



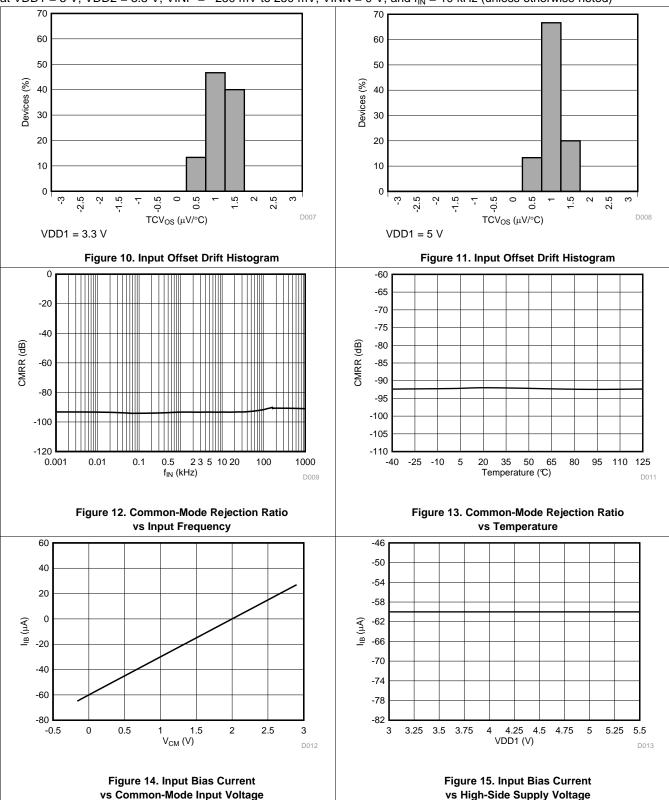
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Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = -250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



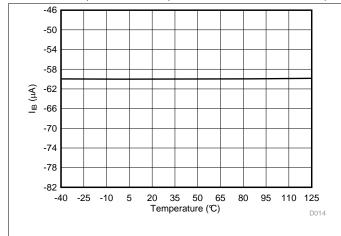
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TEXAS INSTRUMENTS

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = -250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



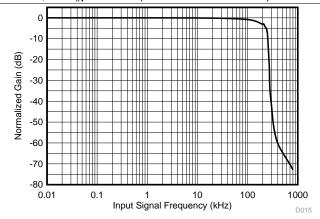
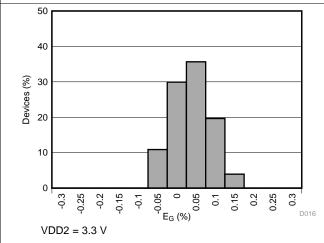


Figure 16. Input Bias Current vs Temperature

Figure 17. Normalized Gain vs Input Frequency



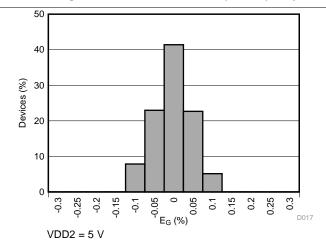
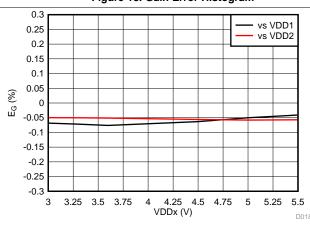


Figure 18. Gain Error Histogram

Figure 19. Gain Error Histogram



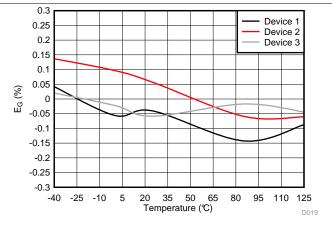


Figure 20. Gain Error vs Supply Voltage Figure 21. Gain Error vs Temperature

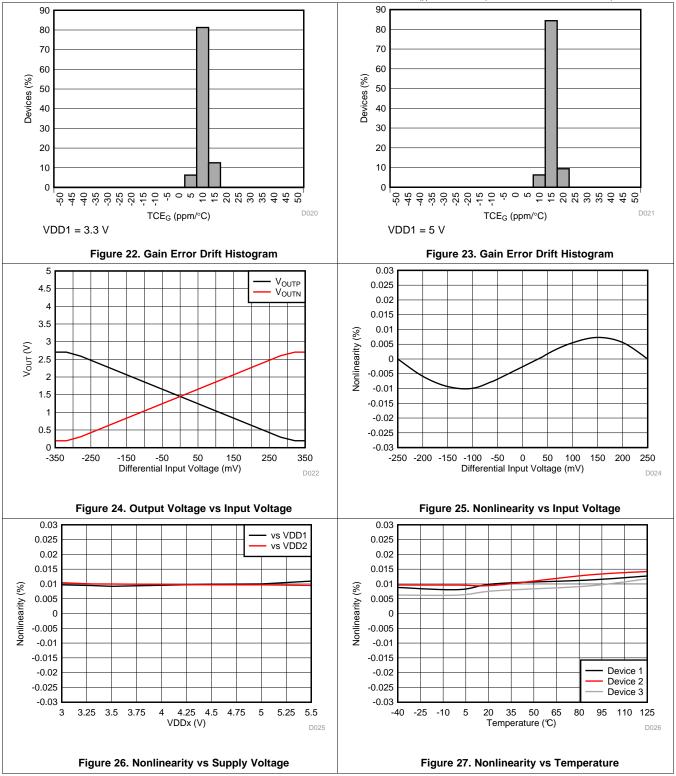
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Typical Characteristics (continued)

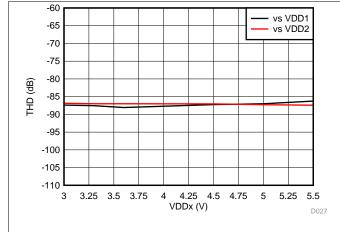
at VDD1 = 5 V, VDD2 = 3.3 V, VINP = -250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



TEXAS INSTRUMENTS

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = -250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



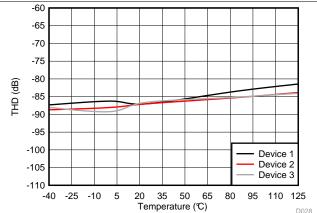
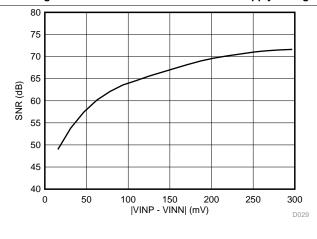


Figure 28. Total Harmonic Distortion vs Supply Voltage





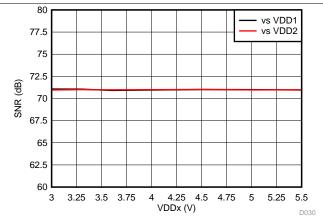
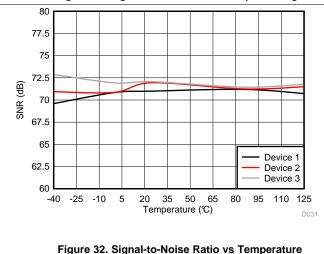


Figure 30. Signal-to-Noise Ratio vs Input Voltage

Figure 31. Signal-to-Noise Ratio vs Supply Voltage



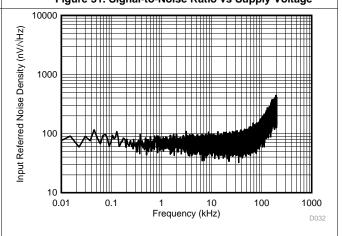


Figure 33. Input-Referred Noise Density vs Frequency

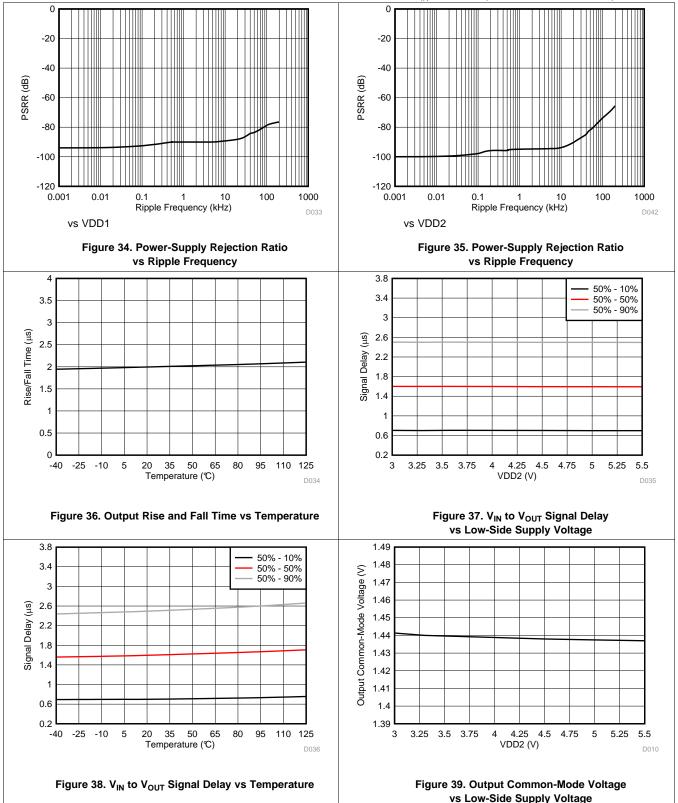
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Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = -250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



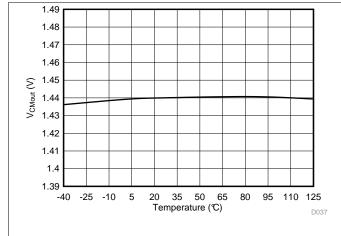
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TEXAS INSTRUMENTS

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = -250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



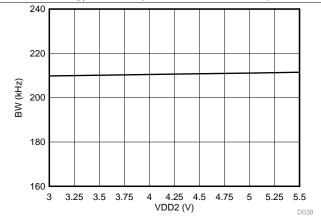
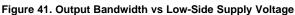
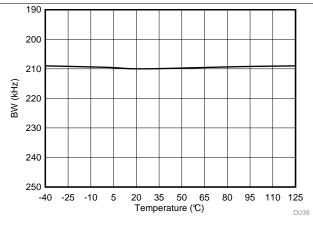


Figure 40. Output Common-Mode Voltage vs Temperature





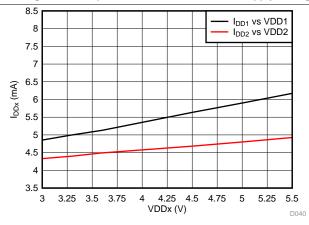


Figure 42. Output Bandwidth vs Temperature

Figure 43. Supply Current vs Supply Voltage

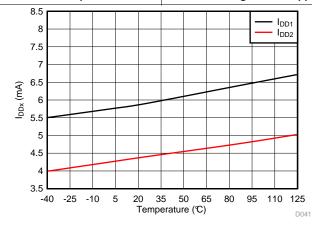


Figure 44. Supply Current vs Temperature

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7 Parameter Measurement Information

7.1 Timing Diagrams



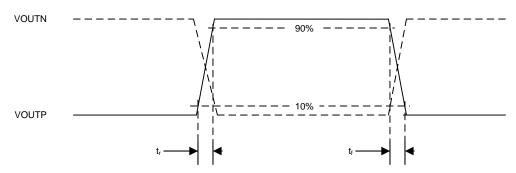


Figure 45. Rise and Fall Time Test Waveforms

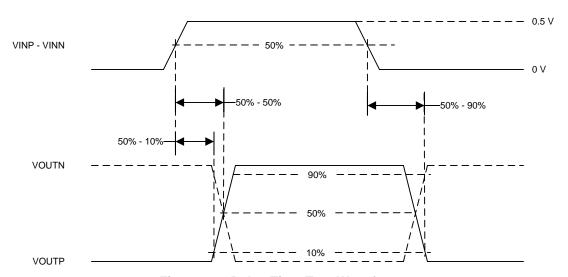


Figure 46. Delay Time Test Waveforms



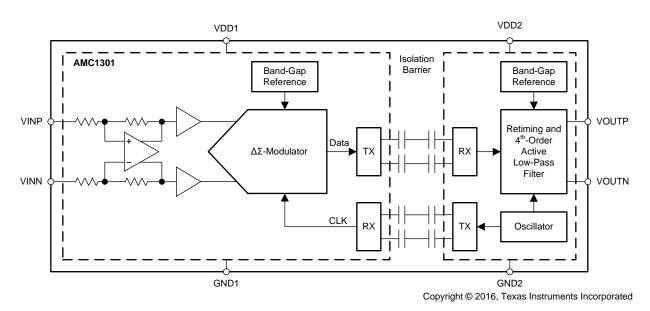
8 Detailed Description

8.1 Overview

The AMC1301 device is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called TX in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential output of the device, as shown in the *Functional Block Diagram*.

The SiO₂-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in *ISO72x Digital Isolator Magnetic-Field Immunity*. The digital modulation used in the AMC1301 device and the isolation barrier characteristics result in high reliability and common-mode transient immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The AMC1301 device incorporates front-end circuitry that contains a fully-differential amplifier followed by a $\Delta\Sigma$ modulator sampling stage. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 with a differential input impedance of 22 k Ω . Consider the input impedance of the AMC1301 device in designs with high-impedance signal sources that may cause degradation of gain and offset specifications. The importance of this effect, however, depends on the desired system performance.

Additionally, the input bias current caused by the internal common-mode voltage at the output of the differential amplifier causes an offset that is dependent on the actual amplitude of the input signal. See the *Isolated Voltage Sensing* section for more details on reducing this effect.

There are two restrictions on the analog input signals (VINP and VINN). First, if the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, then the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) protection turns on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.



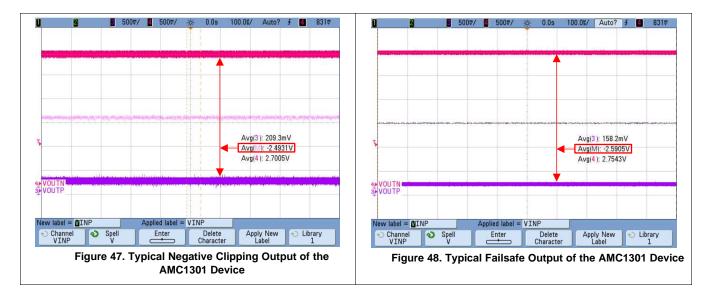
Feature Description (continued)

8.3.2 Fail-Safe Output

The AMC1301 device offers a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the AMC1301 device is missing, or
- When the common-mode input voltage, that is V_{CM} = (VINP + VINN) / 2, exceeds the minimum common-mode over-voltage detection level V_{CMov} of VDD1 2 V.

The fail-safe output of the AMC1301 device is a negative differential output voltage value that differs from the negative clipping output voltage, as shown in Figure 47 and Figure 48. As a reference value for the fail-safe detection on a system level, use the V_{FAILSAFE} maximum value of $-2.545 \, \text{V}$.



8.4 Device Functional Modes

The AMC1301 device is operational when the power supplies VDD1 and VDD2 are applied, as specified in *Recommended Operating Conditions*.



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The AMC1301 device offers unique linearity, high input common-mode and power-supply rejection, low ac and dc errors, and low temperature drift. These features make the AMC1301 device a robust, high-performance, isolated amplifier for industrial applications where high voltage isolation is required.

9.2 Typical Applications

9.2.1 Frequency Inverter Application

Isolated amplifiers are widely used in frequency inverters that are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, electrical and hybrid electrical vehicles, and other industrial applications. The input structure of the AMC1301 device is optimized for use with low-value shunt resistors and is therefore tailored for isolated current sensing using shunts.

Figure 49 shows a typical operation of the AMC1301 device for current sensing in a frequency inverter application. Phase current measurement is done through the shunt resistor, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the AMC1301 device ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive).

Additionally, the AMC1301 device may also be used for isolated voltage measurement of the dc-link, as described in *Isolated Voltage Sensing*.

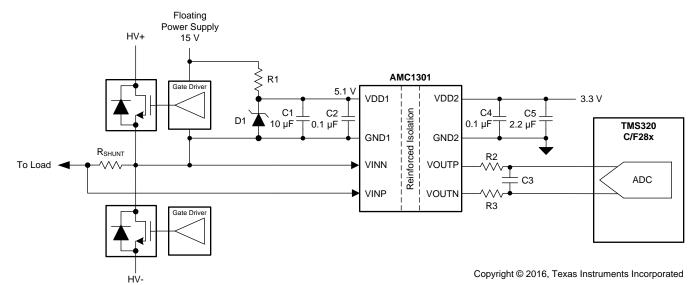


Figure 49. Using the AMC1301 Device for Current Sensing in Frequency Inverters



Typical Applications (continued)

9.2.1.1 Design Requirements

Table 1 lists the parameters for the typical application in Figure 49.

Table 1. Design Requirements

PARAMETER	VALUE			
High-side supply voltage	3.3 V or 5 V			
Low-side supply voltage	3.3 V or 5 V			
Voltage drop across the shunt for a linear response	± 250 mV (maximum)			

9.2.1.2 Detailed Design Procedure

The high-side power supply (VDD1) for the AMC1301 device is derived from the power supply of the upper gate driver. Further details are provided in the *Power Supply Recommendations* section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1301 device (VINN). If a four-pin shunt is used, the inputs of the AMC1301 device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: V_{SHUNT} ≤ ± 250 mV
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: V_{SHUNT} ≤ V_{Clipping}

For best performance, use an RC filter (components R_2 , R_3 , and C_3 in Figure 49) to minimize the noise of the differential output signal. Tailor the bandwidth of this RC filter to the bandwidth requirement of the system. TI recommends an NP0-type capacitor to be used for C_3 .

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, consult the TI Precision Designs 18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise (SLAU515) and 18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power (SLAU513), available for download at www.ti.com.

9.2.1.3 Application Curves

In frequency inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. Figure 50 shows the typical full-scale step response of the AMC1301 device. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.



Figure 50. Step Response of the AMC1301 Device

The high linearity and low temperature drift of offset and gain errors of the AMC1301 device, as shown in Figure 51, allows design of motor drives with low torque ripple.

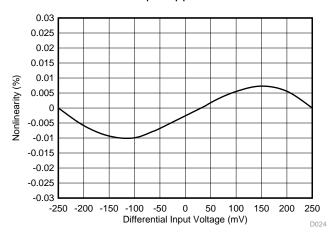


Figure 51. Typical Nonlinearity of the AMC1301 Device



9.2.2 Isolated Voltage Sensing

The AMC1301 device is optimized for usage in current-sensing applications using low-impedance shunts. However, the device may also be used in isolated voltage-sensing applications if the effect of the (usually higher) impedance of the resistor divider used in this case is considered.

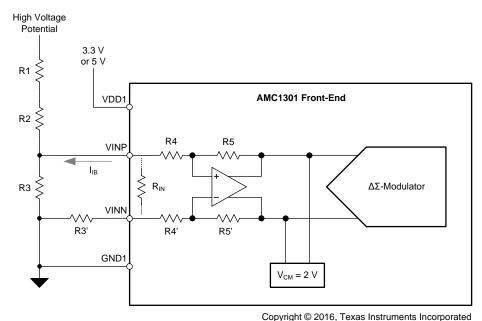


Figure 52. Using the AMC1301 Device for Isolated Voltage Sensing

9.2.2.1 Design Requirements

Figure 52 shows a simplified circuit typically used in high-voltage sensing applications. The high-impedance resistors (R1 and R2) dominate the current value that flows through the resistive divider. The resistance of the sensing resistor R3 is chosen to meet the input voltage range of the AMC1301 device. This resistor and the input impedance of the device (R_{IN} = 18 k Ω) also create a voltage divider that results in an additional gain error. With the assumption of R1 and R2 having a considerably higher value than R3 and omitting R3' for the moment, the resulting total gain error is estimated using Equation 1, with E_G being the initial gain error of the AMC1301 device.

$$\left|\mathsf{E}_{\mathsf{Gtot}}\right| = \left|\mathsf{E}_{\mathsf{G}}\right| + \frac{\mathsf{R}_{\mathsf{3}}}{\mathsf{R}_{\mathsf{IN}}} \tag{1}$$

This gain error may be easily minimized during the initial system-level gain calibration procedure.

9.2.2.2 Detailed Design Procedure

As indicated in Figure 52, the output of the integrated differential amplifier is internally biased to a common-mode voltage of 2 V. This voltage results in a bias current I_{IB} through the resistive network R4 and R5 (or R4' and R5') used for setting the gain of the amplifier. The value of this current is specified in the *Pin Configuration and Functions* section. This bias current generates additional offset and gain errors that depend on the value of the resistor R3. Because the value of this bias current depends on the actual common-mode amplitude of the input signal (as shown in Figure 53), the initial system offset calibration eliminates the offset but not the gain error component. Therefore, in systems with high accuracy requirements, a series resistor is recommended to be used at the negative input (VINN) of the AMC1301 device with a value equal to the shunt resistor R3 (that is, R3' = R3 in Figure 52) to eliminate the effect of the bias current.

This additional series resistor (R3') influences the gain error of the circuit. The effect is calculated using Equation 2 with R4 = R4' = 12.5 k Ω . The effect of the internal resistors R5 = R5' cancels in this calculation.

$$E_G(\%) = \left(1 - \frac{R4}{R4' + R3'}\right) * 100\% \tag{2}$$

9.2.2.3 Application Curve

Figure 53 shows the dependency of the input bias current on the common-mode voltage at the input of the AMC1301 device.

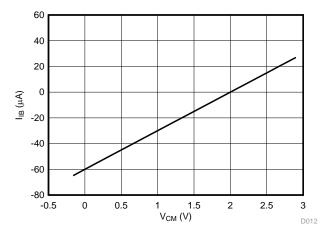


Figure 53. Input Current vs Input Common-Mode Voltage

9.3 Do's and Don'ts

Do not leave the inputs of the AMC1301 device unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives them to the output common-mode of the analog frontend of approximately 2 V. If the high-side supply voltage VDD1 is below 4 V, the internal common-mode overvoltage detector turns on and the output functions as described in the *Fail-Safe Output* section, which may lead to an undesired reaction on the system level.



10 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (VDD1) for the device is derived from the floating power supply of the upper gate driver. For lowest cost, a Zener diode may be used to limit the voltage to 5 V (or 3.3 V, depending on the design) \pm 10%. Alternatively a low-cost, low-dropout (LDO) regulator (for example, the LM317-N) may be used to minimize noise on the power supply. TI recommends a low-ESR decoupling capacitor of 0.1 μ F to filter this power-supply path. Place this capacitor (C₂ in Figure 54) as close as possible to the VDD1 pin of the AMC1301 device for best performance. If better filtering is required, an additional 10- μ F capacitor may be used. The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (VINN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, and GND1 is connected to one of the outer leads of the shunt.

To decouple the digital power supply on the controller side, use a 0.1-µF capacitor placed as close to the VDD2 pin of the AMC1301 device as possible, followed by an additional capacitor from 1 µF to 10 µF.

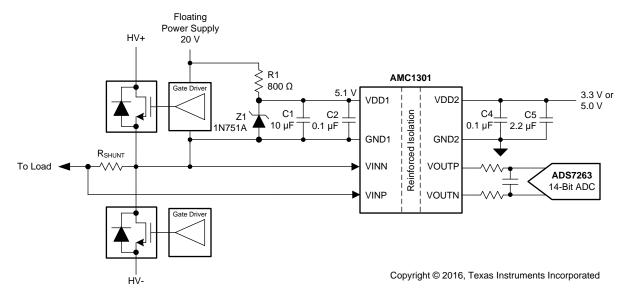


Figure 54. Zener-Diode-Based, High-Side Power Supply



11 Layout

11.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors (as close as possible to the AMC1301 device) and placement of the other components required by the device is shown in Figure 55. For best performance, place the shunt resistor close to the VINP and VINN inputs of the AMC1301 device and keep the layout of both connections symmetrical.

11.2 Layout Example

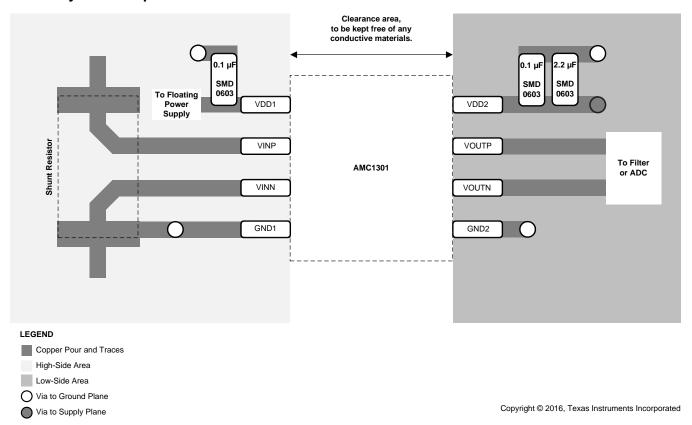


Figure 55. Recommended Layout of the AMC1301 Device



12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.1.2 Related Documentation

For related documentation, see the following:

- Isolation Glossary (SLLA353)
- Dual, 1MSPS, 16-/14-/12-Bit, 4x2 or 2x2 Channel, Simultaneous Sampling Analog-to-Digital Converter (SBAS523).
- LM117, LM317-N Wide Temperature Three-Pin Adjustable Regulator.
- ISO72x Digital Isolator Magnetic-Field Immunity (SLLA181)
- 18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise (SLAU515)
- 18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power (SLAU513)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — TI Glossarv.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGE OPTION ADDENDUM

9-Sep-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
AMC1301DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1301	Samples
AMC1301DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1301	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

9-Sep-2016

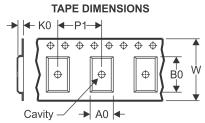
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PACKAGE MATERIALS INFORMATION

www.ti.com 9-Sep-2016

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1301DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 9-Sep-2016



*All dimensions are nominal

ĺ	Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
	AMC1301DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0	



SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOIC



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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