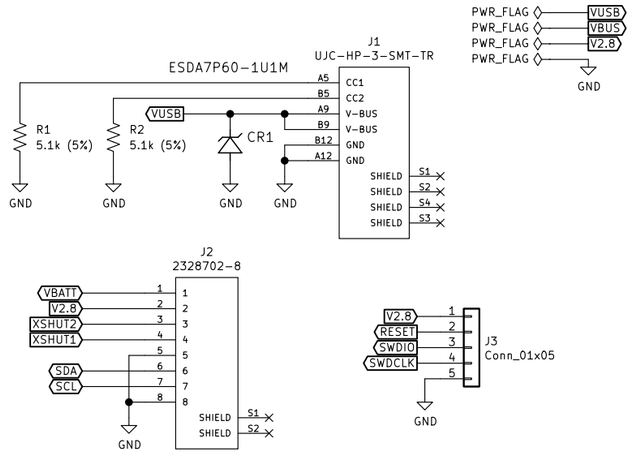
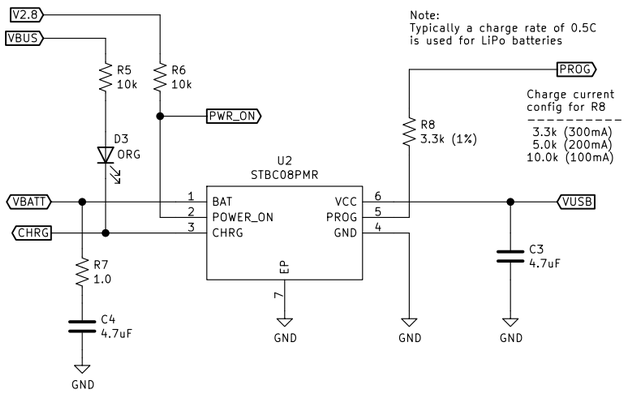
Headers



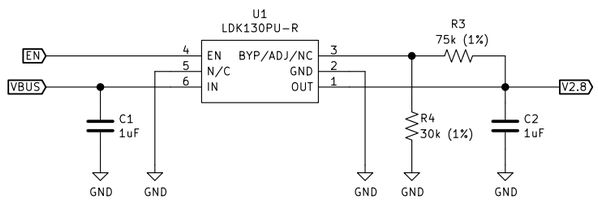
NOTES:
- R1 and R2 must be ±10% or less for power capability detection according to USB protocol
- CR1 is a transient voltage supression (TVS) diode for ESD protection

Charging circuit



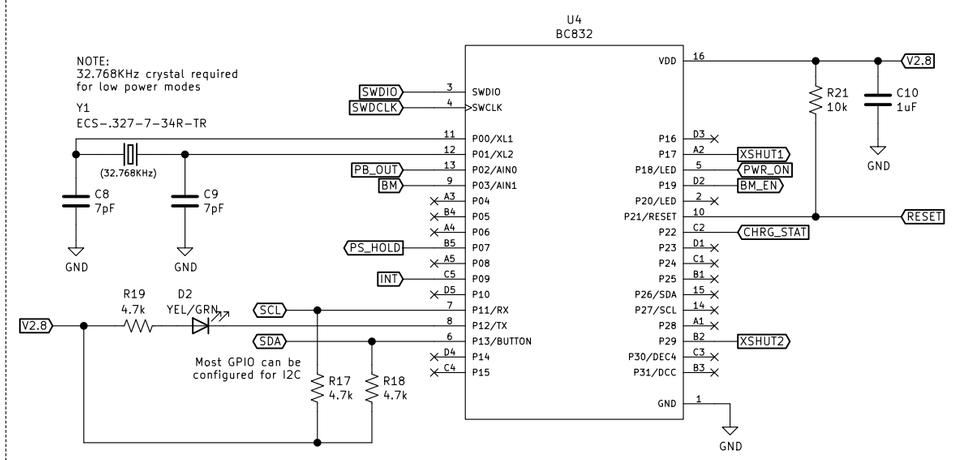
NOTES:
- Rprog = 1000 x (Vprog / Ibat). Vprog in constant current mode is 1.0 V
- Max output current availble is 800mA
- 300mA charge current selected to be well within trace width max current rating
- A 4.7 µF capacitor with a series resistor (0.2 Ω to 1.0 Ω) from BAT to GND is required to keep ripple voltage low when the battery is disconnected

Voltage regulator circuit



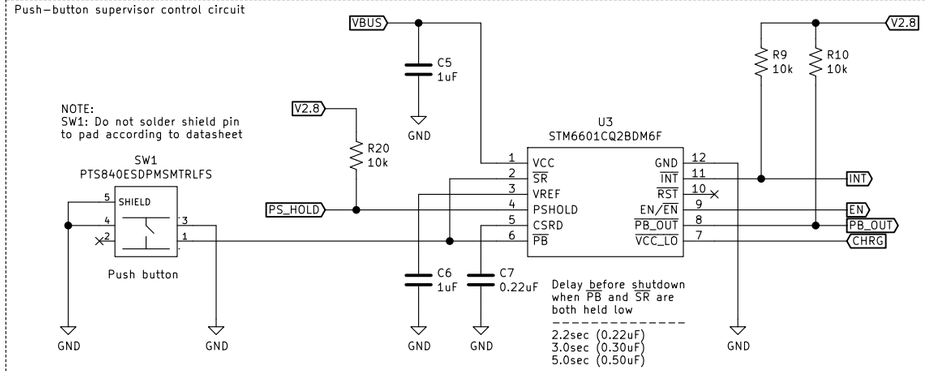
NOTES:
- Vout = Vadj (1 + R3 / R4)
- Rearrange to get R3 = R4(Vout/Vadj − 1)
- According to datasheet, Vadj = 800mV (±16mV)

Bluetooth cirucit



NOTES:
- Cap values for the XTAL are determined by the load capacitance specified by the oscillator datasheet.
- External pull−up resistors values can be found in I2C−bus specification.
  Pull−up are typically fitted only once per bus, near the host.
  Recommended values for pull−up resistors for an AVDD of 2.8V and 100KHz I2C clock is 4.7 kΩ.
  Recommended values for pull−up resistors for an AVDD of 2.8V and 400KHz I2C clock is 1.5 to 2 kΩ.
- BC832 RESET line requires an external pull−up resistor
- BC832 SWDIO line has an internal pull−up resistor (REF: 16.1 DAP − Debug Access Port)
- BC832 SWDCLK line has an internal pull−down resistor (REF: 16.1 DAP − Debug Access Port)

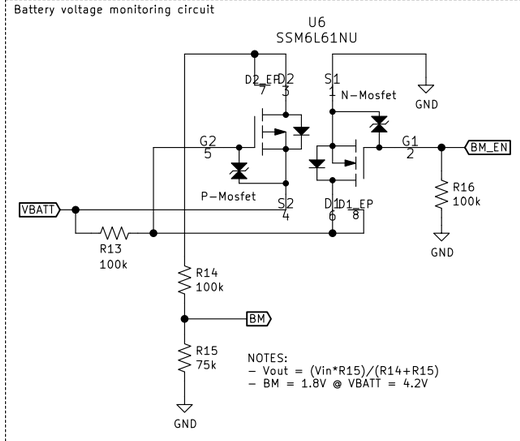
Push−button supervisor control circuit



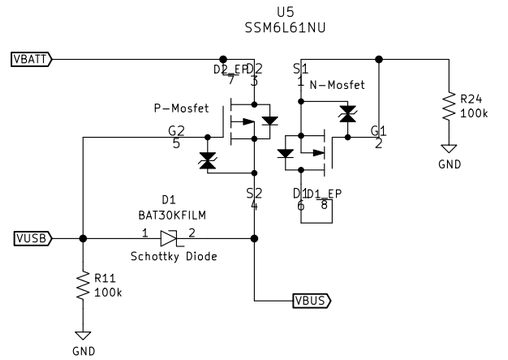
NOTES:
- CSRD cap sets the Smart Reset delay time at 10 s/uF. Recommended capacitor has a low ESR (e.g. ceramic)
- Has a fixed active high EN output, long push deasserts EN, internal pull−up on SR
- Has a fixed power−on lockout voltage at 3.30V and force shut−off at 3.10V
- RST not used with this configuration, active low and open drain, pull−up resistor added
- PS_HOLD driven low by internal 300kΩ resistor during startup, µC shall drive it high
- PB Has internal 100kΩ pull−up resistor
- SR Has internal 100kΩ pull−up resistor (optional order configuration)

NOTE:
- PS_HOLD pulled up to V2.8 to allow for production programming when chip is blank
- After programming, the firmware can pull the signal low to shutdown the LDO

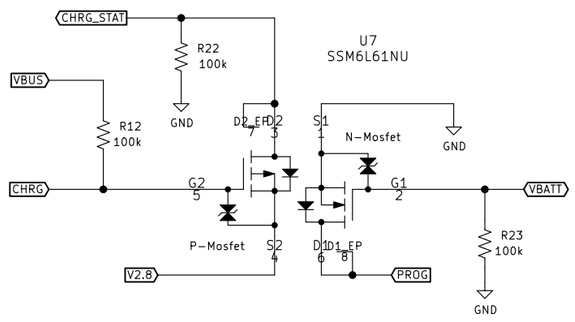
Battery voltage monitoring circuit



Load share circuit



STBC08 Charge status level shifter and enable circuit



Sheet: /		
File: CC_BT.sch		
Title: Plink Primary Board		
Size: A3	Date: 2023−01−23	**Rev: 5.0**
KiCad E.D.A. eeschema (5.1.9)−1		Id: 1/1