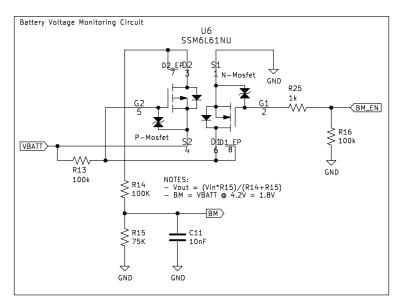


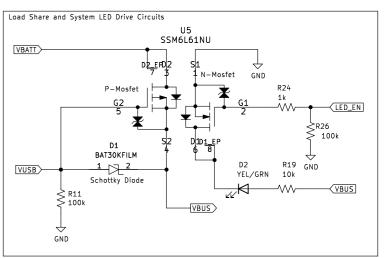
NOTES:
— CSRD cap sets the Smart Reset delay time at 10 s/uF. Recommended capacitor has a low ESR (e.g. ceramic)
— Has a fixed active high EN output, long push deasserts EN, internal pull—up on SR
— Has a fixed power—on lockout voltage at 3.30V and force shut—off at 3.10V
— RST not used with this configuration, active low and open drain, pull—up resistor added
— PS_HOLD driven low by internal $300k\Omega$ resistor during startup, μ C shall drive it high
— PB Has internal $100k\Omega$ pull—up resistor (optional order configuration)

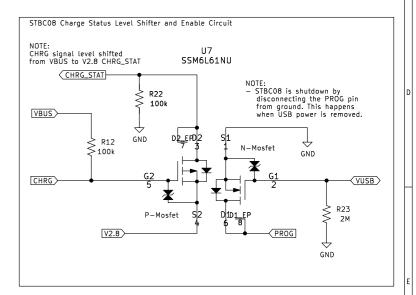
REF: nRF52832_PS_v1.1 - 16.1 DAP - Debug Access Port

SWDIO line has an internal pull-up resistor
 SWDCLK line has an internal pull-down resistor

production programming when chip is blank After programming, the firmware can pull the PS_HOLD low to shutdown the LDO







Designed by Andrew Green Sheet: / File: BT.kicad_sch Title: SIDFLC Size: A3 Date: KiCad E.D.A. eeschema 7.0.10-7.0.10~ubuntu22.04.1 Rev: V7.0 ld: 1/1