Headers

USB-C connector with only power pins available

ESDA7P60-1U1M

J1
UJC-HP-3-SMT-TR

R1 5.1k (5%)
R2 5.1k (5%)
CR1

VUSB

CC1
CC2
V-BUS
V-BUS
GND
GND
SHIELD S1
SHIELD S2
SHIELD S4
SHIELD S3

A5 B5 A9 B9 B12 A12

PWR_FLAG — VUSB
PWR_FLAG — VBUS
PWR_FLAG — V2.8
PWR_FLAG — GND

GND GND GND GND

Interface port
J2 2328702-8

VBATT 1
V2.8 2
XSHUT1 3
XSHUT2 4
5
SDA 6
SCL 7
8
SHIELD S1
SHIELD S2

GND

SWD Program Port

V2.8 1
RESET 2
SWDCLK 3
SWDIO 4
5

J3 Conn_01x05

GND

NOTES:
– R1 and R2 must be ±10% or less for power capability detection according to USB protocol
– CR1 is a transient voltage supression (TVS) diode for ESD protection

Charging circuit

V2.8
VBUS

R5 10k
R6 10k
PWR_ON

D3 ORG

R8 10k (1%)

PROG

Charge current config for Rprog
———————————
3.3k (300mA)
5.0k (200mA)
10.0k (100mA)

U2 STBC08PMR

1 BAT   VCC 6
2 POWER_ON   PROG 5
3 CHRG   GND 4
EP 7

VBATT
CHRG

C4 4.7uF
C3 4.7uF
VUSB

GND GND GND GND

Note:
Typically a charge rate of 0.5C is used for 3.7V LiPo batteries

NOTES:
– Rprog = 1000 x (Vprog / Ibat). Vprog in constant current mode is 1.0 V
– Disconnecting the PROG pin from ground can be used to shutdown the IC

Voltage regulator circuit

U1 LDK130PU-R

EN 4
VBUS 6 IN
N/C 5

BYP/ADJ/NC 3
OUT 1

R3 75k (1%)

C1 1uF
R4 30k (1%)
C2 1uF

V2.8

GND GND GND GND GND

NOTES:
– Vout = Vadj (1 + R3 / R4)
– Rearrange to get R3 = R4(Vout/Vadj − 1)
– According to datasheet, Vadj = 800mV (±16mV)

Bluetooth circuit

NOTE:
– 32.768KHz crystal required for low power modes

Y1 ECS-.327-CDX-2216
(32.768KHz)

C8 7pF
C9 7pF

SWDIO 4 SWCLK
SWDCLK 5 SWDIO

VCC 25

U4 BMD-350-A-R

24 P0.00/XL1   P0.31/AIN7 30
23 P0.01/XL2   P0.30/AIN6 29
28 P0.02/AIN0   P0.29/AIN5 31
44 P0.03/AIN1   P0.28/AIN4 45   BM_EN
27 P0.04/AIN2   P0.27 32   LED_EN
21 P0.05/AIN3   P0.26 34
19 P0.06   P0.25 33
22 P0.07   P0.24 35
16 P0.08   P0.23 36
   P0.09/NFC1   P0.22 41
   P0.10/NFC2   P0.21/RESET 7   CHRG_STAT
18 P0.11   P0.20/TRACECLK
   P0.12   P0.19 42   RESET
12 P0.13   P0.18/TRACED[0] 43
14 P0.14/TRACED[3] P0.17 10
11 P0.15/TRACED[2] P0.16/TRACED[1] 9

PB_OUT
INT
PS_HOLD
SCL
SDA
BM
XSHUT1
XSHUT2
PWR_ON

R17 4.7k
R18 4.7k
V2.8

GND

R21 10k
C10 1uF
C12 10nF
C13 100nF

V2.8

GND GND GND

GND

Most GPIO can be configured for I2C

NOTE:
– P30 and P31 are wired for DCDC a converter and cannot be used as regular GPIO
– P0.09 are P0.10 are NFC pins but can be configured in software as GPIO

NOTES:
– Cap values for the XTAL are determined by the load capacitance specified by the oscillator datasheet.
– External pull-up resistors values can be found in I2C-bus specification.
– Pull-up are typically fitted only once per bus, near the host.
  Recommended values for pull-up resistors for an AVDD of 2.8V and 100KHz I2C clock is 4.7 kΩ.
  Recommended values for pull-up resistors for an AVDD of 2.8V and 400KHz I2C clock is 1.5 to 2 kΩ.
– BC832 RESET line requires an external pull-up resistor
– BC832 SWDIO line has an internal pull-up resistor (REF: 16.1 DAP – Debug Access Port)
– BC832 SWDCLK line has an internal pull-down resistor (REF: 16.1 DAP – Debug Access Port)

Push-button supervisor control circuit

NOTE:
– Do not solder shield pin to pad according to datasheet

VBUS
C5 1uF
GND

V2.8
R20 10k

SW1 PTS840ESDPMSMTRLFS
SHIELD
Push button

PS_HOLD

U3 STM6601CQ2BDM6F

1 VCC   GND 12
2 SR   INT 11
3 VREF   RST 10
4 PSHOLD   EN/EN 9
5 CSRD   PB_OUT 8
6 PB   VCC_LO 7

R9 10k
R10 10k
V2.8

INT
EN
PB_OUT

C6 1uF
C7 0.22uF

GND GND

GND

Delay before shutdown when PB and SR are both held low
———————————
2.2sec (0.22uF)
3.0sec (0.30uF)
5.0sec (0.50uF)

NOTES:
– CSRD cap sets the Smart Reset delay time at 10 s/uF. Recommended capacitor has a low ESR (e.g. ceramic)
– Has a fixed active high EN output, long push deasserts EN, internal pull-up on SR
– Has a fixed power-on lockout voltage at 3.30V and force shut-off at 3.10V
– RST not used with this configuration, active low and open drain, pull-up resistor added
– PS_HOLD driven low by internal 300kΩ resistor during startup, µC shall drive it high
– PB Has internal 100kΩ pull-up resistor
– SR Has internal 100kΩ pull-up resistor (optional order configuration)

NOTE:
– PS_HOLD pulled up to V2.8 to allow for production programming when chip is blank
– After programming, the firmware can pull the PS_HOLD low to shutdown the LDO

Battery voltage monitoring circuit

U6 SSM6L61NU

D2 EP D2
S1 N-Mosfet
G2
P-Mosfet
S2
D1 D1 EP
G1

R25 1k
BM_EN

VBATT
R13 100k

R14 4M
R15 3M

R16 100k
GND

BM
C11 10nF

GND GND GND

NOTES:
– Vout = (Vin*R15)/(R14+R15)
– BM = 1.8V @ VBATT = 4.2V

Load Share and System LED drive circuits

U5 SSM6L61NU

VBATT

D2 EP D2
S1 N-Mosfet
G2
P-Mosfet
S2
D1 D1 EP
G1

GND

R24 1k
LED_EN

R26 100k

D1 BAT30KFILM
Schottky Diode

VUSB

R11 100k

D2 YEL/GRN
R19 10k

GND
VBUS
VBUS

STBC08 Charge Status level shifter and Enable circuit

U7 SSM6L61NU

CHRG_STAT
R22 100k

D2 EP D2
S1 N-Mosfet
G2
P-Mosfet
S2
D1 D1 EP
G1

GND

VBUS
R12 100k

CHRG

V2.8
R23 2M

VUSB

PROG

GND

NOTE:
– STBC08 is shutdown by disconnecting the PROG pin from ground. This happens when USB power is removed.

NOTE:
CHRG signal level shifted from VBUS to V2.8

Designed by Andrew Green

Sheet: /
File: BT.kicad_sch
Title: SIDFLC
Size: A3   Date:
KiCad E.D.A. eeschema 7.0.8-7.0.8-ubuntu22.04.1
Rev: V6.0
Id: 1/1