

[illegible]

VIN
 INPUT FILTER
 C5 0.1uF
 C6 1uF
 C8 10uF 1206
 GNDIN
 GNDIN
 GNDIN
 D4 1N5408
 DROP DIODE
 DO-15
 7.2V MAX
 C11 22uF 1206
 C12 0.1uF
 GND2
 GNDIN
 VSERVO
 ALTERNATE PART
 S3JBHR5G
 SMB

[illegible]

The diagram shows a circuit for a 5V regulator. A green line labeled 'VBOOST' enters from the left and connects to the gate of a MOSFET switch labeled 'SW1 L102021ML04Q'. The MOSFET is shown in a simplified schematic with terminals 1, 2, and 3. Terminal 1 is connected to the 5V supply, terminal 2 is connected to the output, and terminal 3 is connected to the VBOOST line. A current of '> 3A' is indicated near the MOSFET. The output of the MOSFET is connected to a 5V supply and a capacitor labeled 'C19 22uF 1206'. The capacitor is connected to ground, which is labeled 'GND' and 'BUS CAP'.

BATTERY CHARGER

MUST BE 5V

The diagram shows a battery charger circuit for a 5V battery (VBAT). The input is VCHG (5V), which is connected to the VDD pin (pin 4) of the MCP73831-2-OT IC (U1). A 1μF capacitor (C1) is connected between VCHG and GND. The IC is also connected to GND at pins 2 (VSS) and 3 (VBAT). The PROG pin (pin 5) is connected to GND through a 10k resistor (R1), labeled "100mA CHARGE CURRENT". The STAT pin (pin 1) is connected to GND through a 1k resistor (R3), labeled "CHARGING". The CHARGE DONE pin (pin 6) is connected to GND through a 1k resistor (R4), labeled "CHARGE DONE". Two LEDs, D1 (ORANGE, 0805) and D2 (GREEN, 0805), are connected in series between the CHARGING and CHARGE DONE pins. A 10μF capacitor (C3) is connected between VBAT and GND.

1 A

D3
MBRM120

CHECK FOOTPRINT

VLV

C7
1uF

GNDBAT

R7
100k

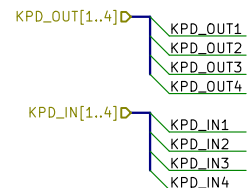
PULLDOWN TO
ENABLE PFET

GNDBAT

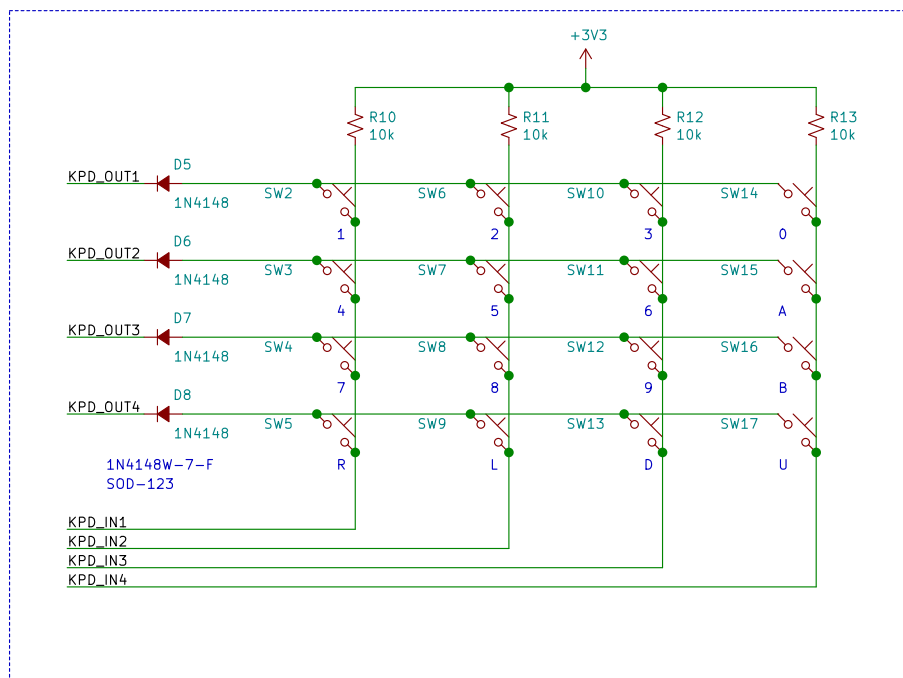
Q2
DMP1045U

3 2

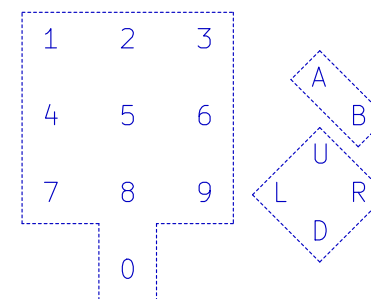
The schematic diagram illustrates a 5V regulator circuit with an active low bypass during charging. The input voltage (VLV) is connected to the VIN pin of the MCP1642D-50 regulator (U2) through a 4.7uF capacitor (C2). The regulator's EN pin is connected to the emitter of a BS5138 PNP transistor (Q1) through a 100 ohm resistor (R2). The transistor's base is connected to the output of the regulator (VOUT) through a 10k resistor (R6). The transistor's collector is connected to the input of the regulator (VIN) through a 100k resistor (R5). The regulator's VOUT pin is connected to the load (VB00ST) through a 10uF capacitor (C4). The bypass current limit is set to 800 mA.



KEYPAD



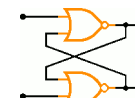
KEYPAD LAYOUT



BUTTONS PTS645 S K 50 SMTR92 LFS
6mm SMT

CAP COLOR
NUMERIC BLACK
A, B RED
D-PAD BLUE

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File: keypad.sch

PANDORA

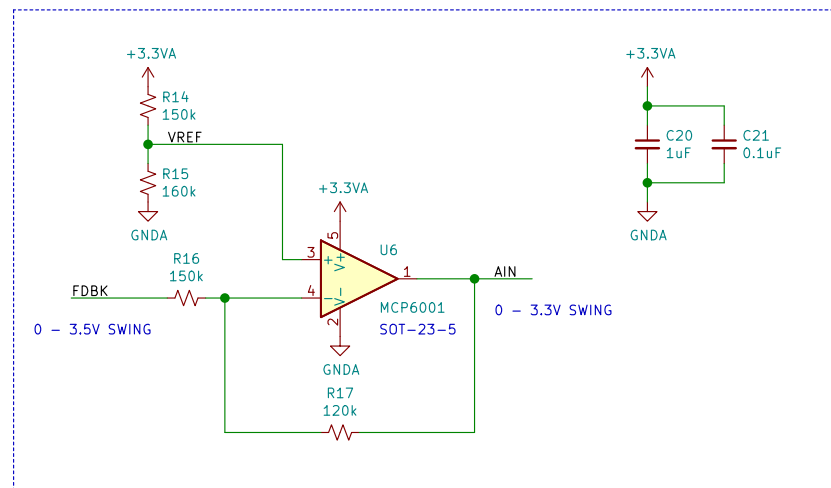
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Size: A4 Date: 2020-02-09
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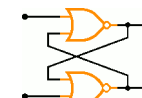
Rev: A
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FDBK  FDBK
AIN  AIN

SERVO FEEDBACK SCALE



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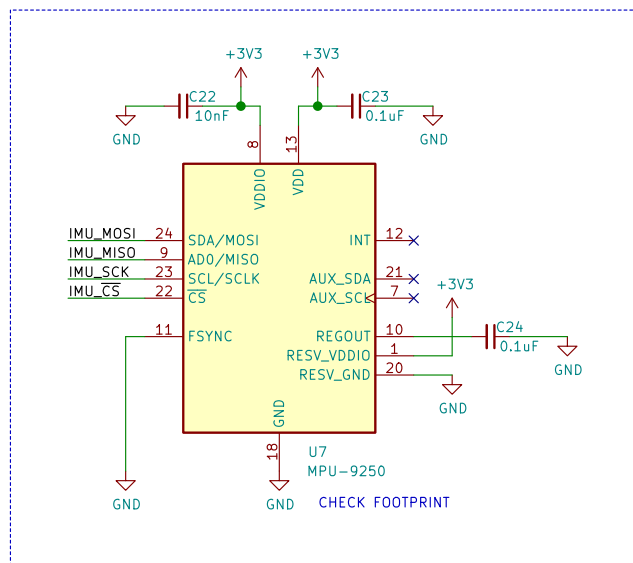
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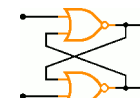
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IMU_SCKD IMU_SCK
 IMU_MOSID IMU_MOSI
 IMU_MISOD IMU_MISO
 IMU_CSD IMU_CS

IMU



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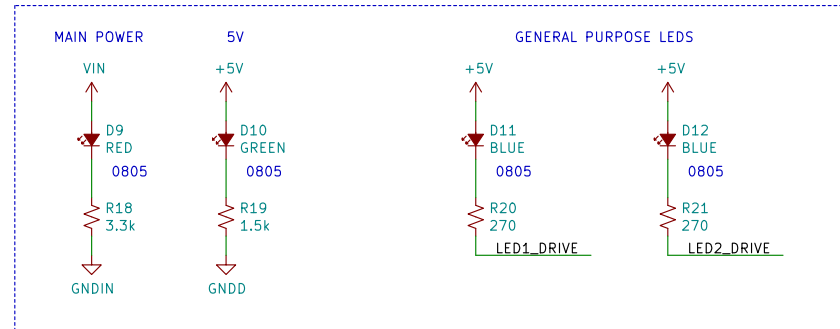
LCD_BLRD_____LCD_BLR
LCD_BLGD_____LCD_BLG
LCD_BLBD_____LCD_BLB

LCD_OUT_BLRD_____LCD_OUT_BLR
LCD_OUT_BLGD_____LCD_OUT_BLG
LCD_OUT_BLBD_____LCD_OUT_BLB

LED1_____LED1
LED2_____LED2

SPEAKERD_____SPK

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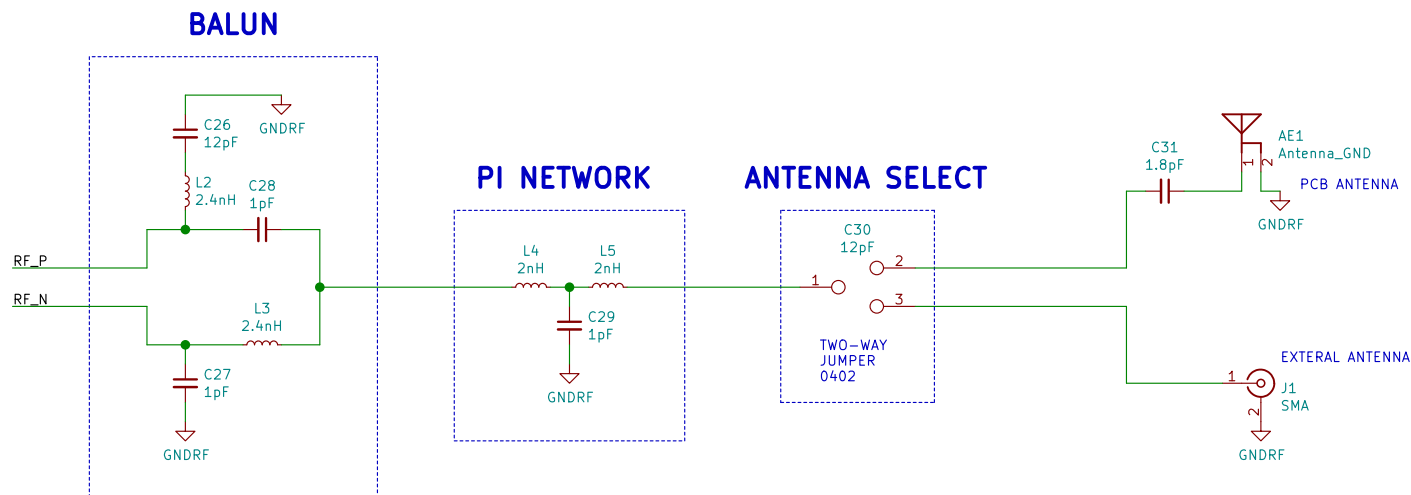
[illegible]

The diagram shows a 2-to-1 multiplexer implemented with two 3-input OR gates and two 2-input AND gates. Two input lines (A and B) are connected to the inputs of the two 2-input AND gates. The output of the top AND gate is connected to the top input of the top 3-input OR gate. The output of the bottom AND gate is connected to the bottom input of the top 3-input OR gate. The output of the top 3-input OR gate is the final output of the multiplexer.

PANDORA

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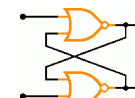
RF_PD RF_P
RF_ND RF_N



BASED ON LAUNCHXL-CC26X2R1 DESIGN
MODIFY APPROPRIATELY

ALL PASSIVES 0402 UNLESS OTHERWISE NOTED

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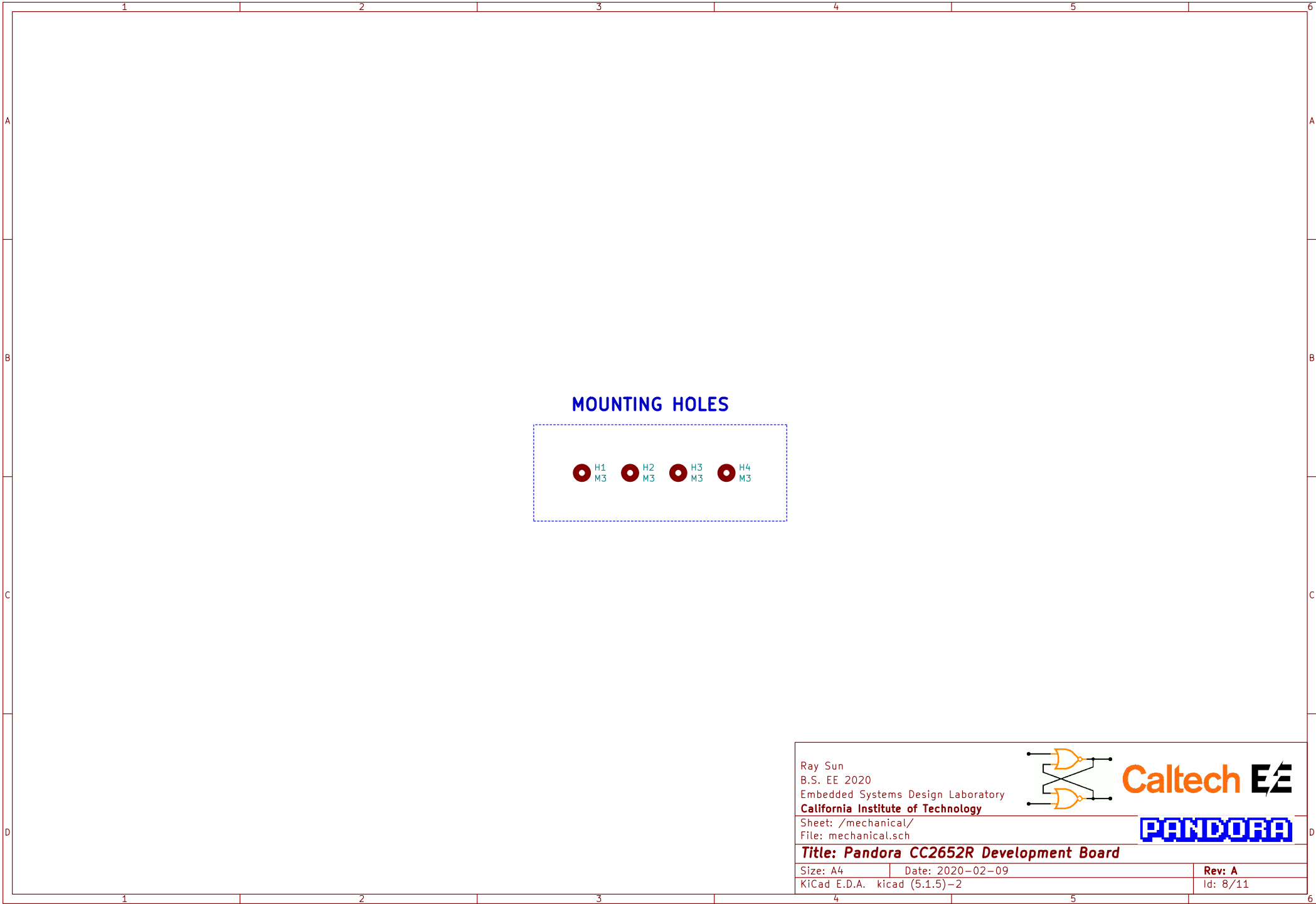
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MOUNTING HOLES

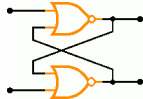
H1
M3

H2
M3

H3
M3

H4
M3

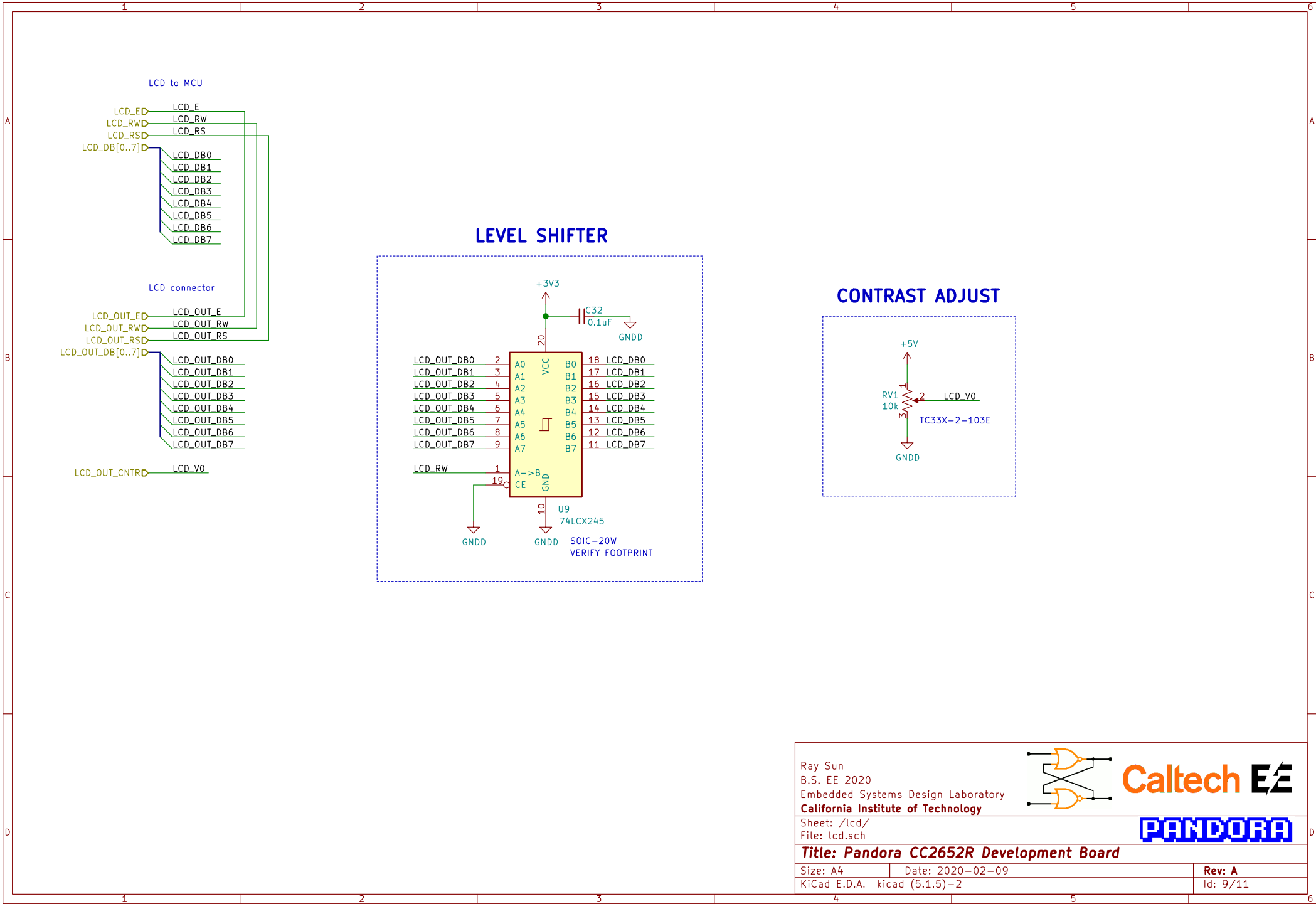
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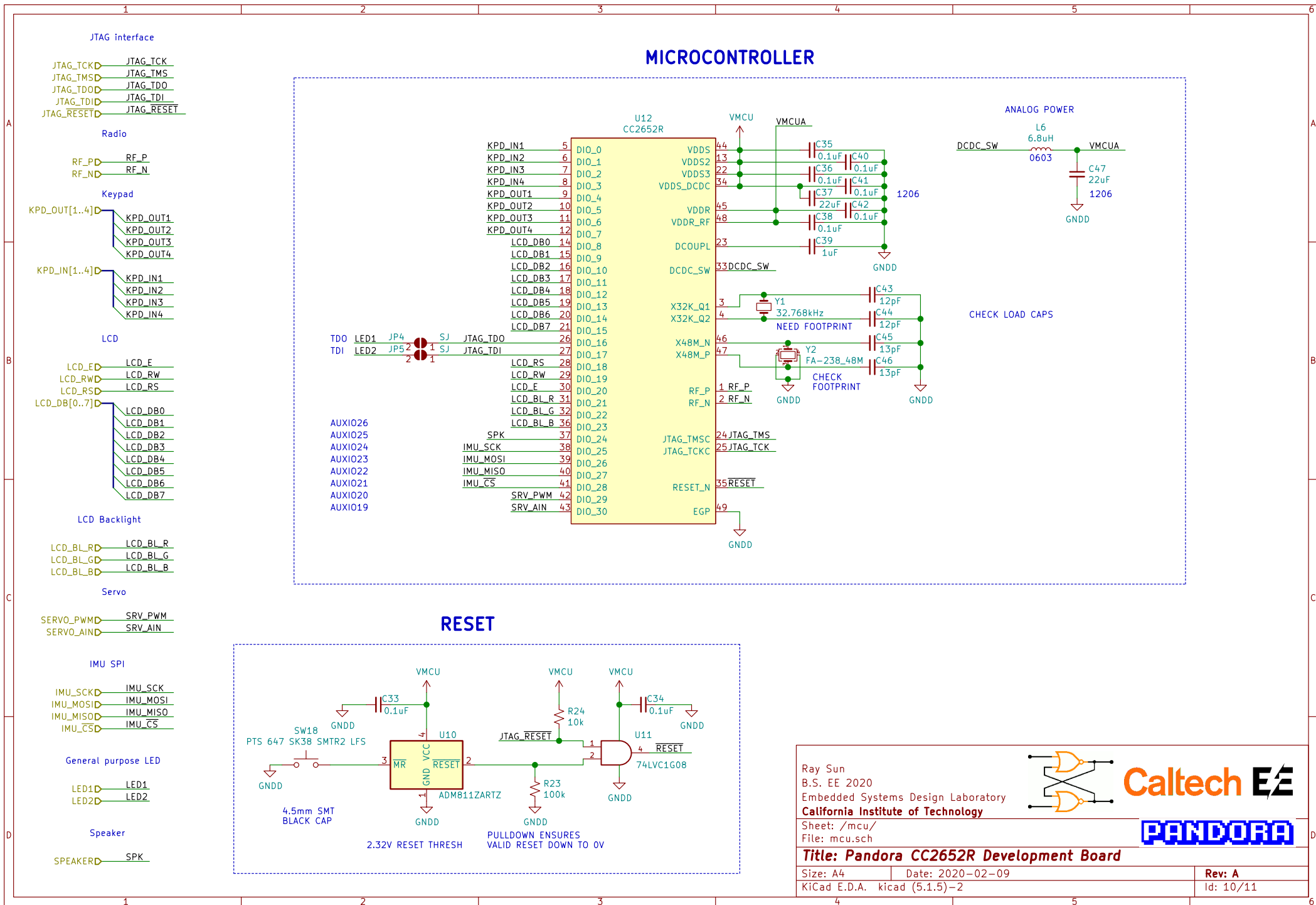


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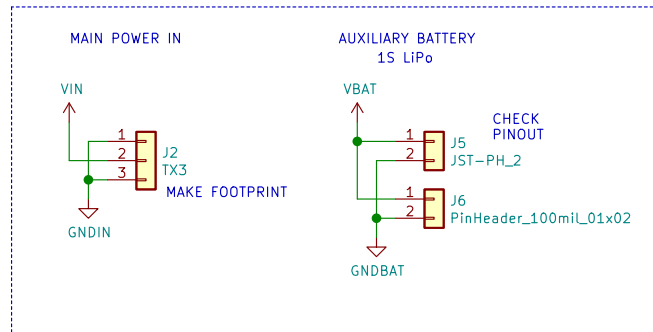
PANDORA

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KiCad E.D.A. kicad (5.1.5)-2		Id: 8/11

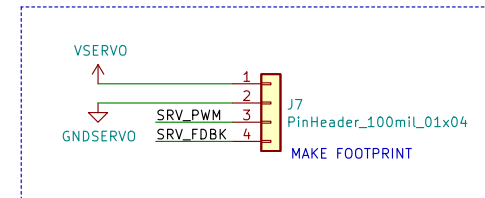




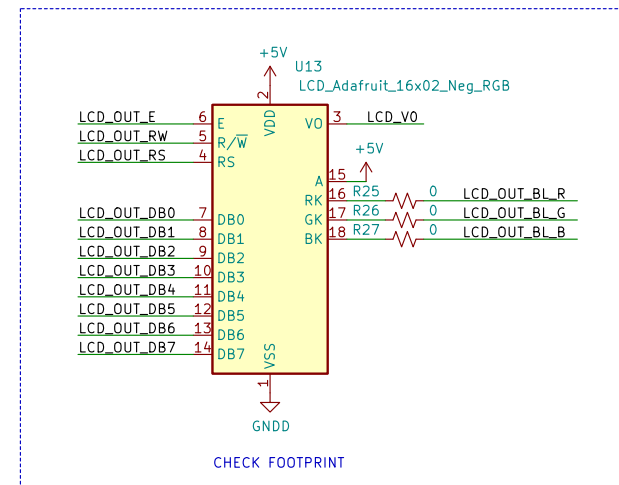
POWER



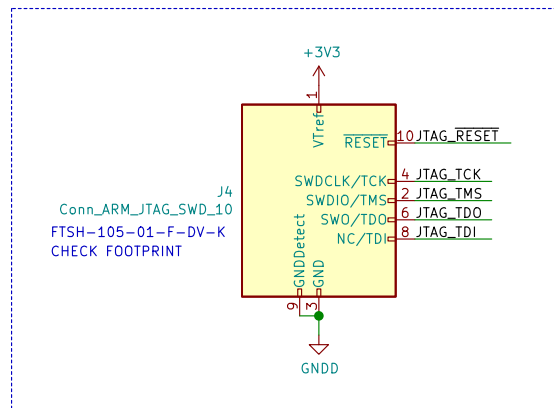
SERVO



LCD



JTAG



AUXILIARY BATTERY CHARGE

