Data Link Connector (OBD-II, SAE J1962)

CN1 — OBD-II
Jumper — J1 — GS

Ground selector:
- chassis (OBD4), default,
- signal (OBD5).

Power supply

IC1 LM2576S-5.0
VIN FBACK
EN GND VO
C1 0.1uF
C2 100uF
L1 100uH
D5 SS34
C3 100uF

Status LEDs

R1 1k RED D1 RX_LED
R2 1k YELLOW D2 TX_LED
R3 27k GREEN D3
R4 5k BLUE D4 ACT_LED

CCD-bus interface (UART mode)

U3 CDP68HC68S1
R5 10, R6 10
R9 120, R10 13k, R11 13k
R7 10k, R8 10k
C4 0.1uF
J3 ST2A, J4 ST2B
ST1A, ST1B
interrupt pin pullup resistors
Jumper selectable CCD-bus bias for standalone operation

Power switch (ON/OFF)

POWER
S1
OBD16
Mounting holes

USB / UART Bridge + Micro-B USB connector

U2 CP2102
C5 1uF, C7 0.1uF, C6 0.1uF
R12 10k, R13 10k
C8 0.1uF
R14 22k, R15 47k
D7 SS34
U7 USBLC6-2SC6
CN2 USB
~4.8V

Reset circuit (ATmega2560)

S2 RESET
R16 10k
D6 1N4148
RST0

SCI-BUS_A/B_ENGINE interface (UART)

data direction -->
U4A 74HC4066 SCI-RX (conf. A)
U4C 74HC4066 SCI-TX (conf. A)
U4B 74HC4066 SCI-RX (conf. B)
U4D 74HC4066 SCI-TX (conf. B)
U4P C17 0.1uF R17 1k C18 470pF
SCI-TX bias. Required by the design of the SCI-bus.
Pull PA# lines low to disable, high to enable data flow.

Crystal oscillator circuit (ATmega2560)

C9 22pF, C10 22pF
Q1 16MHz
XTAL1, XTAL2

ATmega2560-16AU microcontroller

U1 ATMEGA2560-16AU
AVCC 100
VCC_2 31, VCC_3 10, VCC_4 61, VCC 80
RST0 30 RESET
XTAL1 34, XTAL2 33
AREF 98, C16 0.1uF
C12 C13 C14 C15 0.1uF

PA0_(AD0) 78 ... PA7_(AD7) 71
PF0_(ADC0) 97 ... PF7_(ADC7/TDI) 90
PG0_(WR) 51 ... PG5 (OC0B) 1
PB0 (SS/PCINT0) 19 ... PB7 26
PH0 (RXD2) 12 ... PH7 (T4) 27
PC0_(A8) 53 ... PC7_(A15) 60
PJ0_(RXD3/PCINT9) 63 ... PJ7 69
PD0 (SCL/INT0) 43 ... PD7 (T0) 50
PK0_(ADC8/PCINT16) 89 ... PK7 82
PE0 (RXD0/PCINT8) 2 ... PE7 9
PL0 (ICP4) 35 ... PL7 42
GND_2 11, GND_3 62, GND_4 32, GND_5 81, GND 99

SCI-BUS_A/B_TRANSMISSION interface (UART)

data direction -->
U5A 74HC4066 SCI-RX (conf. A)
U5C 74HC4066 SCI-TX (conf. A)
U5B 74HC4066 SCI-RX (conf. B)
U5D 74HC4066 SCI-TX (conf. B)
U5P C19 0.1uF R18 1k C20 470pF
SCI-TX bias. Required by the design of the SCI-bus.
Pull PA# lines low to disable, high to enable data flow.

ISP-10 programming port (ATmega2560)

J2 ISP-10
MOSI, NC, RST0, MISO
VCC, GND1, GND2, GND3, GND4

Misc. connectors

J5 I2C SCL, SDA, SHIELD
J6 +5V

SCI-bus configuration selector

Configuration A:
- PA0: high
- PA1: high
- PA2: high
- PA3: high
- PA4: low
- PA5: low
- PA6: low
- PA7: low

Configuration B:
- PA0: low
- PA1: low
- PA2: low
- PA3: low
- PA4: high
- PA5: high
- PA6: high
- PA7: high

Battery voltage sensor

R19 12k
R20 5k
BATT
A voltage divider scales down 12V below 5V for an analog input pin.

External EEPROM (4kB)

U6 24LC32A EEPROM Array
R21 10k
R22 4k7, R23 4k7
C21 0.1uF
WP, A2, A1, A0, VCC, SDA, SCL, GND

ADC lowpass filter

C11 0.1uF
L2 10uH
AVCC

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