d i g i t a l

PDP-8/I
Options

TRAINING DRAWINGS

Volume II

VOLUME II

TRAINING DRAWINGS

OPTIONS
PDP-8/I

CONTENTS

F

E

MUY

DVI

T1   MA + 1 → PC   MA + 1 → PC

[SC≠0 OR 1]•[MQ10=MQ11]

[SC=0 OR 1]+[MQ10≠MQ11]

T2

MEM → MB

MEM → IR

MEM → MB

MQ11(0)   MQ11(1)

MEM ADD TO AC

MEM ADD TO AC   MEM ADD TO AC

MBO4(0)•MBO5(0)•MBO6(0)•MBO7(0)   AC → AC

MBO4(0)•MBO5(1)   AC + MQ → AC

MBO4(0)•MBO6(1)   AC + SC → AC

MBO4(1)•MBO5(0)•MBO6(0) + MBO7(1)   0 → AC

MBO4(1)•MBO5(1)   MQ → AC

MBO4(1)•MBO6(1)   SC → AC

SCL + ASR + LSR + SHL   MUY + DVI

MB7-11 → SC   0 → SC

L , AC & MB SHIFT RIGHT

[SC=0•L(1)]

[SC≠0 + L(0)]

0 → EAE ON

MQ ROTATE LEFT

EAE END

SC=12   SC≠12

L & AC ROTATE LEFT

T3

MBO7(1)   AC → MQ

MB8-10 → EAE IR

MUY + DVI + ASR + LSR   MUY + DVI + ASR + LSR

0 → L

NMI   N̄M̄Ī

0 → SC

NORM   N̄Ō̄R̄M̄

1 → PAUSE

1 → EAE ON

SCL   S̄C̄L̄

1 → PAUSE

1 → EAE ON

SC=11   SC≠11

0 → EAE ON   + 1 → SC

EAE END

+ 1 → SC

SC=13   SC≠13

MQ10(0)   MQ10(0)   MQ10(1)   MQ10(1)

MQ11(0)   MQ11(1)   MQ11(0)   MQ11(1)

MEM ADD → AC   AC → AC   MEM ADD → ĀC̄   ĀC̄ → AC

0 → EAE ON

EAE END

T4

MUY + DVI + ASR + LSR + SHL + SCL   MUY + DVI + ASR + LSR + SHL + SCL

BRK REQ   B̄R̄K̄ R̄Ē̄Q̄

DATA   PROGRAM

PC → MA   DATA ADD → MA   0 → MA   PC → MA

1 CYCLE   3 CYCLE   JMS → IR

1 → E   1 → B   1 → WC   1 → E   1 → F

PROGRAM   DATA

BRK REQ   B̄R̄K̄ R̄Ē̄Q̄

0 → MA   DATA ADD → MA   PC → MA

JMS → IR   1 CYCLE   3 CYCLE

1 → E   1 → B   1 → WC   1 → F

ASR   L → 0 AC → MQ → LOST

LSR   L → AC → MQ → LOST   0

SHL AND NMI   LOST ← L ← AC ← MQ ← 0

MUY   0 → L → AC → MQ → LOST

DVI   L → AC → MQ → INVERT

D-BS-KE8I-0-2 EAE Control

II-2

D-BS-KE8I-0-3 Multiplier Quotient and Step Counter

FREQUENCY SOURCE
J3Ø
M4Ø1 OR M4Ø5 OR M5Ø1

M4Ø1 VARIABLE CLOCK

+3V   K2
J2
CLOCK ENABLE

M4Ø1
CAP
COMM   INT CAP   (+) OUTPUT
D2
N2 R2 T2
S2 P2

CLOCK

M4Ø5 CRYSTAL CLOCK

CRYSTAL CLOCK   (+) OUTPUT
D2

CLOCK TRANSFORMER
(DEC 16-5570)

AUTO TAP AT FAN

115V AC   6.3V AC
50 OR 60∿

M5Ø1 SCHMITT TRIGGER TO LINE FREQUENCY

R2
C2
SCHMITT TRIGGER   (-) OUTPUT
F2

CLOCK CONTROL
M7Ø8
H3Ø

D2
MB3 (Ø)   T2
MB4 (Ø)   S2
MB5 (1)   R2
MB6 (Ø)   P2
MB7 (1)   N2
MB8 (1)   M2
MB9 (Ø)   N1
MB9 (1)   U2
MB1Ø (1)   L1
MB11 (1)   A1
IOP1 (Ø)   L2
IOP2 (Ø)   R1
INITIALIZE   P1
IOP4 (Ø)   F2

S1   V2   K2   V1

H1   → I/O BUS IN SKIP
C1   → I/O BUS IN INT
J2   → CLOCK ENABLE (TO FREQUENCY SOURCE)
D1   → FLAG T.P.
E1   → INTERRUPT ENABLE T.P.
K1   → FLAG BUFFER T.P.

NOTE
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH (H)
LEVELS PER DEC STD 054

CLOCK ICT   LOAD COUNTER   CLOCK P4   OVERFLOW

CLOCK COUNTER
M7Ø9
HJ31

JL1   JN1   JK1   JS1
JJ2
JP1
JJ1

MB1Ø (Ø)   JP1
MB1Ø (1)   JJ1

AC0Ø (1)   HE1
AC01 (1)   JA1
AC02 (1)   HV1
AC03 (1)   HH1
AC04 (1)   HU2
AC05 (1)   HK1
AC06 (1)   HT2
AC07 (1)   HL1
AC08 (1)   HR1
AC09 (1)   HN2
AC1Ø (1)   HR2
AC11 (1)   HP1

HF2   → I/O BUS IN ØØ
JD1   → I/O BUS IN Ø1
HF1   → I/O BUS IN Ø2
JB1   → I/O BUS IN Ø4
HU2   → I/O BUS IN Ø3
HU1   → I/O BUS IN Ø5
HJ1   → I/O BUS IN Ø6
HV2   → I/O BUS IN Ø7
HM1   → I/O BUS IN Ø8
HP2   → I/O BUS IN Ø9
HM2   → I/O BUS IN 1Ø
HS1   → I/O BUS IN 11

JF1   → CLOCK TO COUNTER T.P.
JH1   → SET COUNTER T.P.
HE2   → TRANSFER T.P.
JR1   → READ 0-5 T.P.
JM1   → READ 6-11 T.P.
JH2   → GATE (1) T.P.
JM2   → CLOCK AC CLR

THE FOLLOWING CONFIGURATIONS OF THE REAL TIME CLOCK OPTION ARE POSSIBLE:

OPTION TYPE	DESCRIPTION	MODULES	LOCATION
KW8IA	LINE FREQUENCY INTERRUPT	M7Ø8	H3Ø
		M5Ø1	J3Ø
		CLOCK TRANSFORMER	FAN BRACKET✳
KW8IB	VARIABLE CLOCK INTERRUPT	M7Ø8	H3Ø
		M4Ø1	J3Ø
KW8IC	CRYSTAL CLOCK INTERRUPT	M7Ø8	H3Ø
		M4Ø5	J3Ø
KW8ID	KW8IA WITH PRESET AND READOUT	M7Ø8	H3Ø
		M7Ø9	HJ31
		M5Ø1	J3Ø
		CLOCK TRANSFORMER	FAN BRACKET✳
KW8IE	KW8IB WITH PRESET AND READOUT	M7Ø8	H3Ø
		M7Ø9	HJ31
		M4Ø1	J3Ø
KW8IF	KW8IC WITH PRESET AND READOUT	M7Ø8	H3Ø
		M7Ø9	HJ31
		M4Ø5	J3Ø

✳ MTG & WIRING INFORMATION ON PRINT #D-UA-KW8I-Ø-Ø
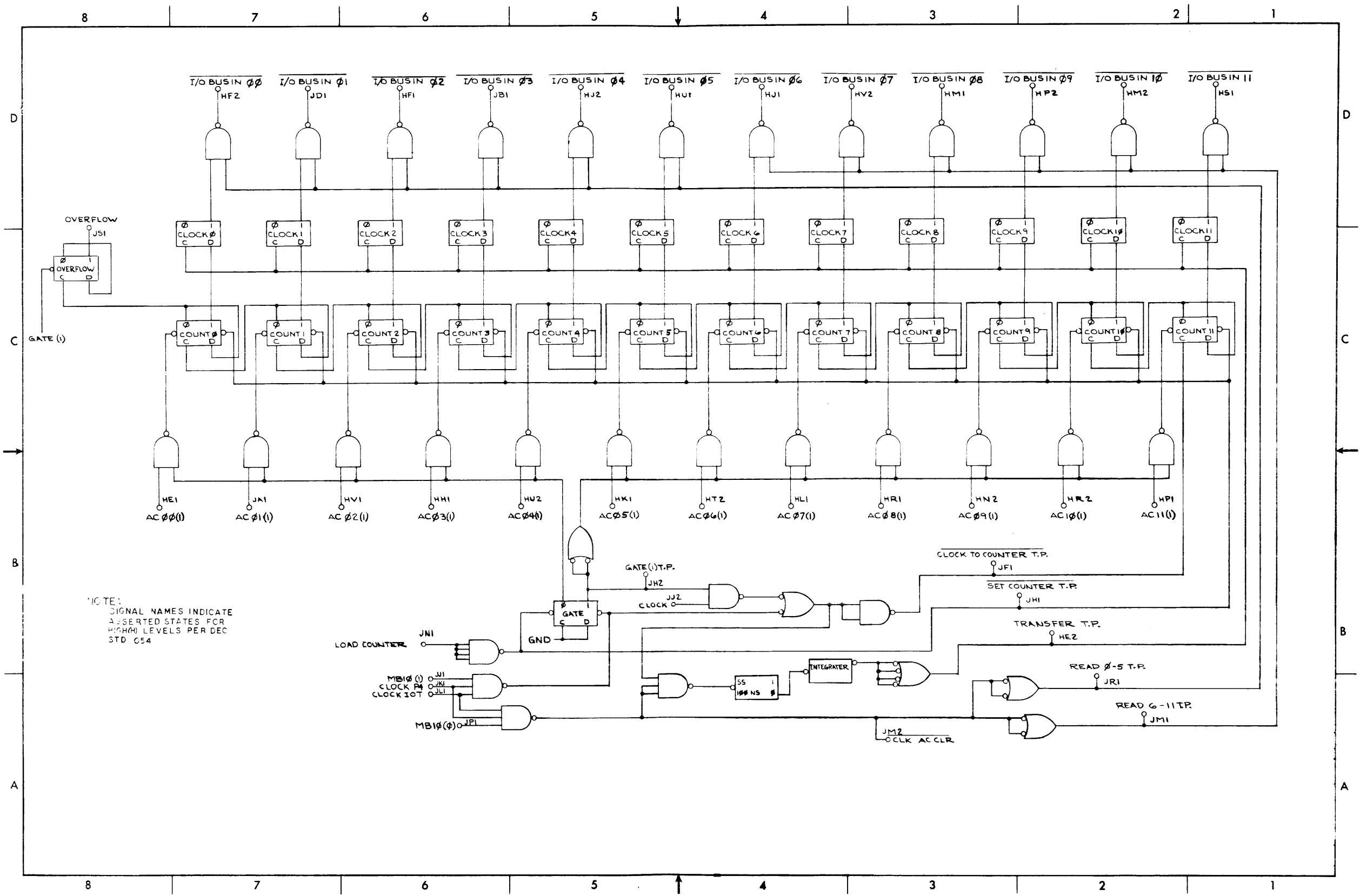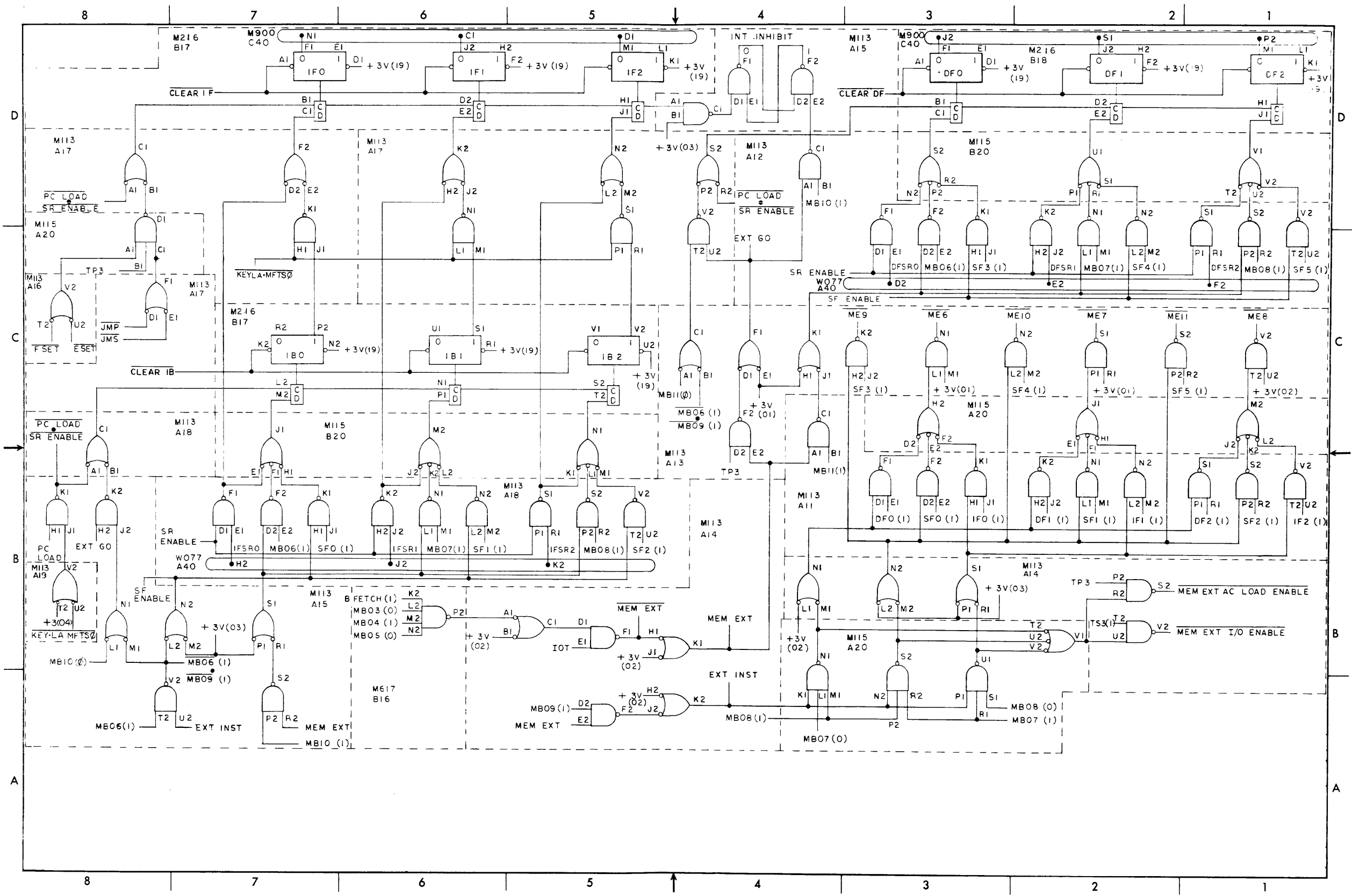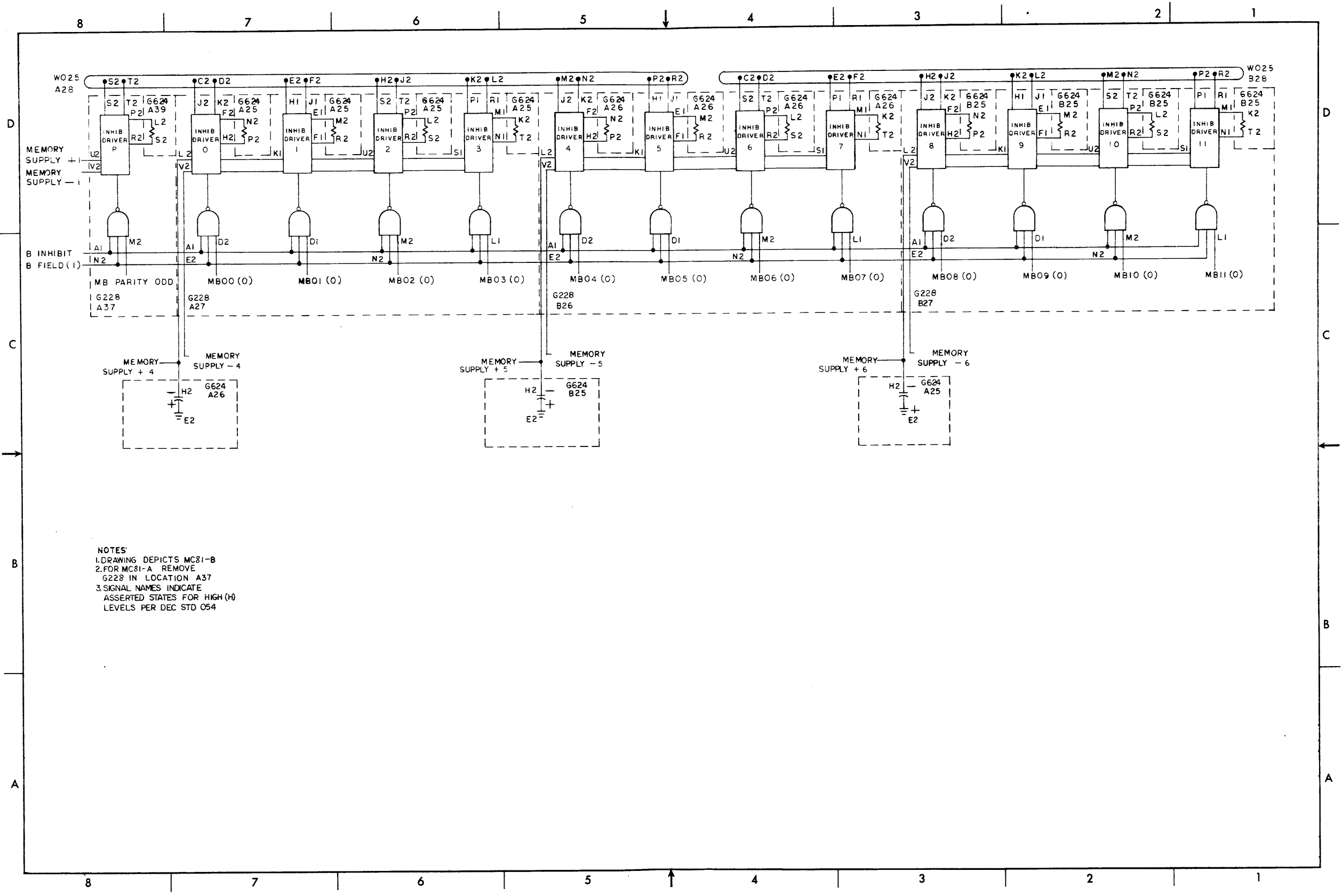
D-BS-KW8I-0-1 Real Time Clock Option KW8I
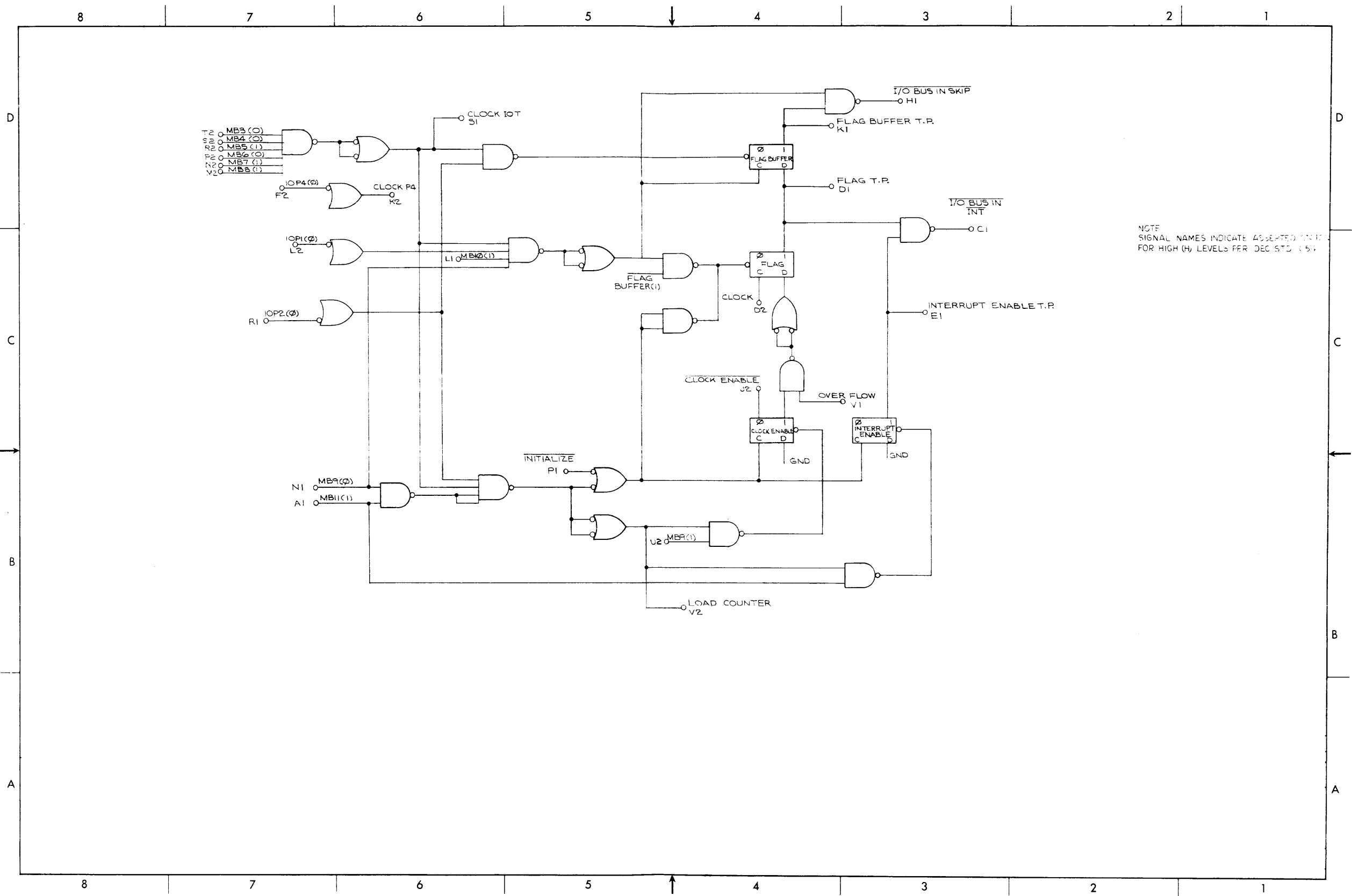
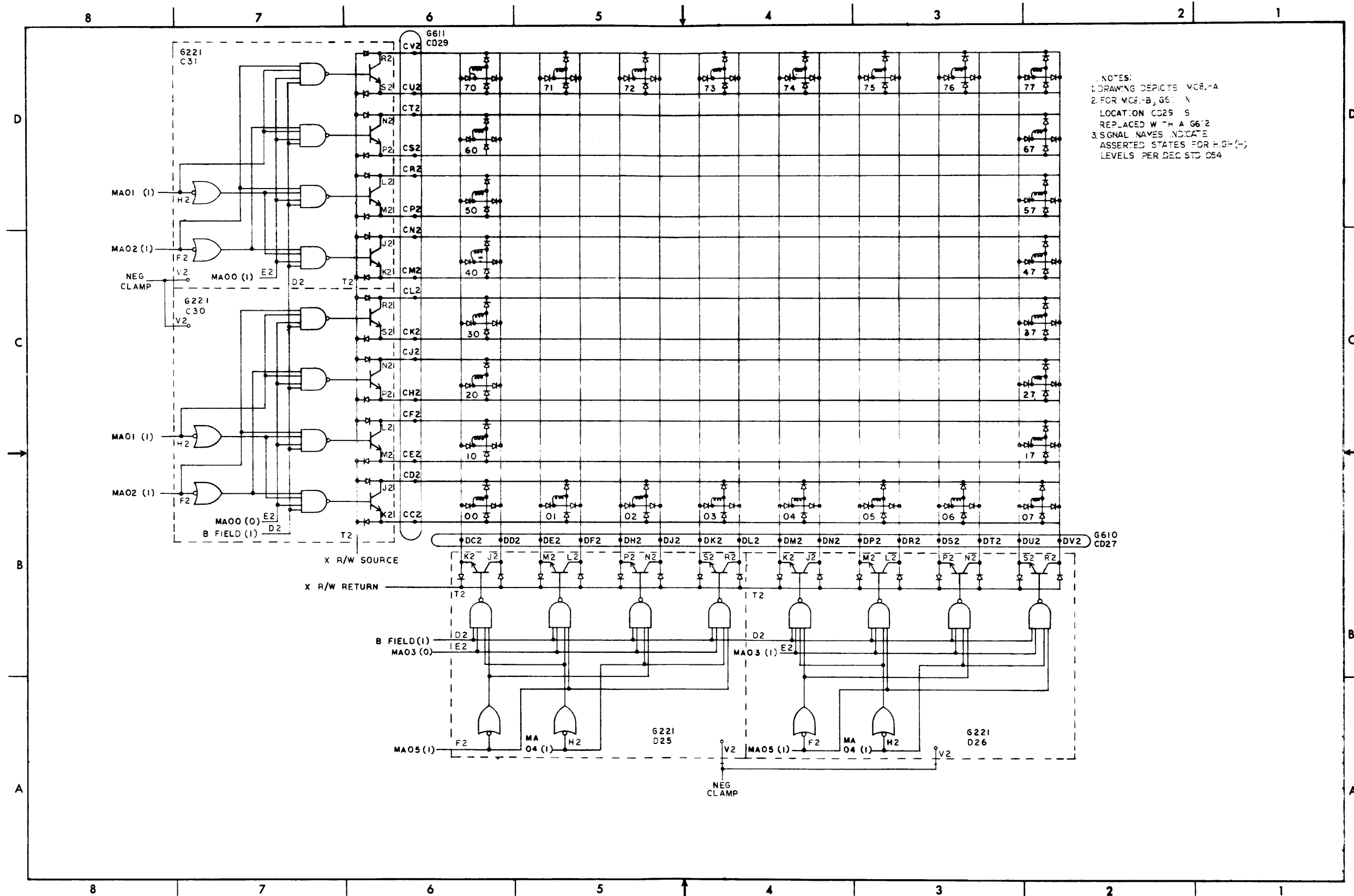D-BS-KW8I-0-2 Clock Control M708

D-BS-KW8I-0-3 Clock Counter M709

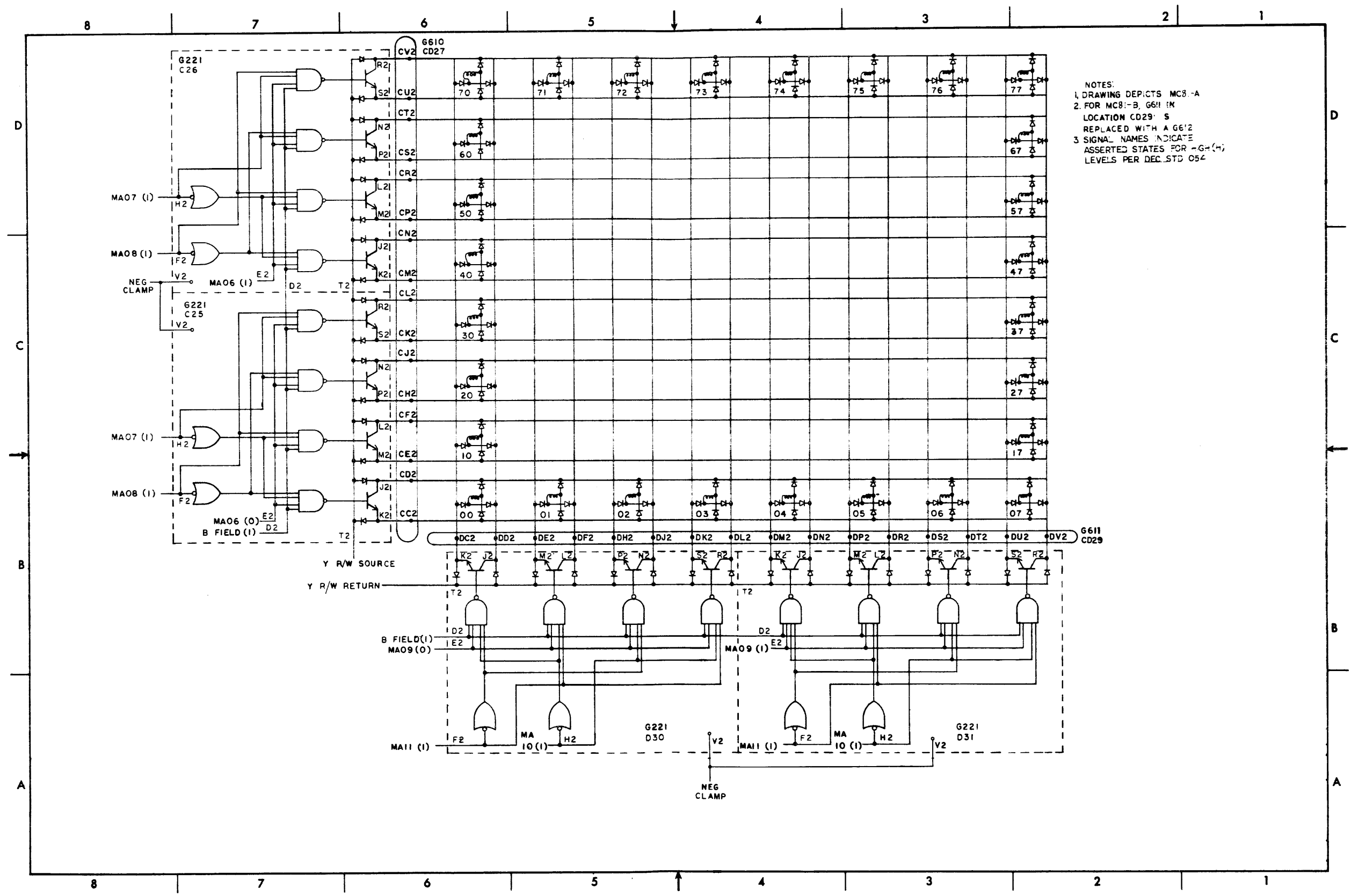D-BS-MC8I-0-1 Memory Extension Control (Sheet 1)

D-BS-MC8I-0-1 Memory Extension Control (Sheet 2)

D–BS–MC8I–0–2 Inhibit Drivers

D-BS-MC8I-0-3 X Axis Selection

D-BS-MC8I-0-4 Y Axis Selection
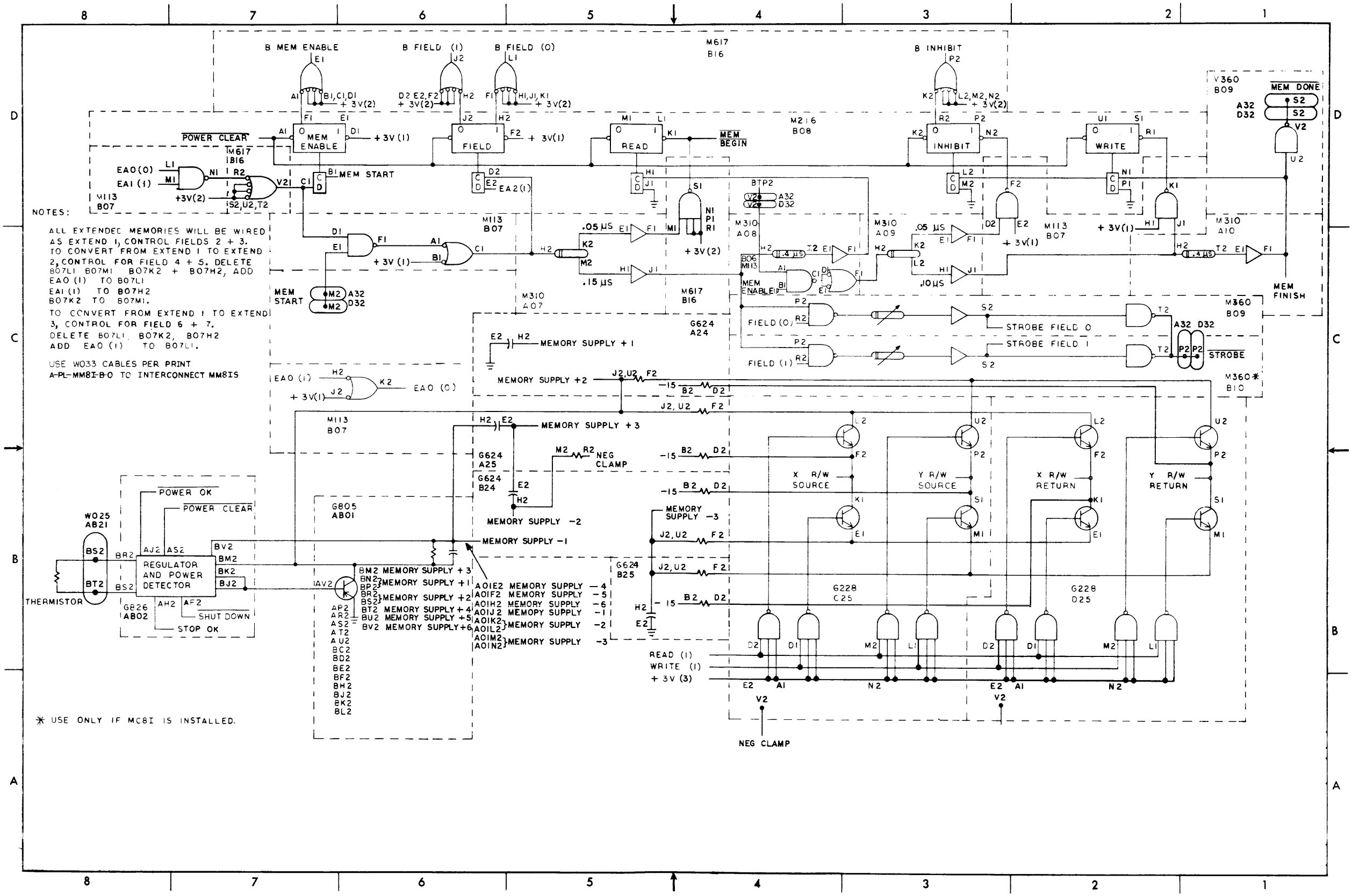
D-BS-MM8I-A-1 Memory Control

D-BS-MM8I-A-2 Sense Amps and Inhibit Drivers

D-BS-MM8I-A-3 X Axis Selection, Field 0
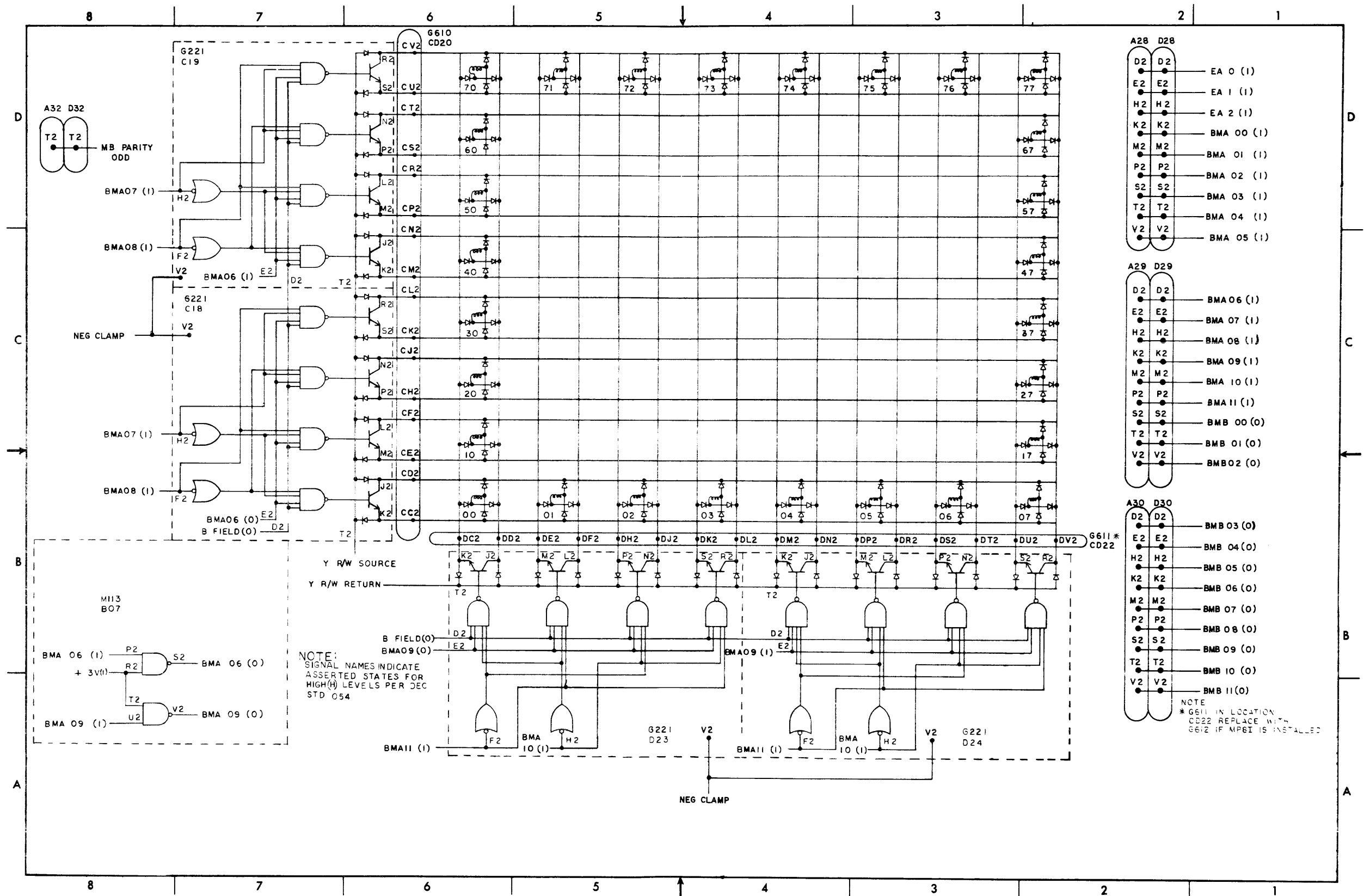
D-BS-MM8I-A-4 Y Axis Selection, Field 0
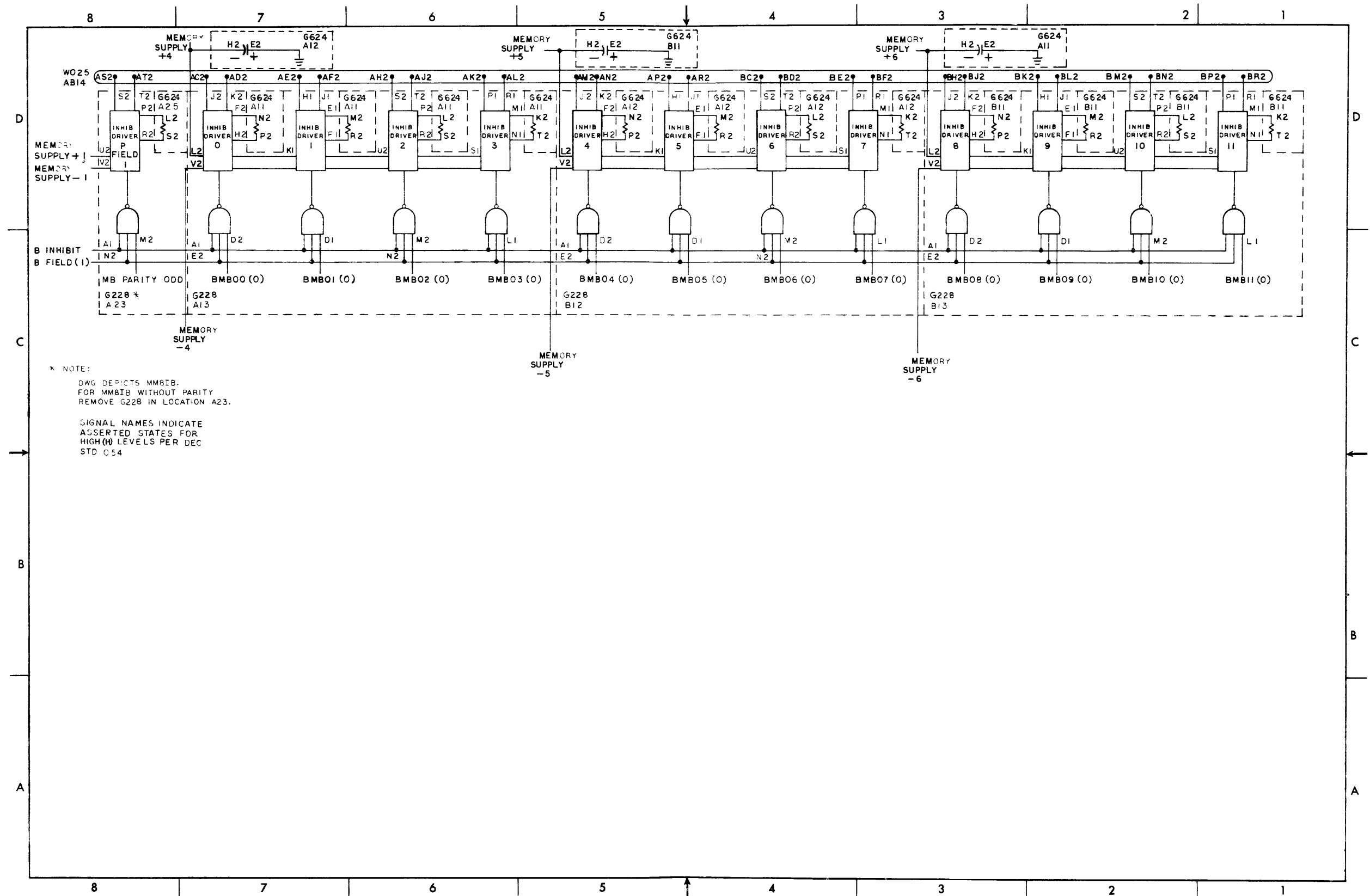
D-BS-MM8I-B-1 Inhibit Drivers, Field 1
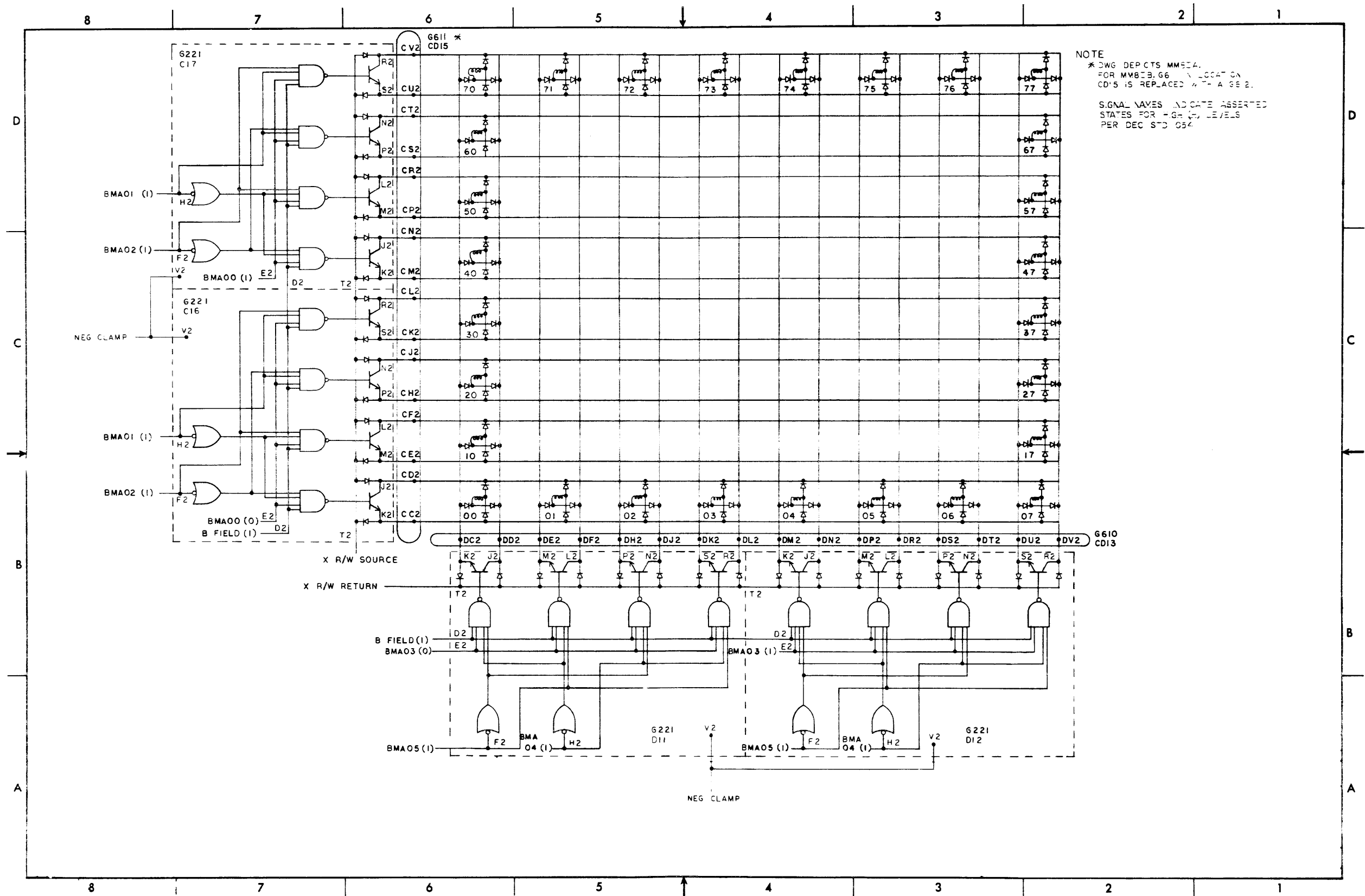
D-BS-MM8I-B-2 X Axis Selection, Field 1
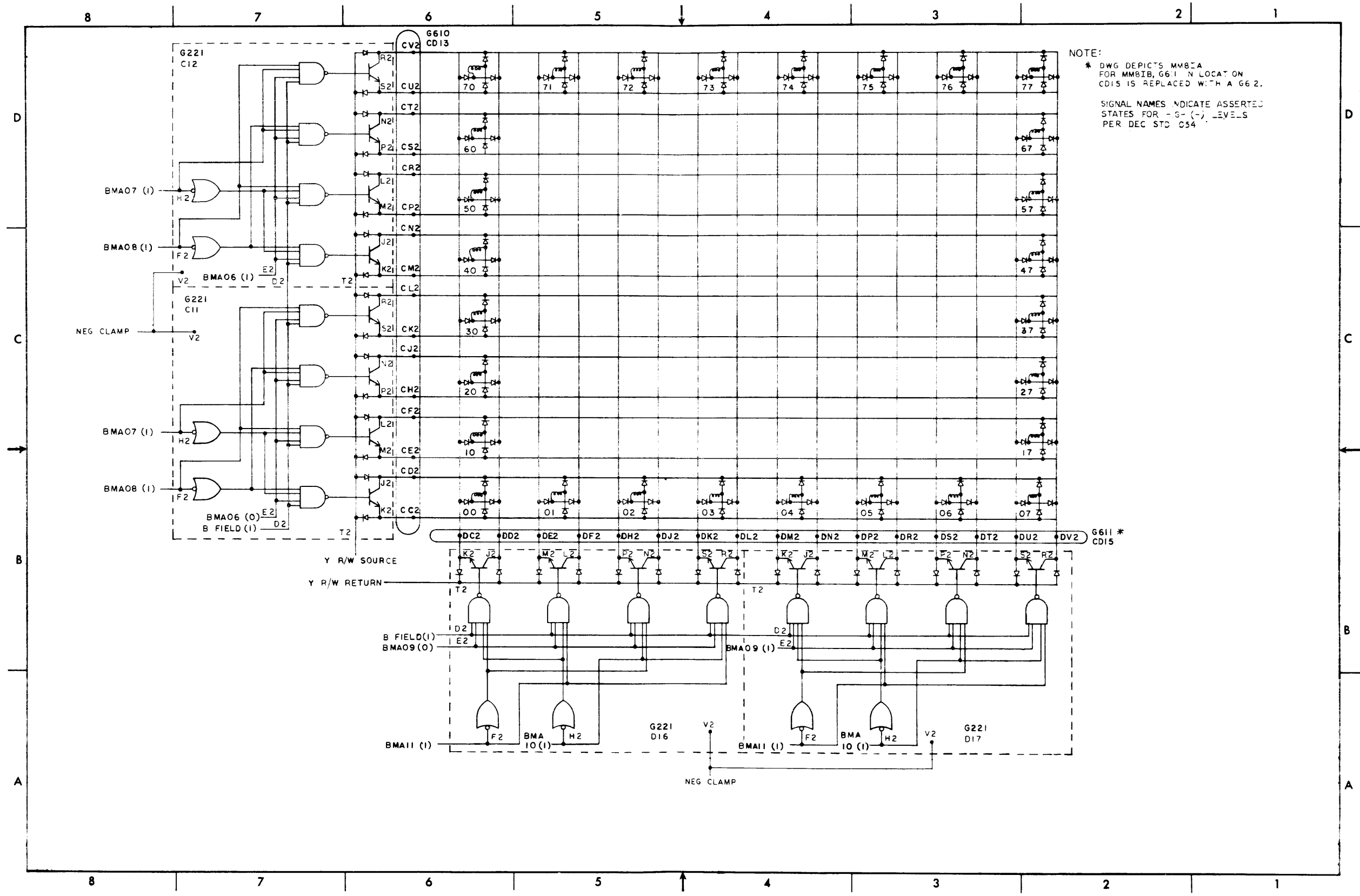
NOTE:
* DWG DEPICTS MM8IA
FOR MM8IB, G6II IN LOCATION
CDI5 IS REPLACED WITH A G6I2.

SIGNAL NAMES INDICATE ASSERTED
STATES FOR -G- (-) LEVELS
PER DEC STD 054

D-BS-MM8I-B-3 Y Axis Selection, Field 1
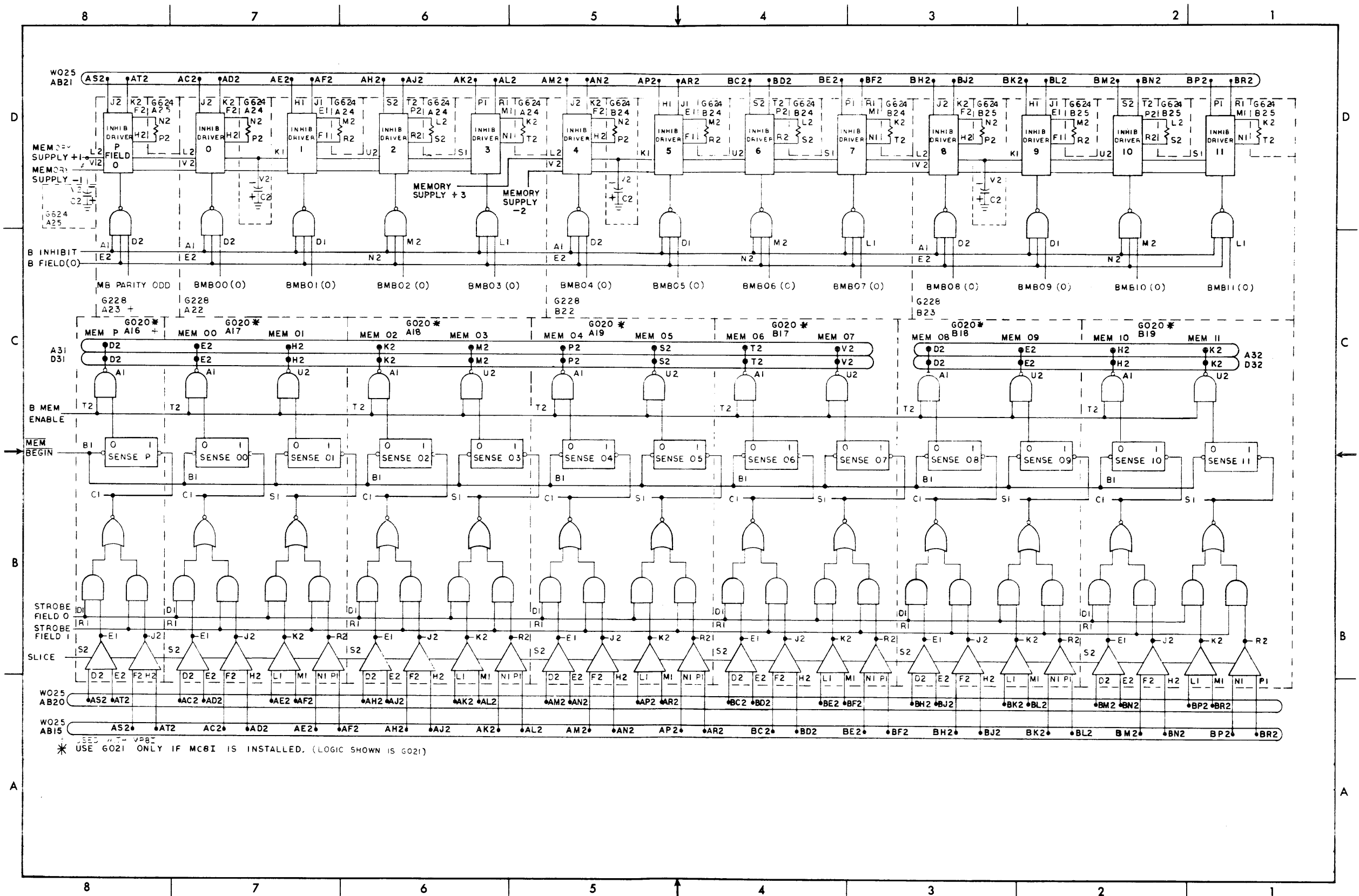
II-18
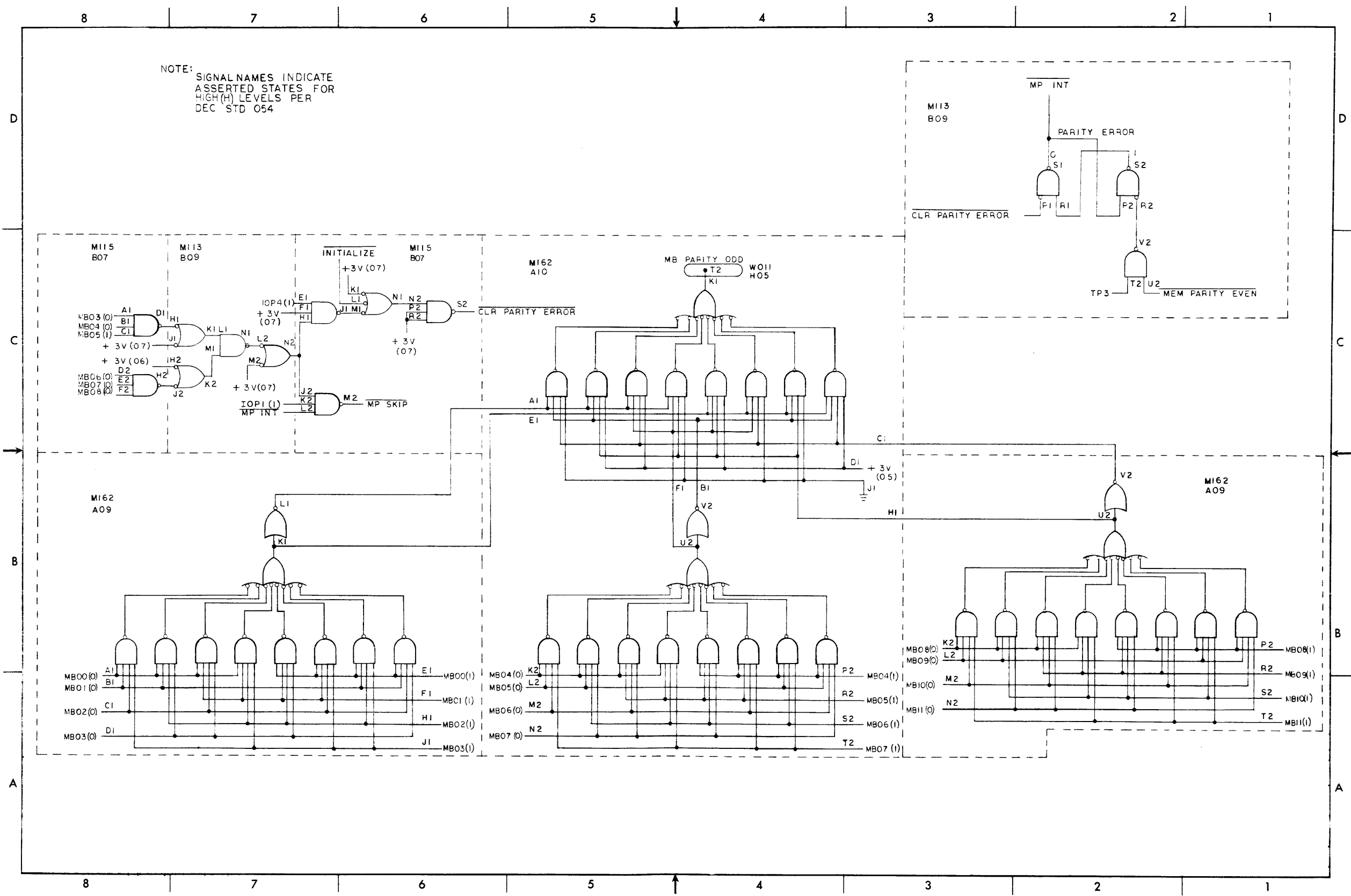
D-BS-MP8I-0-1 Memory Parity Option

II-19
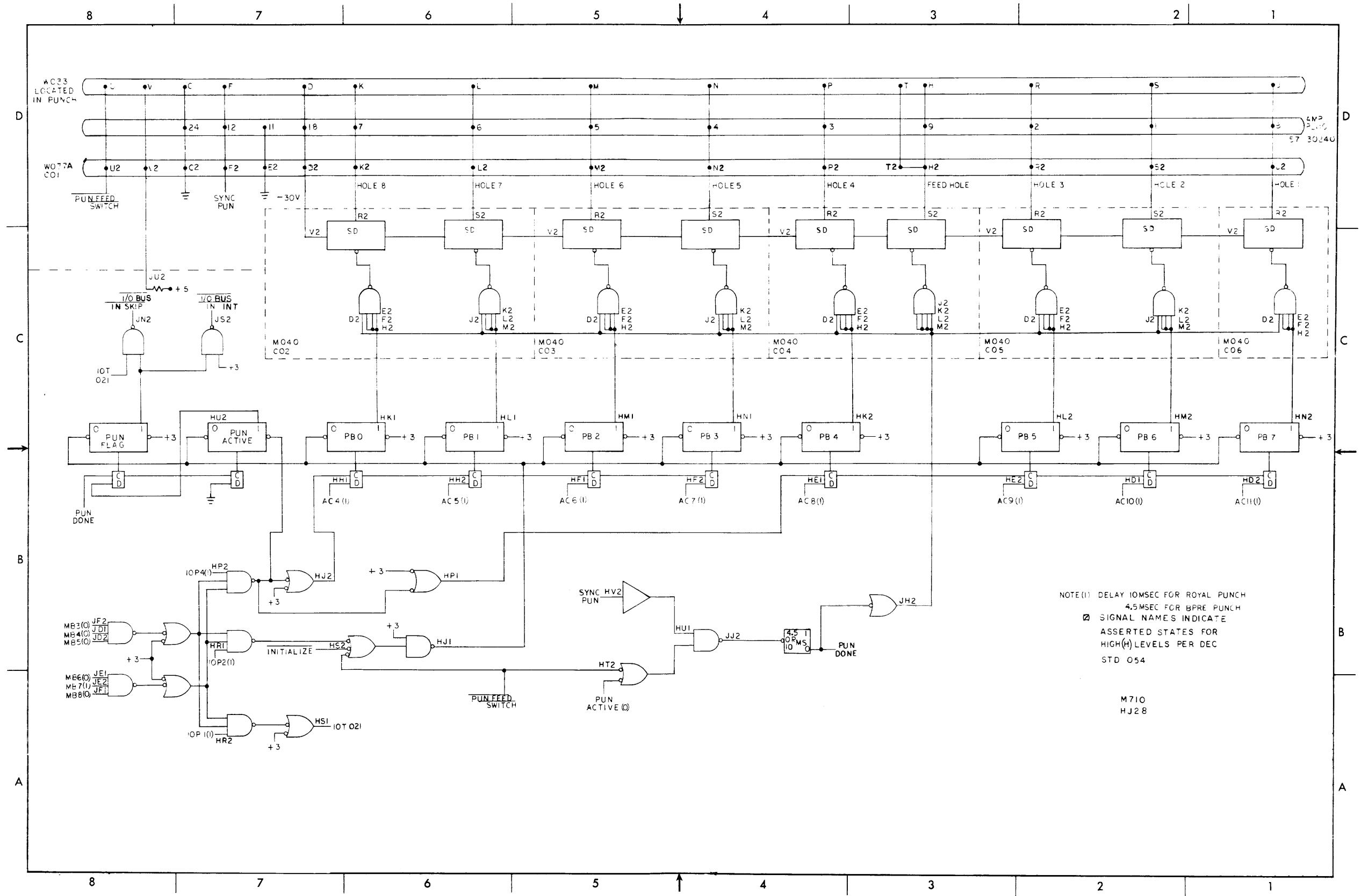
D-BS-PP8I-0-1 High Speed Punch
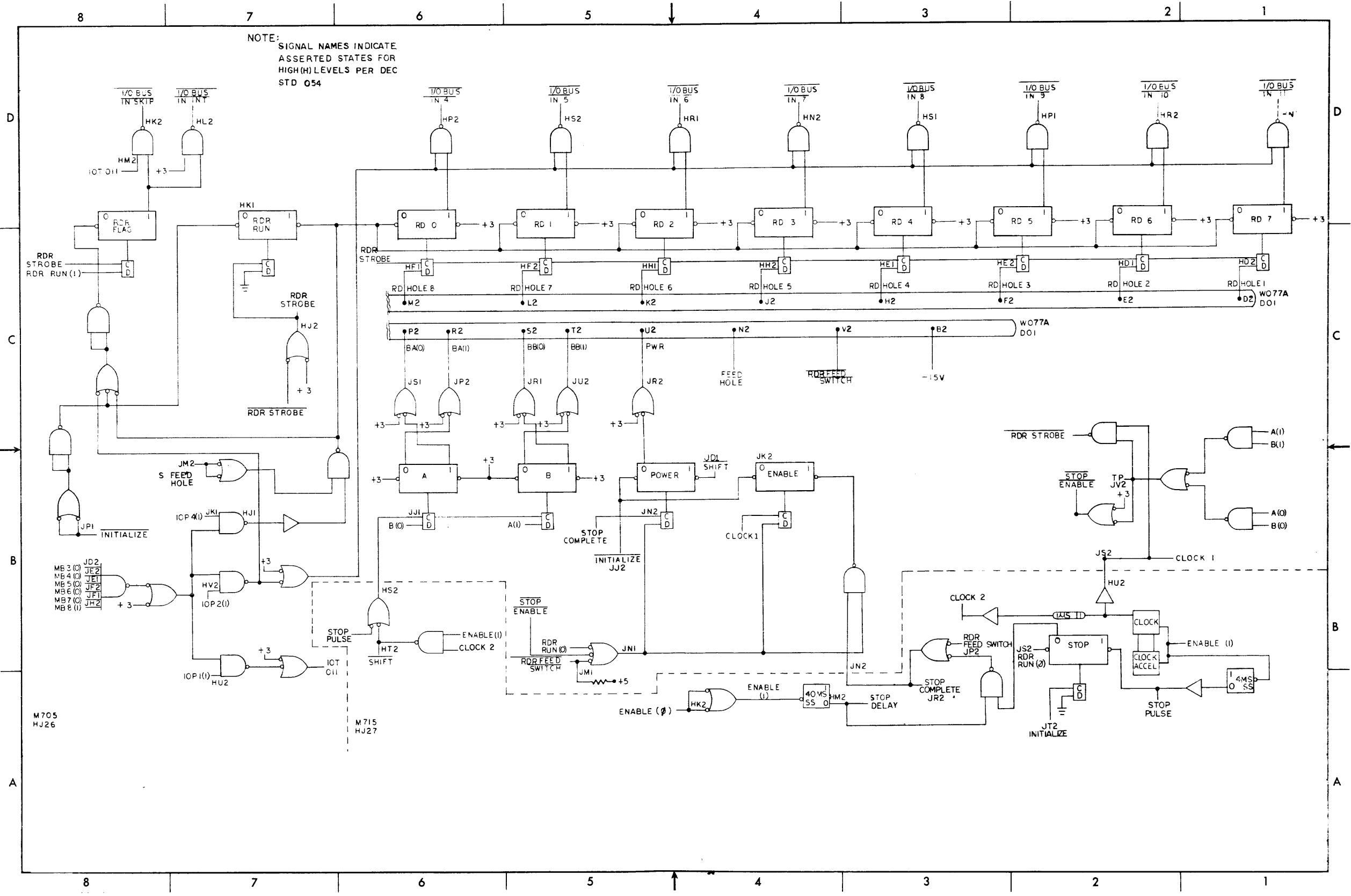
D-BS-PR8I-0-1 High Speed Reader
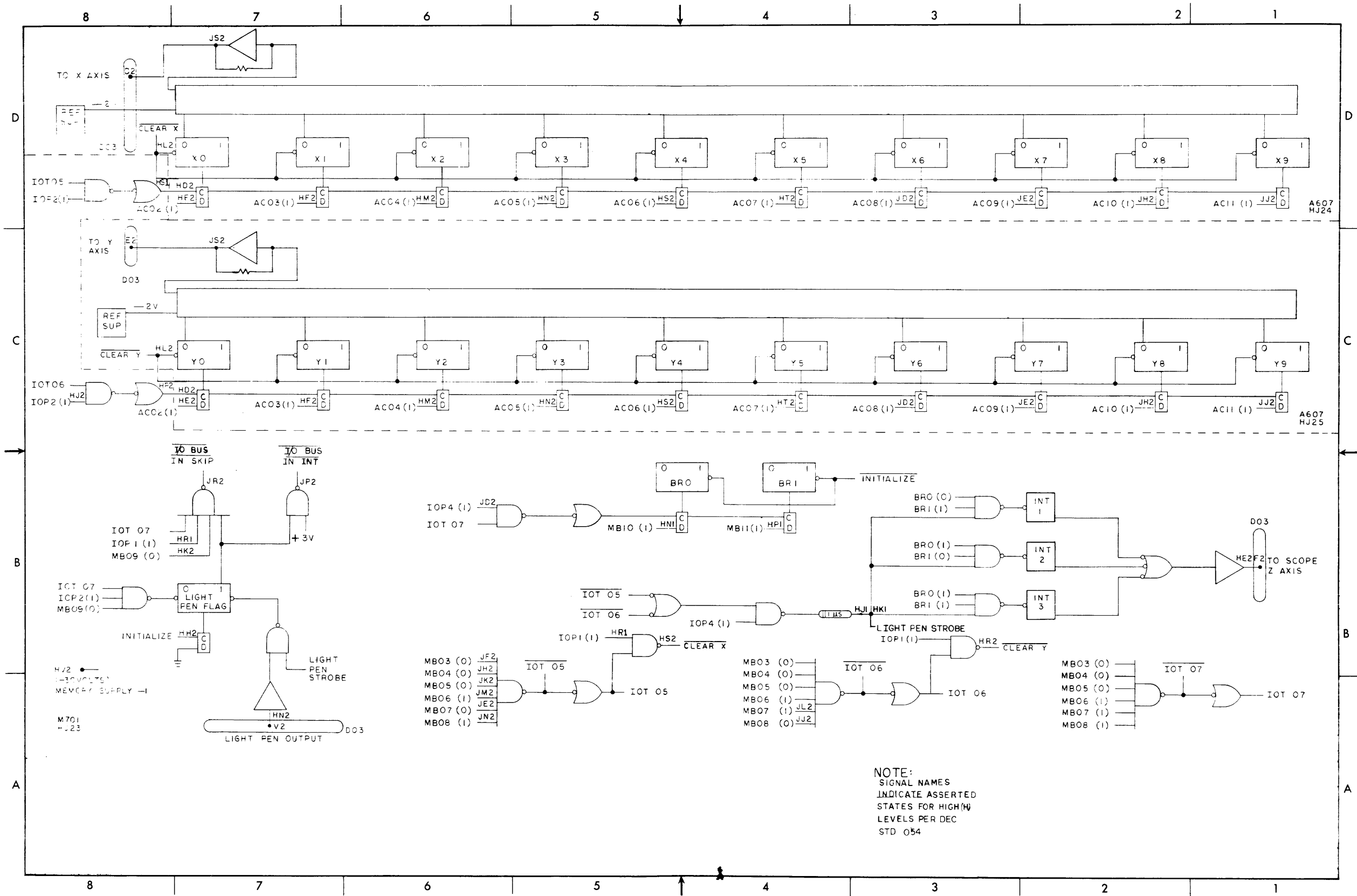
D-BS-VC8I-0-1 Display Control

D-BS-VP8I-0-I Plotter Control

D-BS-TC01-0-2 MF, USR, MR, FR

NOTE 1:
PIN DESIGNATIONS HAVE BEEN
REVERSED TO SHOW CORRECT
LOGICAL FUNCTION.
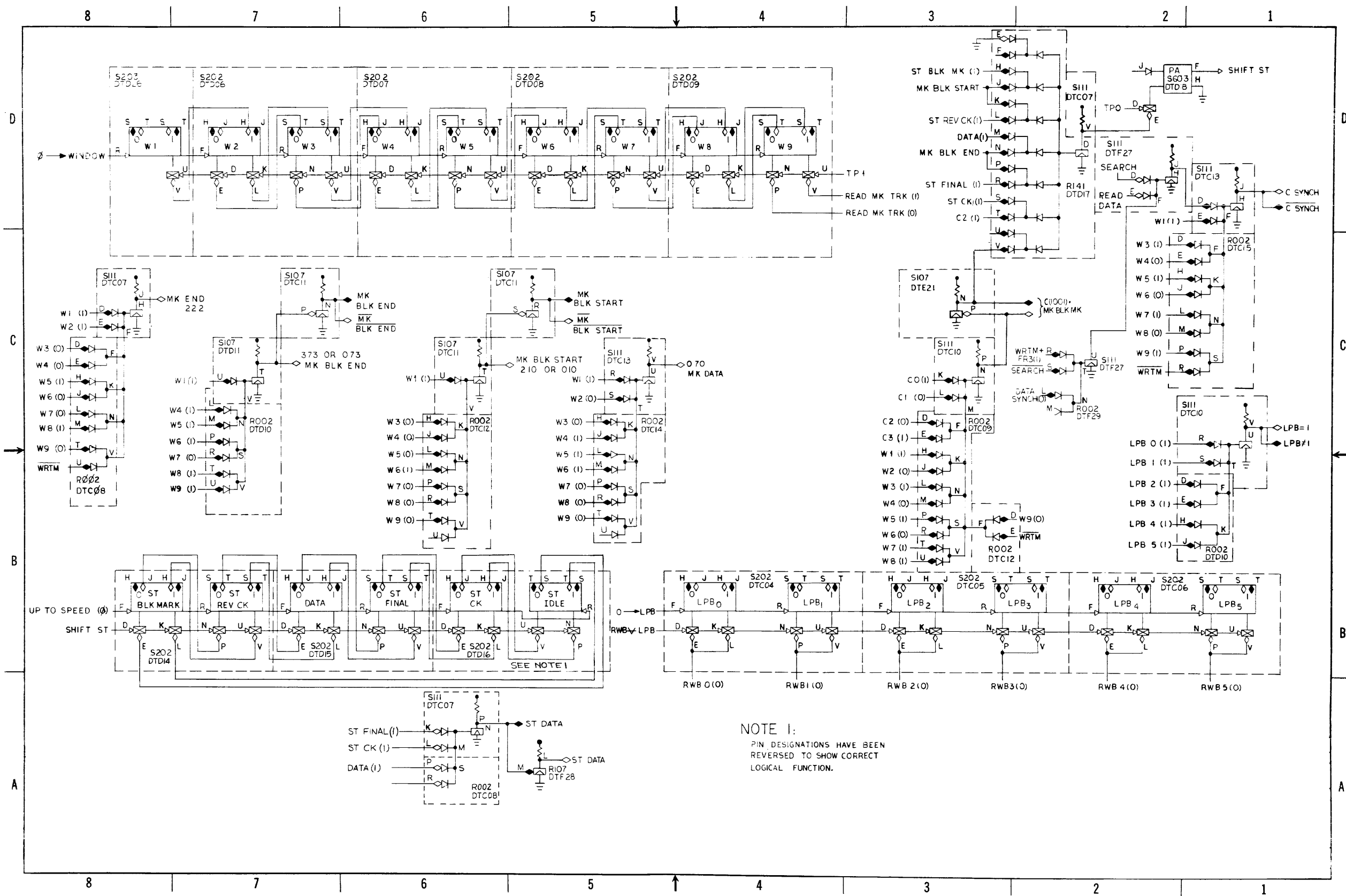
D-BS-TC01-0-3 Window, MK TRK, STATE, LPB
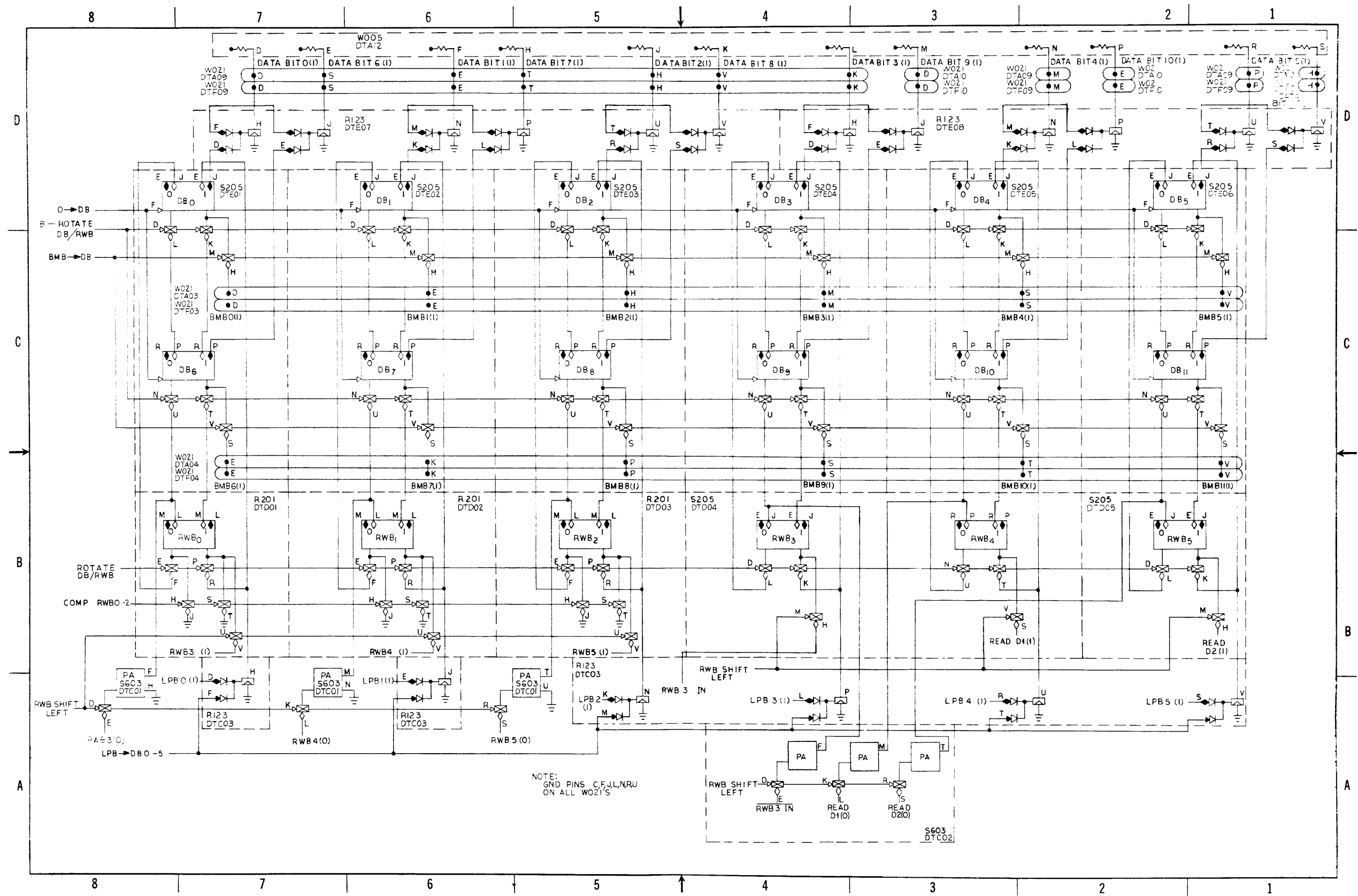
D-BS-TC01-0-4 DB and RWB Registers

D-BS-TC01-0-5 Control Pulses
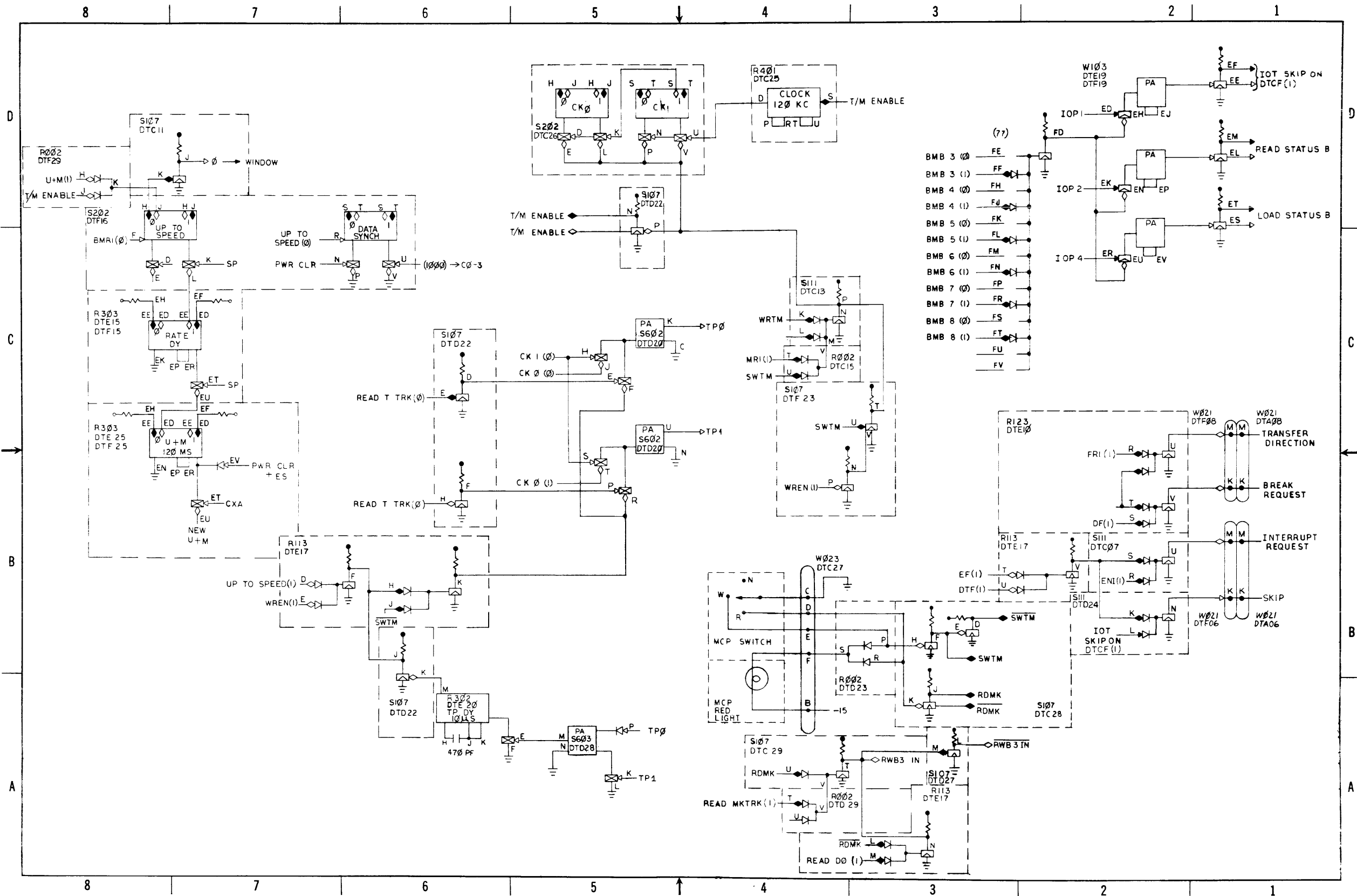
D-BS-TC01-0-6 TP GEN, TT GEN
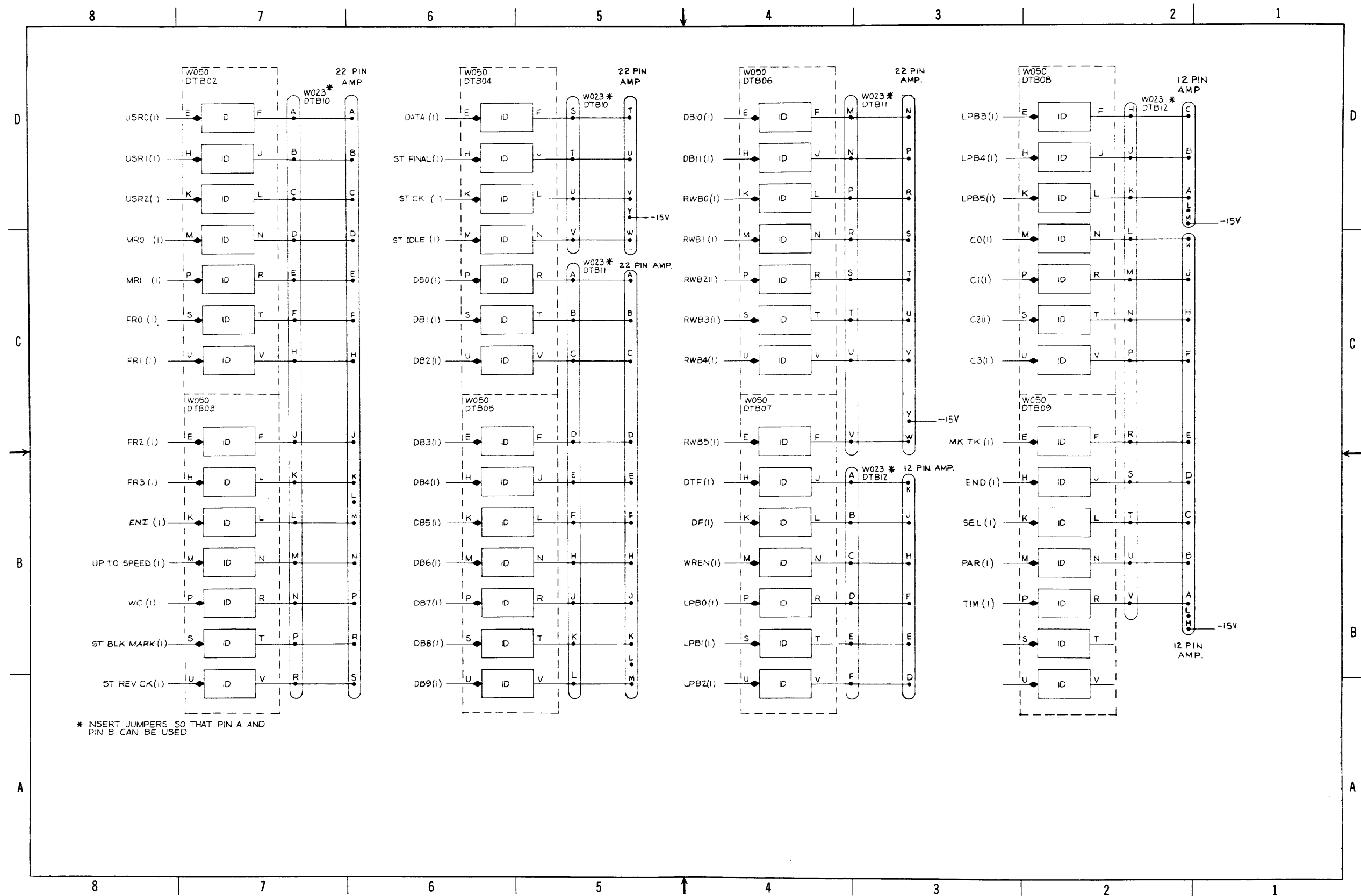
D-BS-TC01-0-12 Panel Indicators Drivers

WO23* DTB10

22 PIN AMPHENOL CONNECTOR (FEMALE) (MALE)   INDICATOR BRACKET   4910**

A	USR0	A	A	
B	USR1	B	B	
C	USR2	C	C	
D	MR0	D	D	
E	MR1	E	E	
F	FR0	F	F	
H	FR1	H	H	
J	FR2	J	J	
K	FR3	K	K	
L	ENI	L/M	L/M	
M	US	N	N	
N	WC	P	P	
P	BM	R	R	
R	RC	S	S	
S	D	T	T	
T	F	U	U	
U	C	V	V	
V	I	W	W	
		X/Y/Z	X/Y/Z	-15***

WO23* DTB11

22 PIN AMPHENOL CONNECTOR (FEMALE) (MALE)   INDICATOR BRACKET   4910**

A	DB0	A	A	
B	DB1	B	B	
C	DB2	C	C	
D	DB3	D	D	
E	DB4	E	E	
F	DB5	F	F	
H	DB6	H	H	
J	DB7	J	J	
K	DB8	K	K	
L	DB9	L/M	L/M	
M	DB10	N	N	
N	DB11	P	P	
P	RWB0	R	R	
R	RWB1	S	S	
S	RWB2	T	T	
T	RWB3	U	U	
U	RWB4	V	V	
V	RWB5	W	W	
		X/Y/Z	X/Y/Z	-15***

WO23* DTB12

12 PIN AMPHENOL CONNECTOR (FEMALE) (MALE)   INDICATOR BRACKET   4904**

A	DTF	K	K	
B	DF	J	J	
C	W	H	H	
D	LPB0	F	F	
E	LPB1	E	E	
F	LPB2	D	D	
H	LPB3	C	C	
J	LPB4	B	B	
K	LPB5	A	A	
		N/M	N/M	-15***

WO23* DTB23

12 PIN AMPHENOL CONNECTOR (FEMALE) (MALE)   INDICATOR BRACKET   4904**

L	C0	K	K	
M	C1	J	J	
N	C2	H	H	
P	C3	F	F	
R	MR	E	E	
S	END	D	D	
T	SE	C	C	
U	PAR	B	B	
V	TIM	A	A	
		N/M/L	N/M/L	-15***

WO23 DTC 27

WRTM RDMK INDICATOR

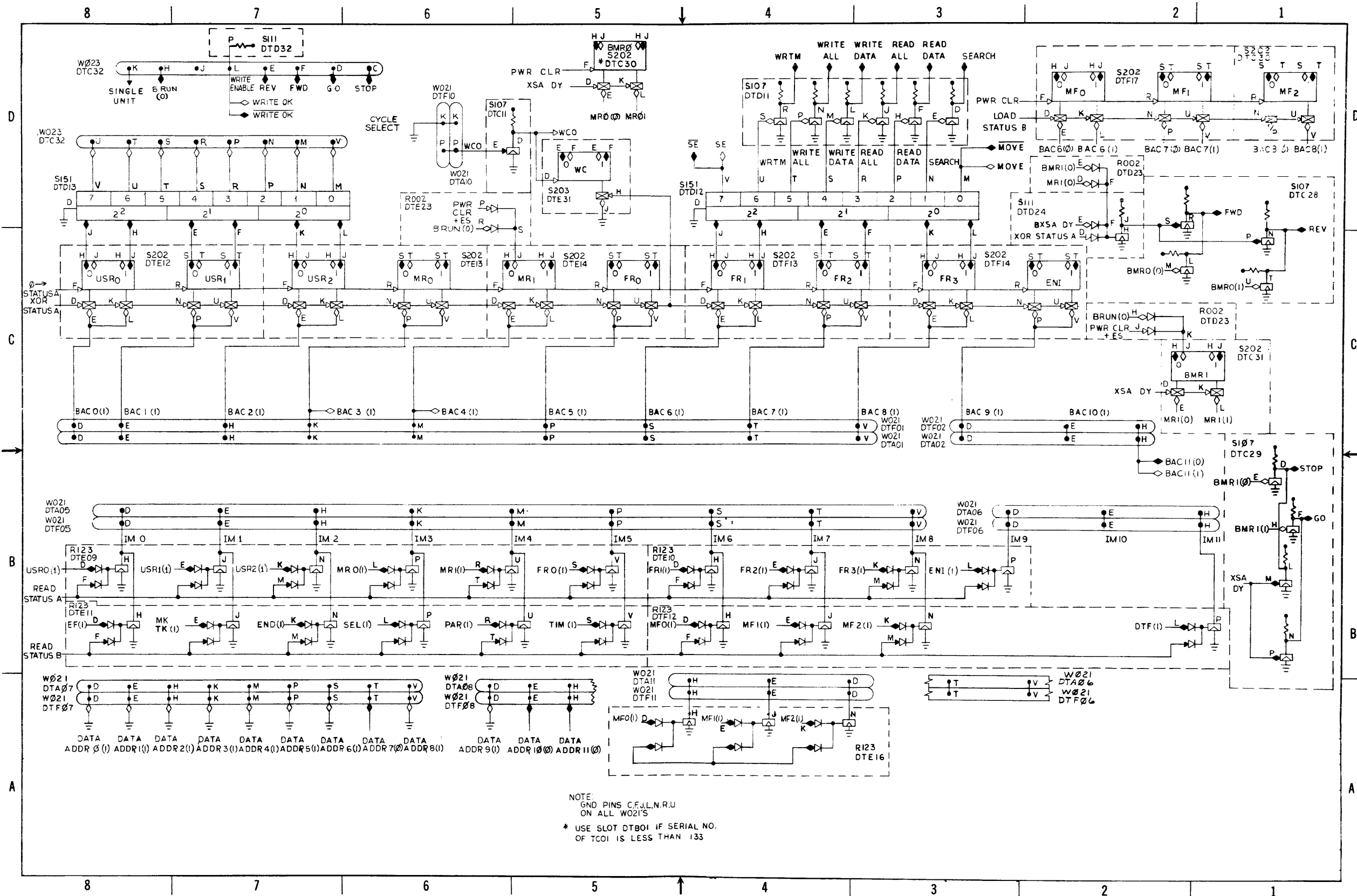|	
B	
F	
C	NORMAL
D	WRTM
E	RDMK

* INSERT JUMPERS IN WO23'S SO PINS A AND B CAN BE USED

** 4910 AND 4904'S WITH TRANSISTORS REPLACED BY A JUMPER FROM BASE TO COLLECTOR

*** -15 JUMPERED TOGETHER AND TIED TO -15 ON SIDE PANEL WITH "FASTON" TAB CONNECTOR

D-BS-TC01-0-13 Maintenance Control Panel
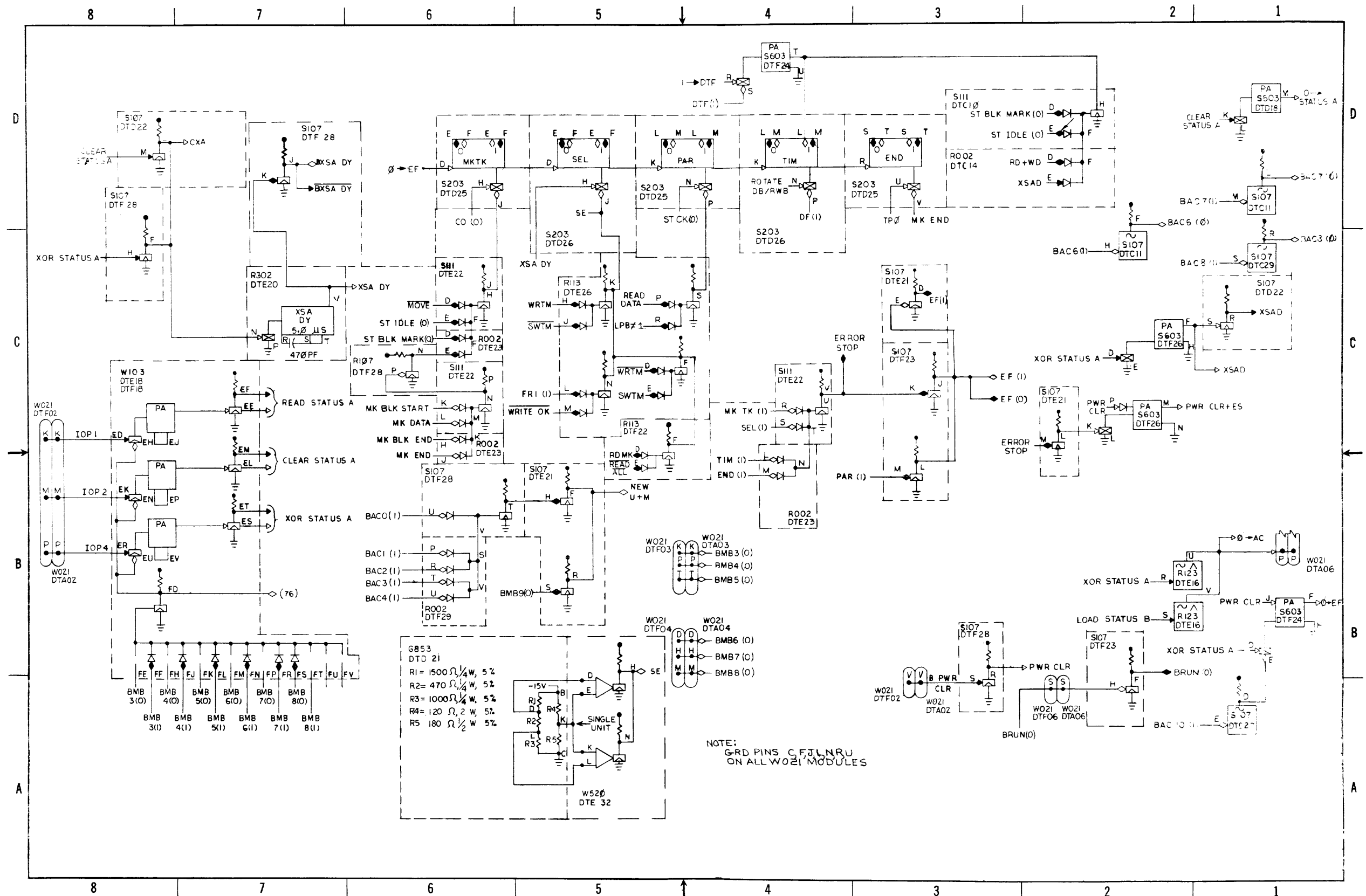
D-BS-TC01-0-14 Error Flags
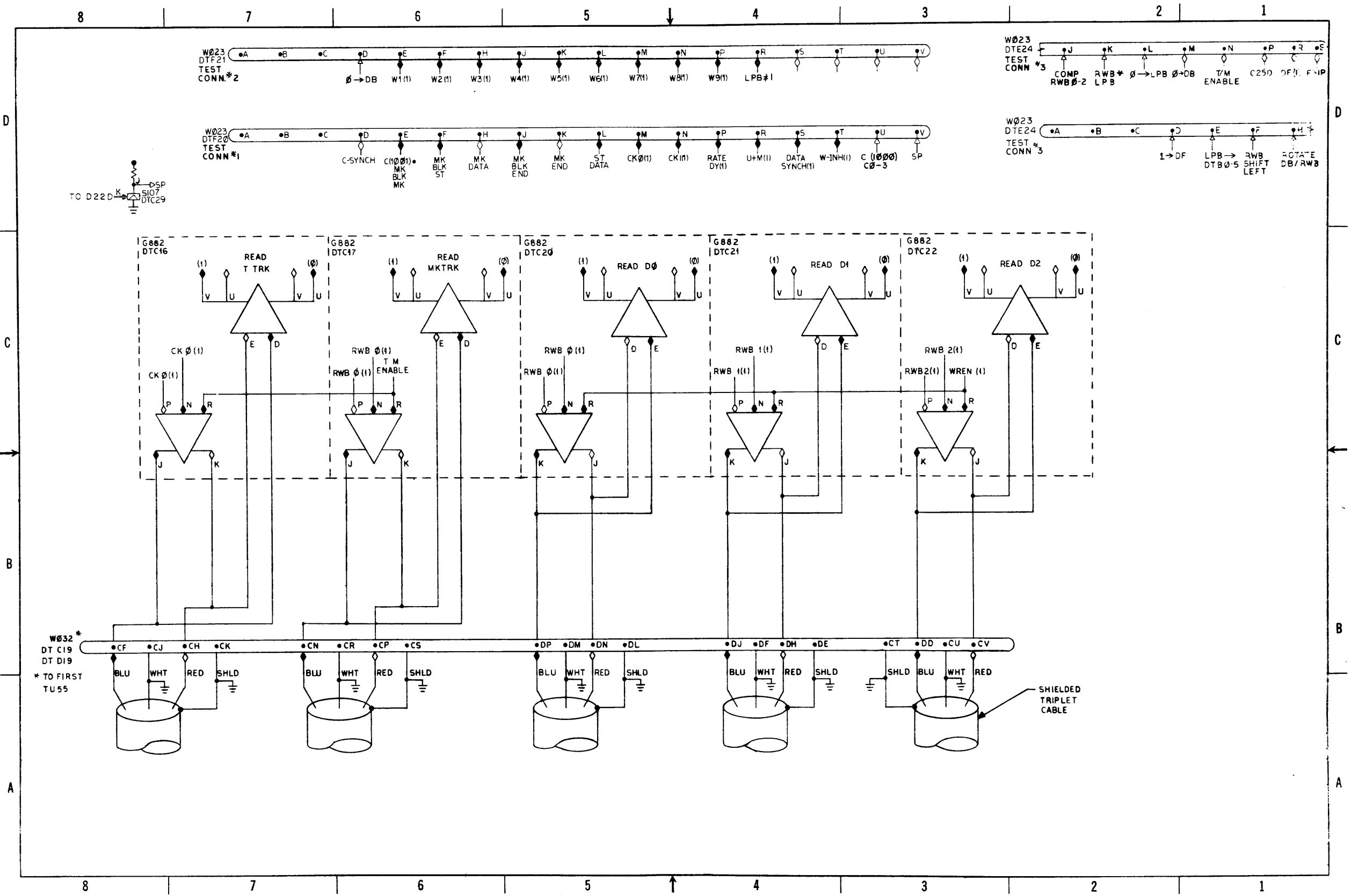
D-BS-TC01-0-15 R/W Amps, SP GEN, Test Conn.
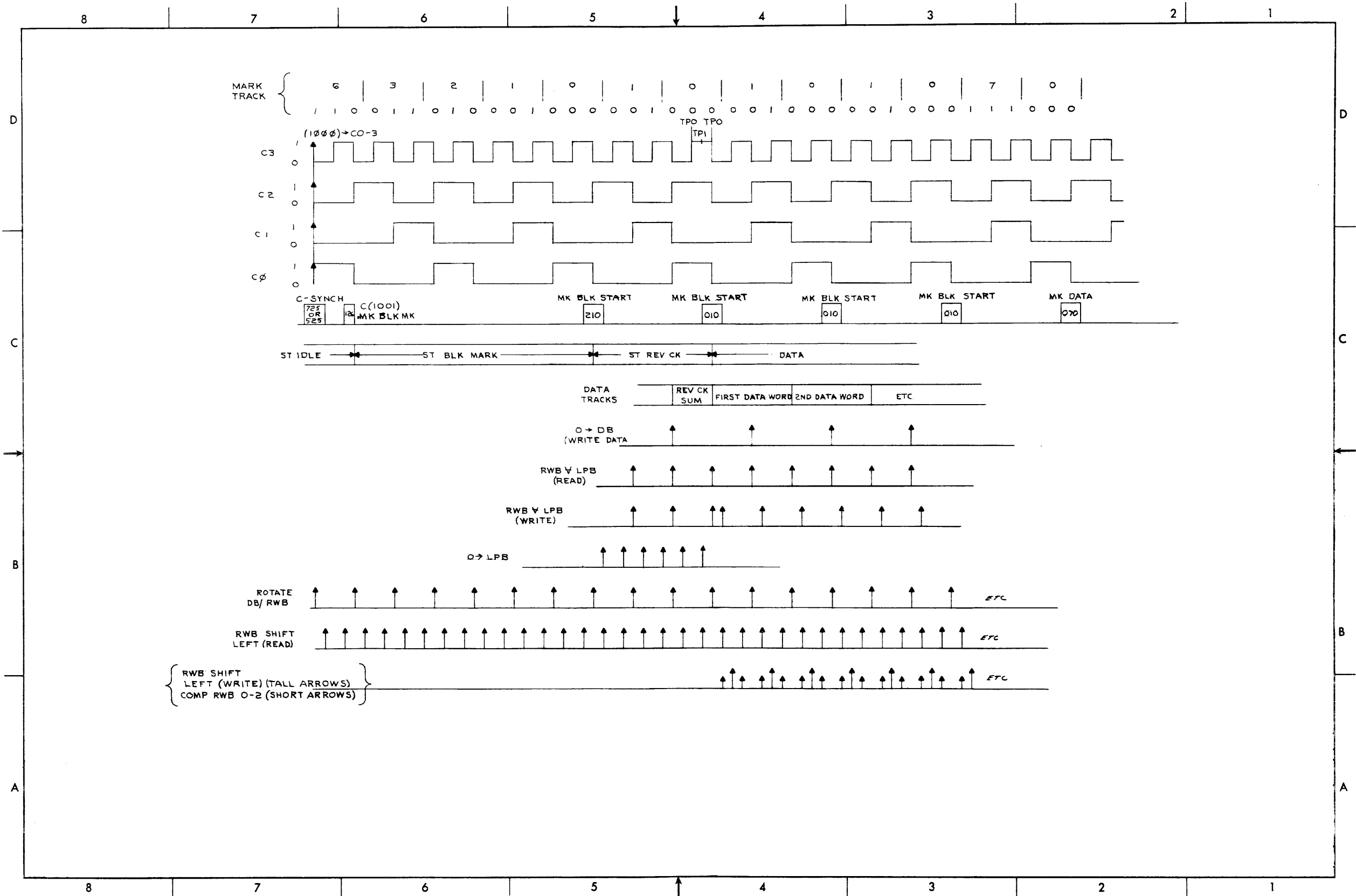
D-TD-TC01-0-17 Timing (Sheet 1)
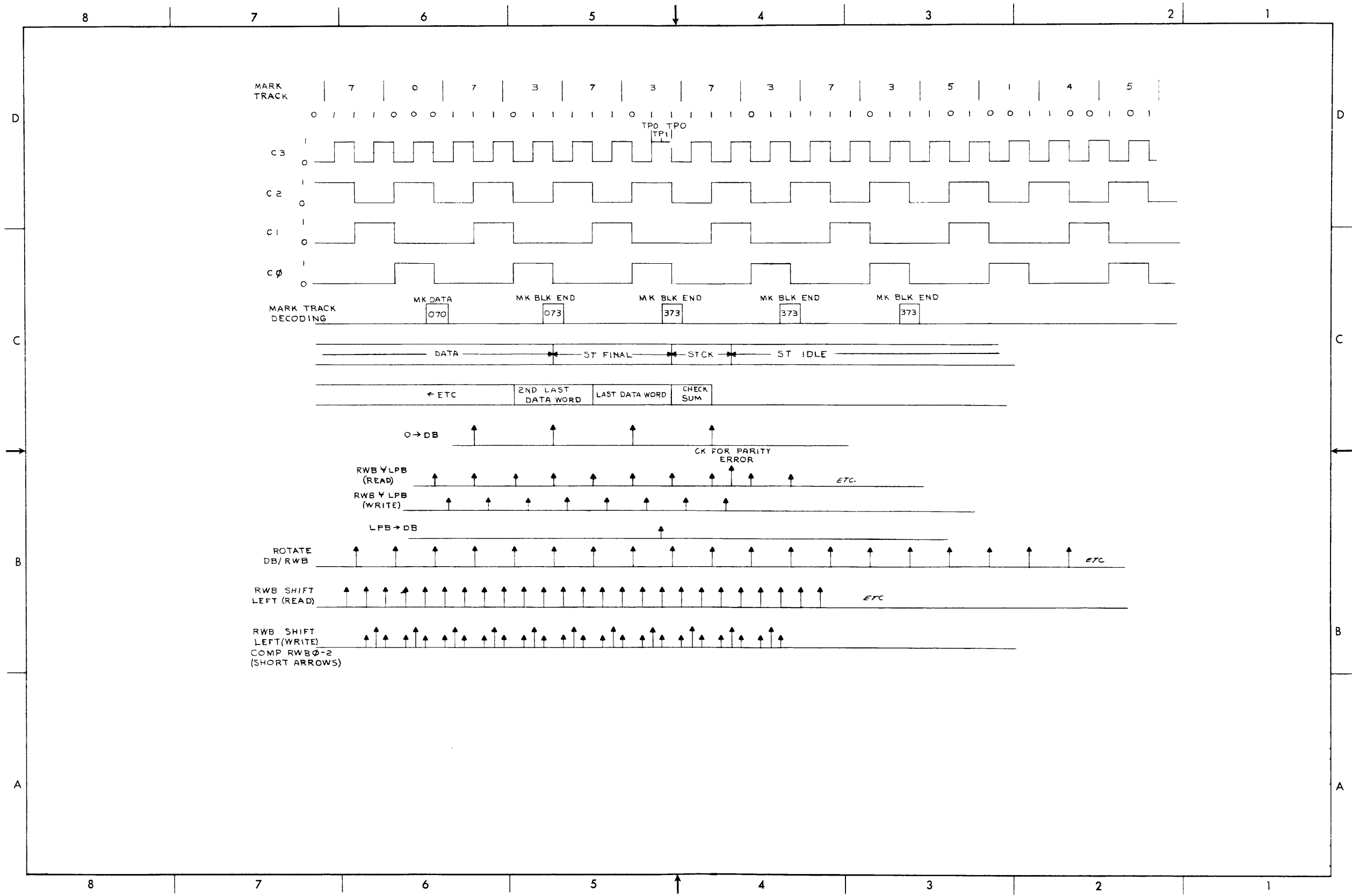
D-TD-TC01-0-17 Timing (Sheet 2)
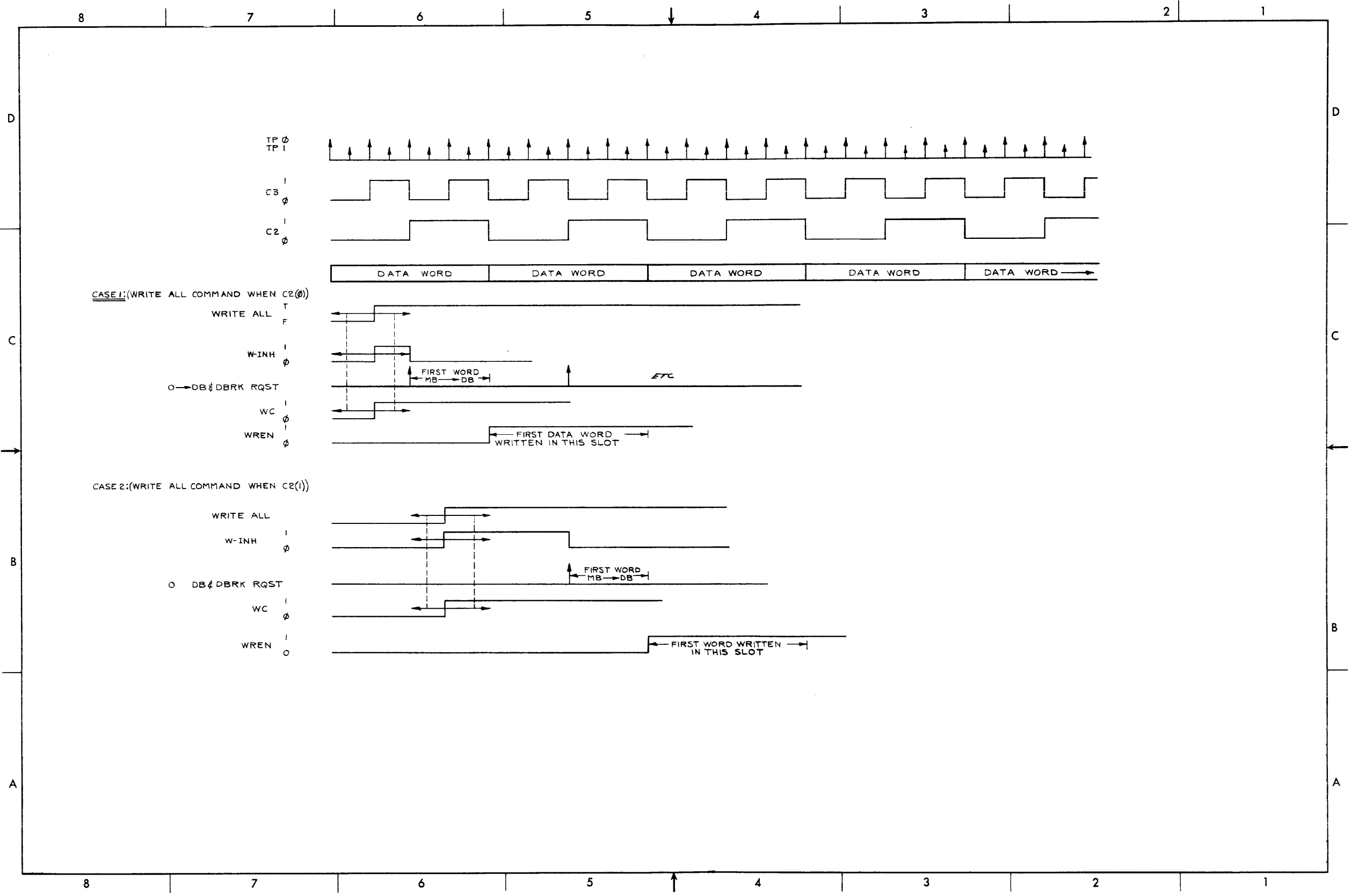
D-TD-TC01-0-17 Timing (Sheet 3)
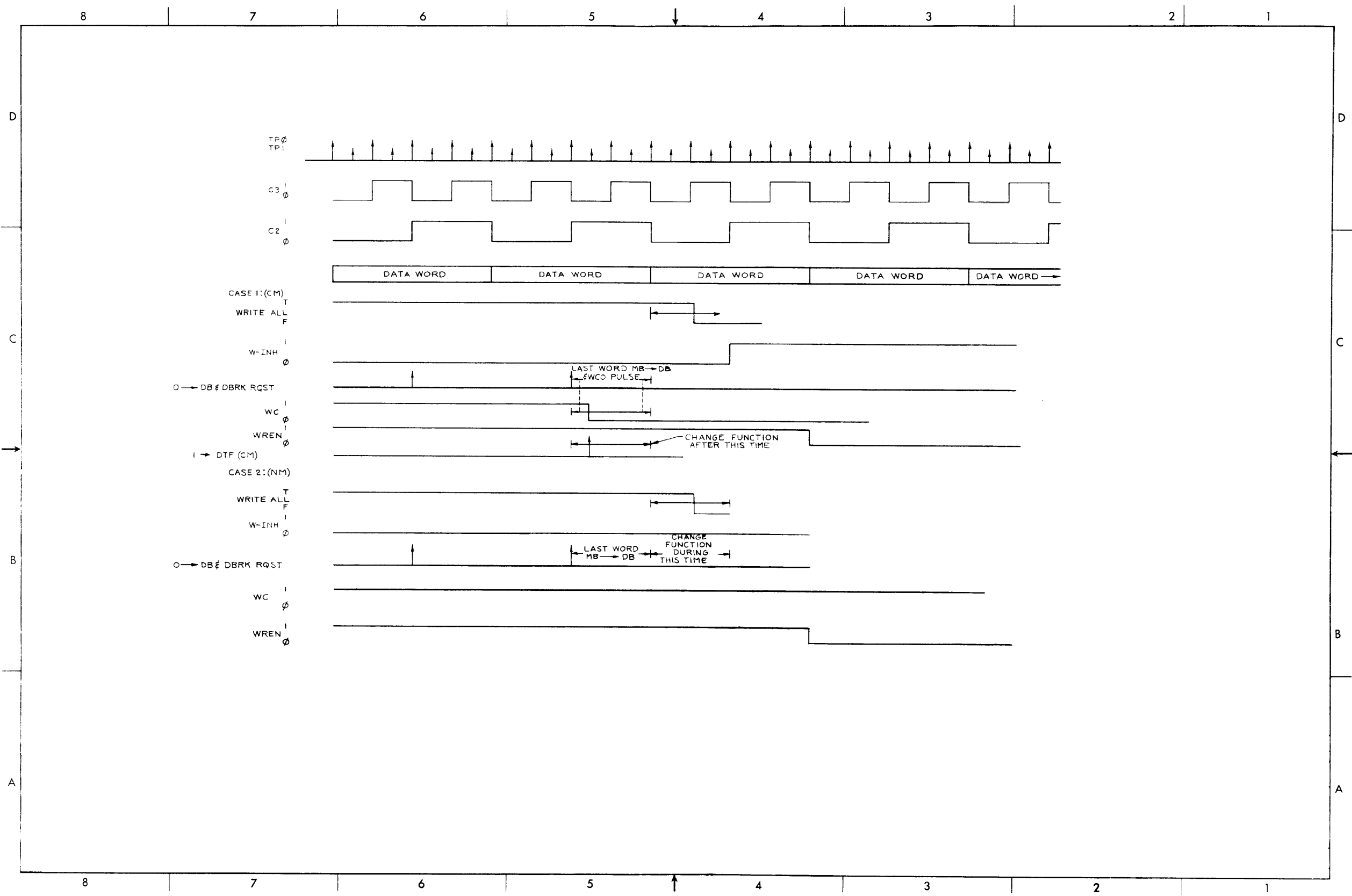
D-TD-TC01-0-17 Timing (Sheet 4)
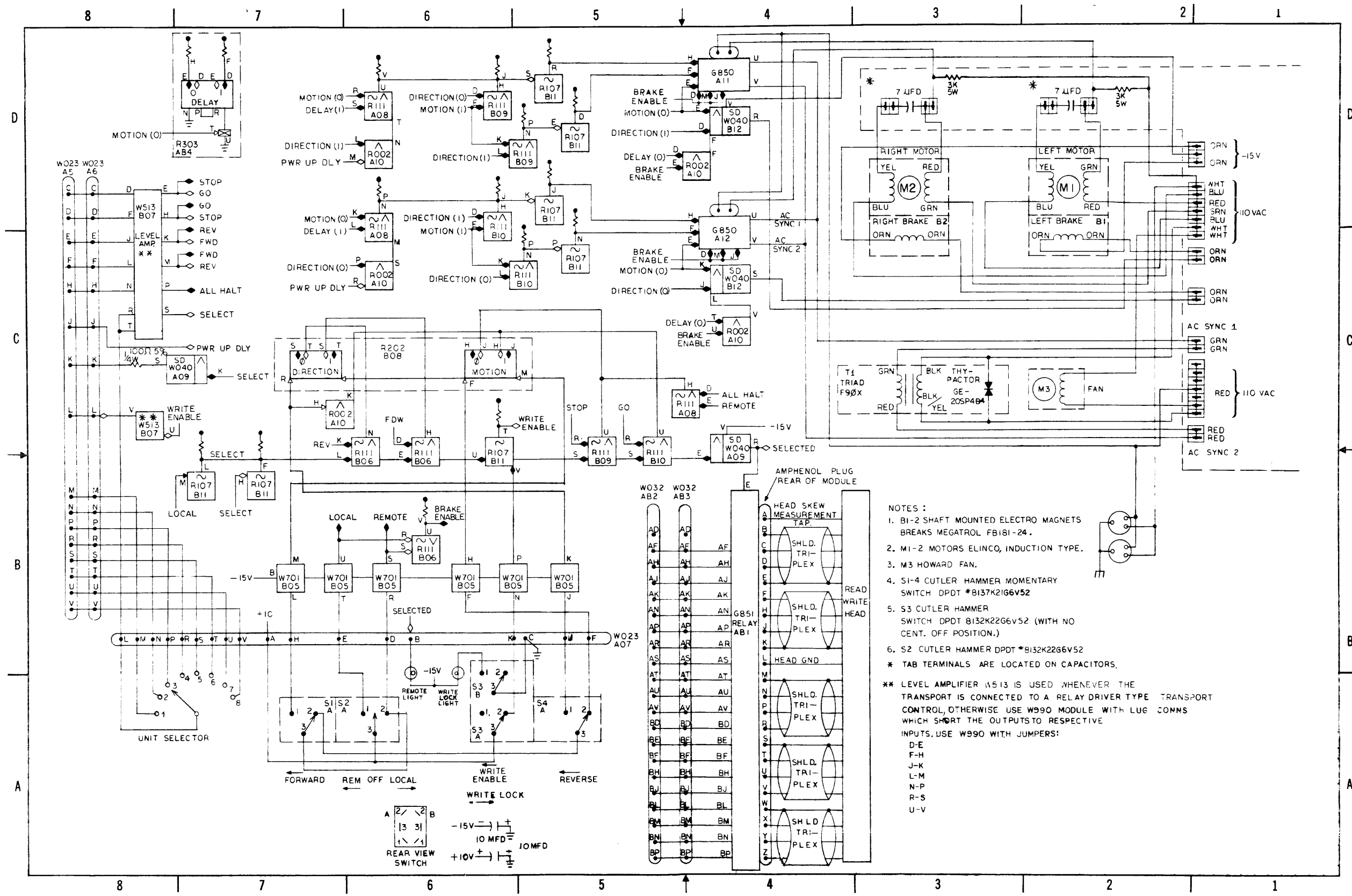
NOTES:
1. B1-2 SHAFT MOUNTED ELECTRO MAGNETS BREAKS MEGATROL FB181-24.
2. M1-2 MOTORS ELINCO, INDUCTION TYPE.
3. M3 HOWARD FAN.
4. S1-4 CUTLER HAMMER MOMENTARY SWITCH DPDT #8137K21G6V52
5. S3 CUTLER HAMMER SWITCH DPDT 8132K22G6V52 (WITH NO CENT. OFF POSITION.)
6. S2 CUTLER HAMMER DPDT #8132K22G6V52
* TAB TERMINALS ARE LOCATED ON CAPACITORS.
** LEVEL AMPLIFIER W513 IS USED WHENEVER THE TRANSPORT IS CONNECTED TO A RELAY DRIVER TYPE TRANSPORT CONTROL, OTHERWISE USE W990 MODULE WITH LUG CONNS WHICH SHORT THE OUTPUTS TO RESPECTIVE INPUTS. USE W990 WITH JUMPERS:
  D-E
  F-H
  J-K
  L-M
  N-P
  R-S
  U-V

D-BS-TU55-0-2 Solid State DECtape TU55

II-37

D-BS-DF32-0-1 Disk Control

D-BS-DS32-0-1 Disk Expander

D-BS-DF32-0-2 Disk Memory Address

D-BS-DF32-0-3 Disk Extended Memory Address

D-BS-DF32-0-4 Disk Memory Buffer

D-BS-DF32-0-5 Disk Head Diode Switch Matrix

1 | 2 | 3 | 4 | 5 | 6 | 7 | 8

WØ21 C17
D — DATA BIT Ø (I)
E — DATA BIT I (I)
H — DATA BIT 2 (I)
K — DATA BIT 3 (I)
M — DATA BIT 4 (I)
P — DATA BIT 5 (I)
S — DATA BIT 6 (I)
T — DATA BIT 7 (I)
V — DATA BIT 8 (I)

WØ21 C18
D — DATA BIT 9 (I)
E — DATA BIT IØ (I)
H — DATA BIT 11 (I)
K — CYCLE SELECT
M
P — WORD COUNT OVER FLOW
S
T
V

WØ21 C15
D — DATA ADDR Ø (I)
E — DATA ADDR 1 (I)
H — DATA ADDR 2 (I)
K — DATA ADDR 3 (I)
M — DATA ADDR 4 (I)
P — DATA ADDR 5 (I)
S — DATA ADDR 6 (I)
T — DATA ADDR 7 (I)
V — DATA ADDR 8 (I)

WØ21 C16
D — DATA ADDR 9 (I)
E — DATA ADDR IØ (I)
H — DATA ADDR 11 (I)
K — BREAK REQUEST
M — TRANSFER DIRECTION
P — B (BREAK)
S — ADDRESS ACCEPTED
T
V

WØ21 C19
P — AE 1
E — AE 2
H — AE 3
K
M
P
S
T
V

WØ21 C13 | WØ21 D13
D D — AC Ø
E E — AC 1
H H — AC 2
K K — AC 3
M M — AC 4
P P — AC 5
S S — AC 6
T T — AC 7
V V — AC 8

WØ21 C14 | WØ21 D14
D D — AC 9
E E — AC IØ
H H — AC 11
K K — SKIP
M M — INTERRUPT
P P — AC CLEAR
S S — B RUN (I)
T T
V V

WØ21 CØ9 | WØ21 DØ9
D D — BAC Ø (1)
E E — BAC 1 (1)
H H — BAC 2 (1)
K K — BAC 3 (1)
M M — BAC 4 (1)
P P — BAC 5 (1)
S S — BAC 6 (1)
T T — BAC 7 (1)
V V — BAC 8 (1)

WØ21 CIØ | WØ21 DIØ
D D — BAC 9 (1)
E E — BAC IØ (1)
H H — BAC 11 (1)
K K — IOP 1
M M — IOP 2
P P — IOP 4
S S — T1
T T — T2
V V — POWER CLEAR

WØ21 C11 | WØ21 D11
D D — BMB Ø (1)
E E — BMB 1 (1)
H H — BMB 2 (1)
K K — BMB 3 (Ø)
M M — BMB 3 (1)
P P — BMB 4 (Ø)
S S — BMB 4 (1)
T T — BMB 5 (Ø)
V V — BMB 5 (1)

WØ21 C12 | WØ21 D12
D D — BMB 6 (Ø)
E E — BMB 6 (1)
H H — BMB 7 (Ø)
K K — BMB 7 (1)
M M — BMB 8 (Ø)
P P — BMB 8 (1)
S S — BMB 9 (1)
T T — BMB IØ (1)
V V — BMB 11 (1)

WØ12 D16 | GANGED SWITCH | WØ21 D17

NOTE:
SWITCH IN POSITION 1 FOR -DP-E
SWITCH IN POSITION 2 FOR PDP-8S
SWITCH IS SHOWN IN POSITION 1

DBMB

NOTES:
GND PINS C,F,J,L,N,R,U ON ALL WØ21'S.

D-BS-DF32-0-7 I/O Connectors

PDP-8S

DATA
BREAK
LOGIC

PDP-8

FRONT PANEL
POWER SWITCH

POWER
CONTROL

COMPUTER
BREAKER

110 V. A.C.

POWER SUPPLY
728

+10V
-15V
GND.

110 V. A.C.

H05/307
H06/308
A01/301
A02/302
A03/303
A04/304
A05/305
A06/306
A07
A08
A09
A10
A11

ME34
MF34
ME35
MF35
PE01
PF02
PE03
PF03
PE04
PF04
ME36

D16
D17
C09
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19

DF 32
-0-

A05 B32
B31-SPARE

DATA
PCA
TIMING
ADDRESS

Disc

DS 32
-1-

C12 C24
D24-SPARE

DATA
PCA
TIMING
ADDRESS

Disc

DS 32
-2-

C12 C24
D24-SPARE

DATA
PCA
TIMING
ADDRESS

Disc

DS 32
-3-

C12 C24
D24-SPARE

DATA
PCA
TIMING
ADDRESS

Disc

D15
A01
A04

C09
C10
C11

D09
D10
D11

C09
C10
C11

D09
D10
D11

C09
C10
C11

D09
D10
D11

⇑ DC POWER

⇓ AC POWER

MOTOR
CONTROLLERS

D-IC-DF32-0-8 Disk System Interconnections

II-45

D-BD-DF32-0-9 Disk Block Diagram

D-TD-DF32-0-10 Disk Timing (Sheet 1)

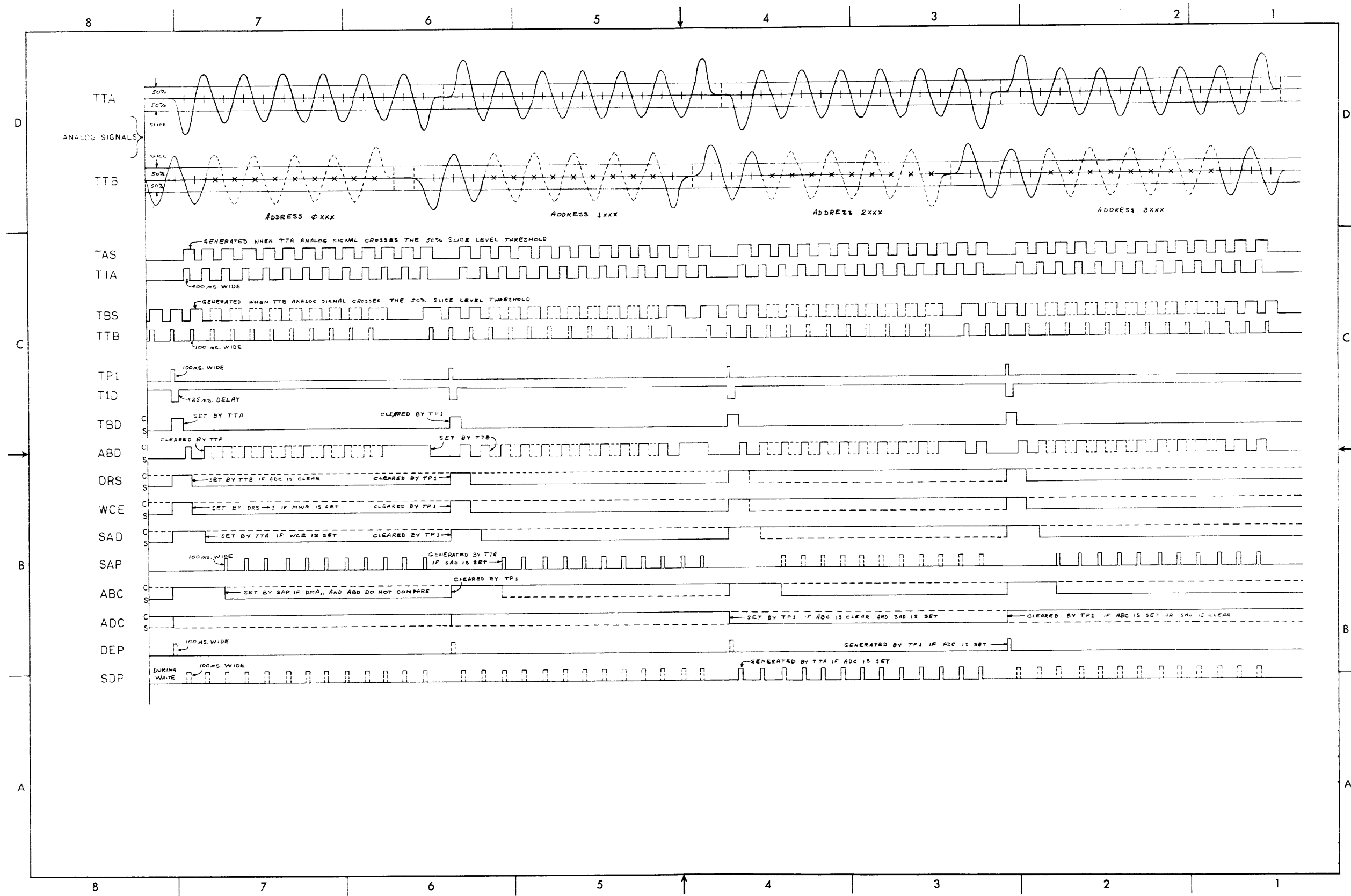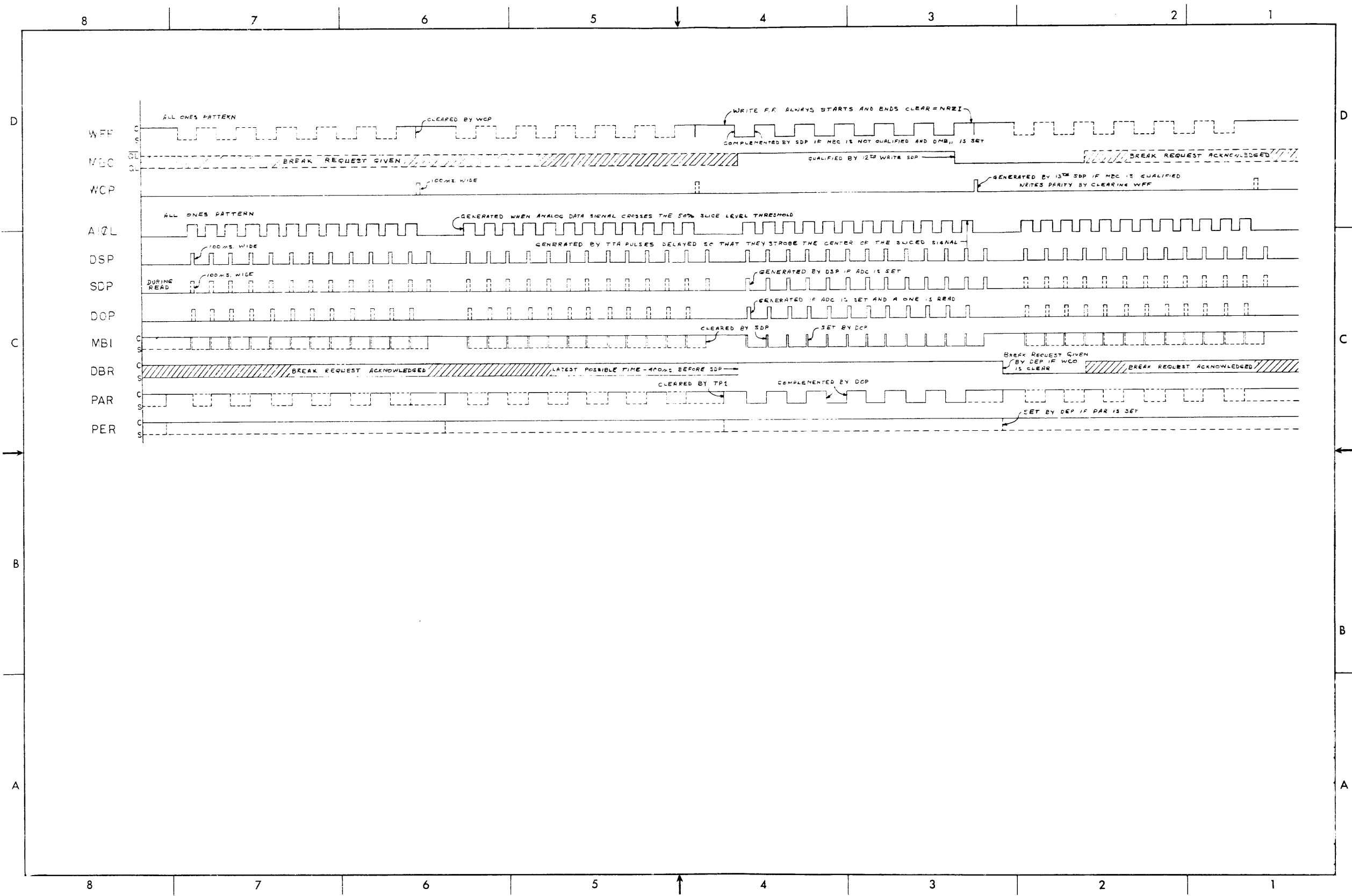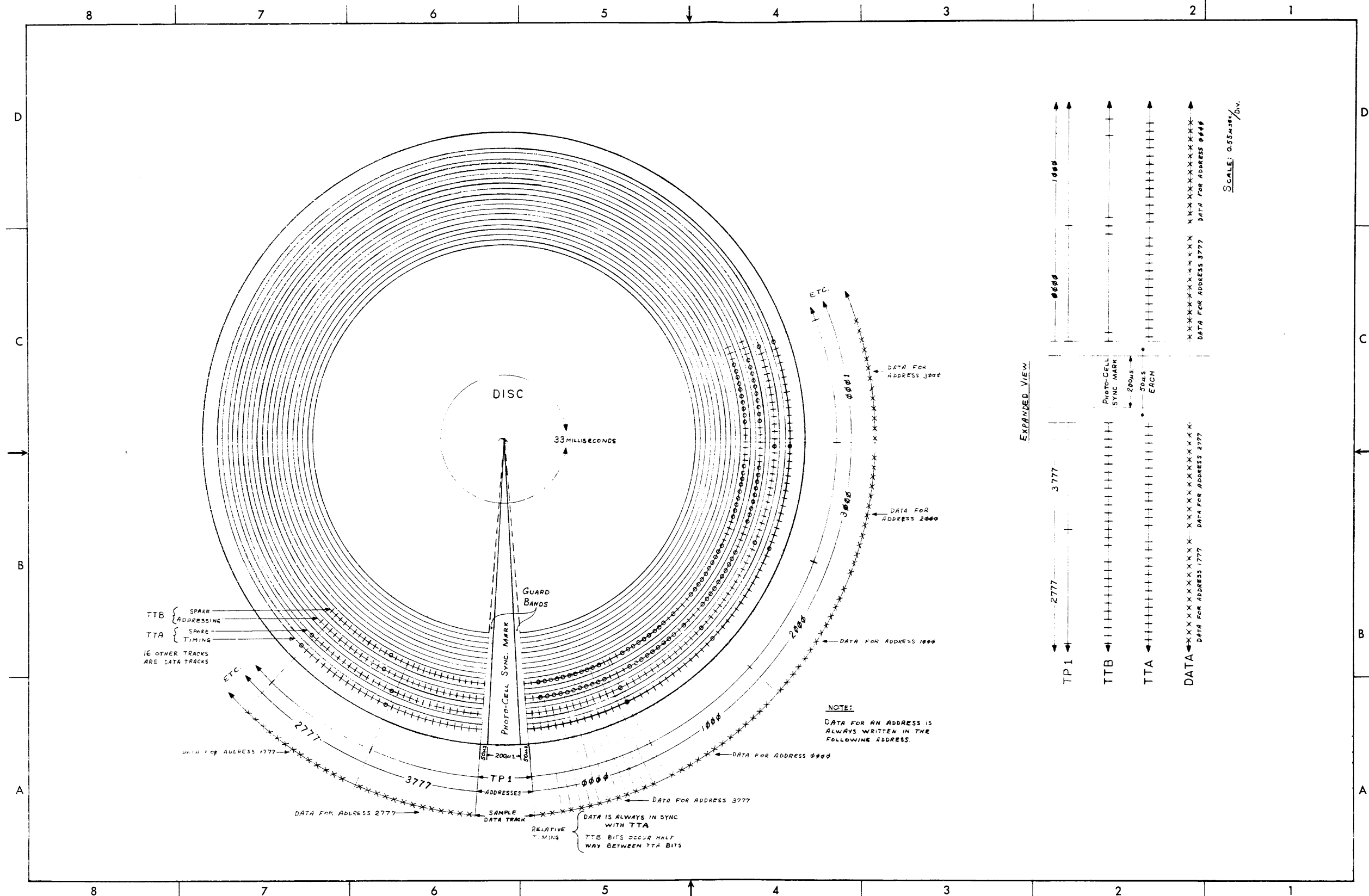II-47

D-TD-DF32-0-10 Disk Timing (Sheet 2)

DISC

33 MILLISECONDS

GUARD BANDS

TTB { SPARE
      { ADDRESSING
TTA { SPARE
      { TIMING

16 OTHER TRACKS
ARE DATA TRACKS

PHOTO-CELL SYNC. MARK

DATA FOR ADDRESS 3000

DATA FOR ADDRESS 2000

DATA FOR ADDRESS 1000

ETC.

0001

3000

2000

1000

ETC.

DATA FOR ADDRESS 1777

2777

3777

TP 1
ADDRESSES

0000

DATA FOR ADDRESS 0000

DATA FOR ADDRESS 3777

DATA FOR ADDRESS 2777

SAMPLE DATA TRACK

RELATIVE TIMING

50nS | 200nS | 50nS

NOTE:
DATA FOR AN ADDRESS IS
ALWAYS WRITTEN IN THE
FOLLOWING ADDRESS.

DATA IS ALWAYS IN SYNC
WITH TTA

TTB BITS OCCUR HALF
WAY BETWEEN TTA BITS

EXPANDED VIEW

TP 1

TTB

TTA

DATA

2777   3777   0000   1000

PHOTO-CELL SYNC MARK

50nS EACH

200nS

DATA FOR ADDRESS 3777   DATA FOR ADDRESS 0000

DATA FOR ADDRESS 1777   DATA FOR ADDRESS 2777

SCALE: 0.55 nSEC/DIV.

D-TD-DF32-0-11 Disk Electrical Aid